PNP Silicon Low-Power Transistor

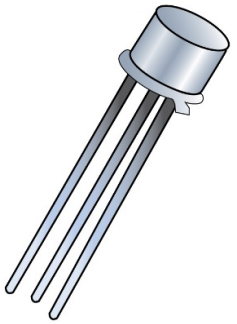
2N5415_2N5416

Product Overview

This family of 2N5415 and 2N5416 epitaxial planar transistors are military qualified up to a JANS level for high-reliability applications per MIL-PRF-19500/485 . These devices are also available in TO-39 and low profile U4 and UA packaging.

Qualified Levels: JAN, JANTX, JANTXV and JANS.

Figure 1. TO-5 Package



Also available in:

TO-205AD (TO-39) package (short-leaded)

2N5415S – 2N5416S

U4 package (surface mount)

2N5415U4 – 2N5416U4

UA package (surface mount)

2N5415UA – 2N5416UA

Features

- JEDEC registered 2N5415 through 2N5416 series
- JAN, JANTX, JANTXV, and JANS qualifications are available per MIL-PRF-19500/485. (See Part Nomenclature for all available options.)
- RoHS compliant

Applications/Benefits

- General purpose transistors for low power applications requiring high frequency switching.
- Low package profile
- Military and other high-reliability applications

Table of Contents

1. Maximum Ratings

Table 1-1. Maximum Ratings at 25 °C Unless Otherwise Noted

Parameters / Test Conditions	Symbol	2N5415	2N5416	Unit
Collector-Emitter voltage	V_{CEO}	200	300	V
Collector-Base voltage	V_{CBO}	200	350	V
Emitter-Base voltage	V_{EBO}	6.0	6.0	V
Collector current	I_C	1.0	1.0	A
Operating and storage junction temperature range	T_J, T_{stg}	–65 to +200		°C
Thermal resistance junction-to-ambient	$R_{\Theta JA}$	234		°C/W
Thermal resistance junction-to-case	$R_{\Theta JC}$	17.5		°C/W
Total power dissipation at T_A = +25 °C [1] at T_C = +25 °C [2]	P_T	0.75 10		W

Notes:

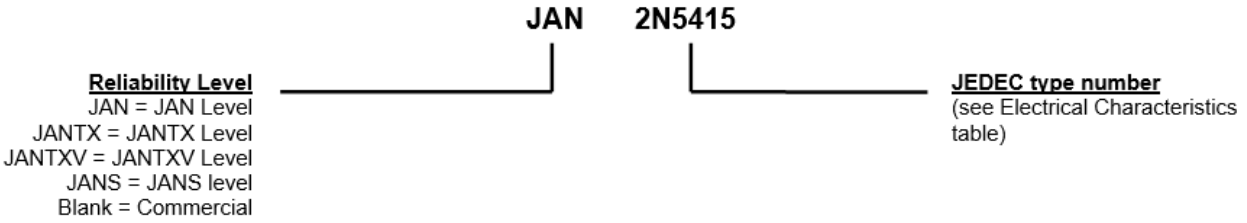
1. Derate linearly 4.29 mW/°C for TA > +25 °C
2. Derate linearly 57.2 mW/°C for T_C > +25 °C

1.1 Mechanical Packaging

- Case: Hermetically sealed, kovar base, nickel cap
- Terminals: Leads are gold plated kovar. Solder dip (Sn63/Pb37) is available upon special request. **Note:** Solder dipping will eliminate RoHS compliance.
- Marking: Part number, date code, manufacturer's ID
- Polarity: NPN
- Weight: Approximately 1.14 grams
- See Package Dimensions.

2. Part Nomenclature

Figure 2-1. Part Nomenclature



2.1 Symbols and Definitions

Table 2-1. Symbols and Definitions

Symbol	Definition
C_{obo}	Common-base open-circuit output capacitance
I_{CEO}	Collector cutoff current, base open
I_{CEX}	Collector cutoff current, circuit between base and emitter
I_{EBO}	Emitter cutoff current, collector open
h_{FE}	Common-emitter static forward current transfer ratio
V_{CEO}	Collector-emitter voltage, base open
V_{CBO}	Collector-base voltage, emitter open
V_{EBO}	Emitter-base voltage, collector open

3. Electrical Characteristics at T_A = +25 °C, Unless Otherwise Noted

Table 3-1. Off Characteristics

Parameters/Test Conditions		Symbol	Min.	Max.	Unit
Collector-Emitter breakdown voltage					
I_C = 50 mA, I_B = 5 mA, L = 25 mH; f = 30–60 Hz	2N5415 2N5416	$V_{(BR)CEO}$	200 300	—	V
Emitter-Base cutoff current V_{EB} = 6.0V		I_{EBO}	—	20	µA
Collector-Emitter cutoff current					
V_{CE} = 200V, V_{BE} = 1.5V V_{CE} = 300V, V_{BE} = 1.5V	2N5415 2N5416	I_{CEX}	—	50	µA
Collector-Emitter cutoff current					
V_{CE} = 150V V_{CE} = 250V	2N5415 2N5416	I_{CEO1}	—	50	µA
Collector-Emitter cutoff current					
V_{CE} = 200V V_{CE} = 300V	2N5415 2N5416	I_{CEO2}	—	1	mA
Collector-Base cutoff current					
V_{CB} = 175V V_{CB} = 280V	2N5415 2N5416	I_{CBO1}	—	50	µA
V_{CB} = 200V V_{CB} = 350V	2N5415 2N5416	I_{CBO2}	—	500	µA
V_{CB} = 175V, T_A = +150 °C V_{CB} = 280V, T_A = +150 °C	2N5415 2N5416	I_{CBO3}	—	1	mA

Table 3-2. On Characteristics

Parameters/Test Conditions	Symbol	Min.	Max.	Unit
Forward-Current transfer ratio I_C = 50 mA, V_{CE} = 10V I_C = 1 mA, V_{CE} = 10V I_C = 50 mA, V_{CE} = 10V, T_A = +150 °C	h_{FE}	30 15 15	120	—
Collector-Emitter saturation voltage I_C = 50 mA, I_B = 5 mA	$V_{CE(sat)}$	—	2.0	V
Base-Emitter voltage non-saturation I_C = 50 mA, V_{CE} = 10V	V_{BE}	—	1.5	V

Table 3-3. Dynamic Characteristics

Parameters/Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of common emitter small-signal short-circuit forward current transfer ratio I_C = 10 mA, V_{CE} = 10V, f = 5 MHz	$\lvert h_{fe} \rvert$	3	15	—
Small-signal short circuit forward-current transfer ratio I_C = 5 mA, V_{CE} = 10V, f ≤ 1 kHz	h_{fe}	25	—	—

.....continued

Parameters/Test Conditions	Symbol	Min.	Max.	Unit
Output capacitance V_{CB} = 10V, I_E = 0, 100 kHz ≤ f ≤ 1 MHz	C_{obo}	—	15	pF

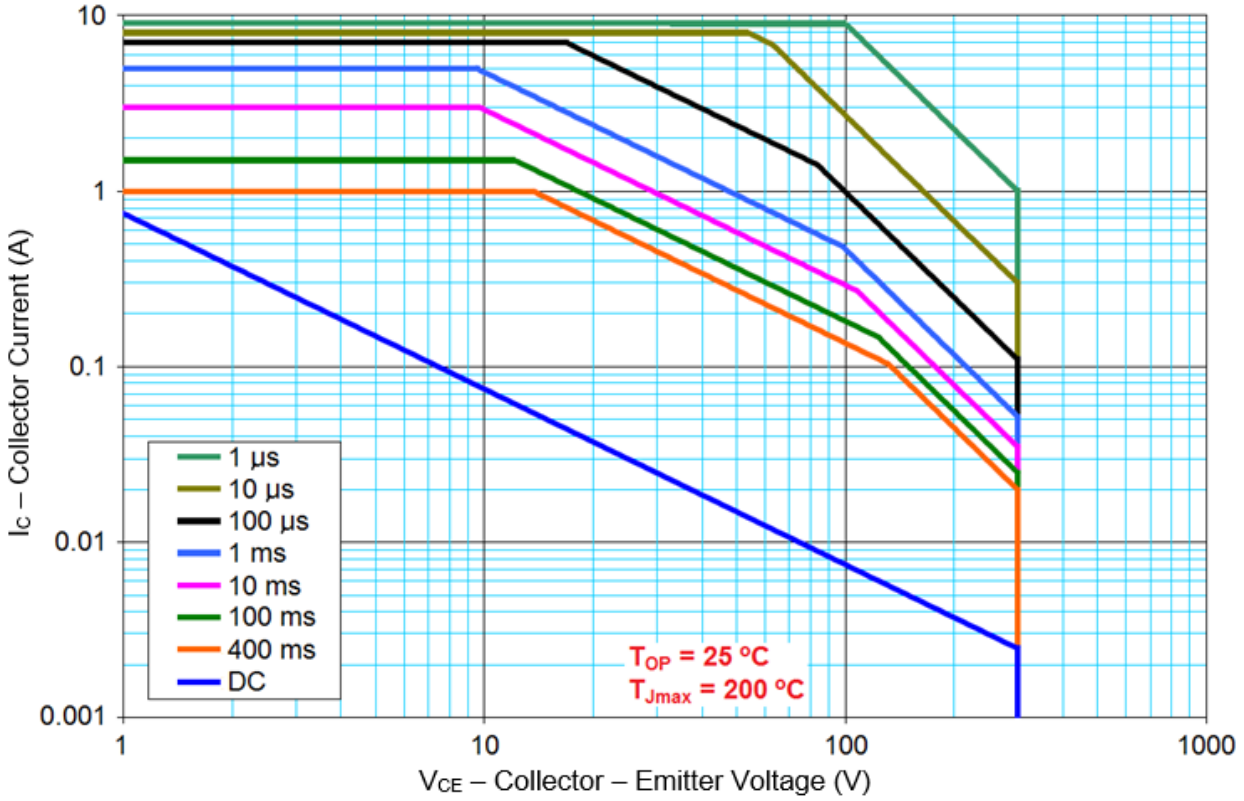
Table 3-4. Switching Characteristics

Parameters/Test Conditions	Symbol	Min.	Max.	Unit
Turn-On time V_{CC} = 200V, I_C = 50 mA, I_{B1} = 5 mA	t_{on}	—	1	µs
Turn-Off time V_{CC} = 200V, I_C = 50 mA, I_{B1} = I_{B2} = 5 mA	t_{off}	—	10	µs

Safe Operating Area

- DC Tests
  T_C = +25 °C, t_P = 0.4 seconds, 1 Cycle
- Test 1
  V_{CE} = 10V, I_C = 1 A
- Test 2
  V_{CE} = 100V, I_C = 100 mA
- Test 3
  V_{CE} = 200V, I_C = 24 mA (2N5415 only)
- Test 4
  V_{CE} = 300V, I_C = 10 mA (2N5416 only)

Figure 3-1. Maximum Safe Operating Area (T_J = 200 °C)



4. Graphs

Figure 4-1. Thermal Impedance Graph ($R_{\Theta JA}$)

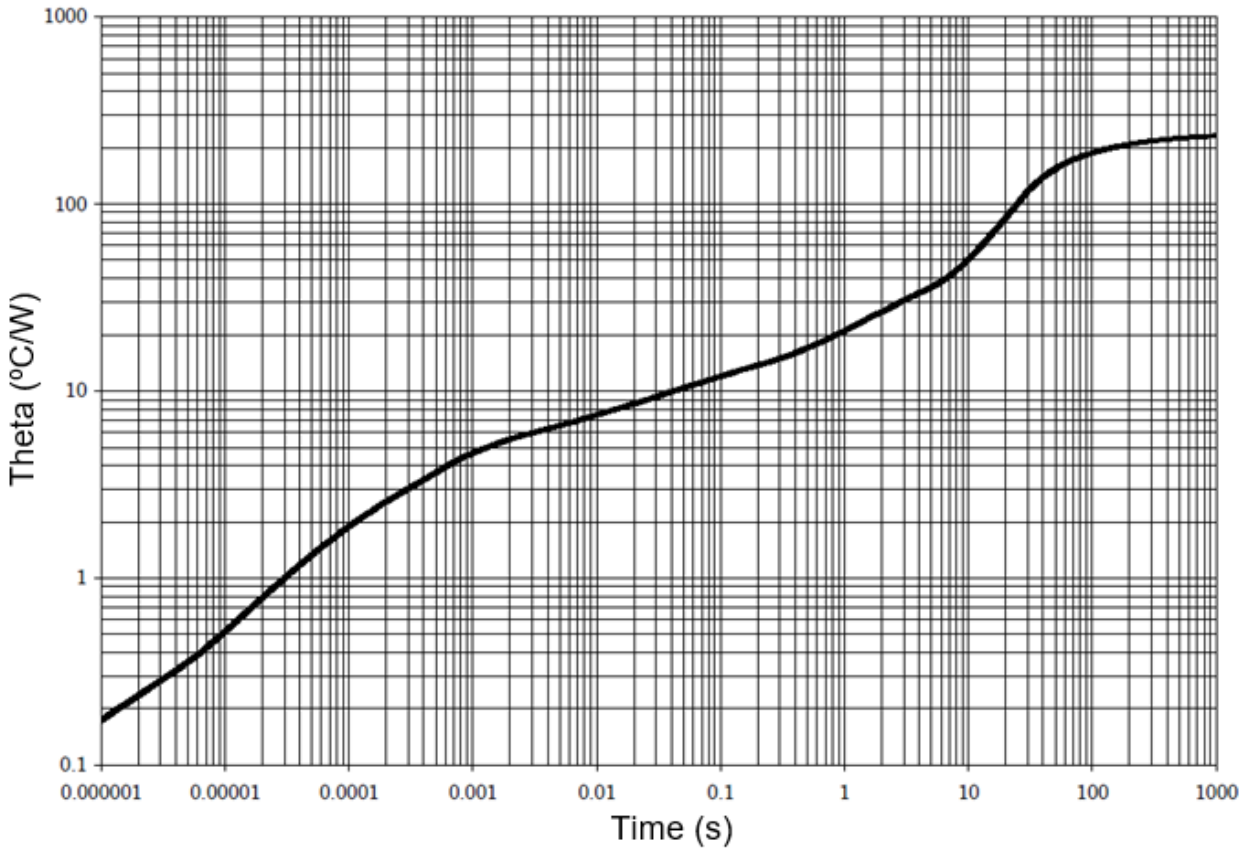
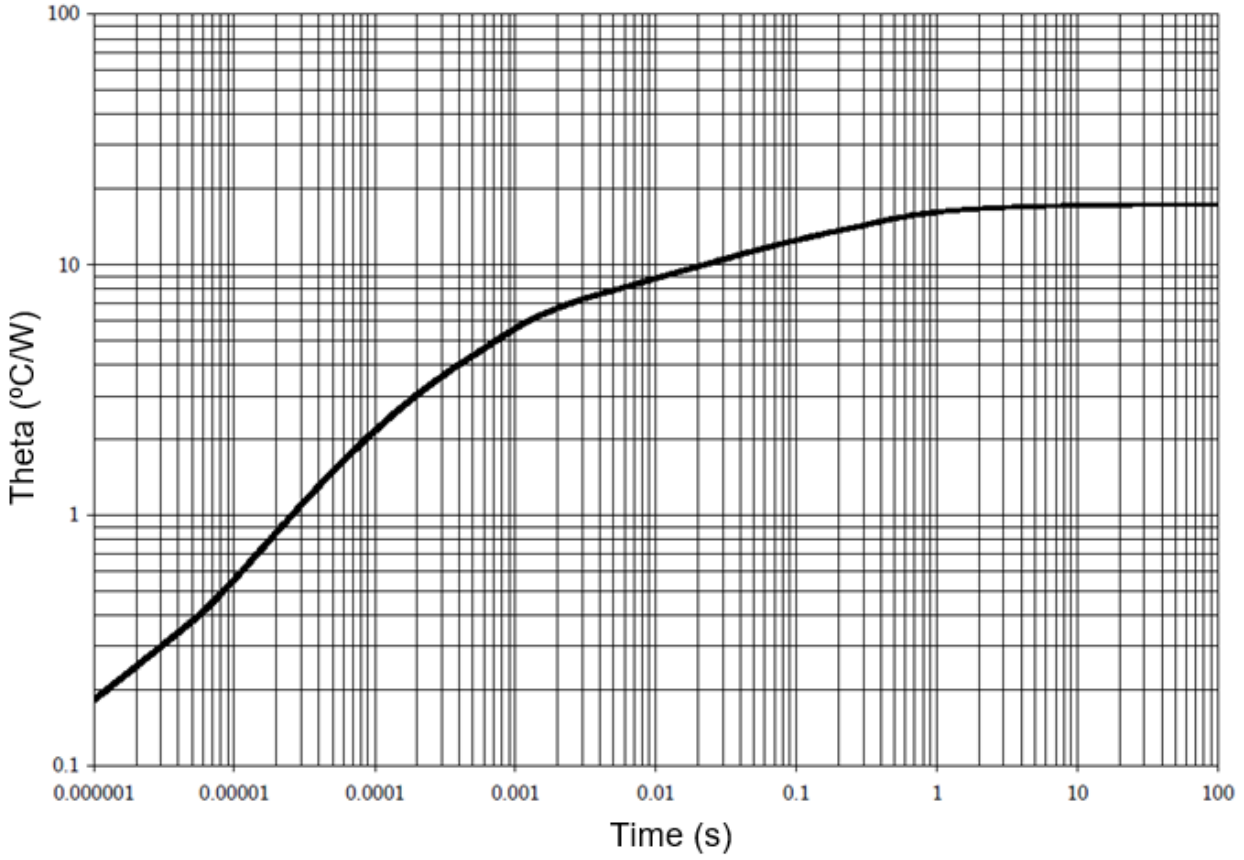
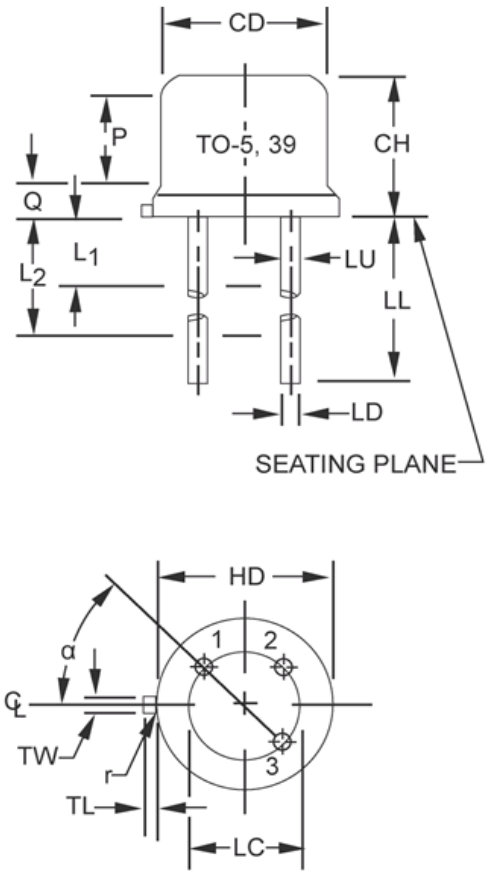


Figure 4-2. Thermal Impedance Graph ($R_{\Theta JA}$)

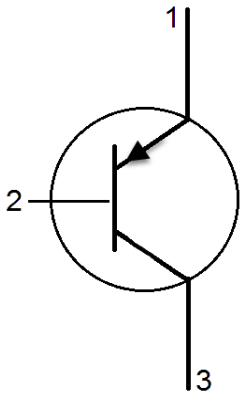


5. Package Dimensions

Figure 5-1. Package Dimensions



Symbol	Dimensions				Note
	Inch		Millimeters		
	Min.	Max.	Min.	Max.	
CD	0.305	0.335	7.75	8.51	—
CH	0.240	0.260	6.10	6.60	—
HD	0.335	0.370	8.51	9.40	—
LC	0.200 TP		5.08 TP		6
LD	0.016	0.021	0.41	0.53	7
LL	See notes 7, 12, and 13				—
LU	0.016	0.019	0.41	0.48	7, 13
L1	—	0.050	—	1.27	13
L2	0.250	—	6.35	—	13
P	0.100	—	2.54	—	5
Q	—	0.050	—	1.27	4
TL	0.029	0.045	0.74	1.14	3
TW	0.028	0.034	0.71	0.86	10, 11
r	—	0.010	—	0.25	11
α	45° TP		45° TP		6



Notes:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Symbol CD shall not vary more than 0.010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane 0.054 inch (1.37 mm) +0.001 inch (0.03 mm) -0.000 inch (0.00 mm) below seating plane shall be within 0.007 inch (0.18 mm) radius of true position (TP) relative to tab. Device may be measured by direct methods or by gauge.
7. Symbol LD applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Lead diameter shall not exceed 0.042 inch (1.07 mm) within L1 and beyond LL minimum.
8. Lead designation, shall be as follows: 1 - emitter, 2 - base, 3 - collector.
9. Lead number three is electrically connected to case.
10. Beyond r maximum, TW shall be held for a minimum length of 0.011 inch (0.28 mm).
11. Symbol r applied to both inside corners of tab.
12. For transistor types 2N5415 and 2N5416, dimension LL shall be 1.5 inches (38.1 mm) minimum and 1.75 inch (44.4 mm) maximum.
13. All three leads
14. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	12/2024	Updated links to Microchip website.
A	12/2024	Document converted to Microchip template and assigned literature number DS00005746.
Rev. 1	07/2013	Microsemi document LDS-0305 was created.

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