5.5V TO 100V WIDE INPUT VOLTAGE, SYNCHRONOUS BUCK CONTROLLER

Description

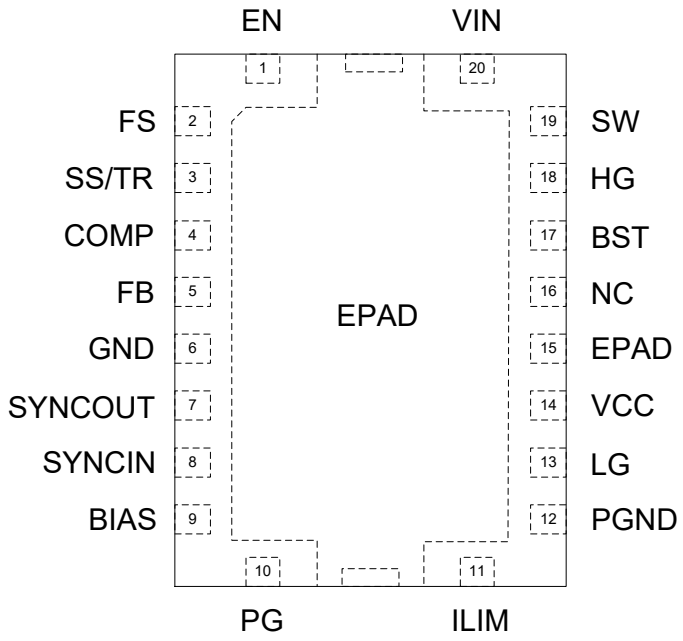
The AP6ACO5 is an adjustable switching frequency, synchronous DC-DC buck controller with adjustable frequency from 100kHz to 1.2MHz. The control scheme is a voltage mode with line feed forward to enable easy compensation. The device with a minimum-on-time of 40ns controlled high-side MOSFET supports a high conversion ratio, which allows voltage step down from 48V to low-voltage rail reducing system complexity and cost. The device operates at nearly 100% duty cycle if needed during input voltage drops as low as 5.5V.

The AP6ACO5 gate drivers can source 2.3A and sink 3.5A current enough to drive large MOSFETs for up to 50A output current with as high as 95% efficiency. The AP6ACO5 mode is programmable in PFM for high light load efficiency or PWM to maintain low output ripple across all loading conditions.

With its high level of integration and minimal need for external components, the AP6ACO5 simplifies board layout and reduces space requirements. This makes it ideal for distributed power architecture.

The AP6ACO5 is available in the standard Green V-QFN3545-20/SWP package with enhanced thermal power pad.

Pin Assignments



Features

- V_{IN} 5.5V to 100V
- V_{OUT} Adjustable from 0.8V to 60V
- 0.8V ±1% V_{REF}
- 2.3A/3.5A Source/Sink Gate Drive Current
- Adjustable Switching Frequency 100kHz to 1.2MHz
- FSS Modulation
- Enable Pin with 5% Tolerance
- Overcurrent Protection (OCP) with Hiccup
- Thermal Protection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- General-purpose point-of-load DC/DC power conversion
- Telecommunication systems
- Distributed power systems
- Home audio devices
- Consumer electronics
- Network systems
- FPGA, DSP, and ASIC supplies
- Green electronics

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

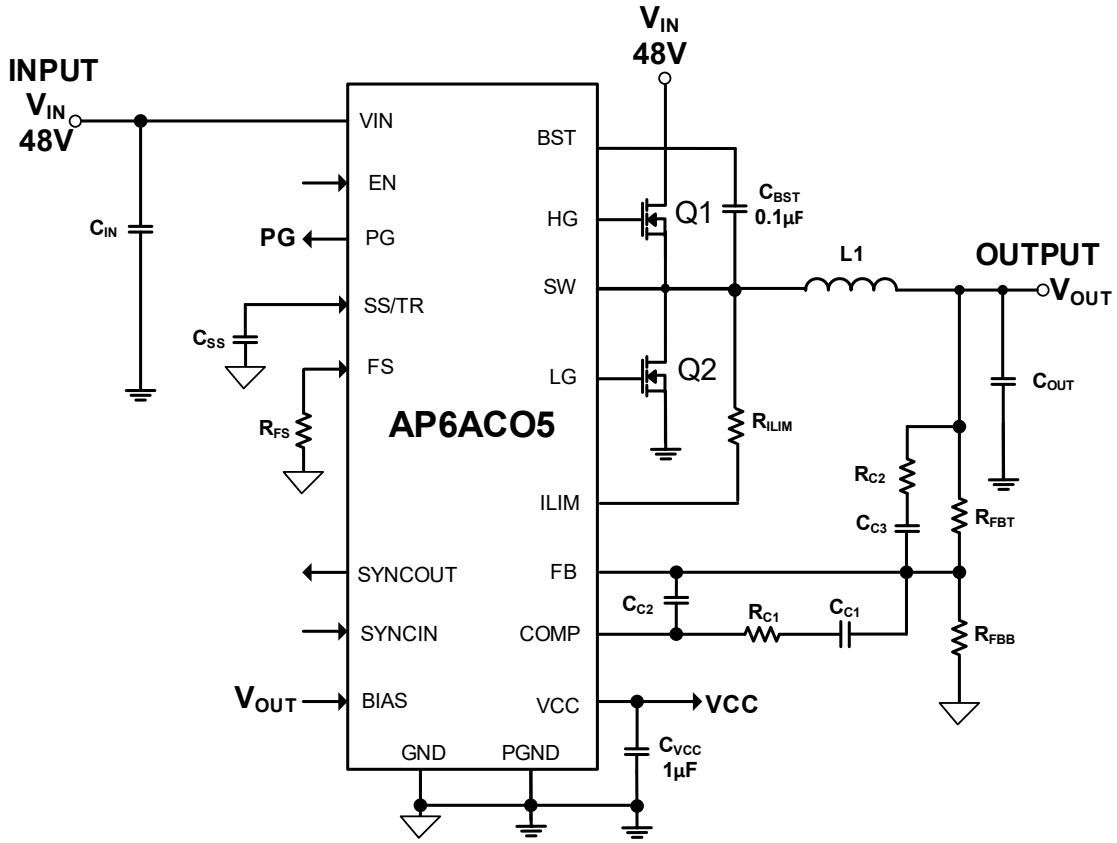


Figure 1. Typical Application Circuit

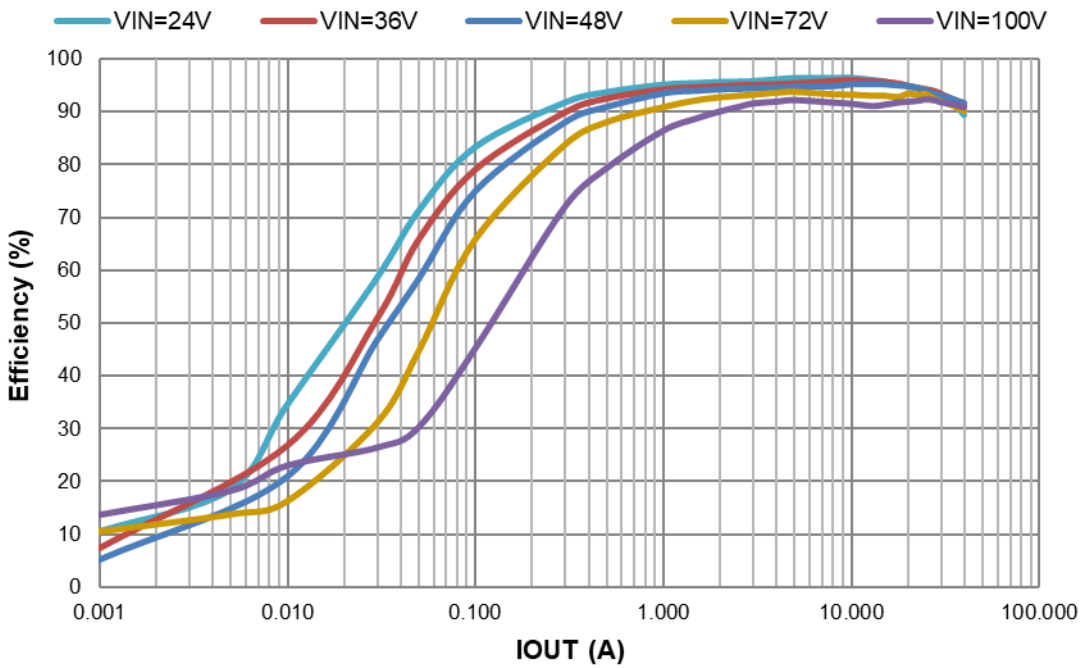


Figure 2. Efficiency vs. Output Current, 12V_{OUT}, I_{OUT} = 1mA to 40A, f_{SW} = 100kHz, PFM

Notes:
V_{IN} = 24V/36V/48V => 60V HS FET = DMTH6004LPS; 60V LS FET = DMT62M8LPS
V_{IN} = 72V/100V => 150V HS FET = DMT15H017LPS; 120V LS FET = DMT12H007LPS

Pin Descriptions

Pin Name	Pin Number	Function
EN	1	Enable input and undervoltage lockout programming pin. If the EN voltage is below 0.41V, the controller is in the shutdown mode with all functions disabled. If the EN voltage is greater than 0.41V but less than 1.2V, the regulator is in standby mode with the VCC regulator operating, the SS pin grounded, and no switching at the HG and LG outputs. When the EN voltage is set above 1.2V, the SS/TRK voltage can ramp, and pulse-width modulated gate-drive signals are delivered to the HG and LG pins.
FS	2	Set the internal oscillator clock frequency. Connect a resistor from this pin to ground to set switching frequency.
SS/TR	3	Soft-start pin for the regulator. The SS/TR pin controls the soft-start and sequence of the output. A single capacitor from SS/TR to GND determines the output ramp rate. See the “Output Tracking and Sequencing” section for more application detail about soft-start, output tracking, and sequencing. Connect a minimum 2.2nF capacitance from SS/TR to GND.
COMP	4	Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
FB	5	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive divider connected to it from the output voltage to this pin. The feedback regulation voltage is 0.8V. See “Setting the Output Voltage”.
GND	6	Analog ground that is used for the controller. Single point connection to the external MOSFET Q2 and EPAD.
SYNCOUT	7	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the high-side MOSFET gate drive. Connect SYNCOUT of the master AP68CO5 to the SYNCIN pin of a second AP68CO5 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turn-on transitions. Note that the SYNCOUT pin does not provide 180° interleaving when the controller is operating from an external clock that is different from the free-running frequency set by the R_{FS} resistor.
SYNCIN	8	Connect SYNCIN to VCC or HIGH for forced PWM. Connect SYNCIN to GND for PFM operation. Apply an external clock source for synchronization with positive edge trigger and PWM.
BIAS	9	The internal regulator will draw current from BIAS instead of VIN when BIAS is tied to a voltage higher than 4.7V. For output voltages of 5V to 14V this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin. If no supply is available, tie to PGND.
PG	10	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start interval.
ILIM	11	Current limit and current sense comparator input. A current sourced from the ILIM pin through an external resistor program the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for $R_{DS(ON)}$ sensing or to a current sense resistor connected to the source of the low-side MOSFET.
PGND	12	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low-side MOSFET or the ground side of a shunt resistor.
LG	13	Low-side MOSFET gate drive output. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
VCC	14	Internal power supply output pin to connect an additional capacitor. Connect a 1µF (typical) capacitor as close as possible to the VCC and PGND. This pin is not active when EN is low.
EP	15	The EP pin is internally connected to the exposed pad of the package. Solder to the GND and PGND planes to reduce thermal impedance.
NC	16	No electrical connection.
BST	17	High-Side Gate Drive Boost Input. BST supplies the drive for the high-side N-Channel MOSFET with a 0.1µF or greater capacitor from SW to BST to power the high side switch.
HG	18	High-side MOSFET gate drive output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
SW	19	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
VIN	20	Supply voltage input for the VCC LDO regulator.

Functional Block Diagram

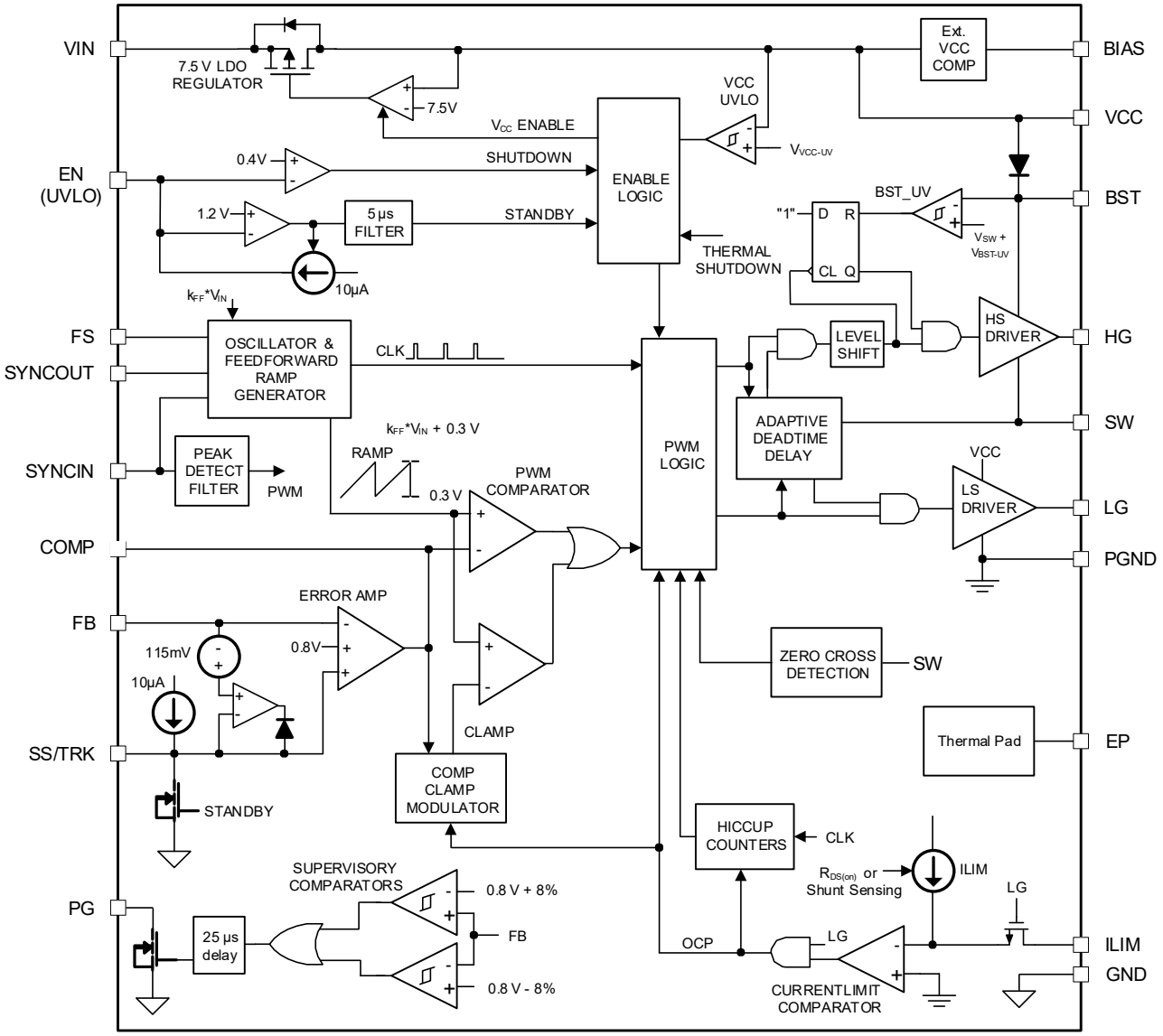


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to +105	V
V_{SW}	Switch Node Voltage	-1.0 to V_{IN} +0.3 (DC)	V
V_{SW}	Switch Node Voltage	-2.5 to V_{IN} +5 (ns)	V
V_{EN}	Enable/UVLO Voltage	-0.3 to +105	V
V_{BST}	Bootstrap Voltage	V_{SW} -0.3 to V_{SW} +6.0	V
V_{FB}	Feedback Voltage	-0.3 to +6.0	V
V_{FS}	Frequency Adjust	-0.3 to +6.0	V
V_{PG}	Power Good Voltage	-0.3 to +6.0	V
T_{ST}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+300	°C
ESD Susceptibility (Note 5)			
HBM	Human Body Model	±1000	V
CDM	Charged Device Model	±500	V

Notes: 4. Stresses greater than the *'Absolute Maximum Ratings'* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and can be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Package Thermal Information

Symbol	Parameter	Rating, JEDEC (Note 6)	AP6ACO5 EVM (Note 7)	Unit
θ_{JA}	Junction to Ambient	37	23	°C/W
$\theta_{JC(top)}$	Junction to Case (Top)	28	21	°C/W
θ_{JB}	Junction to Board (Bottom)	12	9	°C/W
Ψ_{JT}	Junction to Top Characterization Parameter	0.4	0.3	°C/W
Ψ_{JB}	Junction to Board Characterization Parameter	12	9	°C/W
$\theta_{JC(bot)}$	Junction to Case (Bottom)	2.1	1.7	°C/W

Notes: 6. Device mounted on FR-4 substrate, JEDEC 4 layer 50mm x 50mm PCB board (2oz copper), with minimum recommended pad layout.
7. Device mounted on Diodes evaluation board. See user guide for more details.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.) (Note 8)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	5.5	100	V
V_{OUT}	Output Voltage	0.8	60	V
T_J	Operating Junction Temperature Range	-40	+125	°C

Note: 8. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, V_{IN} = 48V, R_{FS} = 100kΩ, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +125°C, and input range from 5.5V to 80V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
UVLO	VCC Undervoltage Lockout Threshold	—	—	4.5	—	V
—	Hysteresis	—	—	200	—	mV
V_{CC}	V_{CC} Regulation Voltage	V_{SS}/T_{RK} = 0, 9V ≤ V_{IN} ≤ 80V, 0 < I_{VCC} ≤ 20mA	7.1	7.5	7.8	V
I_{SC_LDO}	V_{CC} Short-Circuit Current	V_{SS}/T_{RK} = 0, V_{CC} = 0	40	50	120	mA
B_{IAS}	Ext. VCC Switchover Voltage	—	—	4.7	—	V
	Hysteresis	—	—	100	—	mV
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0, No Load	—	10	—	μA
I_Q	Supply Current (Quiescent)	E_N = 1.5V, No Load, Non-Switching	—	1.5	—	mA
Error Amplifier						
V_{REF}	FB Reference Voltage	FB Connected to COMP	0.792	0.8	0.808	V
I_{FB_BIAS}	FB Input Bias Current	V_{FB} = 0.8V	-0.1	0.004	—	μA
AVOL	DC Gain	—	—	94	—	dB
G_{BW}	Unity Gain Bandwidth	—	—	6.5	—	MHz
I_{COMP_SRC}	EA Maximum Source Current	V_{FB} = V_{REF}-100mV, V_{COMP} = 1V	1000	—	—	μA
I_{COMP_SNK}	EA Maximum Sink Current	V_{FB} = V_{REF}+100mV, V_{COMP} = 1V	1000	—	—	μA
V_{COMP_H}	COMP Output High Voltage	V_{FB} = 0, COMP Sourcing 1mA	—	4.5	—	V
V_{COMP_L}	COMP Output Low Voltage	COMP Sinking 1mA	—	0.25	—	V
Enable						
V_{EN_SD}	EN Rising Threshold from Shutdown to Standby	—	—	0.41	—	V
	Hysteresis	—	—	30	—	mV
V_{EN_TH}	EN Rising Threshold from Standby to Active On	—	1.146	1.2	1.236	V
I_{EN}	EN Current	—	9	10	11	μA
Soft-Start and Voltage Tracking						
I_{SS}	SS/TRK Capacitor Charging Current	V_{SS}/T_{RK} = 0	8.5	10	12	μA
R_{SS}	SS/TRK Discharging FET Resistance	V_{EN} = 1V, V_{SS}/T_{RK} = 0.1V	—	12	—	Ω
$V_{SS\text{-}FB}$	SS/TRK to FB Offset	—	—	62	—	mV
V_{CC_CLAMP}	SS/TRK Clamp Voltage	V_{SS}/T_{RK} – V_{FB}, V_{FB} = 0.8V	—	120	—	mV
PG						
PG_{UV_FALL}	Undervoltage Falling Threshold	Percent of Output Regulation, Fault	88	92	96	%
PG_{UV_RISE}	Undervoltage Rising Threshold	Percent of Output Regulation, Good	—	94	—	%
PG_{OV_RISE}	Overvoltage Rising Threshold	Percent of Output Regulation, Fault	103	109	115	%
PG_{OV_FALL}	Overvoltage Falling Threshold	Percent of Output Regulation, Good	—	106	—	%
PG Low	PG Low Voltage	I_{PG} = -3mA	—	—	0.15	V
PG Delay	PG Rising Edge Delay	—	—	25	—	μs
	PG Falling Edge Delay	—	—	25	—	μs

Electrical Characteristics (T_A = +25°C, V_{IN} = 48V, R_{FS} = 100kΩ, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +125°C, and input range from 5.5V to 80V, unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Frequency and External Clock Synchronization						
f_{SW1}	Switching Frequency 1	R_{FS} = 100kΩ (1%)	—	100	—	kHz
f_{SW2}	Switching Frequency 2	R_{FS} = 24.9kΩ (1%)	—	400	—	kHz
f_{SW3}	Switching Frequency 3	R_{FS} = 12.5kΩ (1%)	—	780	—	kHz
F_{RANGE_CLK}	SYNCIN External Clock Frequency Range Using	% of Nominal Frequency Set by FS	-20	—	50	%
$V_{SYNCI-IH}$	Minimum SYNCIN Input Logic High	—	2.0	—	—	V
$V_{SYNCI-IL}$	Maximum SYNCIN Input Logic Low	—	—	—	0.6	V
t_{SYNCPW}	SYNCIN Minimum Pulse Width	Minimum High State or Low State Duration	50	—	—	ns
$V_{SYNCO-OH}$	SYNCOUT High State Output Voltage	$I_{SYNCOUT}$ = -1mA (Sourcing)	3	—	—	V
$V_{SYNCO-OL}$	SYNCOUT Low State Output Voltage	$I_{SYNCOUT}$ = 1mA (Sinking)	—	—	0.4	V
$t_{SYNCOUT}$	Delay from HG Rising to SYNCOUT Leading Edge	V_{SYNCIN} = 0, f_{SW} = 100kHz, R_{FS} = 100kΩ	—	1030	—	ns
t_{SYNCIN}	Delay from SYNCIN Leading Edge to HG Rising	50% to 50%	—	220	—	ns
F_{JITTER}	Frequency Spread Spectrum in Percentage of f_{SW}	—	—	±6	—	%
PWM Control						
$t_{ON(MIN)}$	Minimum Control On-Time	V_{BST}-V_{SW} = 7V, HG 50% to 50%	—	80	—	ns
$t_{OFF(MIN)}$	Minimum Control Off-Time	V_{BST}-V_{SW} = 7V, HG 50% to 50%	—	150	—	ns
$D_{100K(MAX)}$	Maximum Duty Cycle	f_{SW} = 100kHz, 5V < V_{IN} < 80V	—	98	—	%
$D_{400K(MAX)}$	Maximum Duty Cycle	f_{SW} = 400kHz, 5V < V_{IN} < 80V	—	92	—	%
$V_{RAMP(MIN)}$	Ramp Valley Voltage (COMP at 0% Duty Cycle)	—	—	300	—	mV
K_{FF}	PWM Feedforward Gain (V_{IN}/V_{RAMP})	5V < V_{IN} < 80V	—	12	—	V/V
Bootstrap Diode and Undervoltage Threshold						
$V_{BST-FWD}$	Diode Forward Voltage	VCC to BST, BST Sourcing 20mA	—	0.8	—	V
I_{Q-BST}	BST to SW Quiescent Current, Not Switching	V_{SS}/T_{RK} = 0, V_{SW} = 48V, V_{BST} = 54V	—	70	—	μA
V_{BST-UV}	BST to SW Undervoltage Detection	V_{BST}-V_{SW} Falling	—	3.4	—	V
	Hysteresis	—	—	500	—	mV
Overcurrent Protection and Valley Current Limiting						
I_{RS}	ILIM Source Current, RSENSE Mode	Low Voltage Detected at ILIM at +25°C	90	100	110	μA
I_{RDSON}	ILIM Source Current, $R_{DS(ON)}$ Mode	SW Voltage Detected at ILIM at +25°C	180	200	220	μA
$I_{RDSONTC}$	ILIM Current Tempco	R_{DS-ON} Mode	—	4500	—	ppm/°C
I_{RSTC}	ILIM Current Tempco	R_{SENSE} Mode	—	0	—	ppm/°C
$V_{ILIM-TH}$	ILIM Comparator Threshold at ILIM	—	-10	-2	20	mV
$C_{HICC-DEL}$	Hiccup Mode Activation Delay	Clock Cycles with Current Limiting before Hiccup Off-Time Activated	—	128	—	Cycles
C_{HICCUP}	Hiccup Mode Off-Time after Activation	Clock Cycles with No Switching Followed by SS/TRK Release	—	16384	—	Cycles

Electrical Characteristics (T_A = +25°C, V_{IN} = 48V, R_{FS} = 100kΩ, unless otherwise specified. Min/Max limits apply across the recommended junction temperature range, -40°C to +125°C, and input range from 5.5V to 80V, unless otherwise specified.) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Short-Circuit Protection – Duty Cycle Clamp						
$V_{CLAMP-OS}$	Clamp Offset Voltage – No Current Limiting	Clamp to COMP Steady-State Offset Voltage	—	0.2+VIN/75+1	—	V
$V_{CLAMP-MIN}$	Minimum Clamp Voltage	Clamp Voltage with Continuous Current Limiting	—	0.3+VIN/150	—	V
PFM Operation						
V_{ZCD-SS}	Zero Crossing Detect ZCD Soft-Start Ramp	ZCD Threshold Measured at SW Pin 50 Clock Cycles after the First HG Pulse	—	0	—	mV
$V_{ZCD-DIS}$	Zero Crossing Detect ZCD Disable Threshold (CCM)	ZCD Threshold Measured at SW Pin 1000 Clock Cycles after the First HG Pulse	—	550	—	mV
V_{DEM-TH}	Diode Emulation Zero Crossing Threshold	Measured at SW with VSW Rising	-20	-5	20	mV
Gate Driver						
R_{HG-UP}	HG High State Resistance, HG to BST	V_{BST}–V_{SW} = 7V, I_{HG} = -100mA	—	1.3	—	Ω
$R_{HG-DOWN}$	HG Low State Resistance, HG to SW	V_{BST}–V_{SW} = 7V, I_{HG} = 100mA	—	0.6	—	Ω
R_{LG-UP}	LG High State Resistance, LG to VCC	V_{BST}–V_{SW} = 7V, I_{LG} = -100mA	—	1.3	—	Ω
$R_{LG-DOWN}$	LG Low State Resistance, LG to SW	V_{BST}–V_{SW} = 7V, I_{LG} = 100mA	—	0.6	—	Ω
t_{HG-TR} t_{LG-TR}	HG, LG Rise Times	V_{BST}–V_{SW} = 7V, C_{LOAD} = 1nF, 20% to 80%	—	7	—	ns
t_{HG-TF} t_{LG-TF}	HG, LG Fall Times	V_{BST}–V_{SW} = 7V, C_{LOAD} = 1nF, 80% to 20%	—	4	—	ns
t_{HG-DT}	HG Turn-On Dead Time	V_{BST}–V_{SW} = 7V, LG Off to HG On, 50% to 50%	—	25	—	ns
t_{LG-DT}	LG Turn-On Dead Time	V_{BST}–V_{SW} = 7V, HG Off to LG On, 50% to 50%	—	22	—	ns
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown (Note 9)	—	—	+175	—	°C
T_{HYS}	Thermal Hysteresis (Note 9)	—	—	+20	—	°C

Note: 9. Compliance to the datasheet limits assured by one or more methods: production test, characterization, and/or design.

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, BOM = Table 2, unless otherwise specified.)

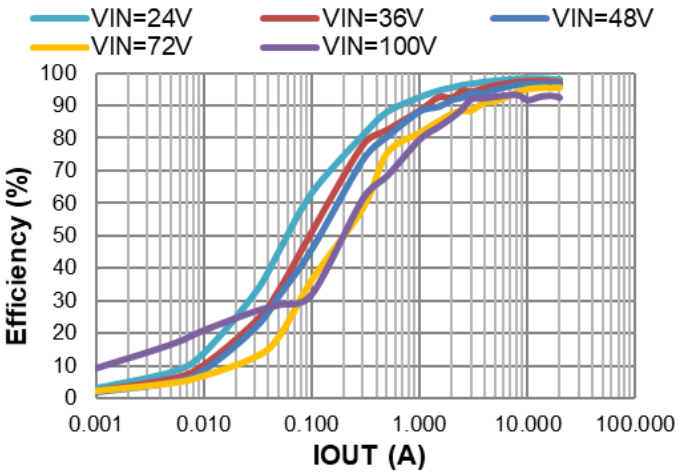


Figure 4. Efficiency vs. IOUT, Vo = 12V/20A, 200kHz, PFM

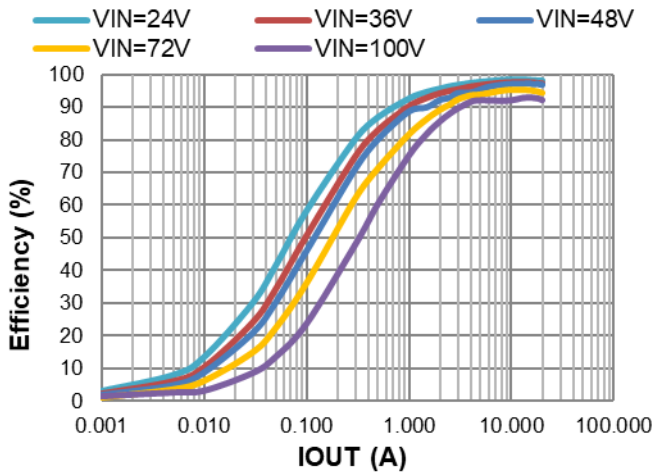


Figure 5. Efficiency vs. IOUT, Vo = 12V/20A, 200kHz, PWM

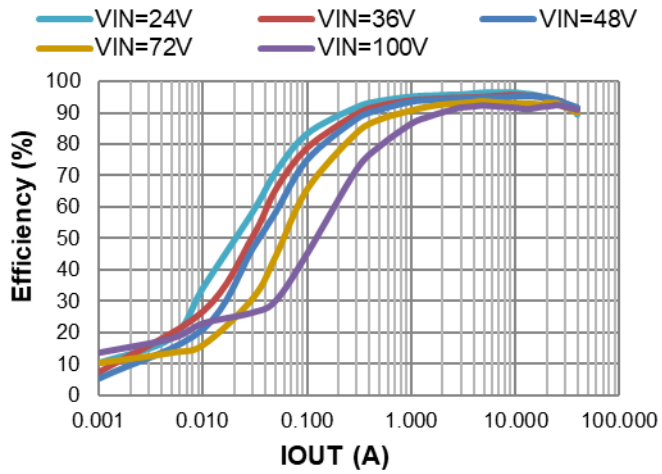


Figure 6. Efficiency vs. IOUT, Vo = 12V/40A, 100kHz, PFM

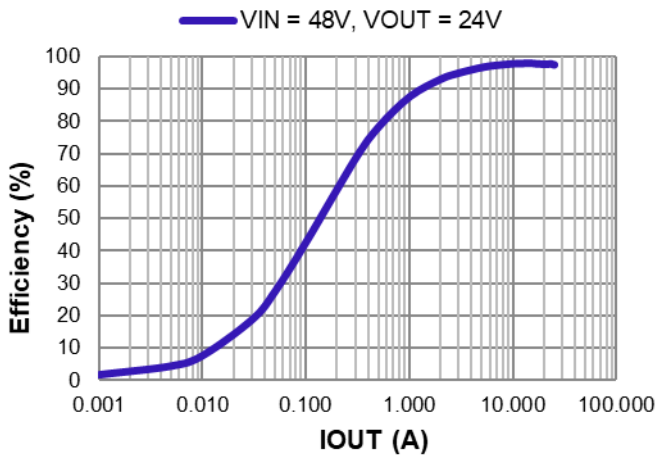


Figure 7. Efficiency vs. IOUT, Vo = 24V/25A, 200kHz, PWM

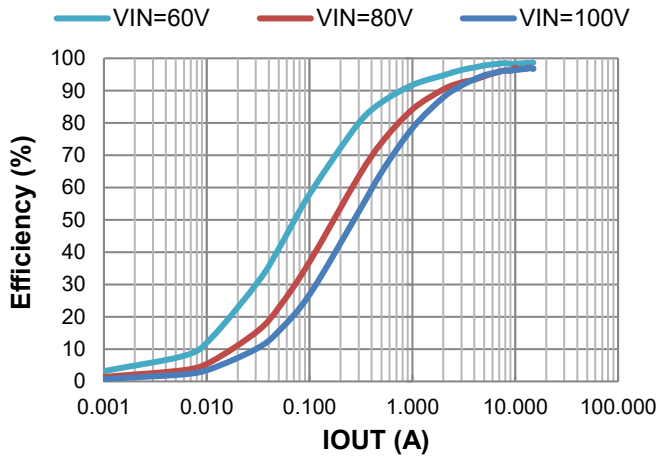


Figure 8. Efficiency vs. IOUT, Vo = 48V/15A, 200kHz, PWM

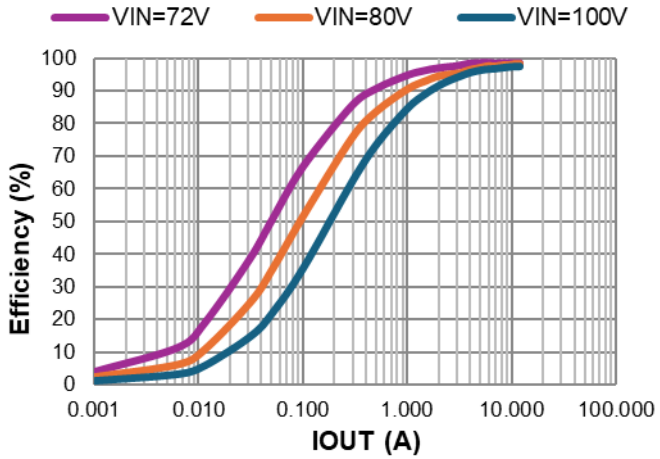


Figure 9. Efficiency vs. IOUT, Vo = 60V/12A, 200kHz, PWM

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

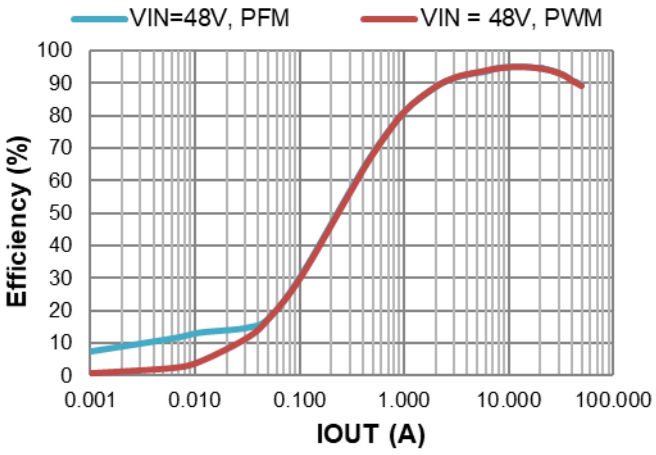


Figure 10. Efficiency vs. IOUT, V_O = 5.0V/50A, 100kHz

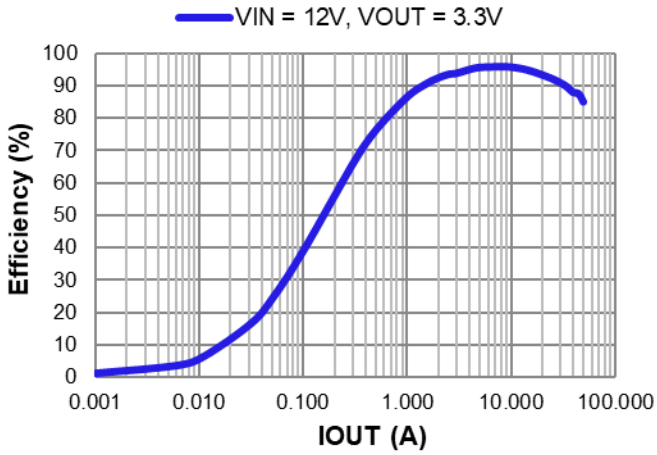


Figure 11. Efficiency vs. IOUT, V_O = 3.3V/50A, 100kHz, PWM

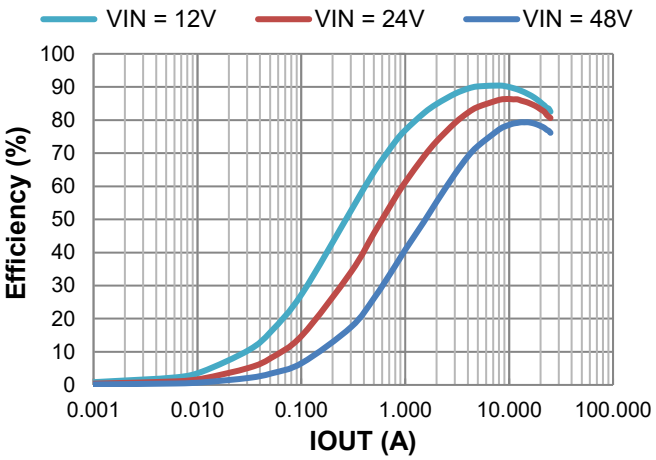


Figure 12. Efficiency vs. IOUT, V_O = 0.8V/25A, 100kHz, PWM

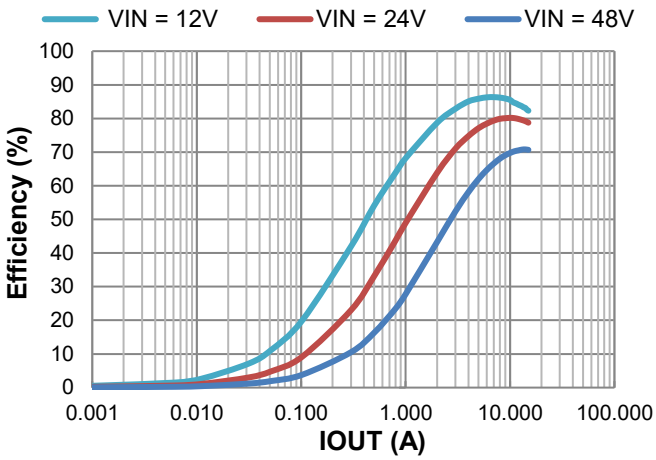


Figure 13. Efficiency vs. IOUT, V_O = 0.5V/20A, 100kHz, PWM

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

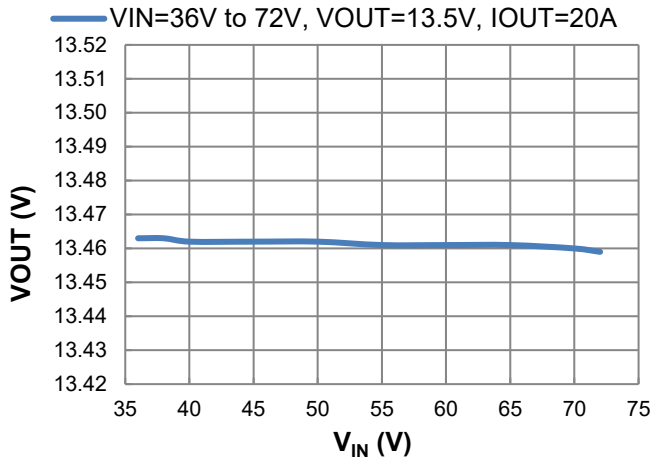


Figure 14. Line Regulation – V_{OUT} (V)

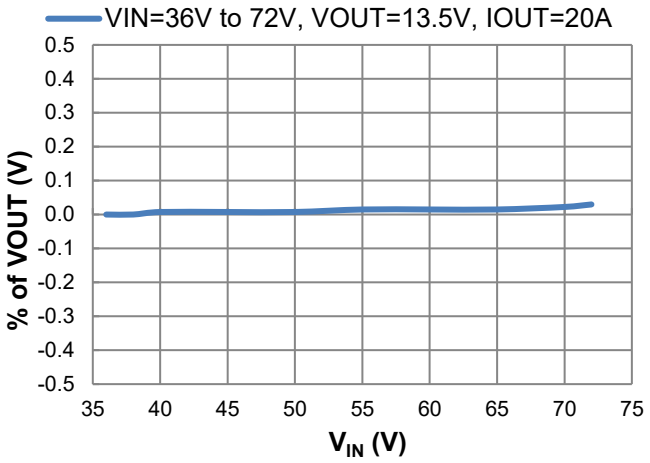


Figure 15. Line Regulation – V_{OUT} (%)

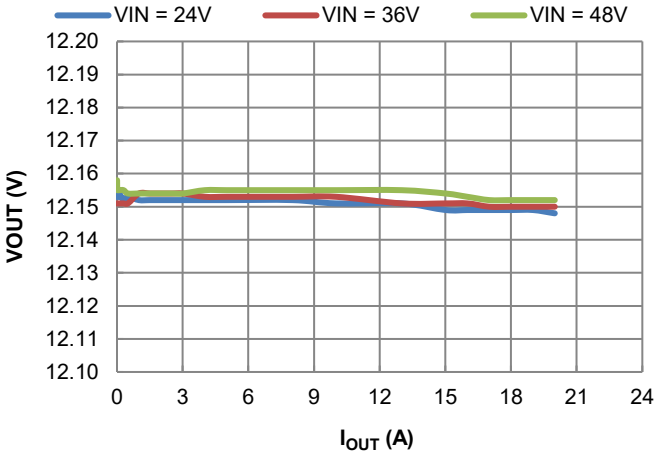


Figure 16. Load Regulation (60V HS/LS FETs)

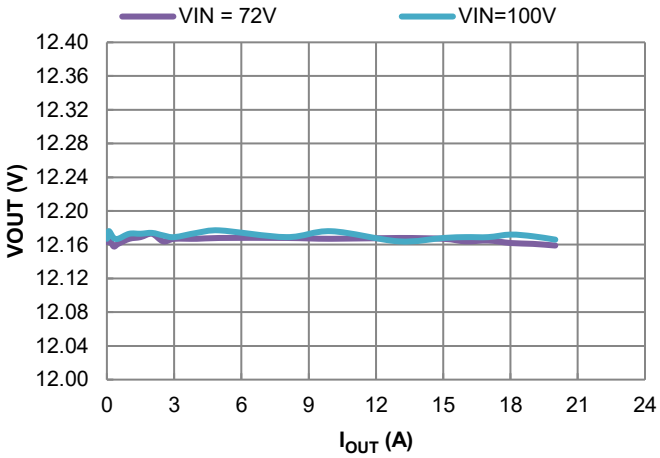


Figure 17. Load Regulation (150V HS/ 120V LS FETs)

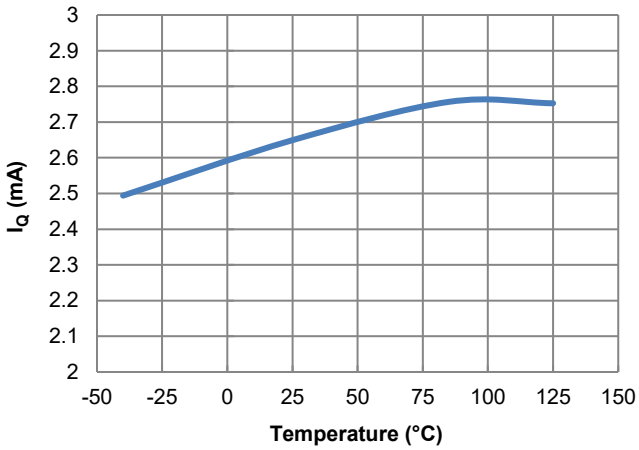


Figure 18. I_Q vs. Temperature, No Load, Non-Switching

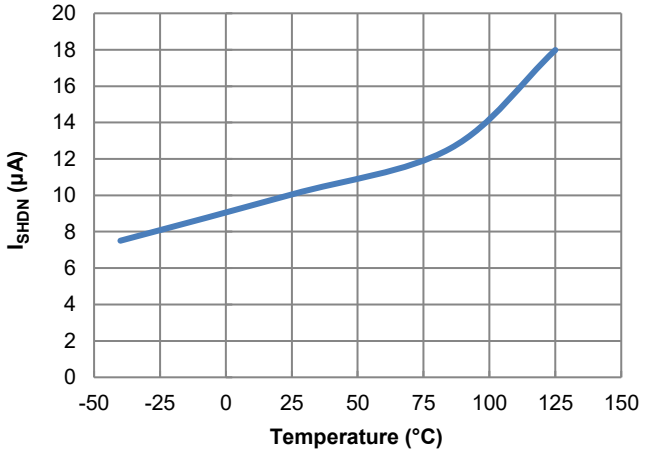


Figure 19. I_{SHDN} vs. Temperature, V_{EN} = 0, I_{OUT} = 0

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

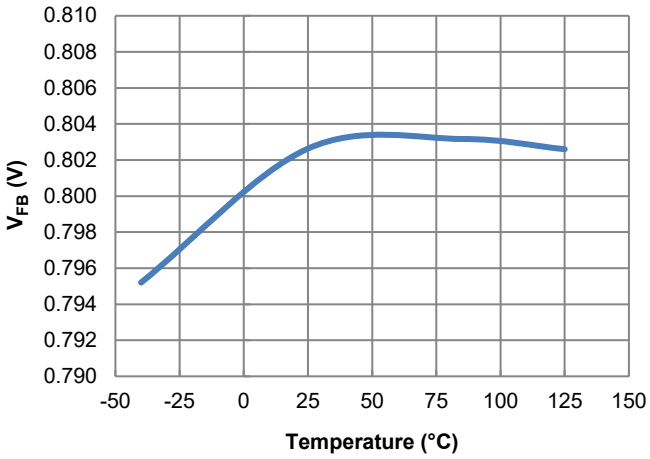


Figure 20. Feedback Voltage vs. Temperature

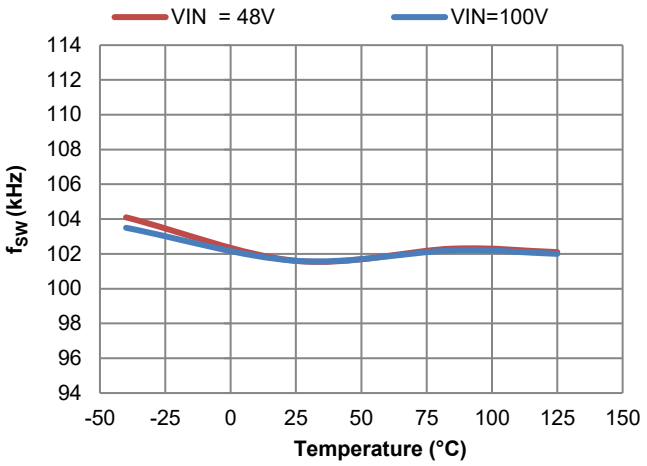


Figure 21. f_{SW} vs. Temperature, f_{SW} = 100kHz

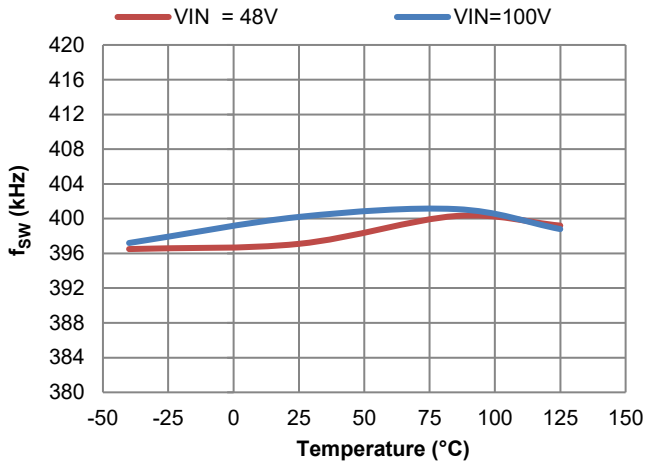


Figure 22. f_{SW} vs. Temperature, f_{SW} = 400kHz

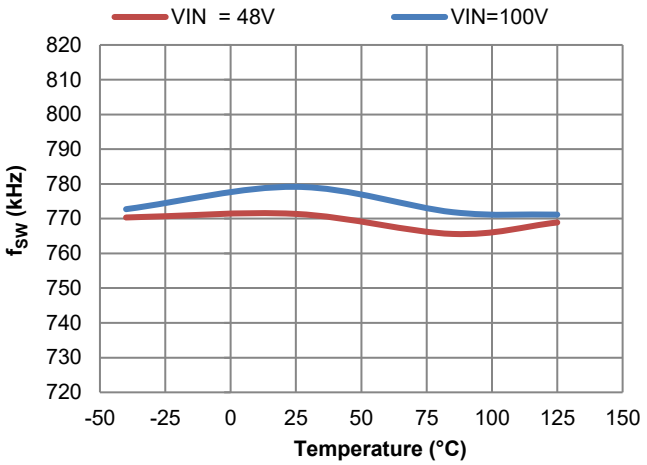


Figure 23. f_{SW} vs. Temperature, f_{SW} = 780kHz

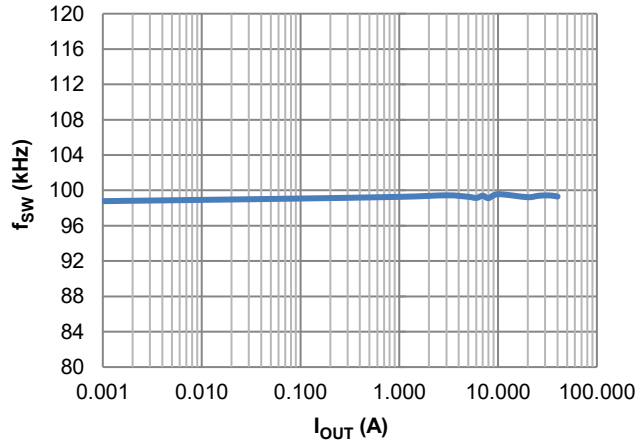


Figure 24. f_{SW} vs. Load, PFM

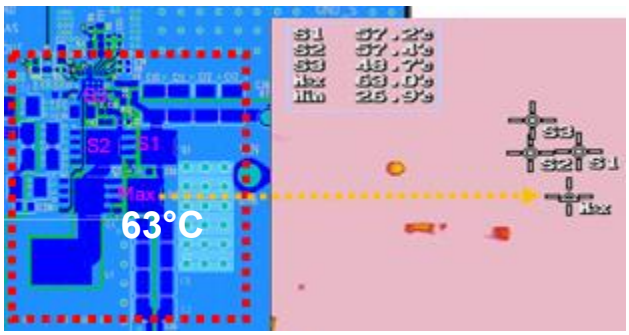


Figure 25. T_{C-MAX} = +63°C (140 Hours), V_{IN} = 48V, V_{OUT} = 13.5V/20A

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

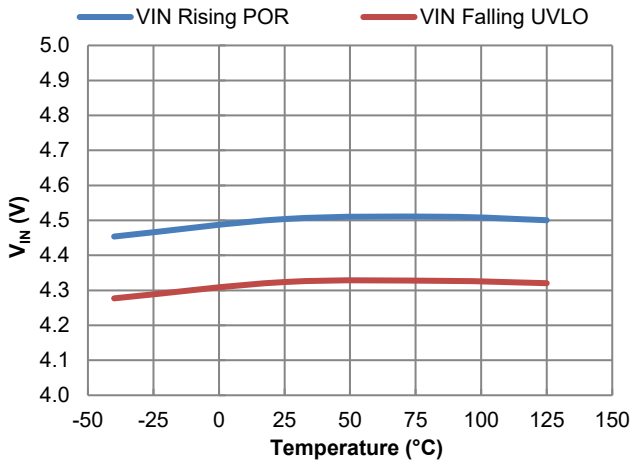


Figure 26. V_{IN} POR and UVLO vs. Temperature

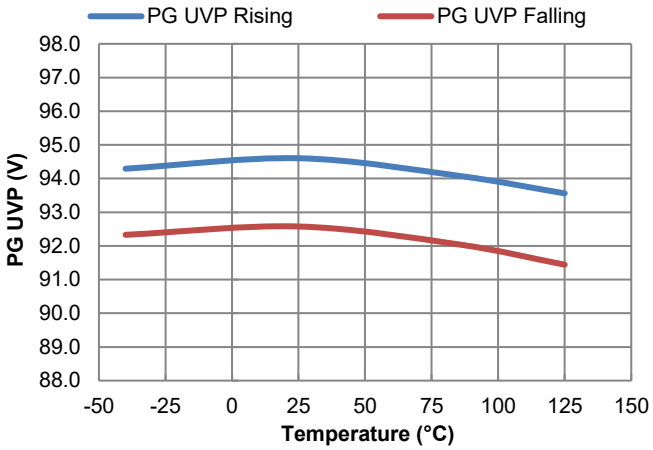


Figure 27. PG UVP Thresholds vs. Temperature

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 400kHz, PWM, BOM = Table 2, unless otherwise specified.) (continued)

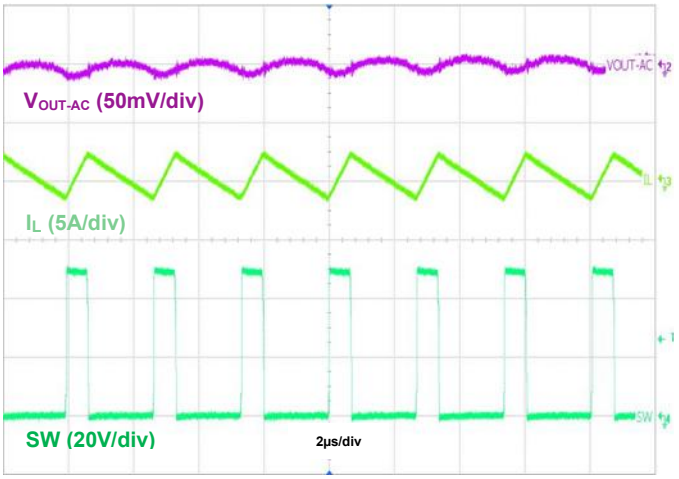


Figure 28. Output Voltage Ripple, I_{OUT} = 0, PWM @400kHz

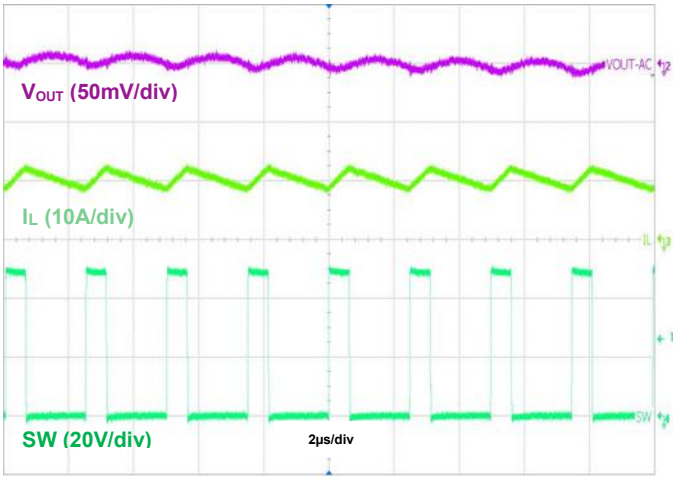


Figure 29. Output Voltage Ripple, I_{OUT} = 10A, PWM @400kHz

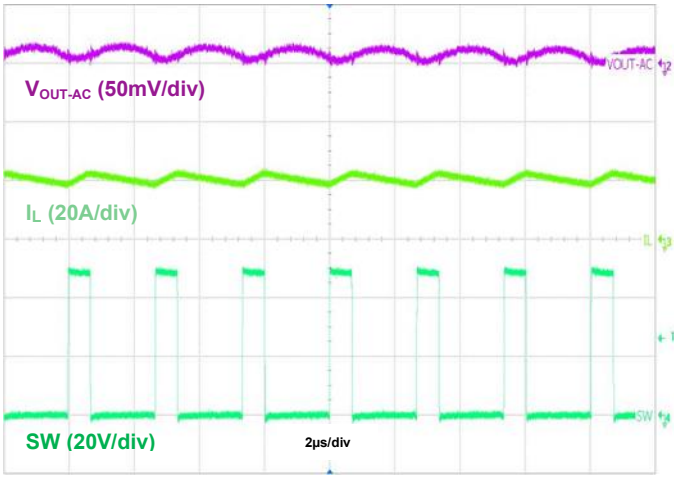


Figure 30. Output Voltage Ripple, I_{OUT} = 20A, PWM @400kHz

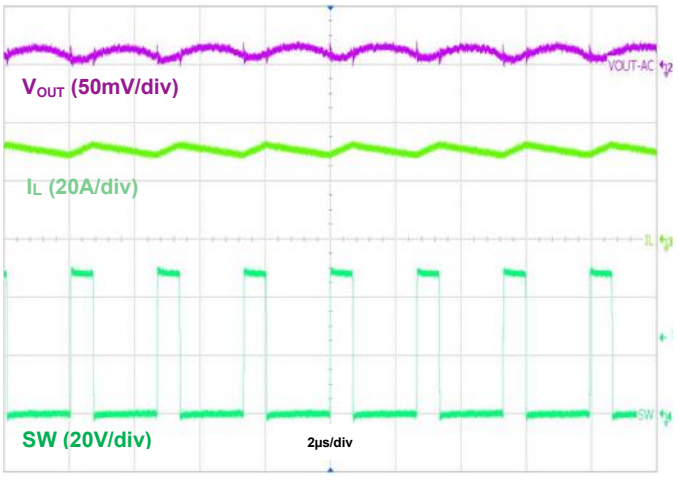


Figure 31. Output Voltage Ripple, I_{OUT} = 30A, PWM @400kHz

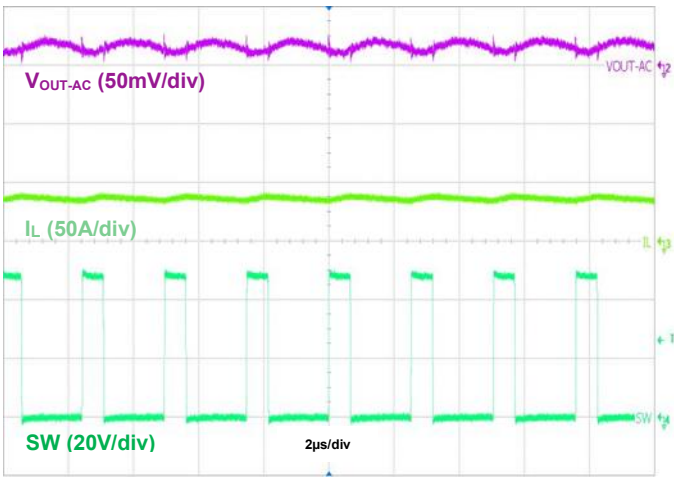


Figure 32. Output Voltage Ripple, I_{OUT} = 35A, PWM @400kHz

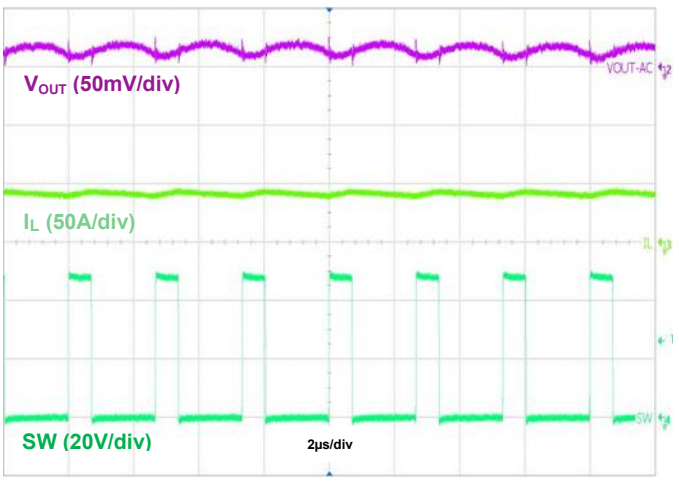


Figure 33. Output Voltage Ripple, I_{OUT} = 40A, PWM @400kHz

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 400kHz, PFM, BOM = Table 2, unless otherwise specified.) (continued)

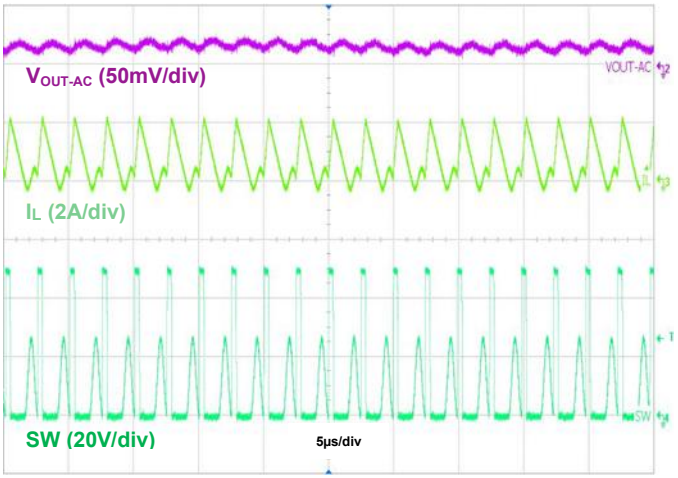


Figure 34. Output Voltage Ripple, I_{OUT} = 0, PFM @400kHz

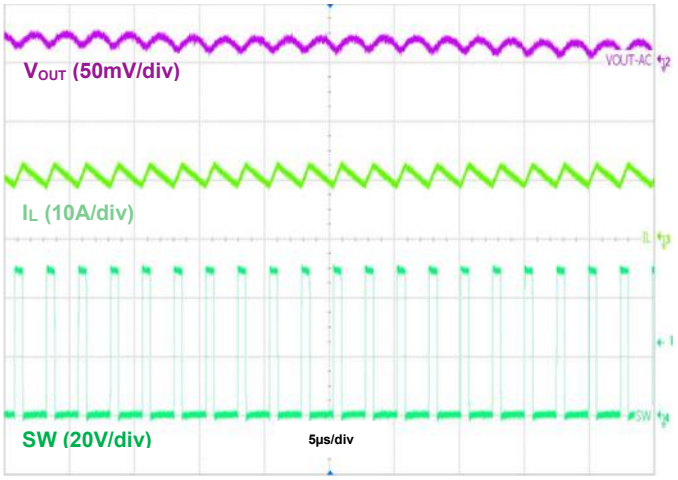


Figure 35. Output Voltage Ripple, I_{OUT} = 10A, PFM @400kHz

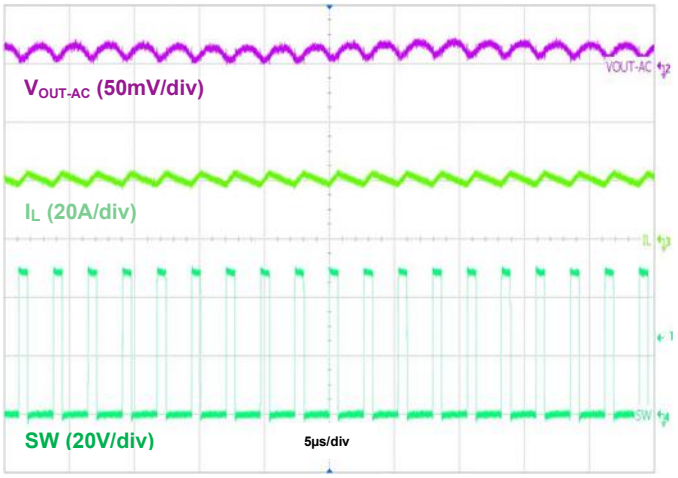


Figure 36. Output Voltage Ripple, I_{OUT} = 20A, PFM @400kHz

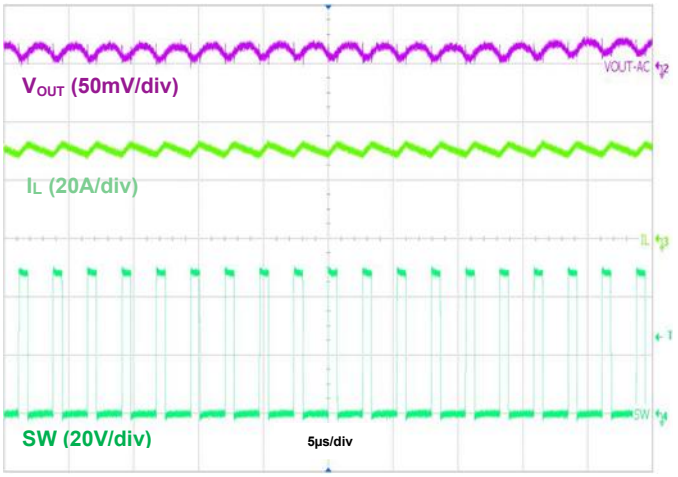


Figure 37. Output Voltage Ripple, I_{OUT} = 30A, PFM @400kHz

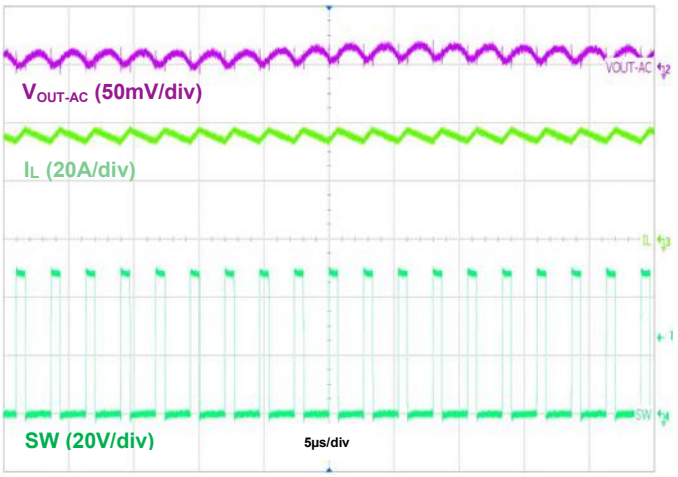


Figure 38. Output Voltage Ripple, I_{OUT} = 35A, PFM @400kHz

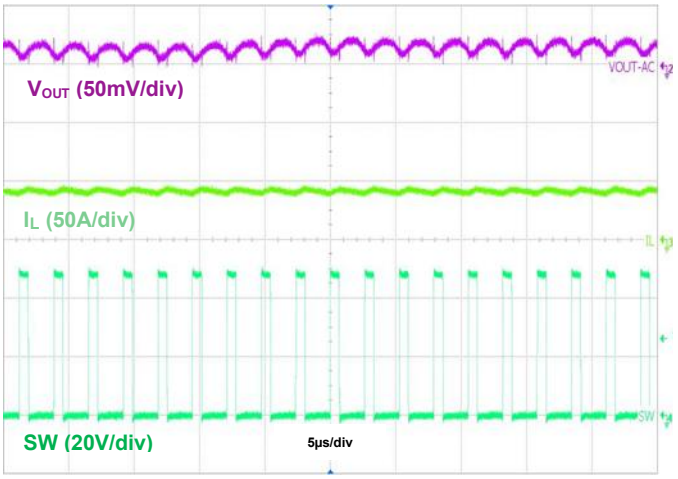


Figure 39. Output Voltage Ripple, I_{OUT} = 40A, PFM @400kHz

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, PWM, BOM = Table 2, unless otherwise specified.) (continued)

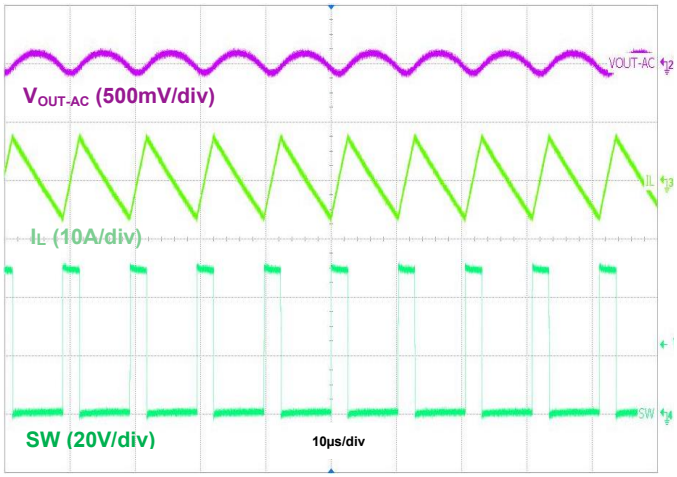


Figure 40. Output Voltage Ripple, I_{OUT} = 0, PWM @100kHz

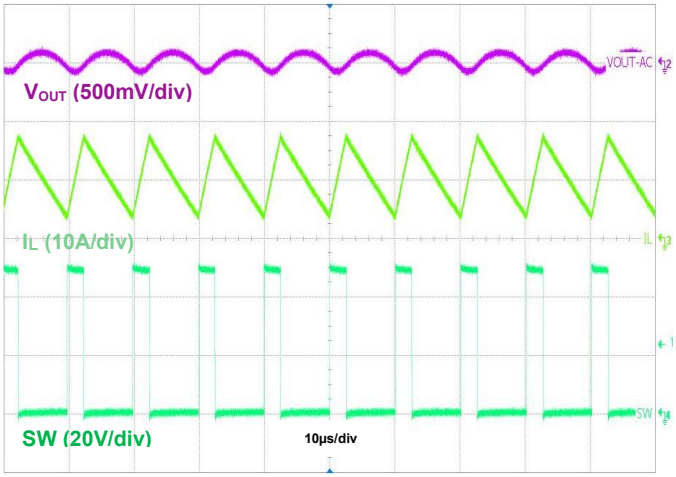


Figure 41. Output Voltage Ripple, I_{OUT} = 10A, PWM @100kHz

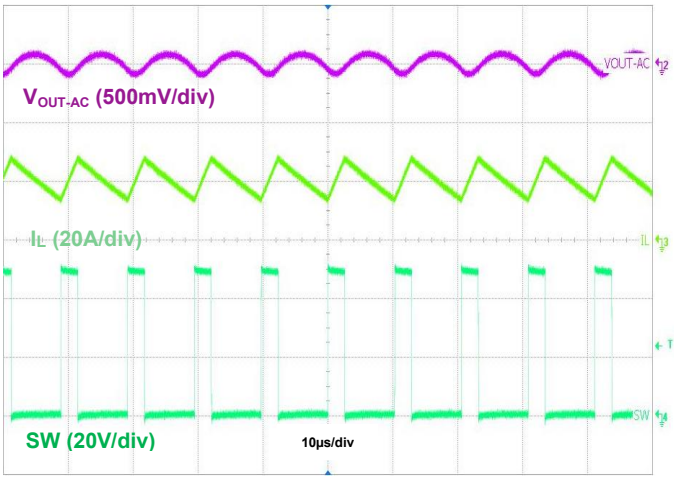


Figure 42. Output Voltage Ripple, I_{OUT} = 20A, PWM @100kHz

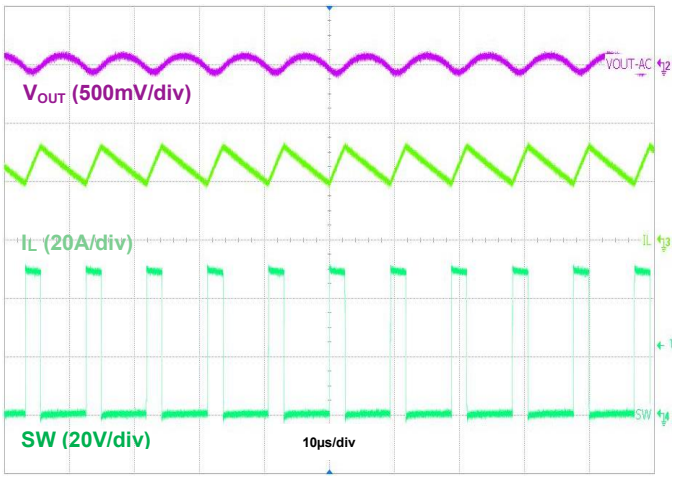


Figure 43. Output Voltage Ripple, I_{OUT} = 25A, PWM @100kHz

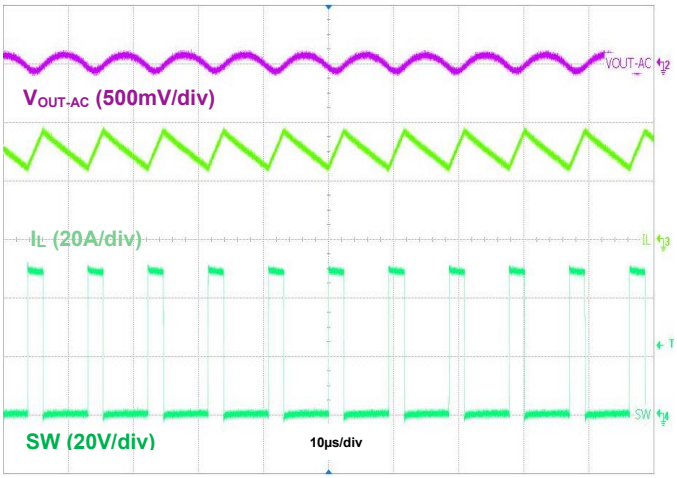


Figure 44. Output Voltage Ripple, I_{OUT} = 30A, PWM @100kHz

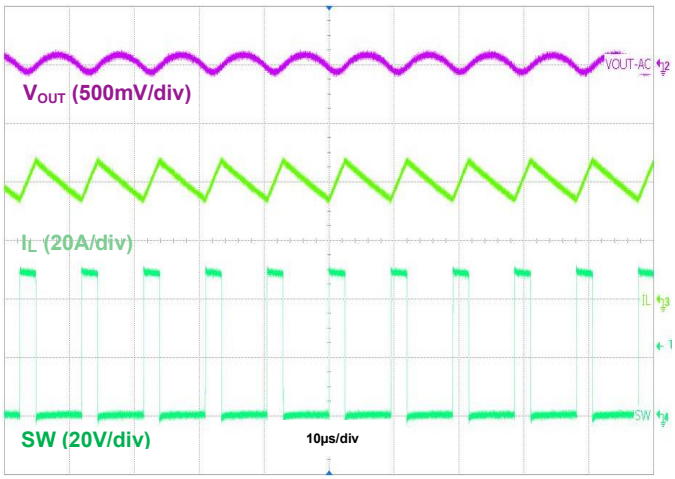


Figure 45. Output Voltage Ripple, I_{OUT} = 40A, PWM @100kHz

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, PFM, BOM = Table 2, unless otherwise specified.) (continued)

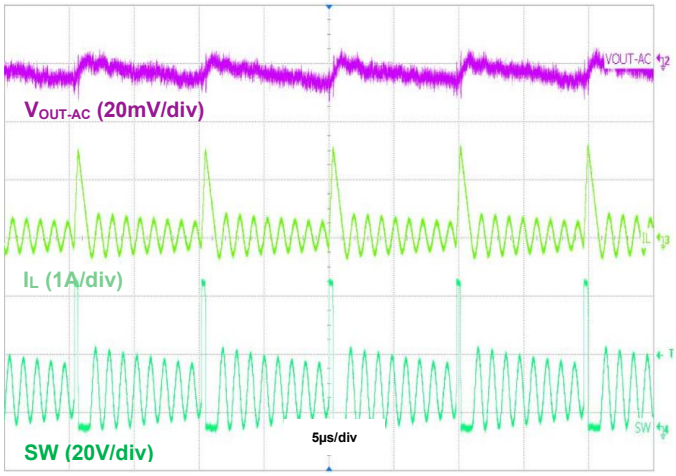


Figure 46. Output Voltage Ripple, I_{OUT} = 50mA, PFM @100kHz

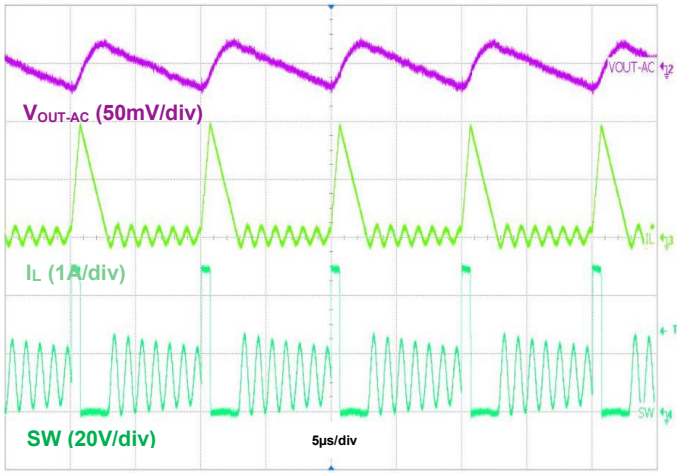


Figure 47. Output Voltage Ripple, I_{OUT} = 500mA, PFM @100kHz

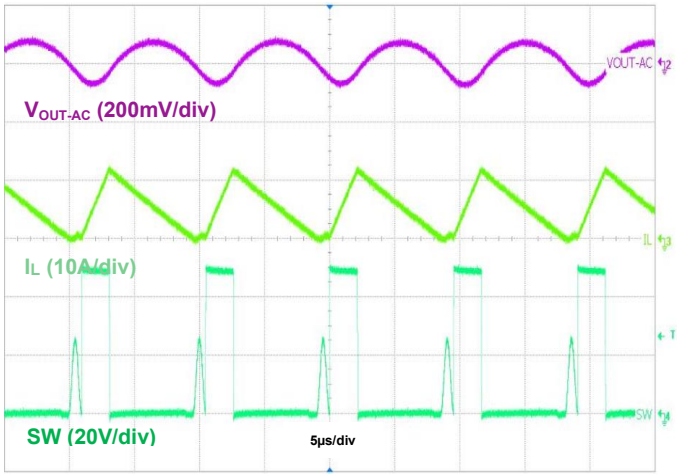


Figure 48. Output Voltage Ripple, I_{OUT} = 5A, PFM @100kHz

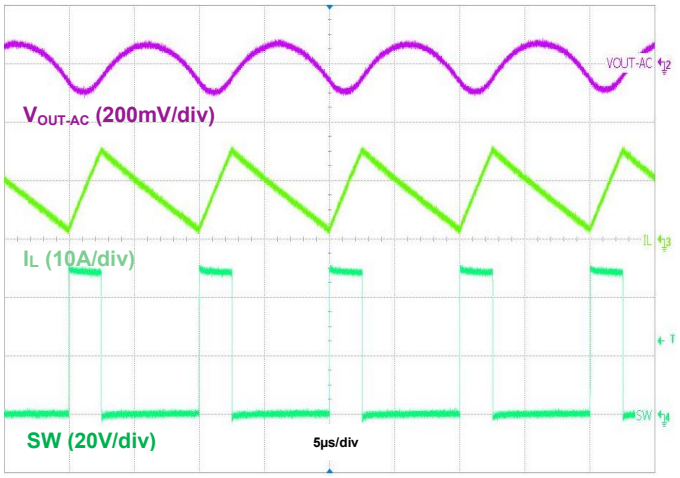


Figure 49. Output Voltage Ripple, I_{OUT} = 8A, PFM @100kHz

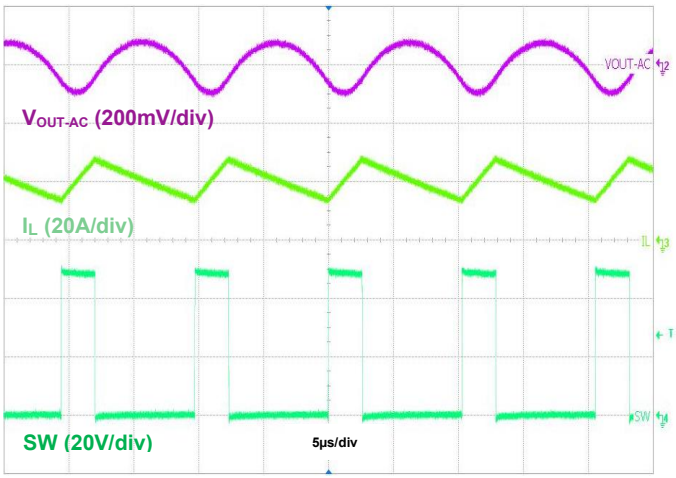


Figure 50. Output Voltage Ripple, I_{OUT} = 20A, PFM @100kHz

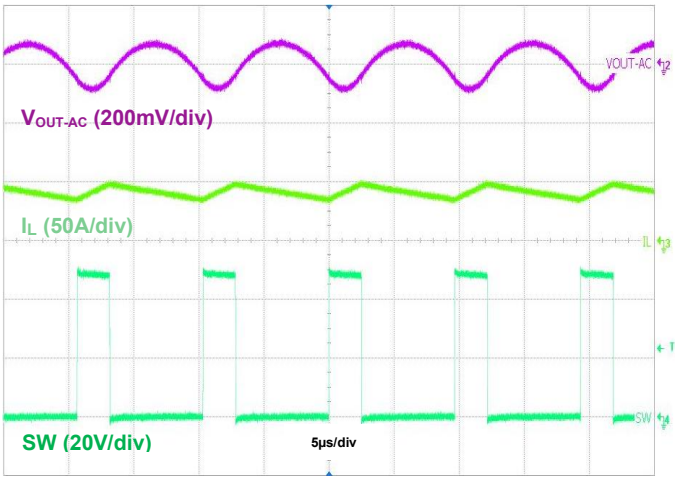


Figure 51. Output Voltage Ripple, I_{OUT} = 40A, PFM @100kHz

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, Set R_{FS} = 24.5kΩ at 400kHz, external SYNCIN, BOM = Table 2, unless otherwise specified.) (continued)

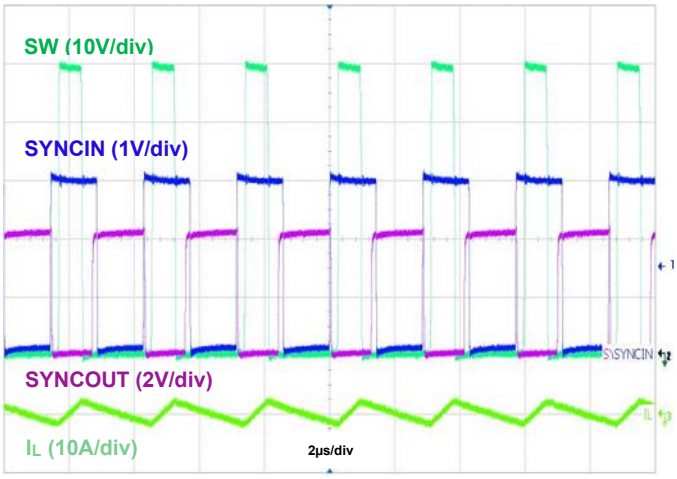


Figure 52. SYNCIN at fsw = 350kHz, I_{OUT} = 0

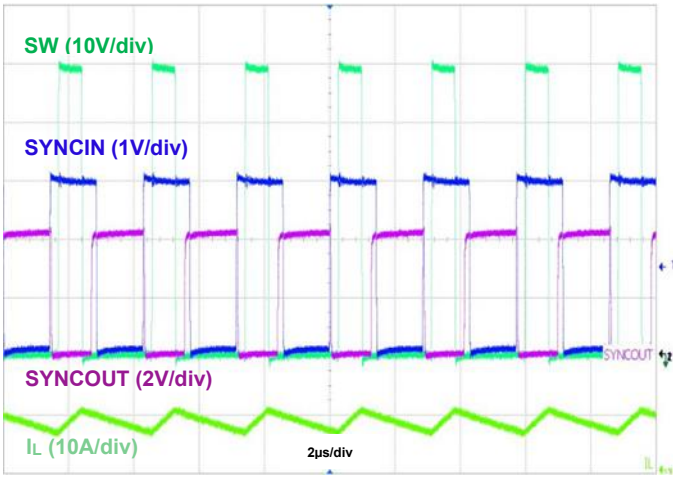


Figure 53. SYNCIN at fsw = 350kHz, I_{OUT} = 8A

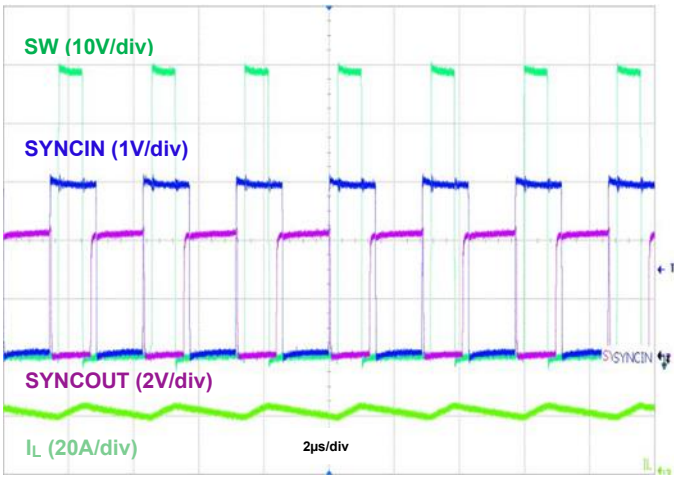


Figure 54. SYNCIN at fsw = 350kHz, I_{OUT} = 20A

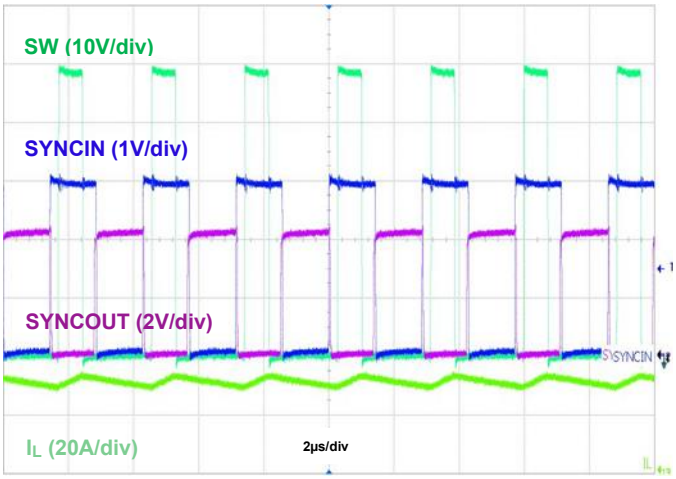


Figure 55. SYNCIN at fsw = 350kHz, I_{OUT} = 30A

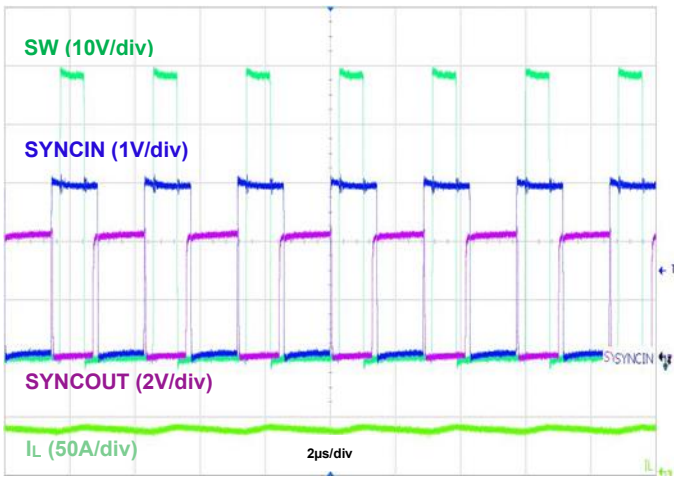


Figure 56. SYNCIN at fsw = 350kHz, I_{OUT} = 35A

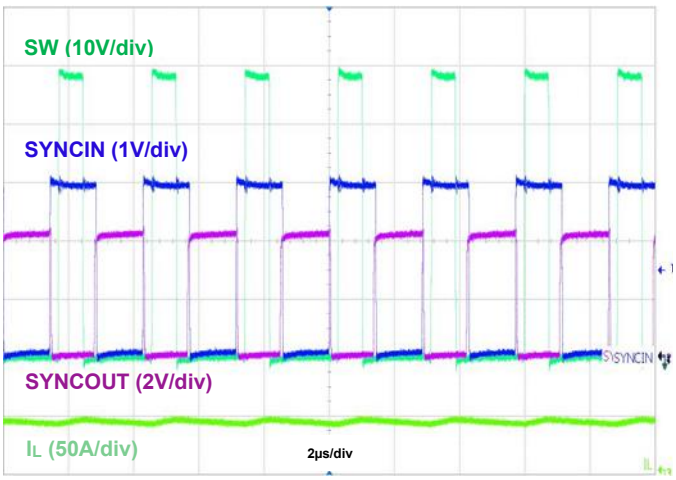


Figure 57. SYNCIN at fsw = 350kHz, I_{OUT} = 40A

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 400kHz, BOM = Table 2, unless otherwise specified.) (continued)

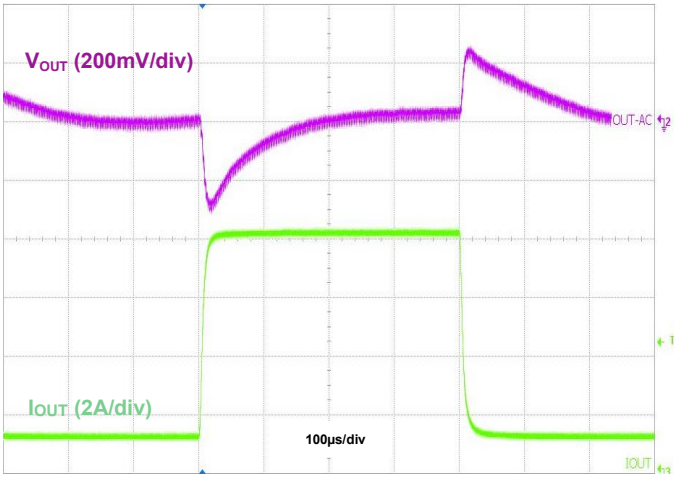


Figure 58. Load Transient, I_{OUT} = 1A to 8A to 1A

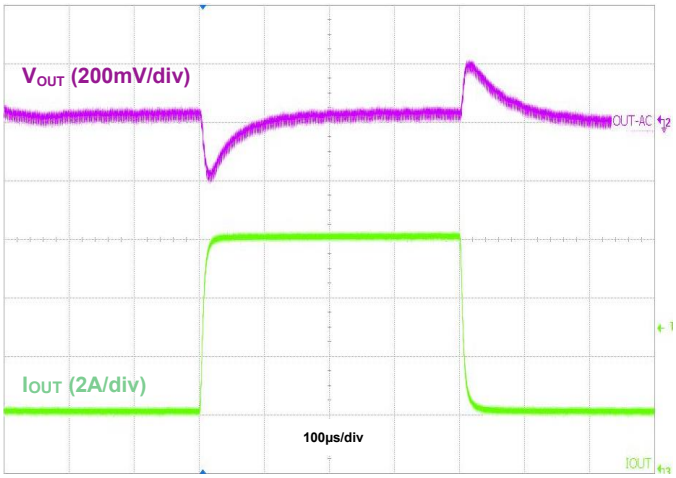


Figure 59. Load Load Transient, I_{OUT} = 2A to 8A to 2A

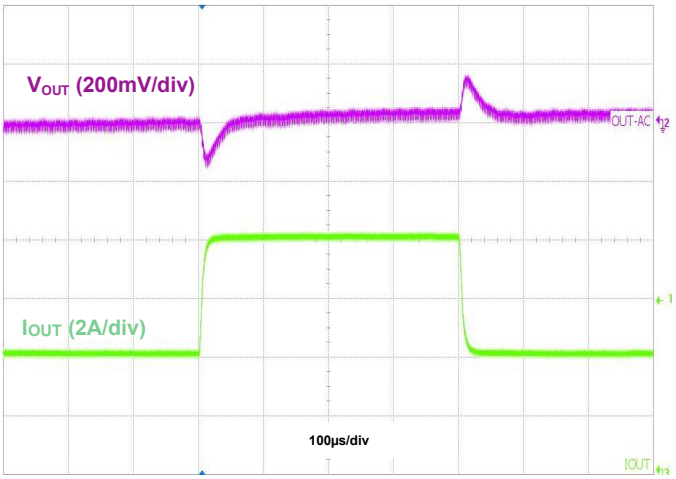


Figure 60. Load Transient, I_{OUT} = 4A to 8A to 4A

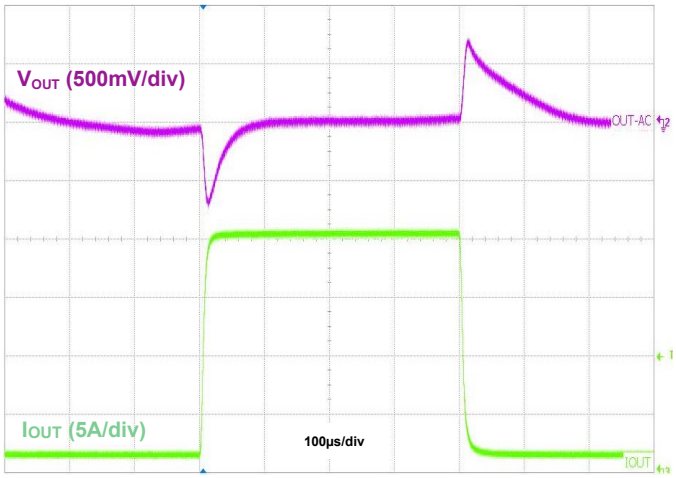


Figure 61. Load Transient, I_{OUT} = 1A to 20A to 1A

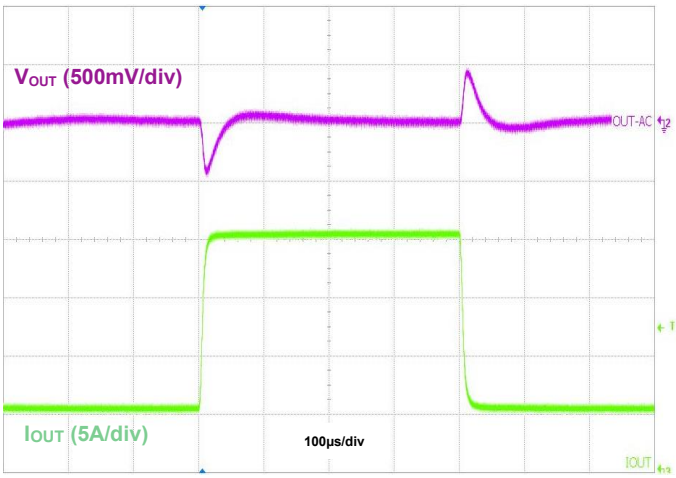


Figure 62. Load Transient, I_{OUT} = 5A to 20A to 5A

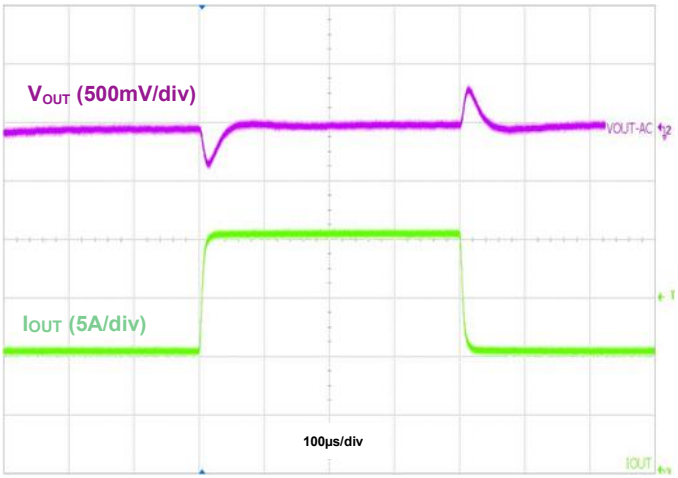


Figure 63. Load Transient, I_{OUT} = 10A to 20A to 10A

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

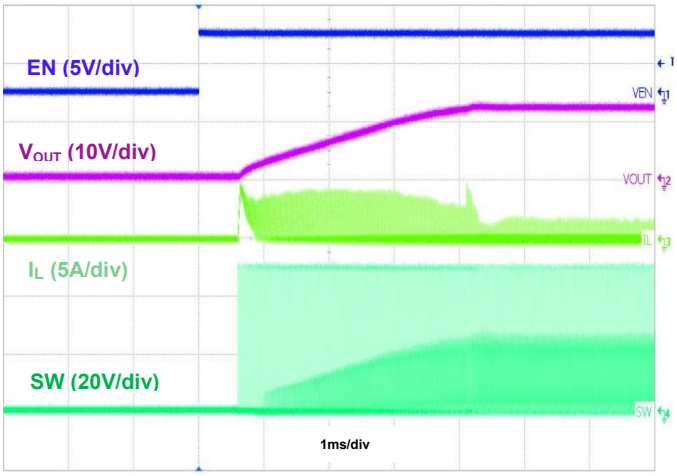


Figure 64. Startup using EN, I_{OUT} = 50mA

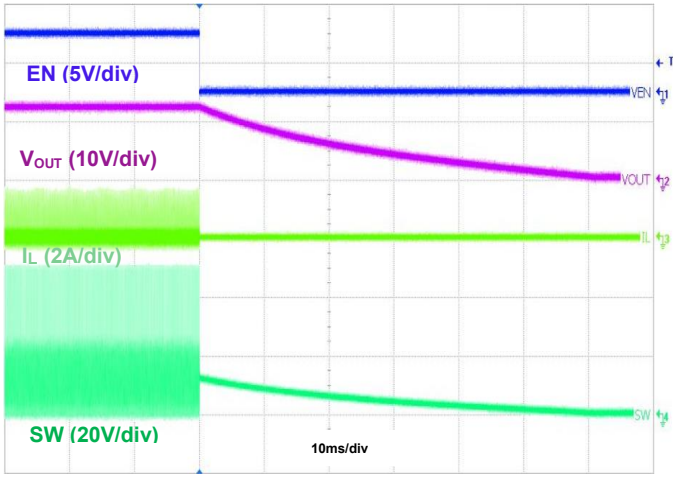


Figure 65. Shutdown using EN, I_{OUT} = 50mA

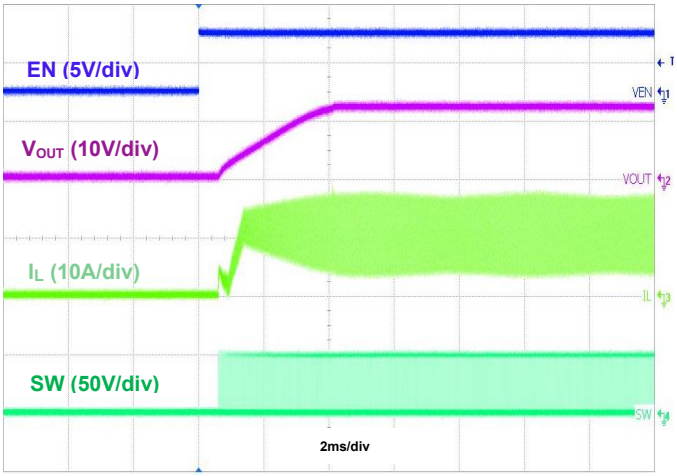


Figure 66. Startup using EN, I_{OUT} = 10A

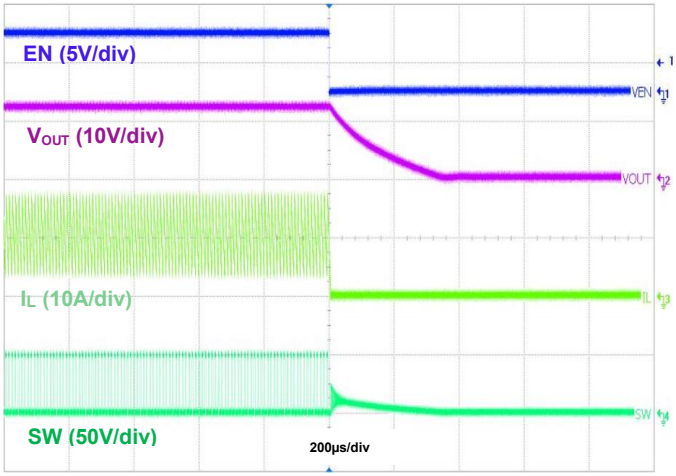


Figure 67. Shutdown using EN, I_{OUT} = 10A

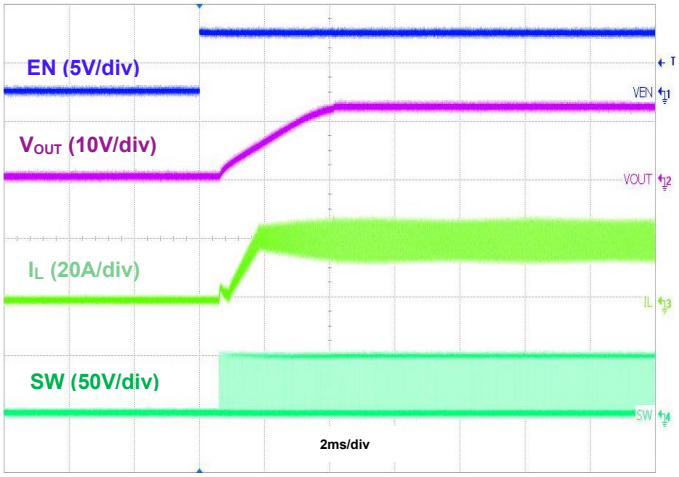


Figure 68. Startup using EN, I_{OUT} = 20A

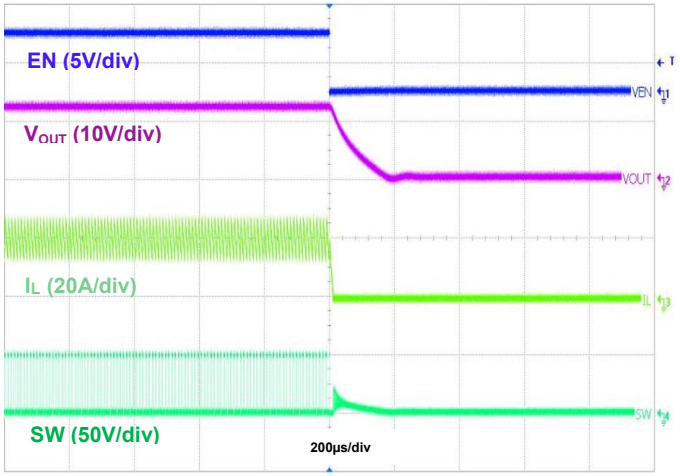


Figure 69. Shutdown using EN, I_{OUT} = 20A

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 2, unless otherwise specified.) (continued)

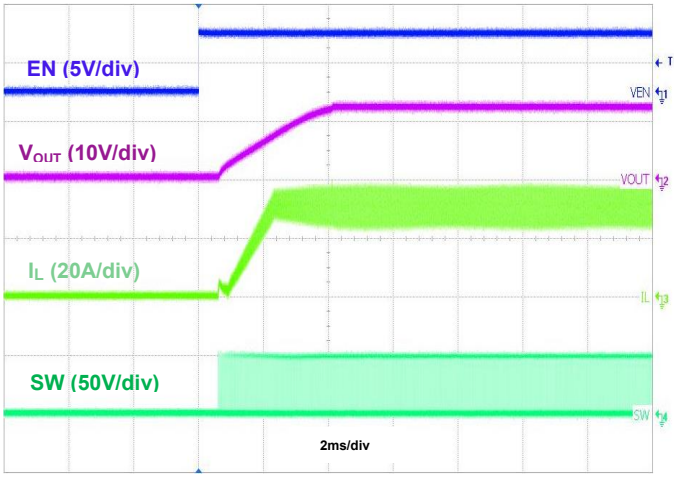


Figure 70. Startup using EN, I_{OUT} = 30A

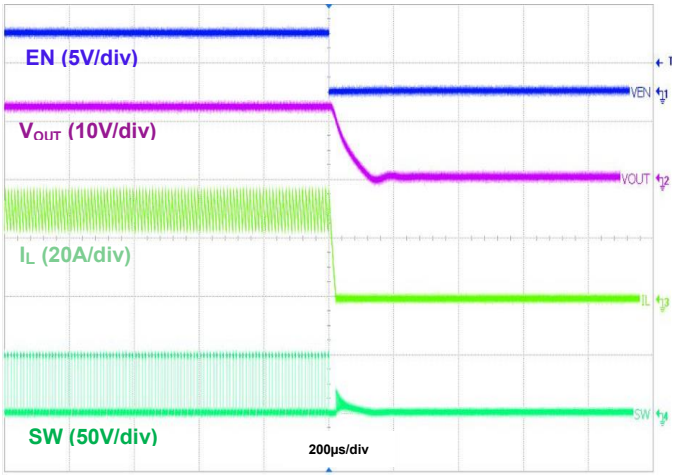


Figure 71. Shutdown using EN, I_{OUT} = 30A

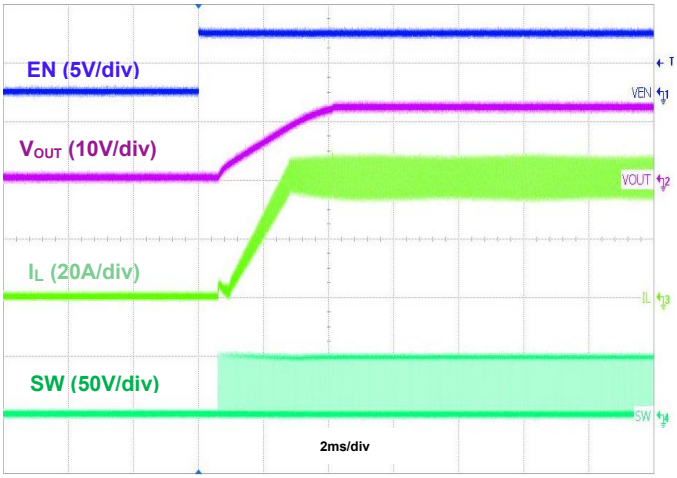


Figure 72. Startup using EN, I_{OUT} = 40A

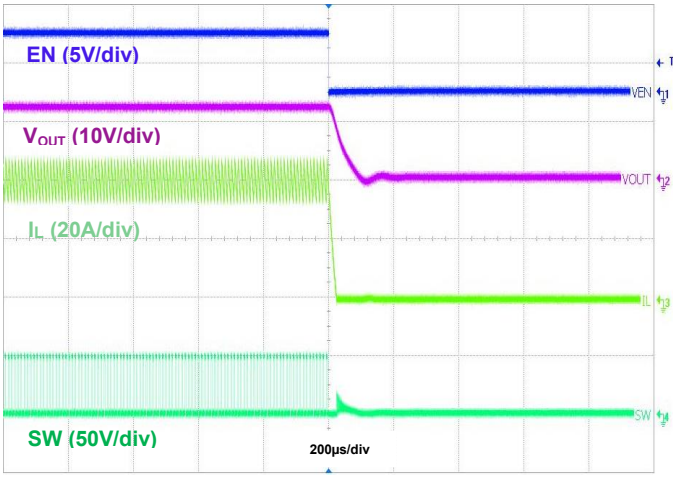


Figure 73. Shutdown using EN, I_{OUT} = 40A

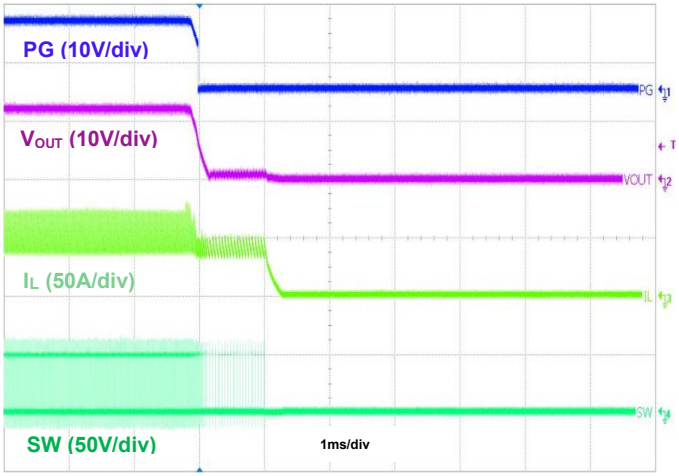


Figure 74. Output Short Protection, I_{OUT} = 0, R_{LIM} = 620Ω

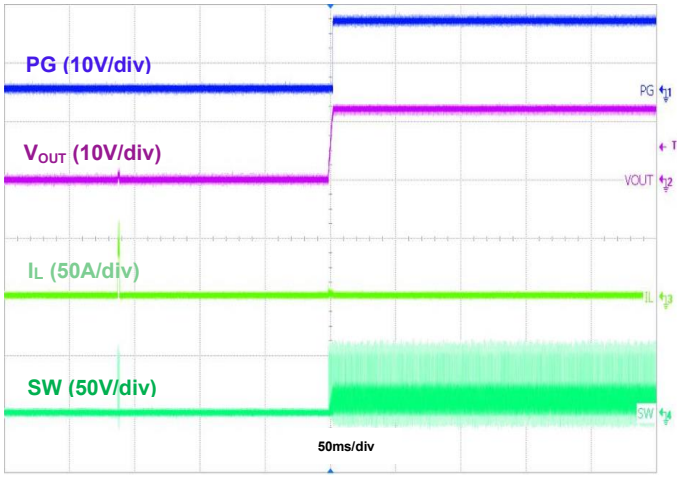


Figure 75. Output Short Recovery, I_{OUT} = 0, R_{LIM} = 620Ω

Typical Performance Characteristics (@ T_A = +25°C, V_{IN} = 48V, V_{OUT} = 12V, f_{SW} = 100kHz, BOM = Table 1, unless otherwise specified.) (continued)

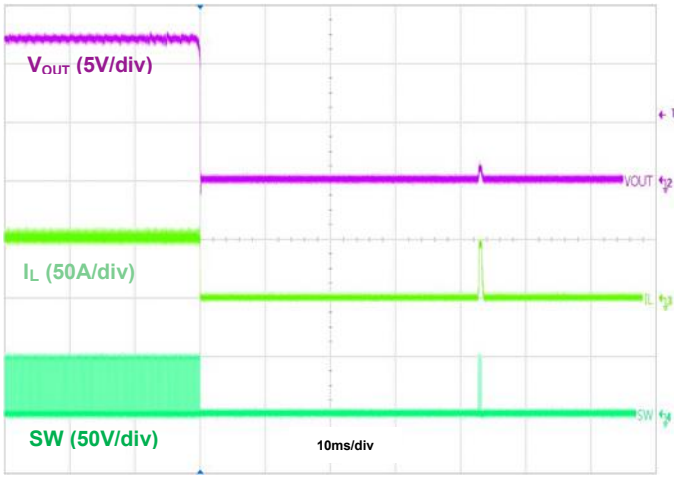


Figure 76. Output Short Protection, I_{OUT} = 0, R_{LIM} = 1.1kΩ

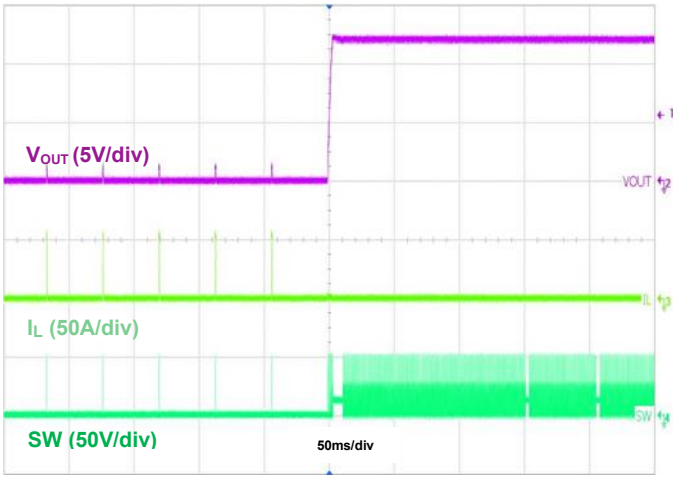


Figure 77. Output Short Recovery, I_{OUT} = 0, R_{LIM} = 1.1kΩ

Application Information

Overview

The AP6ACO5 is a synchronous buck controller, adopting voltage mode with input feedforward, which implements a high efficiency step-down DCDC power supply for excellent line transient response over a 5.5V to 100V wide VIN range. The output voltage range is from 0.8V to 60V. Voltage-mode control supports wide duty cycle range for high input/output voltage conversion ratio and low dropout applications as well. It continues to operate during input voltage drops as low as 4.5V, at nearly 100% duty cycle if needed, making it an excellent choice for high performance automotive as well as industrial control, robotics, Datacom, and networking communication infrastructure.

The device drives external high-side and low-side NMOS power switches with robust 7.5V gate drivers suitable for standard threshold MOSFETs. The AP6ACO5 supports Forced-PWM (PWM) and Diode Emulation Mode. PWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition. The operating frequency is programmable from 100kHz to 1.2MHz and can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. The device features clock synchronization with clock input and clock output. A 180° out-of-phase clock output relative to the internal oscillator at SYNCOUT configures cascaded or multichannel power supplies to reduce input capacitor ripple current and EMI filter size.

The AP6ACO5 features Frequency Spread Spectrum FSS with ±6% jittering span of the setting switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

An external voltage or the output of the buck converter source can power internal VCC via BIAS feature to help increase overall efficiency. This decreases internal self-heating from power dissipated within the internal VCC LDO especially with 5V output voltage.

Cycle-by-cycle current limiting and over current protection can be implemented with either sensing the low-side FET $R_{DS(ON)}$ or a current sense resistor. The AP6ACO5 contain additional features for flexibility and robust design including a configurable soft start, an open-drain power-good monitor for fault reporting and output monitoring, monotonic start-up into pre-biased loads, integrated VCC bias supply regulator and BST diode, external power supply tracking, precision enable input with hysteresis for adjustable line under voltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The AP6ACO5 controller is available in a 4.5mm × 3.5mm thermally enhanced, 20-pin QFN package.

Input Voltage Range

The AP6ACO5 operational input voltage range is from 5.5V to 100V. The device is intended for step-down conversions from 12V, 24V, 48V, 60V, and 72V unregulated, semi-regulated, or fully regulated supply rails. An internal LDO regulator provides a 7.5V V_{CC} bias rail for the gate drive and control circuits with the input voltage is higher than 7.5V plus the necessary regulator dropout specification.

Output Voltage Regulation Point and Accuracy

The feedback reference voltage at the FB pin is typically 0.8V with a system accuracy over the full junction temperature range of ±1%. The junction temperature range for the device is -40°C to +150°C. The AP6ACO5 is generally capable of providing output voltages in the range of 0.8V to a maximum of 60V or slightly less than VIN depending on switching frequency and load current levels. The output voltage regulation level during normal operation is set by the feedback resistor network, R1 and R2 in Figure 1, connected to the output and FB pin.

High-Voltage Internal VCC Bias Supply Regulator and BIAS Auxiliary Supply

Power for the high-side and low-side MOSFET drivers and most other internal control circuitry is derived from the VCC pin. An internal high-voltage VCC regulator directly connects to input voltage pin, supporting up to 100V. The output of the internal VCC regulator is set to 7.5V. When the input voltage is below the VCC set point level, the VCC output tracks VIN with a small voltage drop. Connect a ceramic decoupling capacitor between 1μF and 4.7μF from VCC to PGND for stability.

The VCC regulator output has a current limit of 40mA (minimum). During power up when the VCC voltage exceeds its rising UVLO threshold of 4.5V, the output is enabled if EN is above 1.2V, and then soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of typical 4.3V or if EN goes into a standby or shutdown state.

To improve the overall efficiency and decrease internal self-heating by power dissipated in the LDO, connecting the output voltage or an auxiliary bias supply rail (up to 13V) to the BIAS pin as shown in Figure 78. If the BIAS pin is tied to an external source larger than 4.7V, then the internal VCC LDO is shut off to save power and an internal switch shorts the BIAS pin to the VCC input. By sourcing from a lower BIAS voltage than VIN, power of the system is reduced.

Application Information (continued)

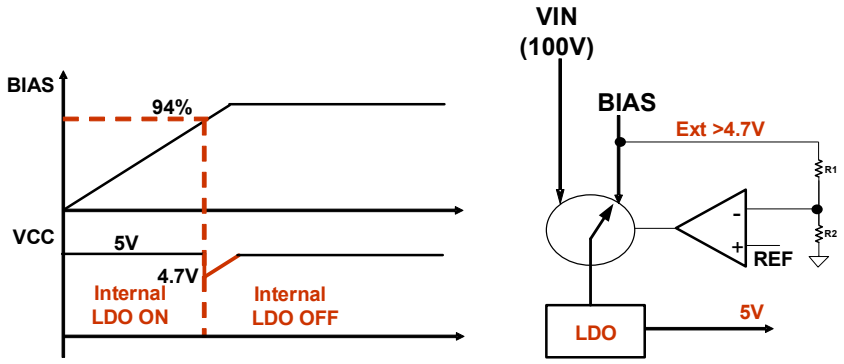


Figure 78. VCC BIAS Supply

Enable and programmable UVLO

The AP6ACO5 can be shut down using the EN pin. Pulling this pin below 1.2V prevents the controller from switching, and less than 0.37V disables most of the internal bias circuitry, including the VCC regulator. The shutdown IQ is about 7.2μA typical at V_{IN} = 48V.

The EN input supports adjustable input under voltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN connects to a comparator-based input referenced to a 1.2V bandgap voltage. An external logic signal can be used to drive the EN input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the AP6ACO5 is to connect EN directly to VIN. This allows self-power-up of the regulator when VCC is within its valid operating range. However, many applications benefit from using a resistor divider R5 and R6 as shown in Figure 79 to establish a precision UVLO level. Use Equation 1 and Equation 2 to calculate the UVLO resistors given the required input power-up and power-down voltages.

$$R5 = \frac{V_{ON} - V_{OFF}}{10\mu A} \quad \text{Eq. 1}$$

$$R6 = \frac{1.26 \cdot R5}{V_{ON} - 1.26V} \quad \text{Eq. 2}$$

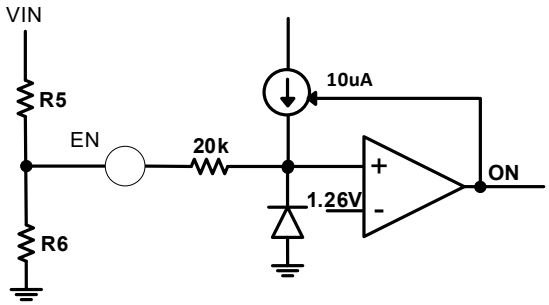


Figure 79. Programming UVLO

Soft-Start, Tracking, Sequencing, and Disable

The enable (EN) input allows the user to control turning on or off the regulator. Once the voltage on the EN pin is above its threshold, the buck controller powers up and soft-start begins.

The SS/TRK pin voltage controls start-up of output voltage. After the EN pin exceeds its rising threshold of 1.2V, the AP6ACO5 begins regulating the output to the level dictated by the feedback resistor network and SS/TRK voltage. A 10μA current source charges the soft-start capacitor connecting SS/TRK pin. Soft start avoids inrush current because of high output capacitance to avoid an overcurrent condition. The inrush stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by Equation 6.

$$C_{SS}\ (nF) = 12.5 * t_{SS}\ (ms) \quad \text{Eq. 3}$$

The SS/TRK pin is internally clamped to VFB + 115mV to allow a quick soft-start recovery from an overload event. There is a 2mA discharge FET to force the SS voltage to start from 0V. The clamp circuit requires a soft-start capacitance greater than 2nF for stability.

Application Information (continued)

Soft-Start, Tracking, Sequencing, and Disable (continued)

The SS/TRK pin also serves as a tracking pin when specific master-slave power supplies sequencing is required. Coincident, ratiometric, and offset tracking (see Power Good Monitor section) modes are achieved by various simple configurations. Ratiometric tracking could be achieved by connecting all the SS/TR pins of each circuit using a common Css. Ratiometric tracking is achieved in Figure 80 by using the same value for the soft-start capacitor on each power rail.

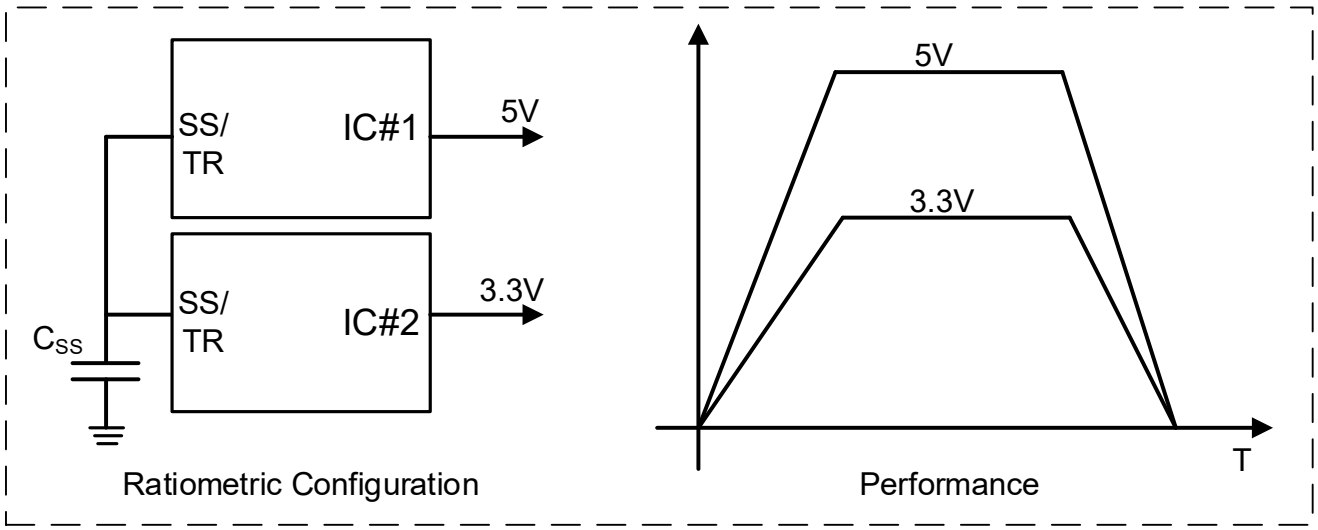


Figure 80. Ratiometric Configuration

By connecting a feedback network from the higher output voltage as shown in the Figure 81 below, coincidental track is implemented. The ratio of R7 and R8 should match with the ratio of feedback resistor divider of IC#2.

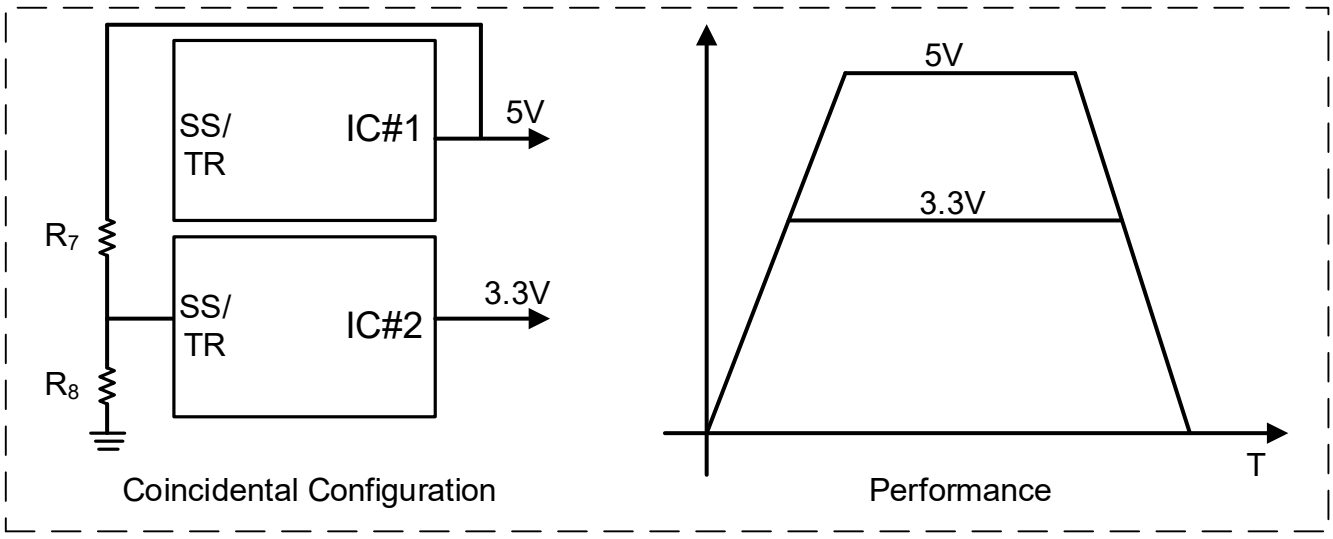


Figure 81. Coincidental Configuration

Application Information (continued)

Power Good Monitor, PG

The AP6ACO5 provides a PG indicator pin to indicate when the output voltage is within a regulation window. When the FB voltage exceeds 94% of the internal reference VREF, the internal PG switch turns off and PG can be pulled high by the external pull-up. If the FB voltage falls below 92% of VREF, the internal PG switch turns on, and PG is pulled low to indicate that the output voltage is out of regulation.

Similarly, when the FB voltage exceeds 108% of VREF, the internal PG switch turns on, pulling PG low. If the FB voltage subsequently falls below 105% of VREF, the PG switch is turned off and PG is pulled high. PG has a built-in deglitch delay of 25μs.

Use the PG signal as shown in Figure 82 for start-up sequencing of downstream converters, fault protection, and output monitoring. PG is an open-drain output that requires a pull-up resistor to a DC power supply not greater than 13V. The typical range of pull-up resistance is 10kΩ to 100kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pull-up rail.

Figure 82 illustrates output sequencing.

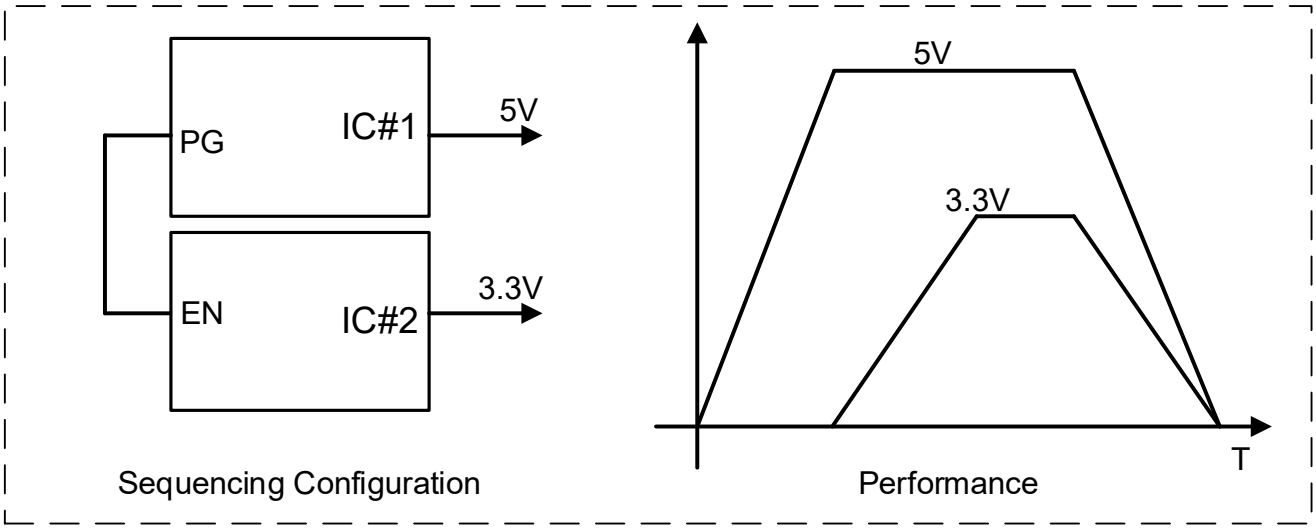


Figure 82. Sequencing Configuration

Switching Frequency and Clock Synchronization

To adjust frequency for optimizing external components for various applications, the AP6ACO5 can connect a resistor from the R_{FS} pin to AGND or synchronize the AP6ACO5 to an external clock signal through the SYNCIN pin.

A free-running switching frequency can be programmed from 100kHz to 1.2MHz by using a resistor from the R_{FS} pin to AGND. The frequency set resistance R_{FS} is calculated by Equation 4. Standard-value resistors for common switching frequencies are given in Table 1.

$$R_{FS}[k\Omega] = \frac{10^4}{FS[kHz]} \quad \text{Eq. 4}$$

Switching Frequency (KHz)	R_{FS} (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10
1100	8.06

Table 1. Frequency Set Resistor R_{FS}

Application Information (continued)

Switching Frequency and Clock Synchronization (continued)

For applications with critical frequency or interference requirements, an external clock source connected to the SYNCIN pin can be used to synchronize the high-side power device turn-on to the rising edge of the clock. The rising edge of SW voltage is phase delayed relative to SYNCIN by approximately 100ns. The AP6ACO5 operates in forced continuous mode when it is synchronized to the external clock. Requirements for the external clock SYNC signal are:

- Clock frequency range: 100kHz to 1MHz
- Clock frequency: -20% to +50% of the free-running frequency set by R_{FS}
- Clock maximum voltage amplitude: 13V
- Clock minimum pulse width: 50ns

Frequency Spread Spectrum

To reduce EMI, the AP6ACO5 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the programmed switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequencies programmed by resistor placed at R_{FS} pin or by using an external clock synchronization application.

Gate Drivers

The AP6ACO5 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{CC} = 7.5V, the low-side driver has a low impedance pulldown path of 0.6Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.3Ω and 0.6Ω pull-up and pull-down impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

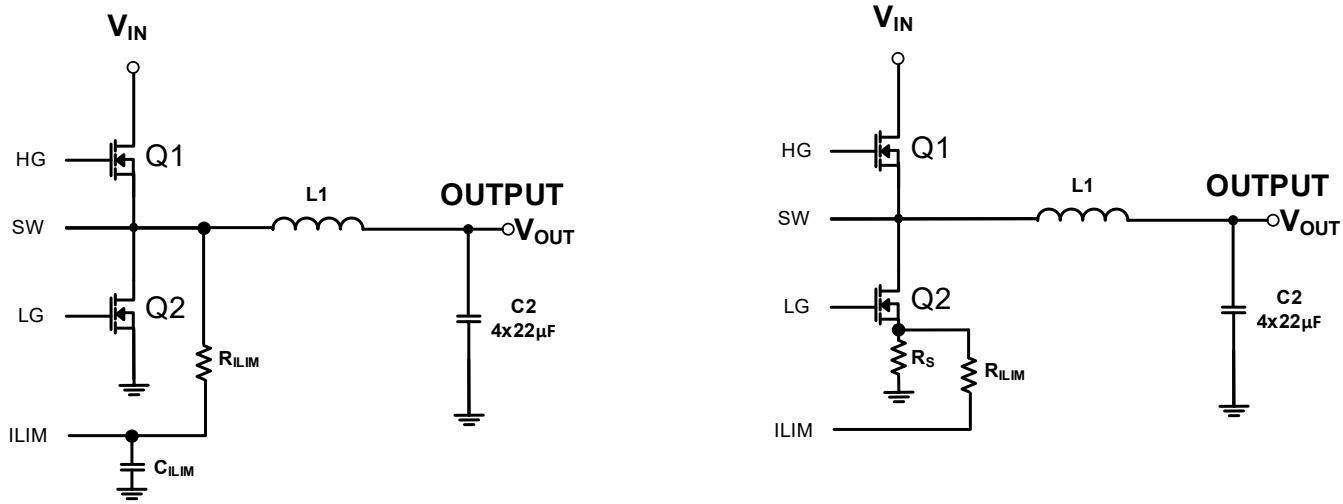
The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, CBST. When the low-side MOSFET conducts, the SW voltage is approximately at 0V and CBST is charged from VCC through the integrated boot diode. Connect a 0.1µF or larger ceramic capacitor close to the BST and SW pins.

There is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

Current Sensing and Overcurrent Protection

The AP6ACO5 implements two current sense schemes in Figure 83, either using the on-state resistance of the low-side MOSFET (lossless method) or alternative implementation with current shunt resistor, R_S, in series with the low-side power MOSFET. These are ways to limit the inductor current during an overload or output short-circuit condition. The controller senses the inductor current during the PWM off time when LG is high.

The ILIM pin sources a reference current that flows in an external resistor, designated R_{ILIM}, to program the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND.



Low-Side MOSFET RDSON Current Sensing

Resistive Shunt, Rs, Current Sensing

Figure 83. Current Sensing Schemes

Application Information (continued)

Current Sensing and Overcurrent Protection (continued)

The AP6ACO5 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly. The ILIM current with R_{DSON} sensing is 200µA at +27°C junction temperature and incorporates a T_C of +4500 ppm/°C to generally track the R_{DSON} temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100µA in R_S mode. This controls the valley of the inductor current during a steady state.

Depending on the chosen mode, select the resistance of RILIM using Equation 5 for using the R_{DSON} of the MOSFET or Equation 6 for using the shunt resistor, R_S.

$$\mathbf{R}_{ILIM} = \frac{\mathbf{I}_{\mathbf{OUT}} - \frac{\Delta \boldsymbol{I}_{\boldsymbol{L}}}{\mathbf{2}}}{\mathbf{200\mu A}} \cdot \boldsymbol{R}_{\boldsymbol{DSON}} \quad \textbf{Eq. 5}$$

$$\mathbf{R}_{ILIM} = \frac{\mathbf{I}_{\mathbf{OUT}} - \frac{\Delta \boldsymbol{I}_{\boldsymbol{L}}}{\mathbf{2}}}{\mathbf{100\mu A}} \cdot \boldsymbol{R}_{\boldsymbol{S}} \quad \textbf{Eq. 6}$$

Where

- ΔI_L is the inductor ripple current
- R_{DSON} is the on-state resistance of the lowside MOSFET
- Rs is the resistive shunt current sense

There could be large voltage swing which could affect the accuracy of the internal comparator during switching action of SW node. In this case, add a small high frequency filter capacitor, C_{ILIM}, across ILIM pin and PGND. Choose the capacitance such that the time constant R_{ILIM}*C_{ILIM} is approximately 6ns.

Pulse Frequency Modulation (PFM) Operation

The AP6ACO5 enters PFM operation at light load conditions for high efficiency when SYNCIN pin is set to logic LOW. During light load conditions, the regulator automatically reduces the switching frequency. As the output current decreases, the inductor current decreases. The inductor current, I_L, eventually reaches 0A, marking the boundary between Continuous Conduction Mode (CCM) and Discontinuous Condition Mode (DCM). During this time, both Q1 and Q2 are off, and the load current is provided only by the output capacitor. When V_{FB} becomes lower than 0.8V, the next cycle begins, and Q1 turns on. Because the AP6ACO5 works in PFM during light load conditions, it can achieve power efficiency of up to 89% at a 5mA load condition.

Likewise, as the output load increases from light load to heavy load, the switching frequency increases to maintain the regulation of the output voltage. The transition point between light and heavy load conditions can be calculated using the following equation:

$$\mathbf{I}_{\mathbf{LOAD}} = \left(\frac{\mathbf{VIN} - \mathbf{VOUT}}{\mathbf{2} \cdot \mathbf{VIN} \cdot \mathbf{L} \cdot \mathbf{fsw}}\right) \cdot \mathbf{VOUT} \quad \textbf{Eq. 7}$$

Where:

- L is the inductor value
- f_{SW} is the switching frequency

The quiescent current of the AP6ACO5 is 1.5mA typical under a no-load, non-switching condition.

The AP6ACO5 operates in PWM when the SYNCIN pin voltage is logic HIGH. Its switching frequency is maintained constant across all load conditions.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of +175°C, the AP6ACO5 shuts down both its high-side and low-side power MOSFETs, pull SS/TR and PG LOW, and turn off VCC. When the junction temperature reduces to the required level (+155°C typical), the device initiates a normal power-up cycle with soft-start.

Application Information (continued)

Setting the Output Voltage

The output voltage can be adjusted from 0.8V using an external resistor divider. Table 1 shows a list of resistor selection for common output voltages. An optional C4 of 10pF to 470pF can be used to boost the phase margin and improve stability as well as the transient performance. R2 in Figure 84 can be determined by the following equation:

$$R_2 = \frac{R_1 \cdot 0.8}{Vout - 0.8} \quad \text{Eq. 8}$$

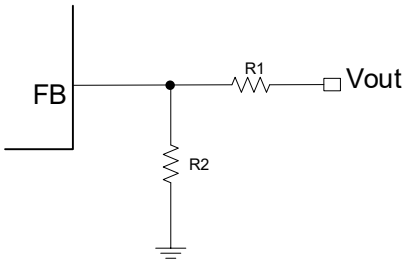


Figure 84. Feedback Divider Network

Table 2 shows a list of recommended component selections for common output voltages for the AP6ACO5 as a reference to Figure 1.

AP6ACO5															
Output Voltage (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	L (µH)	C_{IN1} MLCC* (µF)	C_{IN2} AEC* (µF)	C_{OUT1} MLCC* (µF)	C_{OUT2} AEC* (µF)	C_{BST} (nF)	C_{C3} (pF)	R_{C2} (Ω)	R_{C1} (kΩ)	C_{C1} (pF)	C_{C2} (pF)	f_{SW} (kHz)	R_{LIM} (kΩ)
0.8	21	OPEN	2.2	10 x 4	470 x 2	47 x 4	470	100	470	100	4.12	6800	1000	100	1.1
1.2	21	42.2	2.2	10 x 4	470 x 2	47 x 4	470	100	1500	309	13.7	6800	270	100	1.1
1.8	21	16.9	2.2	10 x 4	470 x 2	47 x 4	470	100	1500	301	14.0	6800	270	100	1.1
2.5	21	10	2.2	10 x 4	470 x 2	47 x 4	470	100	1800	301	14	6800	220	100	1.1
3.3	21	6.65	3.3	10 x 4	470 x 2	47 x 4	470	100	680	76.8	5.49	6800	680	100	1.1
5.0	21	4.02	4.7	10 x 4	470 x 2	47 x 4	470	100	820	61.9	6.65	6800	560	100	1.1
12.0	21	1.5	6.8	10 x 6	470 x 3	47 x 8	470	100	1000	51.1	8.06	6800	470	100	1.1
12.0	21	1.5	6.8	10 x 6	470 x 3	47 x 8	470	100	1000	52.3	8.06	6800	220	200	1.1
24.0	21	0.732	8.2	10 x 6	470 x 3	47 x 8	470	100	1200	42.2	9.76	6800	180	200	0.953
48.0	21	0.357	10	10 x 6	470 x 3	47 x 8	470	100	1200	42.2	9.76	6800	180	200	0.768
60.0	21	0.287	10	10 x 6	470 x 3	47 x 8	470	100	1200	42.2	9.76	6800	180	200	0.620

AP6ACO5															
Output Voltage (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	L (µH)	C_{IN1} MLCC* (µF)	C_{IN2} AEC* (µF)	C_{OUT1} MLCC* (µF)	C_{OUT2} AEC* (µF)	C_{BST} (nF)	C_{C3} (pF)	R_{C2} (Ω)	R_{C1} (kΩ)	C_{C1} (pF)	C_{C2} (pF)	F_{SW} (kHz)	R_{LIM} (Ω)
0.8	21	OPEN	2.2	10 x 4	470 x 2	47 x 4	470	100	560	93.1	4.53	6800	180	400	619
1.5	21	23.7	2.2	10 x 4	470 x 2	47 x 4	470	100	560	90.9	4.53	6800	180	400	619
2.5	21	10	2.2	10 x 4	470 x 2	47 x 4	470	100	560	90.9	4.53	6800	180	400	619
3.3	21	6.65	3.3	10 x 4	470 x 2	47 x 4	470	100	680	75.0	5.62	6800	150	400	619
5.0	21	4.02	4.7	10 x 4	470 x 2	47 x 4	470	100	820	61.9	6.65	6800	120	400	619
12.0	21	1.5	6.8	10 x 6	470 x 3	47 x 8	470	100	1000	51.1	8.06	4700	100	400	619
24.0	21	0.732	10	10 x 6	470 x 3	47 x 8	470	100	1200	42.2	9.76	6800	100	400	422
48.0	21	0.357	10	10 x 6	470 x 3	47 x 8	470	100	1000	46.4	8.87	6800	100	400	422
60.0	21	0.287	10	10 x 6	470 x 3	47 x 8	470	100	1200	42.2	9.76	6800	100	400	422

Table 2. Recommended Component Selections

MLCC* = Multiplayer Ceramic Capacitors

AEC* = Aluminum Electrolytic Capacitors

Note: For other output voltages at different output currents and frequencies, please download the AP6ACO5 Design Tool Calculator for calculations available on Diodes website.

For driving high output currents (>15A to 40A), using two high-side and two low-side external MOSFETs in parallel is recommended because it reduces conduction and switching losses and distributes thermal stress.

Application Information (continued)

Setting the Output Voltage (continued)

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor has to sustain the ripple current produced during the on time on the upper MOSFET. It must hence have a low ESR to minimize the losses.

The RMS current rating of the input capacitor is a critical parameter that must be higher than the RMS input current. As a rule of thumb, select an input capacitor which has RMs rating that is greater than half of the maximum load current.

Due to large di/dt through the input capacitors, both electrolytic and ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur. For most applications, a 10μF ceramic capacitor is sufficient and 0.1μF parallel capacitor also recommended for improving the stability. Please refer to Diodes evaluation board user guide with details of explanations.

Inductor

Calculating the inductor value is a critical factor in designing a buck converter. For most designs, the following equation can be used to calculate the inductor value:

$$L1 = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{SW}} \quad \text{Eq. 9}$$

Where ΔI_L is the inductor ripple current and f_{SW} is the buck converter switching frequency.

Choose the inductor ripple current to be 30% to 40% of the maximum load current. The maximum inductor peak current calculated from:

$$I_{L1(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad \text{Eq. 10}$$

Peak current determines the required saturation current rating, which influences the size of the inductor. Saturating the inductor decreases the converter efficiency while increasing the temperatures of the inductor and the internal MOSFETs. Hence choosing an inductor with appropriate saturation current rating is important.

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications.

For highest efficiency, the inductor's DC resistance should be as low as possible. Use a larger inductance for improved efficiency under light load conditions.

Application Information (continued)

Output Capacitor

The output capacitor keeps the output voltage ripple small, ensures feedback loop stability and reduces the overshoot of the output voltage. The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The converter recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

ESR of the output capacitor dominates the output voltage ripple. The amount of ripples can be approximate from the equation below:

$$\mathrm{Vout}_{\mathrm{capacitor}} = \Delta \mathrm{I}_{\mathrm{inductor}} * (\mathrm{ESR} + \frac{1}{8 \mathrm{f}_{\mathrm{SW}} C_O}) \quad \textbf{Eq. 11}$$

An output capacitor with ample capacitance and low ESR is the best option. For most applications, multiple 22μF ceramic capacitors will be sufficient.

$$C2 = \frac{L(I_{\mathrm{out}} + \frac{\Delta \mathrm{I}_{\mathrm{inductor}}}{2})^2}{(\Delta \mathrm{V} + V_{\mathrm{out}})^2 - {V_{\mathrm{out}}}^2} \quad \textbf{Eq. 12}$$

Where ΔV is the maximum output voltage overshoot.

Bootstrap

The internal driver of the HS FET is equipped with a BST undervoltage detection (UV) circuit. In the event that the voltage difference between BST and SW falls below 3V, the UV detection circuit allows the LS FET on for 400ns to recharge the bootstrap capacitor.

Voltage Mode Control Loop Compensation

Figure 85 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage, V_{OUT}, is regulated to the reference level at 0.8V. The error amplifier output, V_{EA}, is compared with the ramp generator to provide a pulse-width modulated (PWM) waveform. This signal is then used to drive the MOSFETs with the same duty cycle at the SW node to transfer power to the output stage. The L1 and C2 form a low pass filter to smooth the SW from a square wave to a low ripple DC output.

The AP6ACO5 voltage mode implements a voltage ramp, V_{RAMP}, that is proportional to VIN with a gain of 12. This eliminates the feedback loop response dependency on VIN voltage.

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining optional compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage.

The small-signal open-loop response of a buck regulator is the product of modulator, power train, and compensator transfer functions. The power stage transfer function can be represented as a complex 2nd order pole associated with the output LC filter and a zero related to the R_{ESR} of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN}/V_{RAMP}. The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the AP6ACO5 (V_{IN}/V_{RAMP} = 12V/V).

The power stage modulator break frequencies are governed by equations 13 and 14.

$$f_{LC} = \frac{1}{2\pi\sqrt{L1 \cdot C2}} \quad \textbf{Eq. 13}$$

$$f_{esr} = \frac{1}{2\pi \cdot R_{ESR} \cdot C2} \quad \textbf{Eq. 14}$$

Where R_{ESR} is the equivalent series resistor of the output capacitor. C2 is the effective output capacitance of the output capacitor.

Application Information (continued)

Voltage Mode Control Loop Compensation (continued)

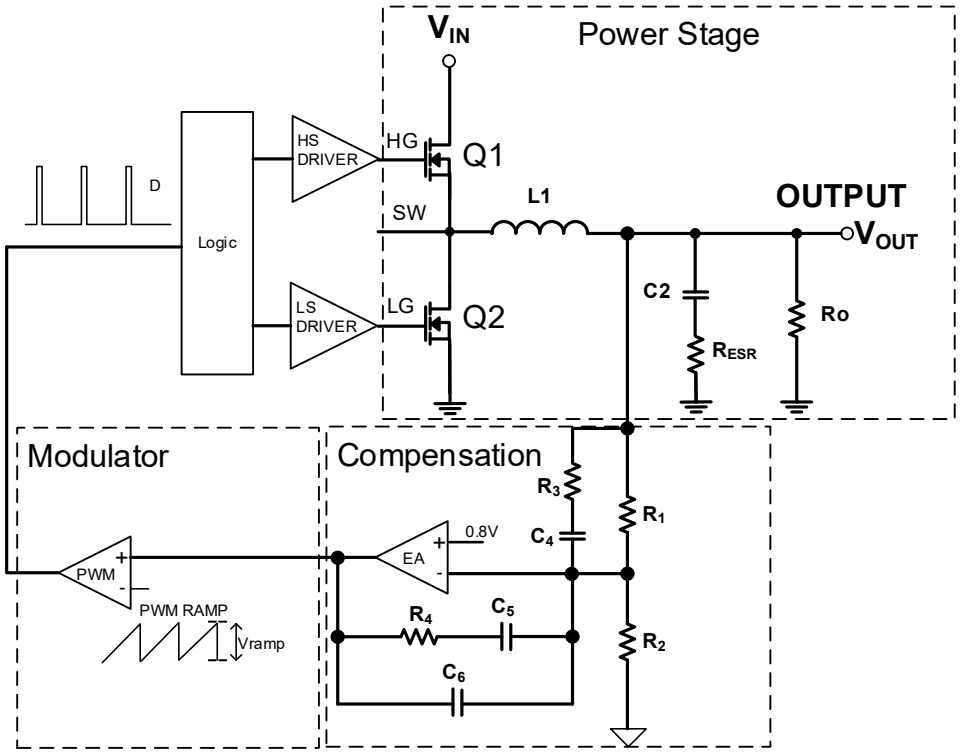


Figure 85. Voltage-Mode Buck Converter Compensation Loop Diagram

The goal of the compensation network is to provide a close loop transfer function with the highest 0dB crossing frequency or gain bandwidth, f_{0dB}, and adequate phase margin. The phase margin is the difference between the close loop phase at f_{0dB} and 180°. The design procedures are:

1. Pick the Gain (R4/R1) for the desired bandwidth, f_{0dB}.
2. Place the 1st Zero approximately 75% below the frequency F_{LC}.
3. Place the 2nd Zero at the frequency F_{LC}.
4. Place the 1st Pole at the f_{ESR} frequency.
5. Place an optional 2nd Pole at approximately half the switching frequency, fsw to reduce system noise. In most cases, adding 2nd Pole will reduce the phase margin.
6. Measure the gain bandwidth, phase margin, θ_M, and gain margin, G_M.
7. Repeat steps 1 to 6 if necessary.

The equations 15 are the compensation design of where to set the Zeroes and Poles:

System Gain - $$Gain = R4/R1$$ **Eq. 15**

1st Zero - $$f_{Z1} = \frac{1}{2\pi \cdot R4 \cdot C5} = \frac{0.75}{2\pi\sqrt{L1 \cdot C2}}$$

2nd Zero - $$f_{Z2} = \frac{1}{2\pi \cdot (R1+R3) \cdot C4} = \frac{1}{2\pi\sqrt{L1 \cdot C2}}$$

1st Pole - $$f_{P1} = \frac{1}{2\pi \cdot R4 \cdot \left(\frac{C5 \cdot C6}{C5+C6}\right)} = \frac{1}{2\pi \cdot R_{ESR} \cdot C2}$$

2nd Pole - $$f_{P2} = \frac{1}{2\pi \cdot R3 \cdot C4} = \frac{fsw}{2}$$

Application Information

Voltage Mode Control Loop Compensation (continued)

Figure 86 is the estimated Gain and Phase V_S frequency loop response of the system.

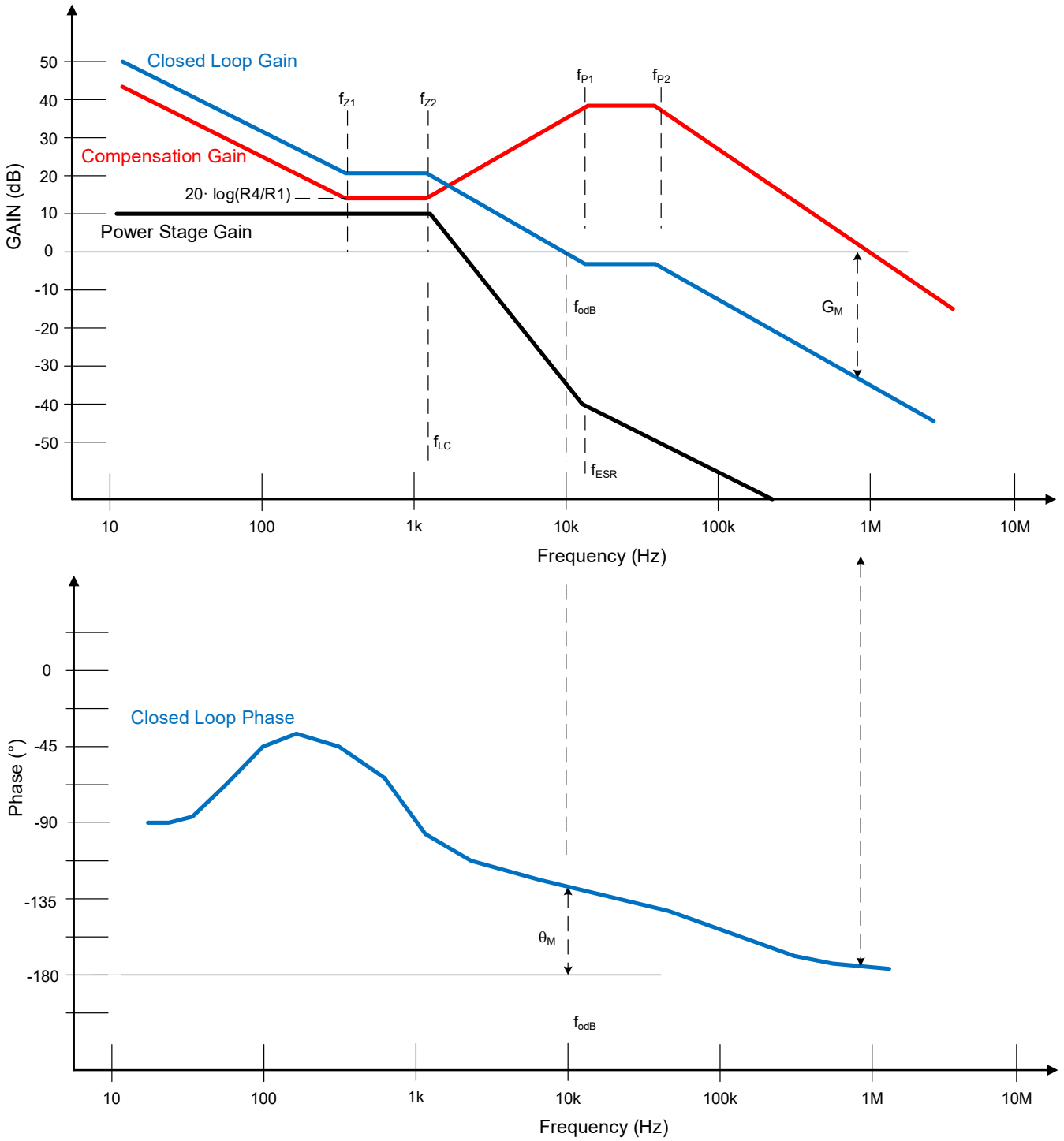


Figure 86. System Gain and Phase Loop Response

The actual system gain has a high peak due to the high Q factor of the output filter which is not shown in the approximation plot. A stable control loop has a gain crossing the 0dB at approximately -20dB/decade slope on a log scale. The θ_M must be greater than 45° and the G_M should be less than -10dB.

Layout

PCB Layout

1. The AP6ACO5 is a high switching frequency converter. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The AP6ACO5 works up to 40A load current so heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended.
2. Place the input capacitors as closely across VIN and GND as possible to the power MOSFET, Q1.
3. Place the inductor as close to SW as possible.
4. Place the output capacitors as close to GND as possible.
5. Place the feedback components as close to FB as possible.
6. If using four or more layers, use at least the 2nd and 3rd layers as GND to maximize thermal performance.
7. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
8. Add as many vias as possible around both the VIN pin and under the VIN plane for heat dissipation to all the VIN layers.
9. See Figure 87 for more details.

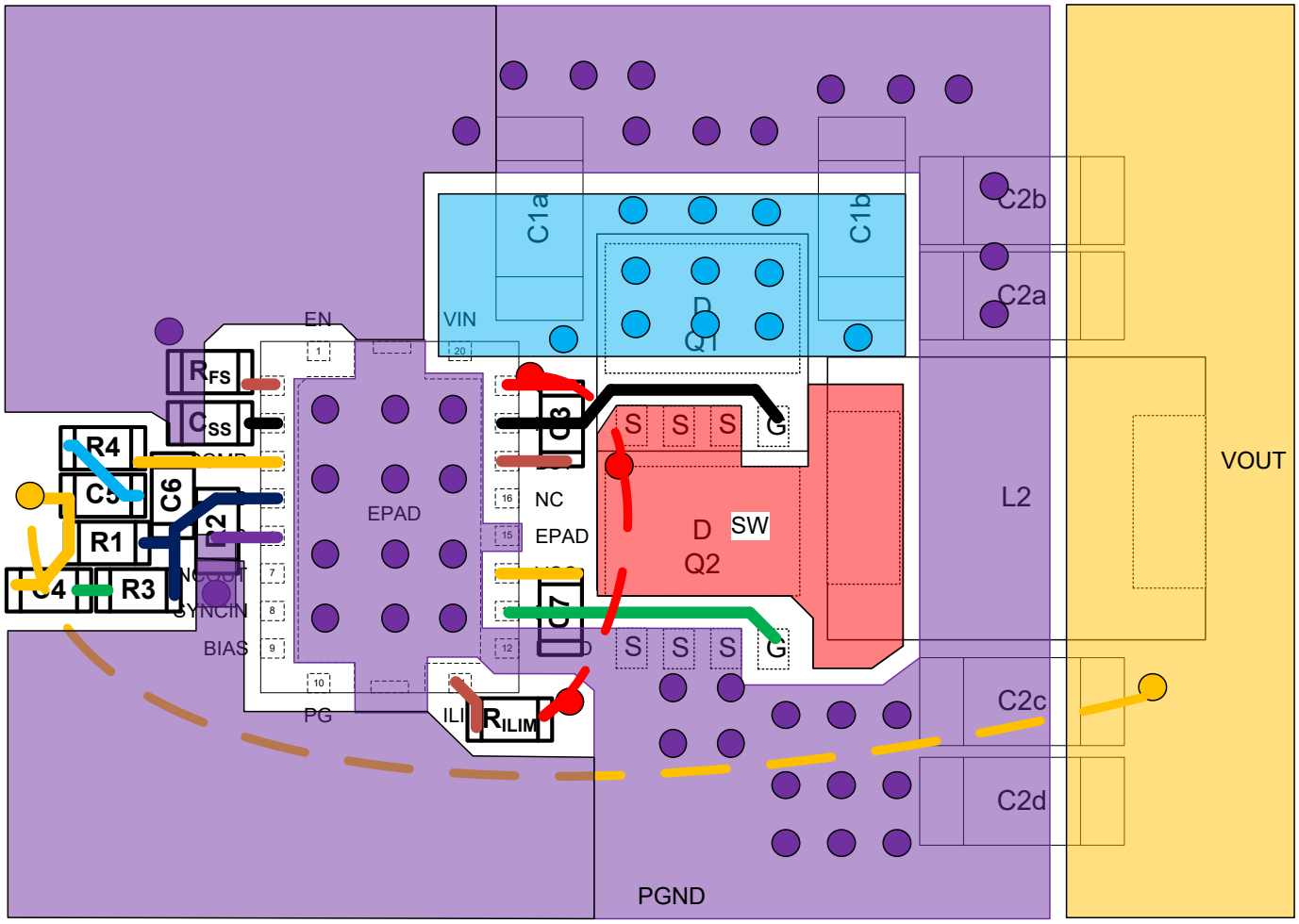
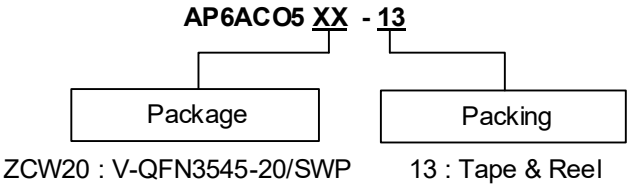


Figure 87. PC Board Layout

Ordering Information (Note 10)



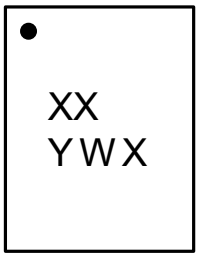
Orderable Part Number	MODE	Package Code	Package	Identification Code	Packing	
					Qty.	Carrier
AP6ACO5ZCW20-13	PFM/PWM	QFN	V-QFN3545-20/SWP	6A	3000	13” Tape and Reel

Note: 10. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

V-QFN3545-20/SWP

(Top View)

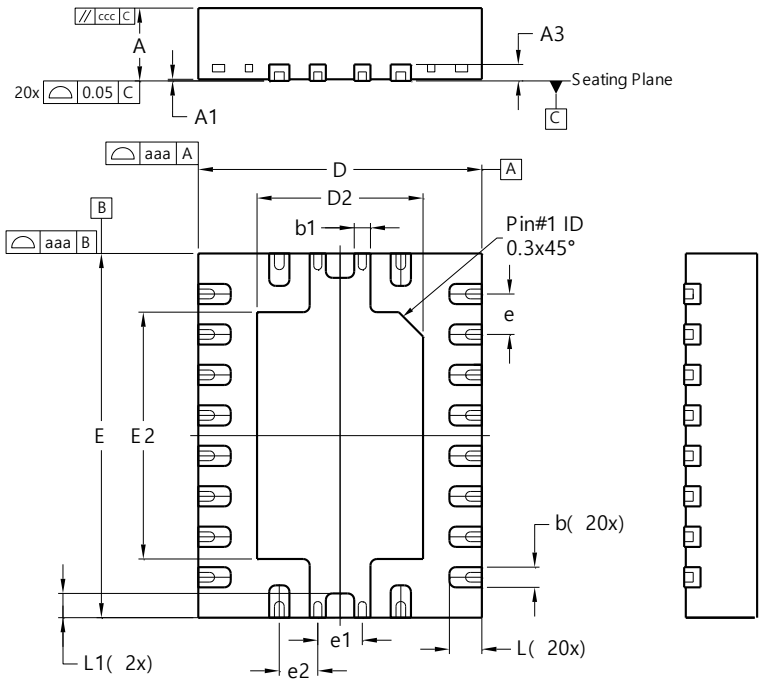


XX: Identification Code
Y: Year: 0 to 9
W: Week: A to Z: Week 1 to 26;
a to z: Week 27 to 52; z Represents 52 and 53 Week
X: Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN3545-20/SWP

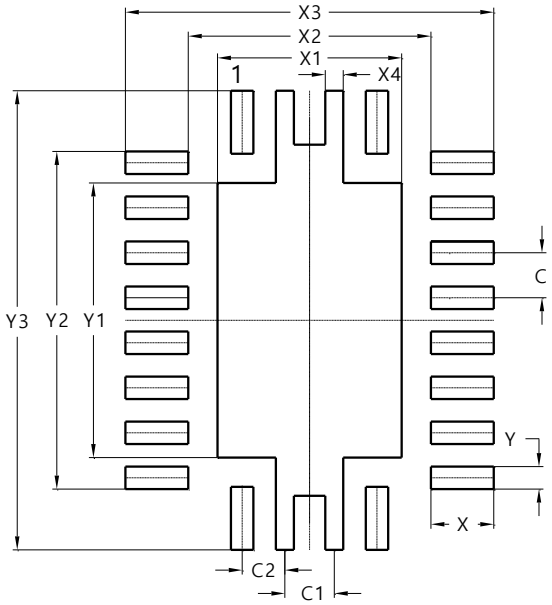


V-QFN3545-20/SWP			
Dim	**Min**	**Max**	**Typ**
A	0.800	1.000	0.900
A1	0.000	0.050	0.020
A3	--	--	0.203
b	0.200	0.300	0.250
b1	0.150	0.250	0.200
D	3.400	3.600	3.500
D2	1.950	2.150	2.050
E	4.400	4.600	4.500
E2	2.950	3.150	3.050
e	0.500 BSC		
e1	0.550 BSC		
e2	0.475 BSC		
L	0.300	0.500	0.400
L1	0.300 REF		
aaa	0.05		
bbb	0.05		
ccc	0.05		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN3545-20/SWP



Dim	Value (in mm)
C	0.050
C1	0.550
C2	0.475
X	0.700
X1	2.050
X2	2.700
X3	4.100
X4	0.200
Y	0.250
Y1	3.050
Y2	3.750
Y3	5.100

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.081 grams (Approximate)

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