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FAIRCHILD SEMICONDUCTOR®

October 2013

FQB50N06 / FQI50N06

N-Channel QFET® MOSFET

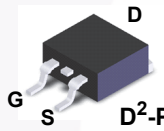
60 V, 50 A, 22 mΩ

Description

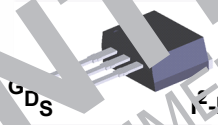
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

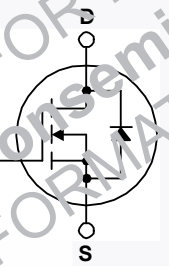
- 50 A , 60 V, $R_{DS(on)}$ = 22 mΩ (Max.) @V_{GS} = 10 V, I_D = 25 A
- Low Gate Charge (Typ. 31 nC)
- Low Crss Typ. 65 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



D²-PAK



I²-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQB50N06TM / FQI50N06TU	Unit
V_{DSS}	Drain-Source Voltage		60	V
I_D	Drain Current - Continuous (T_C = 25°C)		50	A
	- Continuous (T_C = 100°C)		35.4	A
I_{DM}	Drain Current - Pulsed	(Note 1)	200	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	490	mJ
I_{AR}	Avalanche Current	(Note 1)	50	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	12	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *		3.75	W
	Power Dissipation (T_C = 25°C)		120	W
	- Derate above 25°C		0.8	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQB50N06TM FQI50N06TU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (* 1 in² pad of 2 oz copper), Max.	40	

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB50N06	FQB50N06TM	D2-PAK	330mm	24mm	800
FQI50N06	FQI50N06TU	I2-PAK	-	-	50

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	--	[illegible]	[illegible]	µA
		V_{DS} = 48 V, T_C = 150°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25 V, V_{DS} = 0 V	[illegible]	--	10[illegible]	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25 V, V_{DS} = 0 V	[illegible]	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 [illegible]	[illegible].0	--	[illegible] 4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 [illegible] I_D = [illegible]	--	0.018	0.022	Ω
g_{FS}	Forward Transconductance	$V_{[illegible]}$ = 25 V, [illegible] = 2[illegible] A	--	22	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, [illegible] 1.0 MH[illegible]	--	1150	1540	pF
C_{oss}	Output Capacitance		--	440	580	pF
C_{rss}	Reverse Transfer C[illegible]acitanc[illegible]		--	65	90	pF
Switching Char[illegible]teristic[illegible]						
$t_{d(on)}$	Turn-On [illegible]elay Tim[illegible]	V_{DD} = 30 V, I_D = 25 A, R_G = 25 Ω (Note 4)	--	15	40	ns
t_r	[illegible]urn-On R[illegible] Tim[illegible]		--	105	220	ns
$t_{d(off)}$	[illegible] Delay Time		--	60	130	ns
t_f	Turn-Off [illegible]all Time		--	65	140	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 50 A, V_{GS} = 10 V (Note 4)	--	31	41	nC
Q_{gs}	Gate-Source Charge		--	8	--	nC
Q_{gd}	Gate-Drain Charge		--	13	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	50	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	200	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 50 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 50 A, dI_F / dt = 100 A/µs	--	52	--	ns
Q_{rr}	Reverse Recovery Charge		--	75	--	nC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 230µH, I_{AS} = 50A, V_{DD} = 25V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 50A, di/dt $\leq$ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Essentially independent of operating temperature

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Typical Characteristics

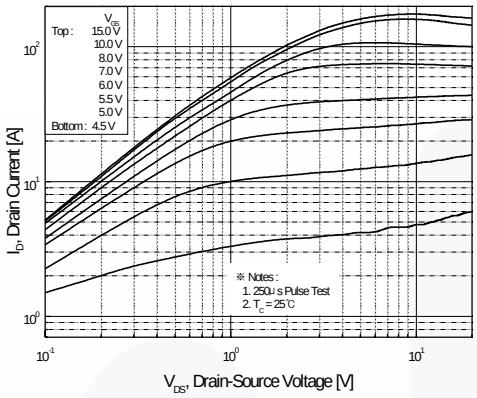

Figure 1. On-Region Characteristics

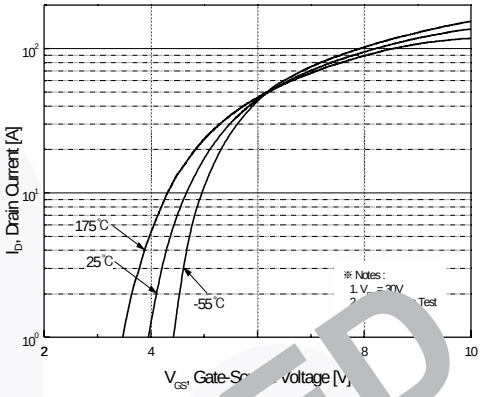

Figure 2. Transfer Characteristics

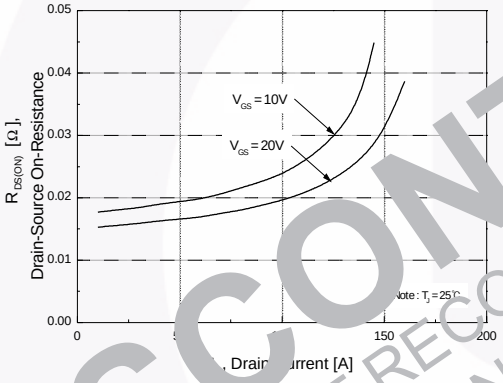

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

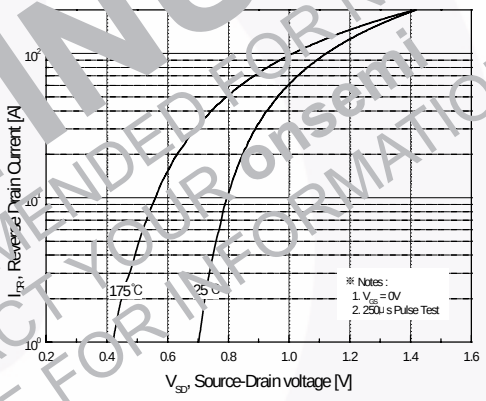

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

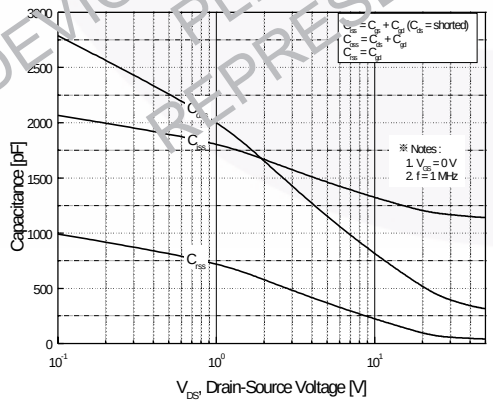

Figure 5. Capacitance Characteristics

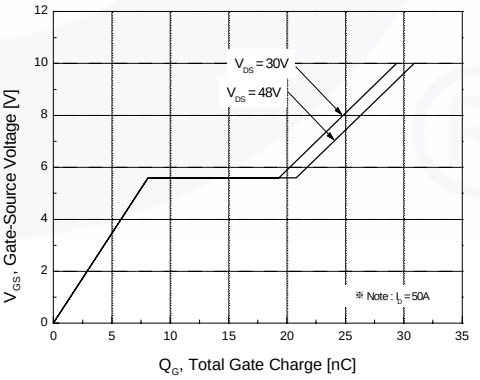

Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

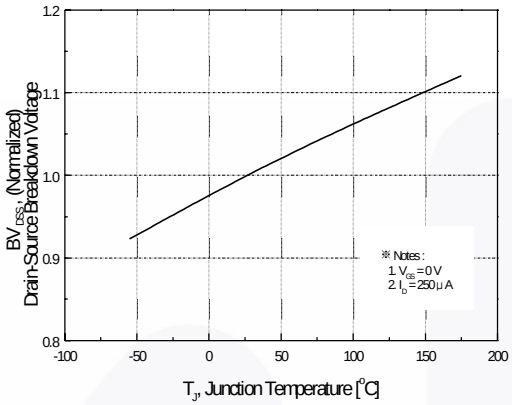

Figure 7. Breakdown Voltage Variation vs. Temperature

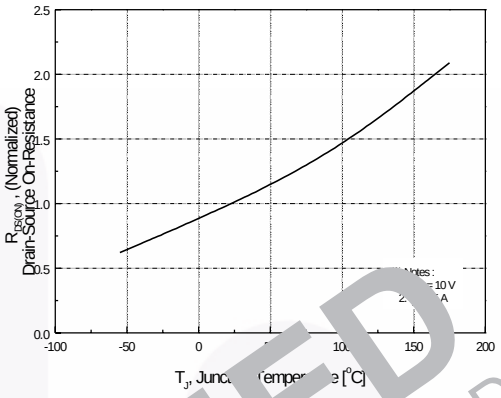

Figure 8. On-Resistance Variation vs. Temperature

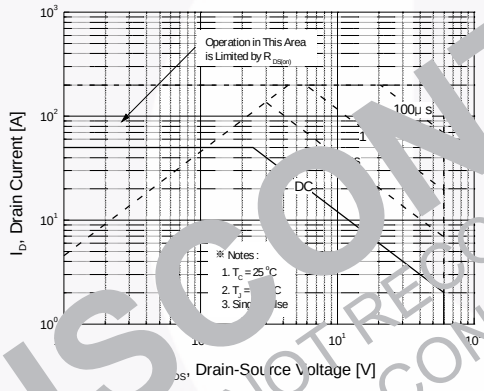

Figure 9. Maximum Safe Operating Area

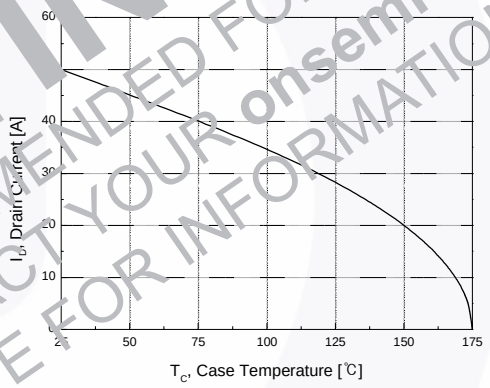

Figure 10. Maximum Drain Current vs. Case Temperature

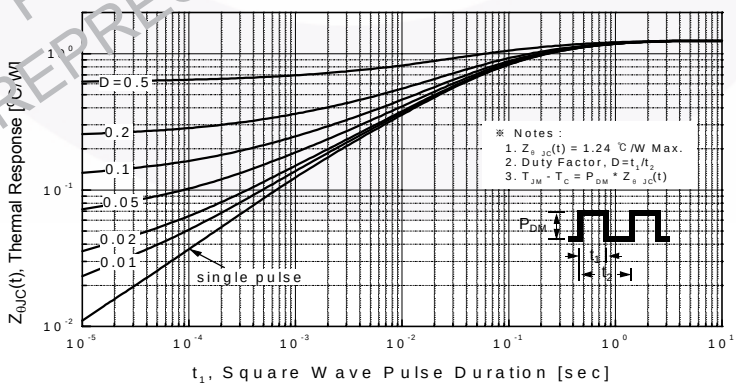

Figure 11. Transient Thermal Response Curve

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Figure 12. Gate Charge Test Circuit & Waveform

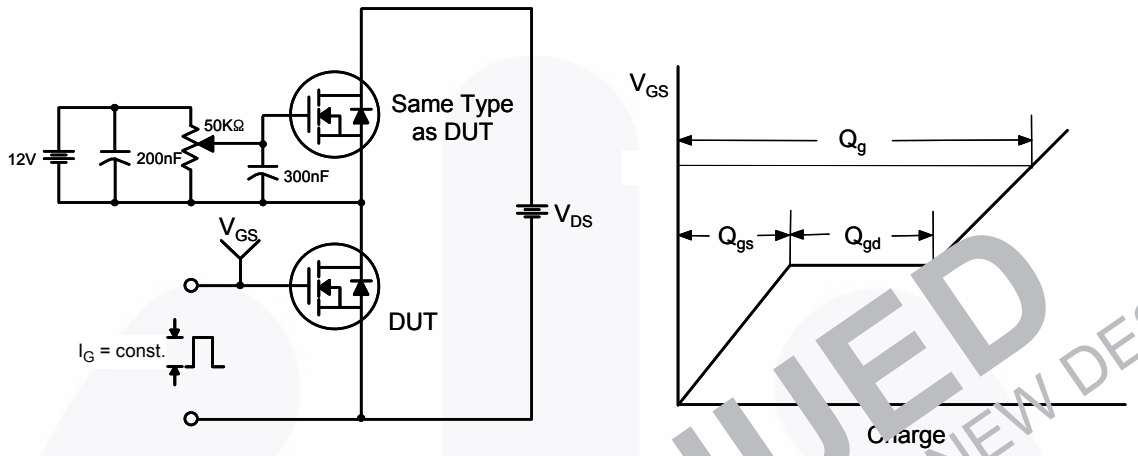

Figure 13. Resistive Switching Test Circuit & Waveforms

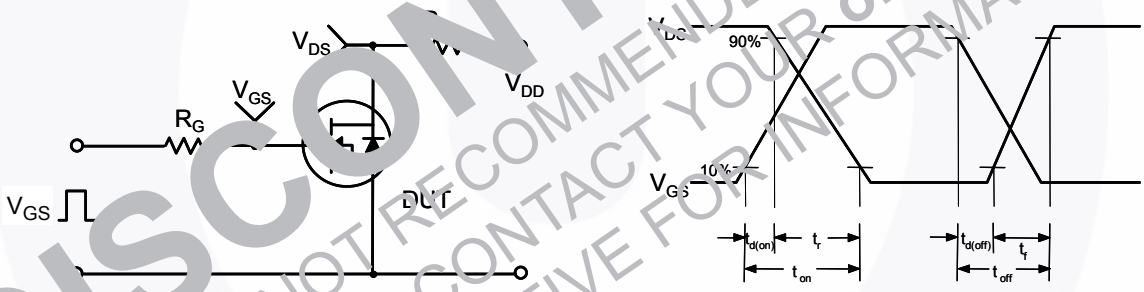

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

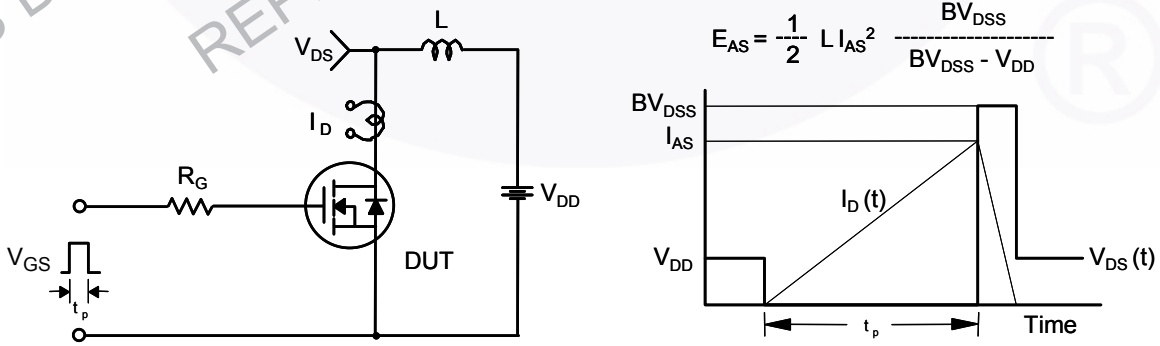

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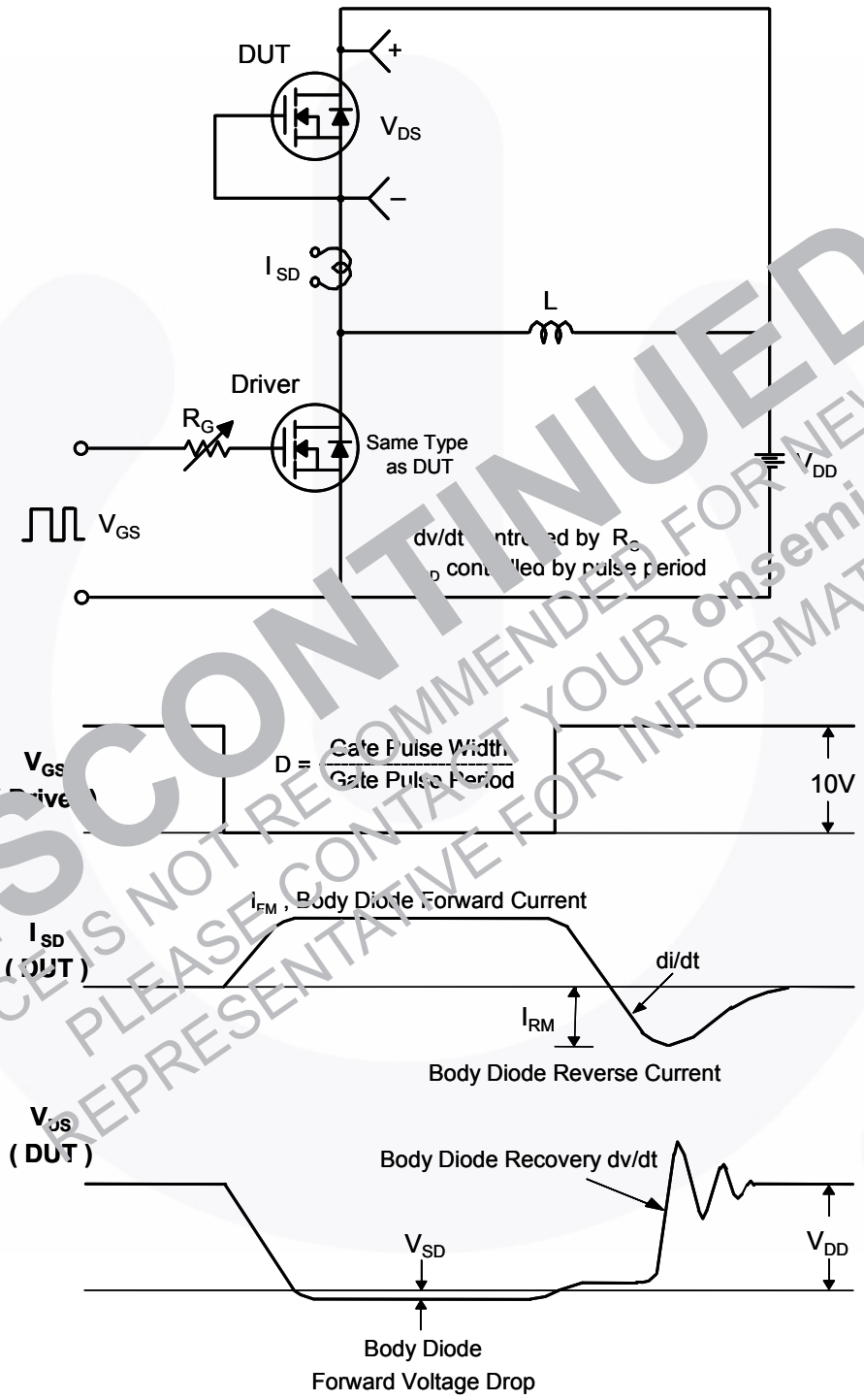
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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Mechanical Dimensions

TO-263 2L (D^2PAK)

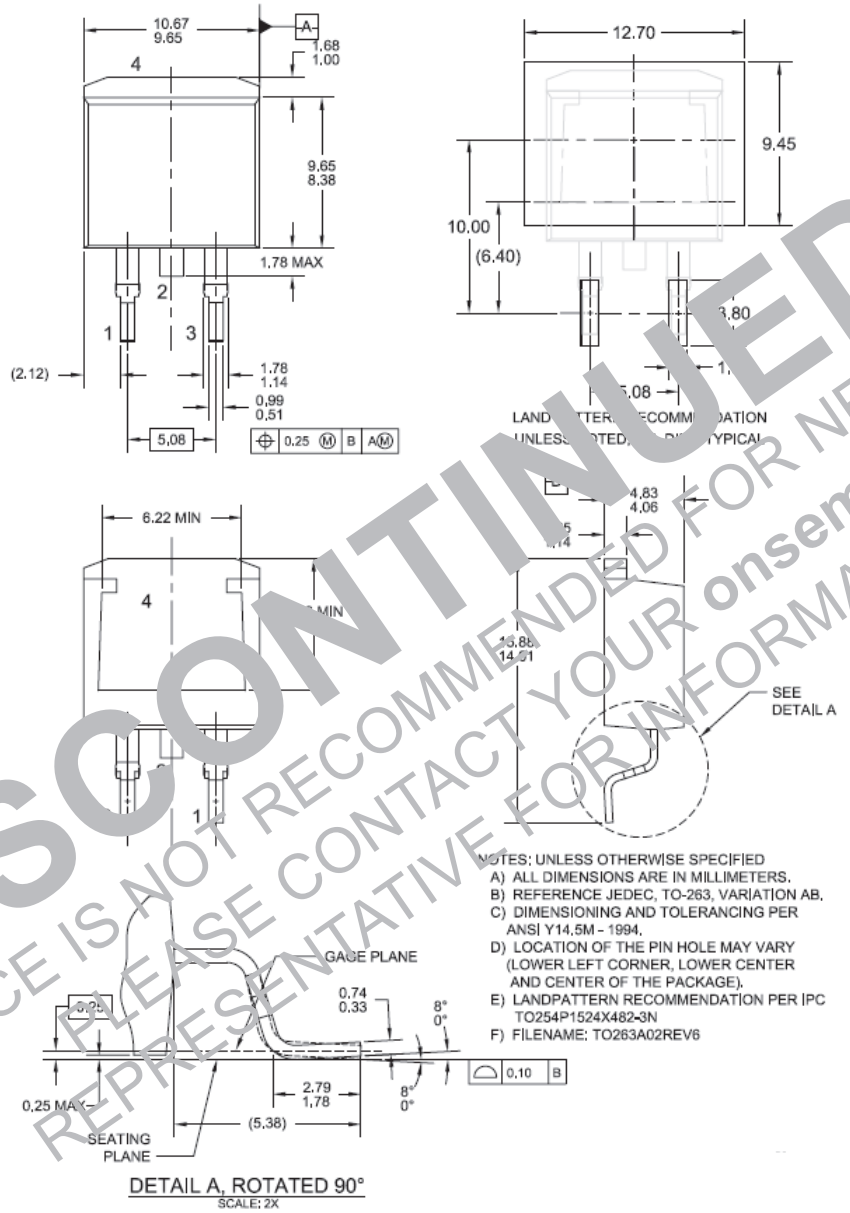

Figure 16. 2LD,TO263, Surface Mount

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Dimension in Millimeters

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Mechanical Dimensions

TO-262 3L (I^2PAK)

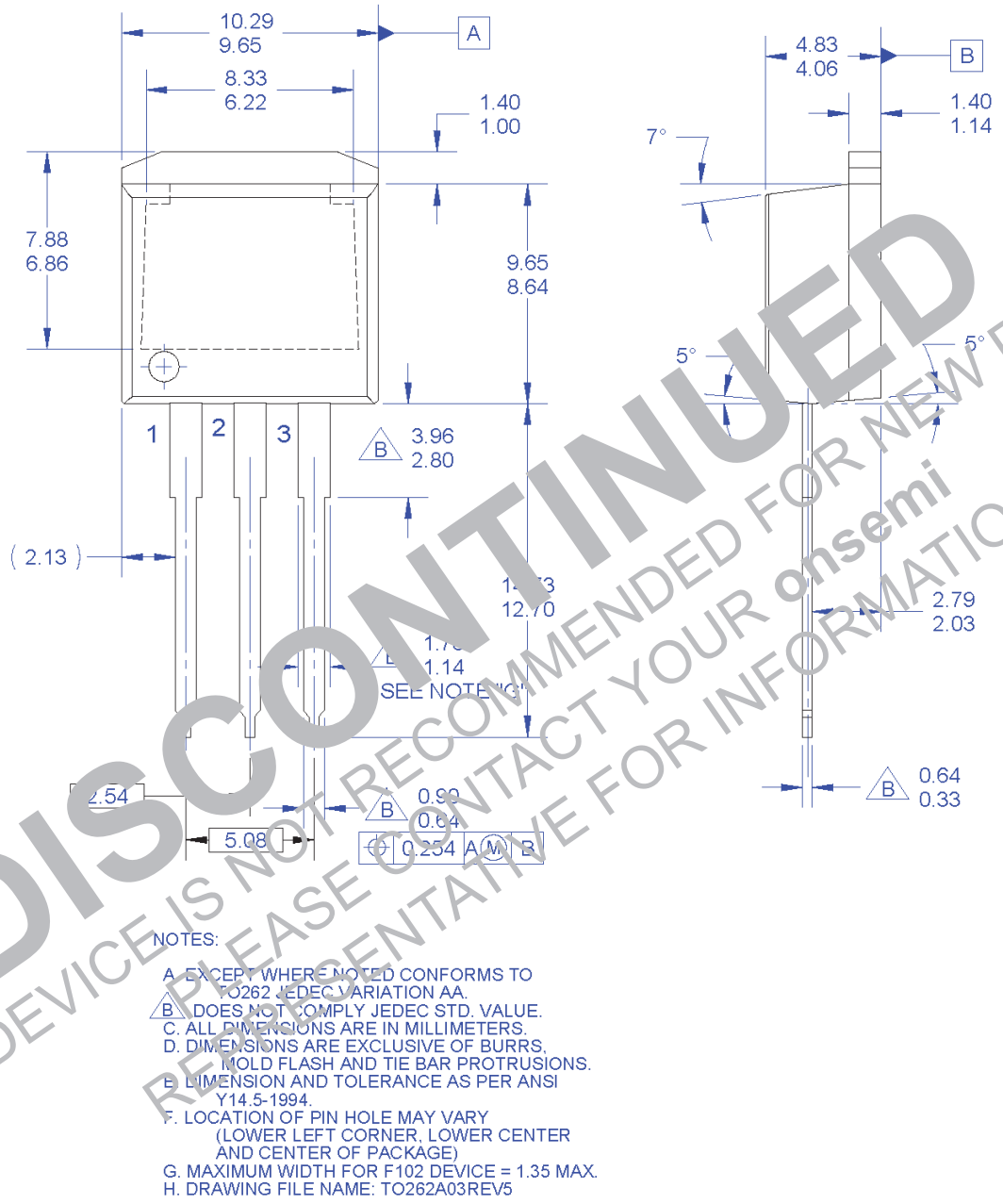

Figure 17. 3LD, TO262, Jedec Variation AA (12PAK)

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Dimension in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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