



MX575ABC25M0000

Ultra-Low Jitter 25MHz LVCMOS XO

ClockWorks® FUSION

General Description

The MX575ABC25M0000 is an ultra-low phase jitter XO with LVCMOS output optimized for high line rate applications.

Features

- 25MHz LVCMOS
- Typical phase noise:
 - 77fs (Integration range: 1.875MHz-5MHz)
- ± 50 ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

Absolute Maximum Ratings¹

Supply Voltage (VIN)	+4.6V
Lead Temperature (soldering, 10s)	260°C
Case Temperature	115°C
Storage Temperature (T _S)	-65°C to +125°C
ESD Machine Model	200V
ESD Rating (HBM)	2kV

Operating Ratings²

Supply Voltage (VIN)	+2.375V to +3.63V
Ambient Temperature (TA)	-40°C to +85°C
Junction Thermal Resistance	
LGA (T _{JA}) Still Air	53°C/W

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, output terminated with 50 Ohms to VDD/2.³

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				95	mA
F0	Center Frequency			25		MHz
	Frequency Stability	Note 4			± 50	ppm
Øj	Phase Noise	Integration Range (12kHz to 5MHz) Integration Range (1.875MHz to 5MHz)		131 77		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		500	ps
	Duty Cycle		45		55	%
VIH	Input High Voltage	3.3V Operation	2		VDD + 0.3	V
VIL	Input Low Voltage	3.3V Operation	-0.3		0.8	V
VOH	Output High Voltage	LVCMOS output levels	VDD - 0.8			V
VOL	Output Low Voltage	LVCMOS output levels			0.6	V

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Guaranteed after thermal equilibrium.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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MX575AB1-2265

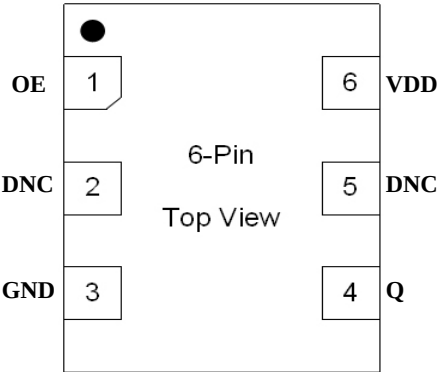
Revision 1.0
tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ABC25M0000	MX575AB	C25M0000	Tube	6-Pin 7mm x 5mm LGA
MX575ABC25M0000-TR	MX575AB	C25M0000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, DNC	O, SE	LVC MOS	Clock Output Frequency = 25MHz
6	VDD	PWR		Power Supply

Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition B
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10-8 atm cc/s
Solvent Resistance	MIL-STD-202, Method 215

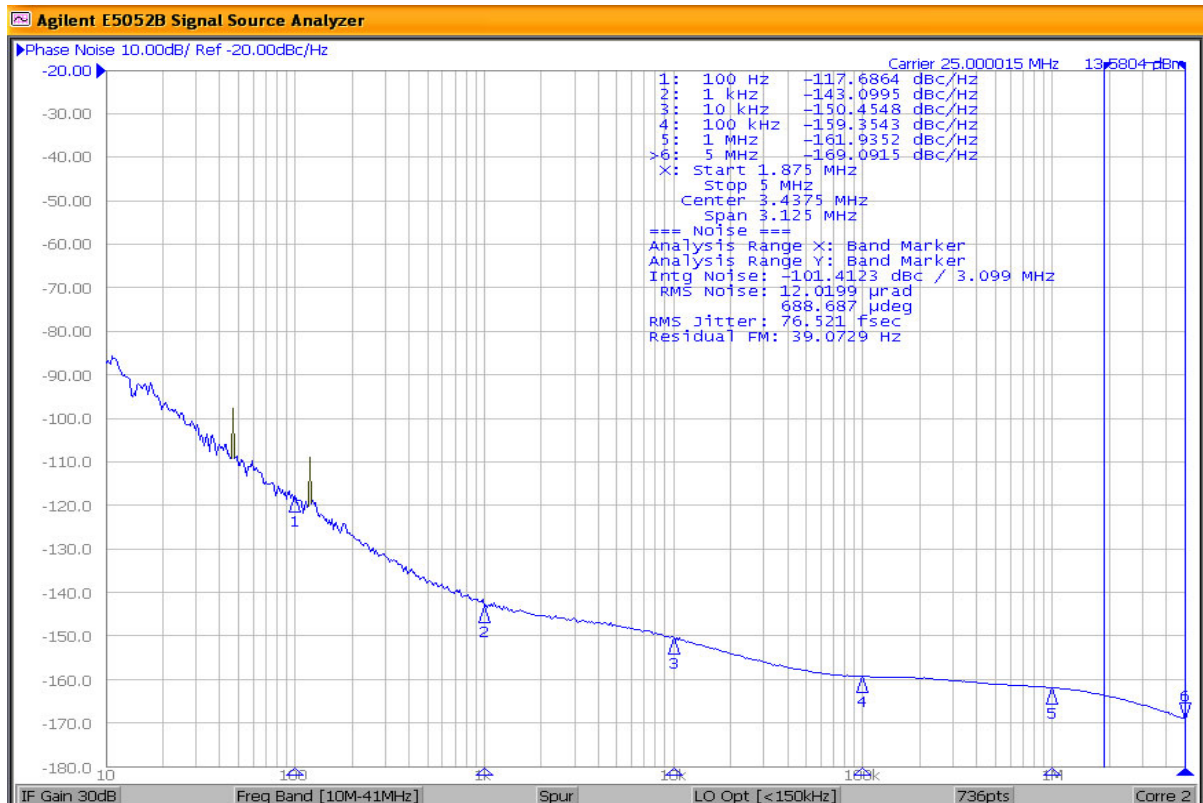


Figure 1. LVC MOS Output 25MHz 1.875MHz-5MHz 77fs

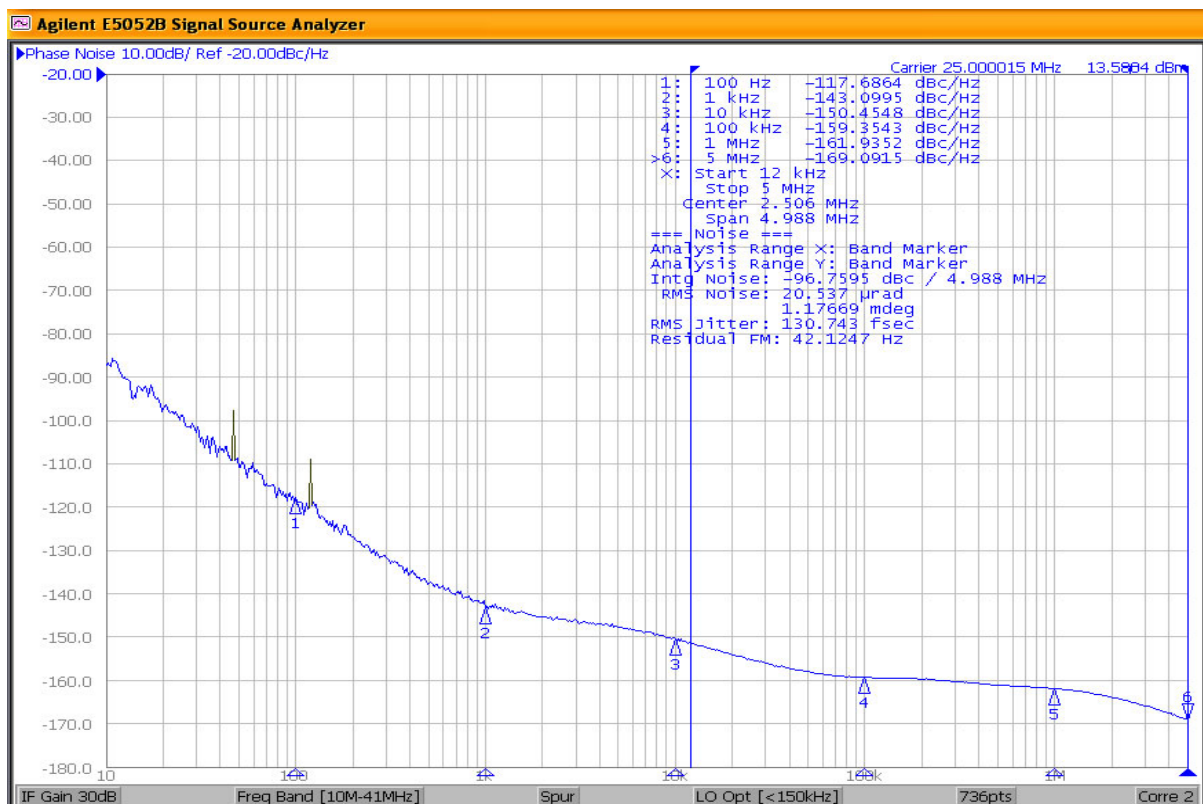
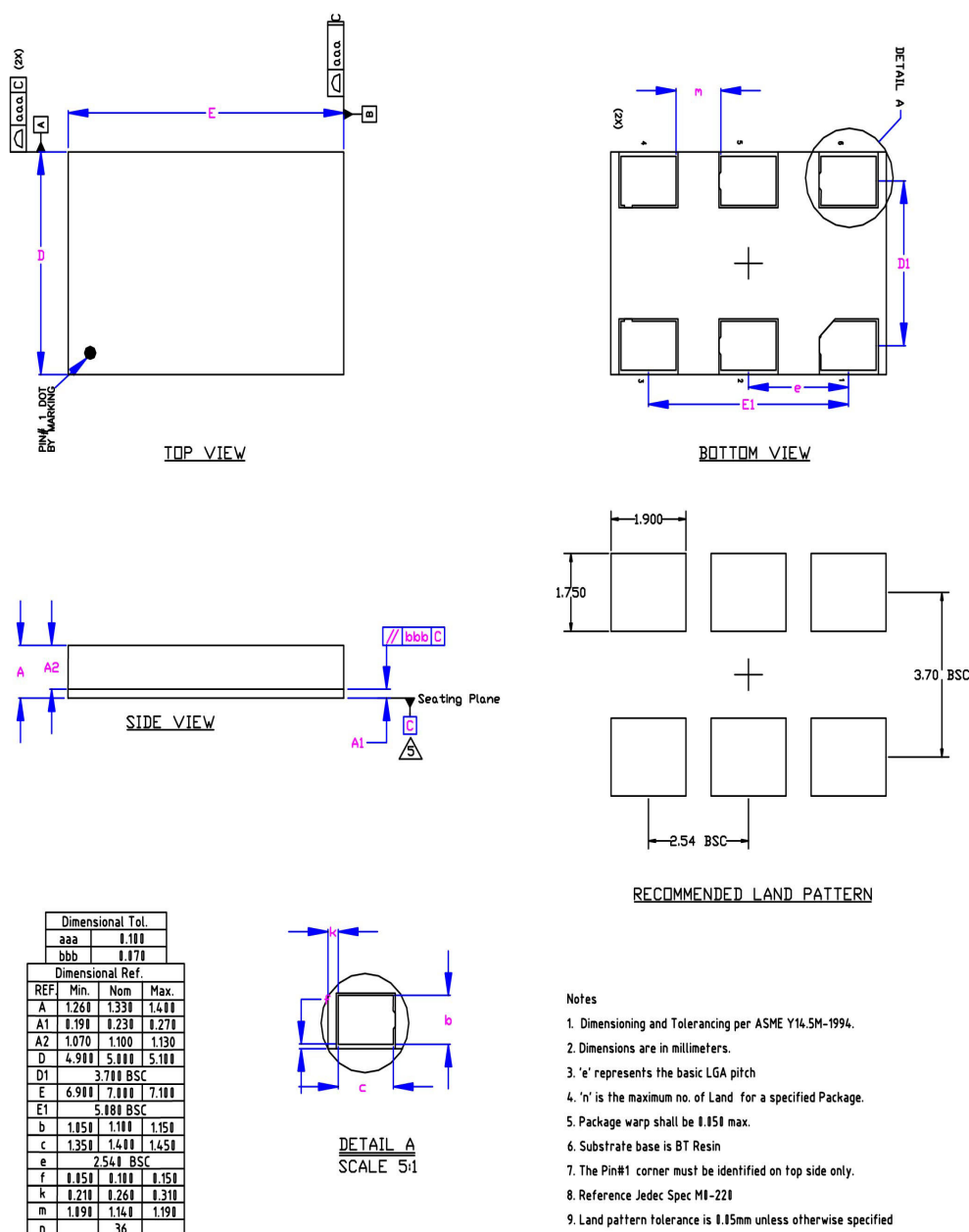


Figure 2. LVC MOS Output 25MHz 12kHz-5MHz 131fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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