DDR Termination Regulator

General Description

The RT9089A is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9089A possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 10μF ceramic output capacitor. The RT9089A supports remote sensing functions and all features required to power the DDRI/DDRII/DDRIII/DDRIV/LPDDRII/LPDDRIII VTT bus termination according to the JEDEC specification.

The RT9089A is available in the thermal efficient package, WDFN-10L 2x2.

Ordering Information

RT9089A□□□

- Pin 1 Orientation
  (2) : Quadrant 2, Follow EIA-481
  (Empty means Pin1 orientation is Quadrant 1)
- Package Type
  QW : WDFN-10L 2x2 (W-Type)
- Lead Plating System
  G: Richtek Green Policy Compliant

Note :

Richtek products are Richtek Green Policy compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.

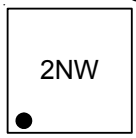
Features

- **VIN Input Voltage Range : 1.1V to 3.5V**
- **VCNTL Input Voltage Range : 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **10mA Source/Sink Reference Output**
- **Meet DDRI, DDRII JEDEC Spec**
- **Support DDRIII, DDRIV, LPDDRII and LPDDRIII Applications**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**

Applications

- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

Marking Information

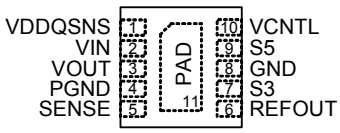


2N : Product Code

W : Date Code

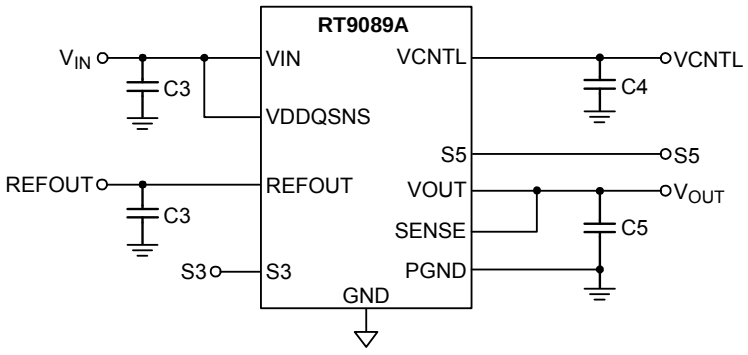
Pin Configuration

(TOP VIEW)



WDFN-10L 2x2

Simplified Application Circuit



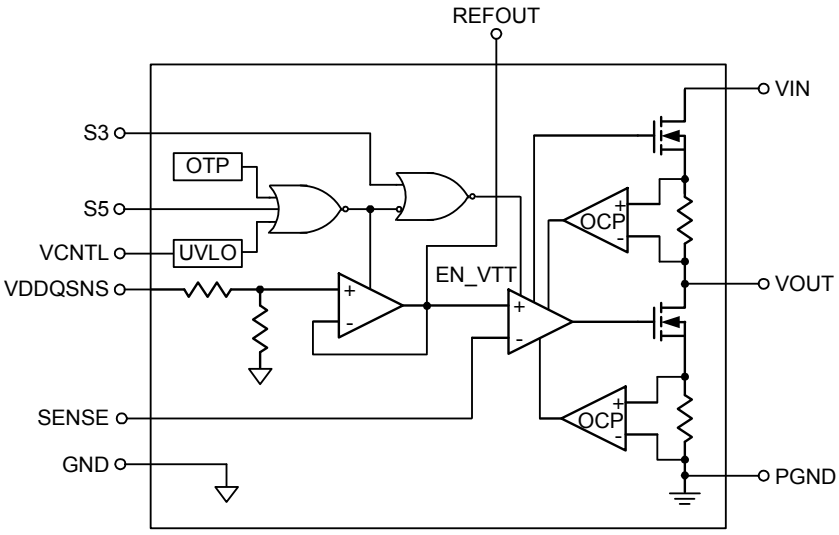
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Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VDDQSNS	Reference input.
2	VIN	Power input of the regulator.
3	VOUT	Power output of the regulator.
4	PGND	Power ground of the regulator.
5	SENSE	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
6	REFOUT	Reference output. Connect to GND through a 0.1μF ceramic capacitor.
7	S3	S3 signal input.
8	GND	Analog ground. Connect to negative terminal of the output capacitor.
9	S5	S5 signal input.
10	VCNTL	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A 4.7μF ceramic decoupling capacitor is required.
11 (Exposed Pad)	PAD	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Functional Block Diagram



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Operation

The RT9089A is a linear sink/source DDR termination regulator with current capability up to 2A. The RT9089A builds in a high-side N-MOSFET which provides current sourcing and a low-side N-MOSFET which provides current sinking. All the control circuits are supplied by the power VCNTL. In normal operation, the error amplifier OP adjusts the gate driving voltage of the power MOSFET to achieve SENSE voltage well tracking the VDDQSNS/2 voltage.

Both the source and sink currents are detected by the internal sensing resistor, and the OCP function will work to limit the current to a designed value when overload happens. Furthermore, the current will be folded back to be one half if VOUT is out of the power good window.

Buffer

This function provides REFOUT output level which is equal to VDDQSNS/2 with 10mA source/sink current capability.

Control Logic

This block includes VCNTL UVLO, VDDQSNS UVLO and Enable/Disable functions, and provides logic control to the whole chip.

Thermal Protection

Both the high-side and low-side power MOSFETs will be turned off when the junction temperature is higher than typically 160°C, and be released to normal operation when junction temperature falls below 120°C typically.

Power State Control

The input pins S3 and S5 of RT9089A, provide simple control of the power state. Table 1 describes S3/S5 terminal logic state and corresponding state of REFOUT/VOUT outputs. VOUT is turn-off and discharged to GND in state S3. When both S5 and S3 pins are LOW, the power state is set to S4/S5. In S4/S5 state, all the outputs are turn-off and discharged to GND.

Table 1. S3 and S5 Control Table

STATE	S3	S5	REFOUT	VOUT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF (Discharge)
S4/S5	LO	LO	OFF (Discharge)	OFF (Discharge)

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Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN, VCNTL ---------- –0.3V to 6V
- Input Voltage, S3, VDDQSNS, SENSE, S5 ---------- –0.3V to 6V
- Output Voltage, VOUT, REFOUT ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-10L 2x2 ---------- 1.25W
- Package Thermal Resistance (Note 2)
  WDFN-10L 2x2, θ_{JA} ---------- 80°C/W
  WDFN-10L 2x2, θ_{JC} ---------- 7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Control Input Voltage, VCNTL ---------- 2.9V to 5.5V
- Supply Input Voltage, VIN ---------- 1.1V to 3.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = $V_{VDDQSNS}$ = 1.5V, V_{CNTL} = 3.3V, V_{SENSE} = 0.75V, C_{OUT} = 10µF x 1, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCNTL Supply Current	I_{VCNTL}	V_{S3} = VCNTL, V_{S5} = VCNTL, no load	--	0.7	1	mA
VCNTL Shutdown Current	I_{SHDN_VCNTL}	V_{S3} = 0V, V_{S5} = 0V, no load	--	65	80	µA
		V_{S3} = 0V, V_{S5} = VCNTL, no load	--	200	400	µA
VIN Supply Current	I_{VIN}	V_{S3} = VCNTL, V_{S5} = VCNTL, no load	--	1	50	µA
VIN Shutdown Current	I_{SHDN_VIN}	V_{S3} = 0V, V_{S5} = 0V, no load	--	0.1	50	µA
Output						
VOUT Output Voltage	V_{OUT}	V_{IN} = 1.5V, $V_{VDDQSNS}$ = 1.5V, I_{OUT} = 0A	--	0.75	--	V
		V_{IN} = 1.35V, $V_{VDDQSNS}$ = 1.35V, I_{OUT} = 0A	--	0.675	--	V
		V_{IN} = 1.2V, $V_{VDDQSNS}$ = 1.2V, I_{OUT} = 0A	--	0.6	--	V
VOUT Output Voltage Offset	V_{OUT_OS}	I_{OUT} = ±2A, V_{IN} = 1.5V, V_{REFOUT} = 0.75V	–25	--	25	mV
		I_{OUT} = ±2A, V_{IN} = 1.35V, V_{REFOUT} = 0.675V	–25	--	25	
		I_{OUT} = ±2A, V_{IN} = 1.2V, V_{REFOUT} = 0.6V	–25	--	25	

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT Source Current Limit		$I_{LIM_VOUT_SR}$	VOUT in PGOOD window	2	--	--	A
VOUT Sink Current Limit		$I_{LIM_VOUT_SK}$	VOUT in PGOOD window	2	--	--	A
VOUT Discharge Resistance		$R_{DISCHARGE}$	$V_{VDDQSNS}$ = 0V, V_{OUT} = 0.3V, V_{S3} = 0V	--	18	25	Ω
VDDQSNS and REFOUT							
VDDQSNS Input Current		$I_{VDDQSNS}$	$V_{VDDQSNS}$ = 1.8V	--	30	--	μA
VDDQSNS Voltage Range		$V_{VDDQSNS}$		0.5	--	1.8	V
REFOUT Voltage Tolerance to $V_{VDDQSNS}$		V_{TOL_REFOUT}	−10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.5V	−15	--	15	mV
			−10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.35V	−13.5	--	13.5	
			−10mA < I_{REFOUT} < 10mA, $V_{VDDQSNS}$ = 1.2V	−12	--	12	
REFOUT Source Current Limit		$I_{LIM_REFOUT_SR}$	V_{REFOUT} = 0V	10	40	--	mA
REFOUT Sink Current Limit		$I_{LIM_REFOUT_SK}$	V_{REFOUT} = VDDQSNS / 2 + 1V	10	40	--	mA
UVLO/S3/S5							
UVLO Threshold		V_{UVLO_VCNTL}	Rising	2.5	2.7	2.85	V
			Hysteresis	--	120	--	mV
S3/S5 Input Voltage	Logic-High	V_{IN_H}		1.7	--	--	V
	Logic-Low	V_{IN_L}		--	--	0.3	
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}	Shutdown temperature	--	160	--	°C
			Hysteresis	--	15	--	

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

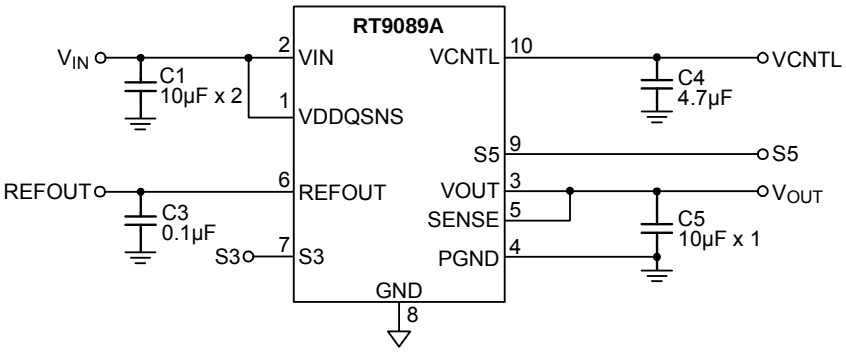
Note 3. Devices are ESD sensitive. Handling precautions are recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Typical Application Circuit

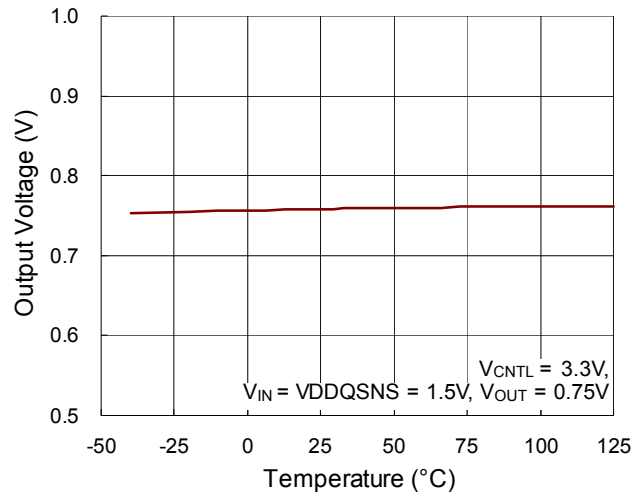


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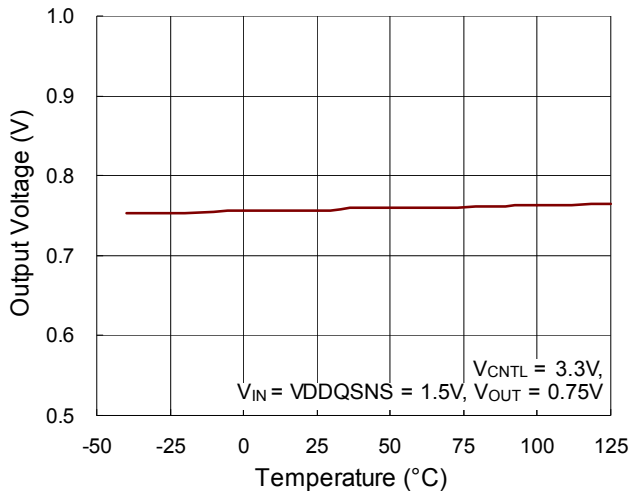
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Typical Operating Characteristics

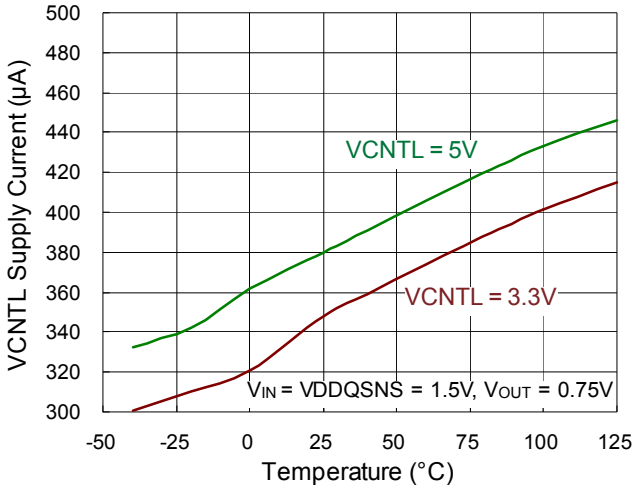
Output Voltage vs. Temperature



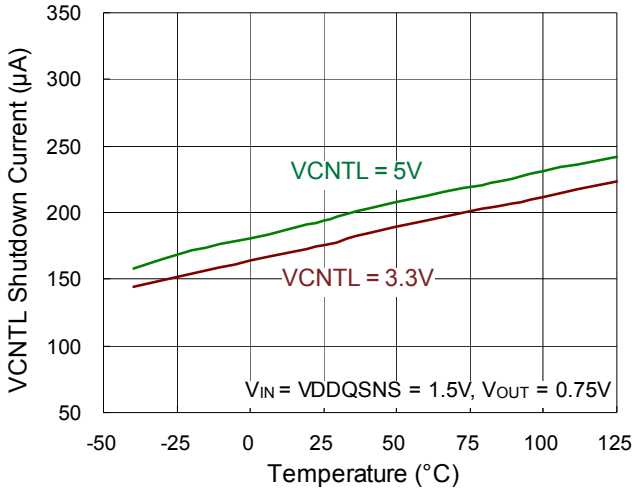
REFOUT Voltage vs. Temperature



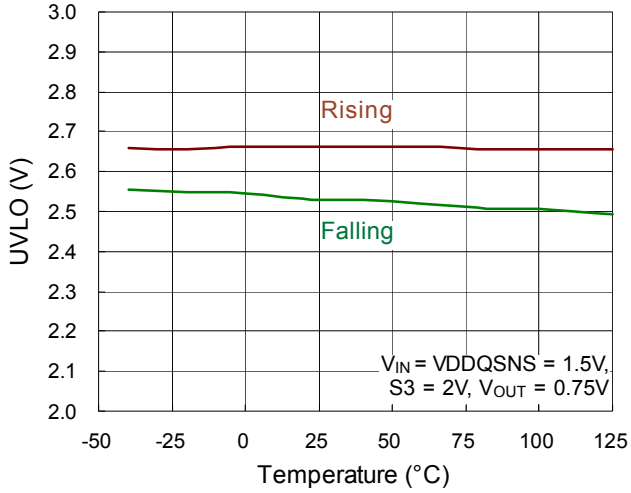
VCNTL Supply Current vs. Temperature



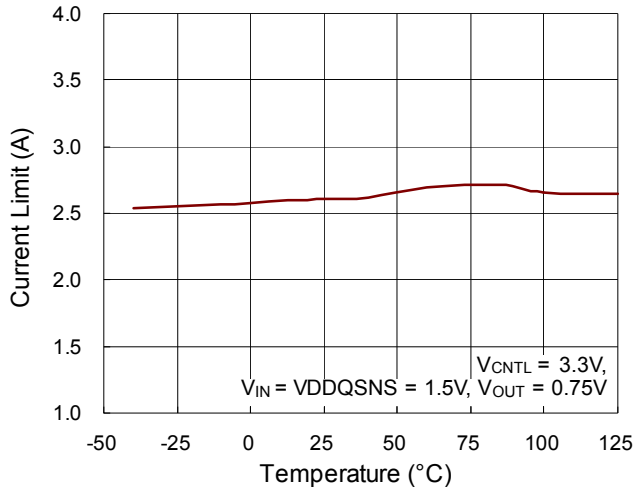
VCNTL Shutdown Current vs. Temperature



UVLO vs. Temperature



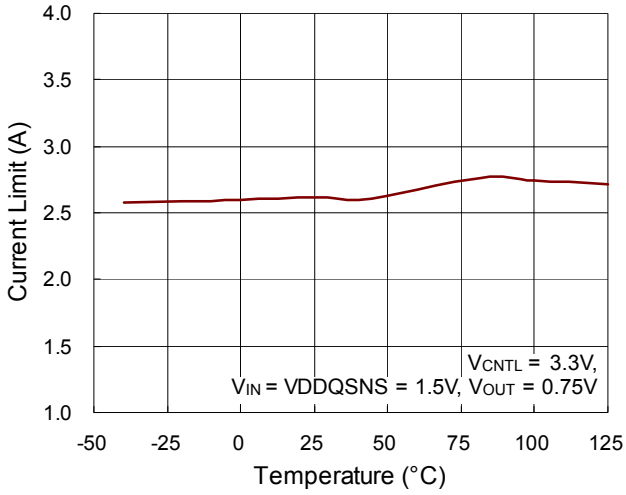
Sourcing Current Limit vs. Temperature



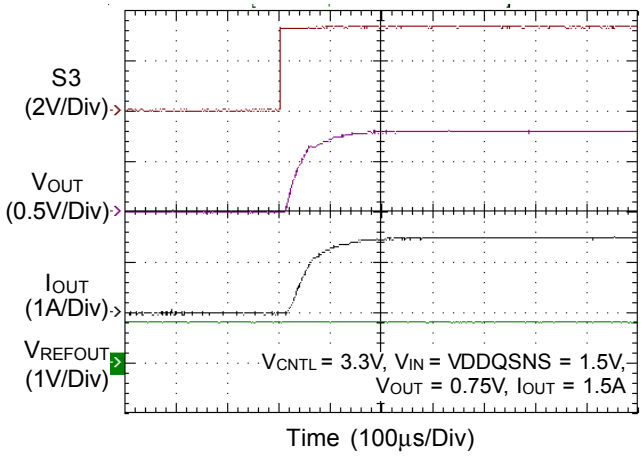
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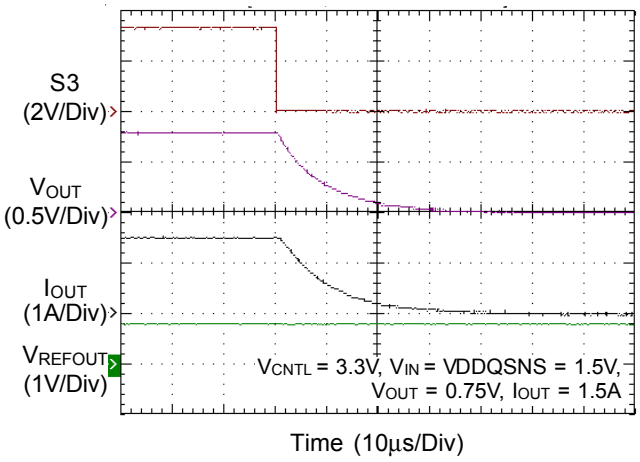
Sinking Current Limit vs. Temperature



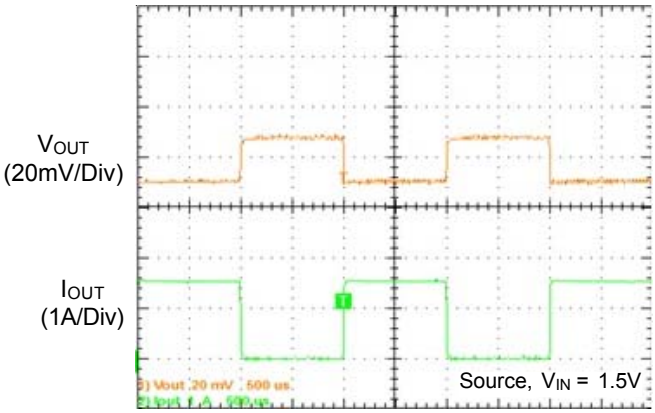
Power On from S3



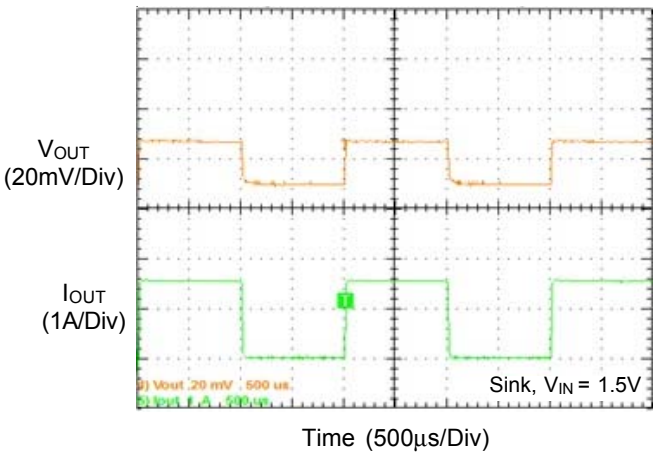
Power Off from S3



0.75V_{OUT} @ 1.5A Transient Response



0.75V_{OUT} @ 1.5A Transient Response



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Application Information

Richtek's component specification does not include the following information in the Application Information section. Thereby no warranty is given regarding its validity and accuracy. Customers should take responsibility to verify their own designs and reserve suitable design margin to ensure the functional suitability of their components and systems.

The RT9089A is a 2A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT9089A possesses a high speed operating amplifier that provides fast load transient response and only requires two 10μF ceramic input capacitor and a 10μF ceramic output capacitors.

Capacitor Selection

Good bypassing is recommended from VIN to GND to help improve AC performance. A 10μF or greater input capacitor placed as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the VIN pin of the IC.

The 1μF ceramic capacitor added close to the VCNTL pin should be kept away from any parasitic impedance from the supply power. For stable operation, the total capacitance of the ceramic capacitor at the VOUT output terminal must be larger than 10μF. The RT9089A is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VOUT output terminal pin as close as possible.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-10L 2x2 package, the thermal resistance, θ_{JA}, is 80°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (80°C/W) = 1.25W for WDFN-10L 2x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

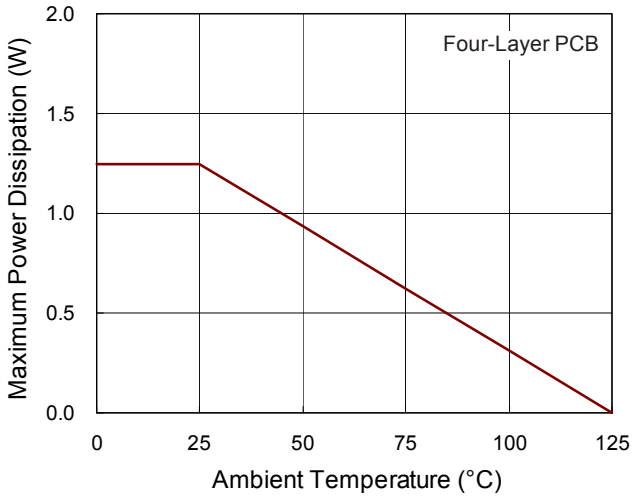
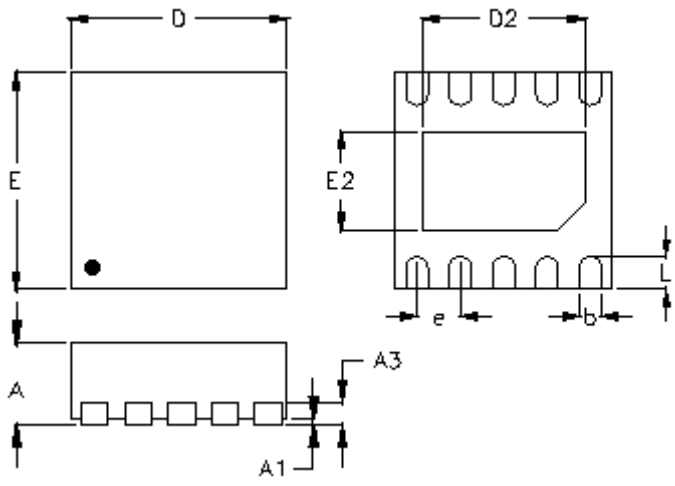


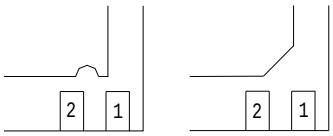
Figure 1. Derating Curve of Maximum Power Dissipation

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D2	1.450	1.550	0.057	0.061
E	1.900	2.100	0.075	0.083
E2	0.850	0.950	0.033	0.037
e	0.400		0.016	
L	0.250	0.350	0.010	0.014

W-Type 10L DFN 2x2 Package

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Datasheet Revision History

Version	Date	Description	Item
06	2023/11/6	Modify	Ordering Information on P1 Electrical Characteristics on P5 Application Information on P9

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