IS25WJ128F

128Mb
1.8V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

DATA SHEET

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128Mb

1.8V SERIAL FLASH MEMORY WITH 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

FEATURES

- **Industry Standard Serial Interface**
  - IS25WJ128F: 128Mbit/16Mbyte
  - 256 bytes per Programmable Page
  - Supports standard SPI, Fast, Dual, Dual I/O, Quad, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
  - Supports Serial Flash Discoverable Parameters (SFDP)

- **High Performance Serial Flash (SPI)**
  - 66MHz Normal and 133Mhz Fast Read
  - 532 MHz equivalent QPI
  - DTR (Dual Transfer Rate) up to 80MHz
  - Selectable Dummy cycles
  - Configurable Drive Strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 Erase/Program Cycles
  - More than 20-year Data Retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform: Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 Bytes per Page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Continuous Read 8/16/32/64-Byte Burst Wrap
  - Selectable Burst Length
  - QPI for Reduced Command Overhead

Low Power with Wide Temp. Ranges
- Single 1.65V to 2.0V Voltage Supply
- 8 µA Standby Current (typ.)
- 0.1 µA Deep Power Down (typ.)
- Temp Grades:
  Extended: -40°C to +105°C
  Auto Grade (A2): -40°C to +105°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Power Supply Lock Protect
  - 3x1024-Byte Dedicated Security Area with OTP User-lockable Bits
  - 128 bit Unique ID for Each Device (Call Factory)

- **Industry Standard Pin-out & Packages**[2]
  - M = 16-pin SOIC 300mil (Call Factory)
  - E = 8-contact XSON 4x4mm
  - K = 8-contact WSON 6x5mm
  - L = 8-contact WSON 8x6mm
  - N = 8-pin SOIC 150mil (Call Factory)
  - B = 8-pin SOIC 208mil
  - G = 24-ball TFBGA (4x6 ball array) (Call Factory)
  - H = 24-ball TFBGA (5x5 ball array)
  - W = KGD (Call Factory)
- Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

Notes:
1. Call Factory for extended or extended+ options
2. Call Factory for other package options

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GENERAL DESCRIPTION

The IS25WJ128F Serial Flash memory offers a versatile storage solution with high flexibility and performance in a simplified pin count package. ISSI's "Industry Standard Serial Interface" Flash is for systems that require limited space, a low pin count, and low power consumption. The device is accessed through a 4-wire SPI Interface consisting of a Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins, which can also be configured to serve as multi-I/O (see pin descriptions).

The device supports Dual and Quad I/O as well as standard, Dual Output, and Quad Output SPI. Clock frequencies of up to 133MHz allow for equivalent clock rates of up to 532MHz (133MHz x 4) which equates to 83Mbytes/s of data throughput. The IS25WJxxxF series of Flash adds support for DTR (Double Transfer Rate) commands that transfer addresses and read data on both edges of the clock. These transfer rates can outperform 16-bit Parallel Flash memories allowing for efficient memory access to support XIP (execute in place) operation.

The memory array is organized into programmable pages of 256-bytes. This family supports page program mode where 1 to 256 bytes of data are programmed in a single command. QPI (Quad Peripheral Interface) supports 2-cycle command further reducing command times. Pages can be erased in groups of 4Kbyte sectors, 32Kbyte blocks, 64Kbyte blocks, and/or the entire chip. The uniform sector and block architecture allows for a high degree of flexibility so that the device can be utilized for a broad variety of applications requiring solid data retention.

GLOSSARY

Standard SPI
In this operation, a 4-wire SPI Interface is utilized, consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Clock (SCK), and Chip Enable (CE#) pins. Commands are sent via the SI pin to encode commands, addresses, or input data to the device on the rising edge of SCK. The SO pin is used to read data or to check the status of the device. This device supports SPI bus operation modes (0, 0) and (1, 1).

Multi I/O SPI
Multi-I/O operation utilizes an enhanced SPI protocol to allow the device to function with Dual Output, Dual Input and Output, Quad Output, and Quad Input and Output capability. Executing these commands through SPI mode will achieve double or quadruple the transfer bandwidth for READ and PROGRAM operations.

QPI
The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the enter QPI (38h) command. The typical SPI protocol requires that the byte-long command code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the command code thus requiring only two serial clocks. This can significantly reduce the SPI command overhead and improve system performance. Only QPI mode or SPI/Dual/Quad mode can be active at any given time. Enter QPI (38h) and Exit QPI (FFh) commands are used to switch between these two modes, regardless of the non-volatile Quad Enable (QE) bit status in the Status Register. Power Reset or Hardware/Software Reset can also return the device into the standard SPI mode.SI and SO pins become bidirectional I/O0 and I/O1, and WP# and HOLD# pins become I/O2 and I/O3 respectively during QPI mode.

DTR
In addition to SPI and QPI features, the device also supports Fast READ DTR operation. Fast READ DTR operation allows high data throughput while running at lower clock frequencies. Fast READ DTR operation uses both rising and falling edges of the clock for address inputs, and data outputs, resulting in reducing input and output cycles by half.

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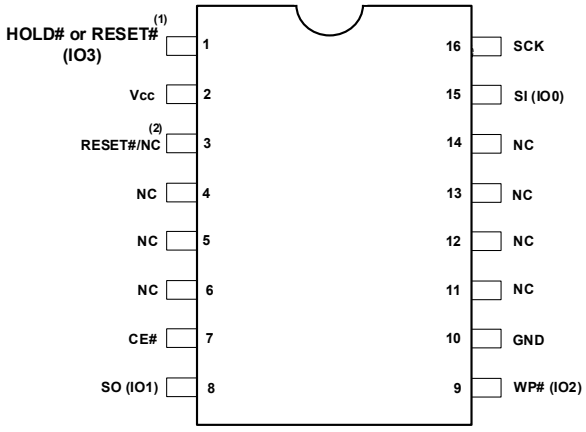
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1. PIN CONFIGURATION

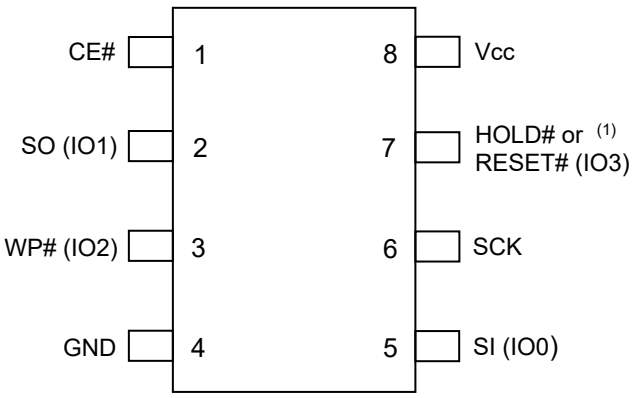


16-pin SOIC 300mil

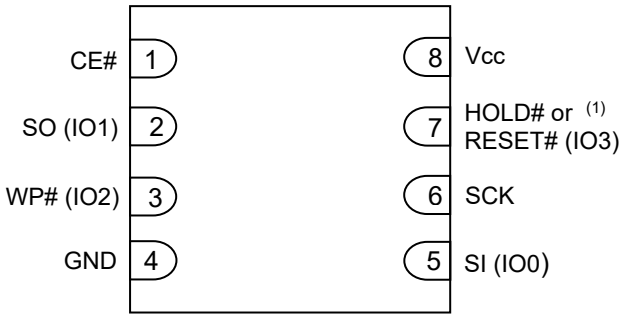
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Notes:

1. **The pin can be configured as Hold# or Reset# by setting bit23 of the Status Register. Pin default is Hold# (IO3)**
2. **Dedicated RESET# pin is available in devices with a dedicated part number.**



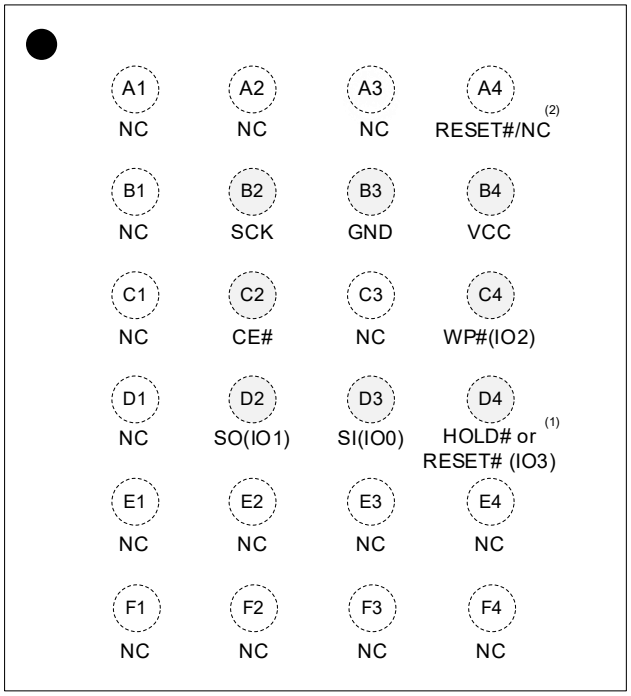
8-pin SOIC 150mil (Package: N)
8-pin SOIC 208mil (Package: B)



8-contact XSON 4x4mm (Package: E)
8-contact WSON 6x5mm (Package: K)
8-contact WSON 8x6mm (Package: L)

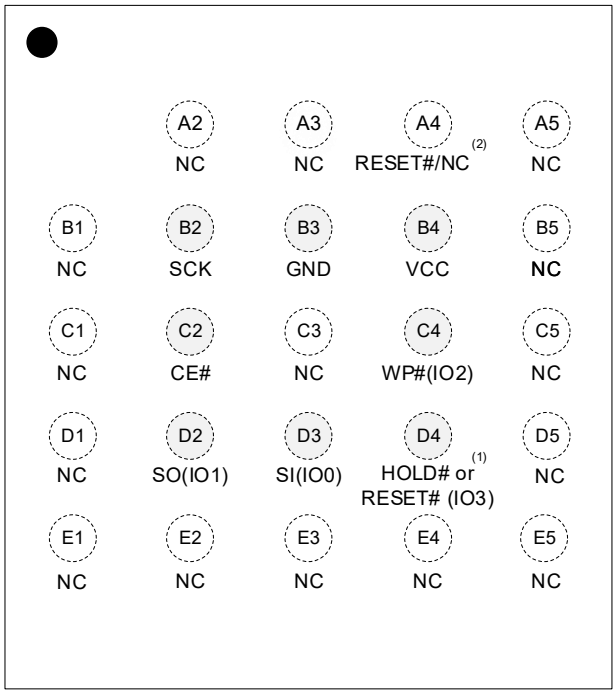
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Top View, Balls Facing Down



24-ball TFBGA, 4x6 Ball Array (Package:G)

Top View, Balls Facing Down



24-ball TFBGA, 5x5 Ball Array (Package:H)

Notes:

1. **The pin can be configured as Hold# or Reset# by setting bit 23 of the Status Register. Pin default is Hold# (IO3)**
2. **Dedicated RESET# pin is available in devices with a dedicated part number.**

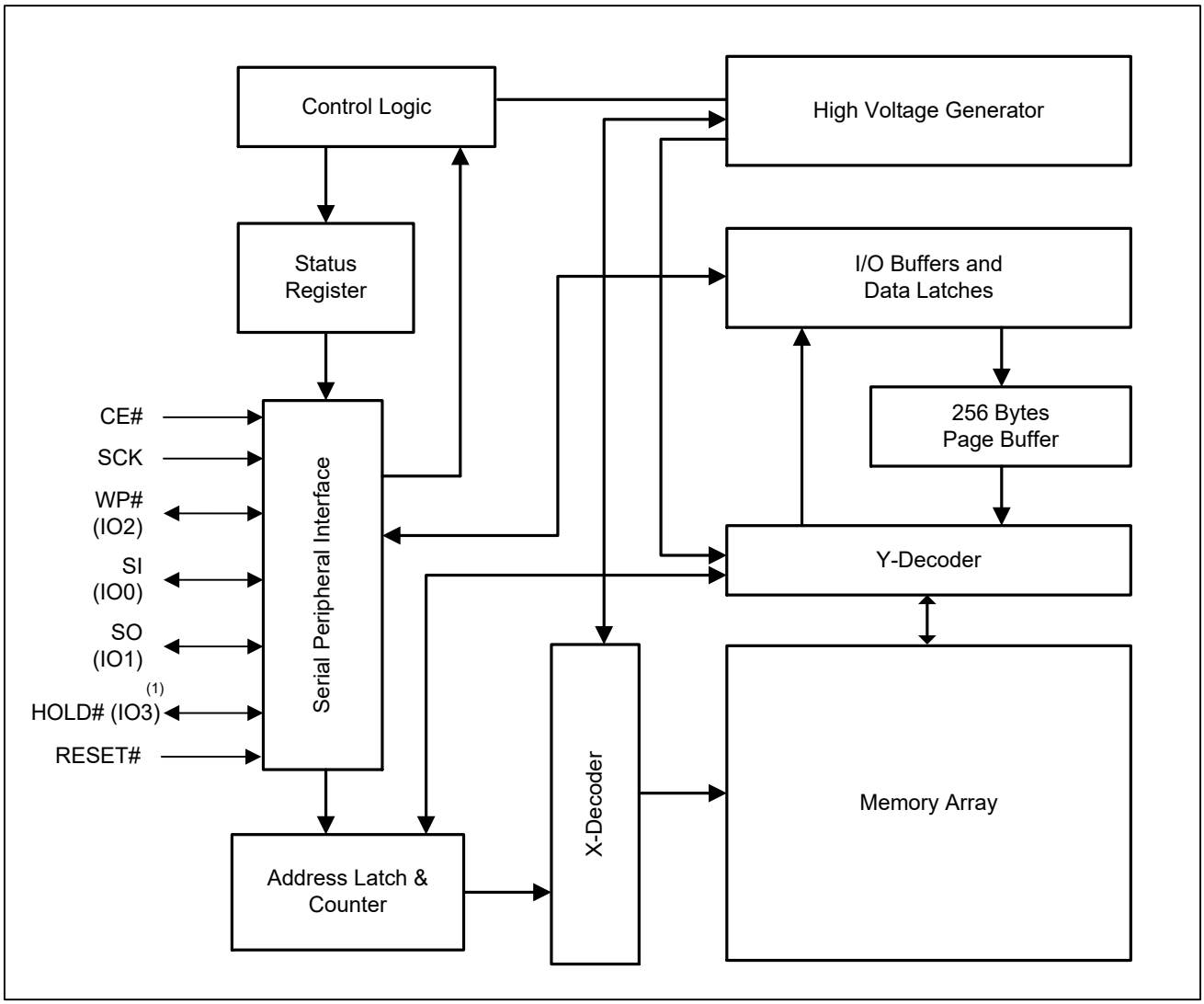
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2. PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	Same as the description in previous page
SI (IO0), SO (IO1)	INPUT/OUTPUT	Same as the description in previous page
WP# (IO2)	INPUT/OUTPUT	Same as the description in previous page
HOLD# (IO3) or RESET# (IO3)	INPUT/OUTPUT	**HOLD# or RESET#/Serial Data IO (IO3):** When the QE bit of Status Register is set to "1", HOLD# pin or RESET# is not available since it becomes IO3. When QE=0, the pin acts as HOLD# or RESET# and either one can be selected by the bit23 setting in Status Register. HOLD# will be selected if P7=0 (Default) and RESET# will be selected if P7=1. The HOLD# pin allows the device to be paused while it is selected. It pauses serial communication by the master device without resetting the serial sequence. The HOLD# pin is active low. When HOLD# is in a low state and CE# is low, the SO pin will be at high impedance. Device operation can resume when HOLD# pin is brought to a high state.
RESET#	INPUT/OUTPUT	**RESET#:** This dedicated RESET# is available in 16-pin SOIC and 24-ball BGA packages. The RESET# pin is a hardware RESET signal. It has an internal pull-up resistor and may be left floating if not used.
SCK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled "NC" stand for "No Connect". Not internally connected.

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3. BLOCK DIAGRAM



Note:

1: HOLD# will be selected if bit23 bit of status register-3 is 0 (Default), and RESET# will be selected if bit23 bit is 1.

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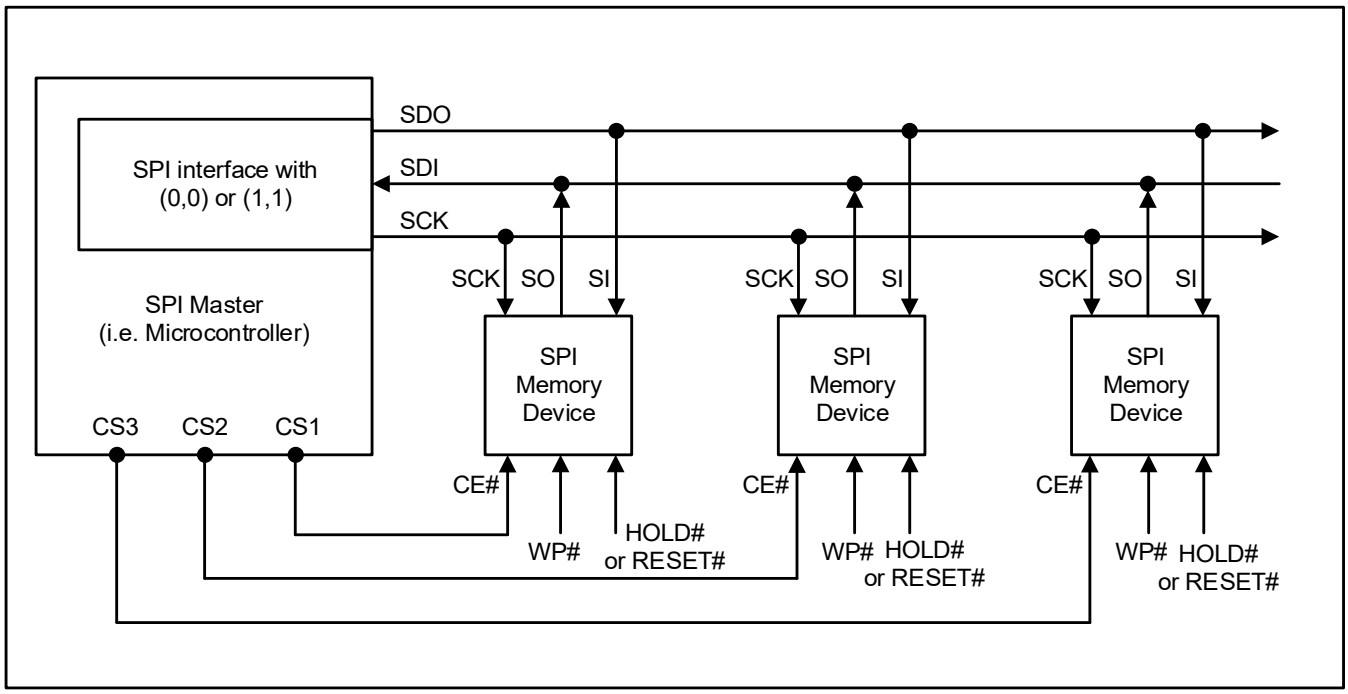
4. SPI MODES DESCRIPTION

Multiple IS25WJ128F devices can be connected on the SPI serial bus and controlled by a SPI Master, i.e. microcontroller, as shown in Figure 4.1. The devices support either of two SPI modes:

Mode 0 (0, 0)
Mode 3 (1, 1)

The difference between these two modes is the clock polarity. When the SPI master is in stand-by mode, the serial clock remains at "0" (SCK = 0) for Mode 0 and the clock remains at "1" (SCK = 1) for Mode 3. Please refer to Figure 4.2 and Figure 4.3 for SPI and QPI mode. In both modes, the input data is latched on the rising edge of Serial Clock (SCK), and the output data is available from the falling edge of SCK.

Figure 4.1 Connection Diagram among SPI Master and SPI Slaves (Memory Devices)



Notes:
1. SI and SO pins become bidirectional IO0 and IO1 respectively during Dual I/O mode and SI, SO, WP#, and HOLD# pins become bidirectional IO0, IO1, IO2, and IO3 respectively during Quad I/O or QPI mode.

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Figure 4.2 SPI Mode Support

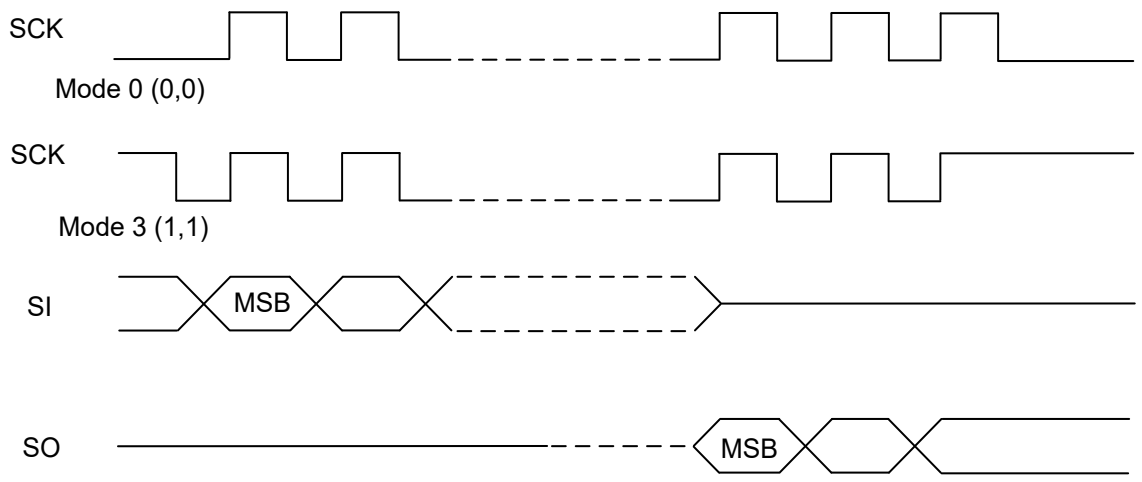
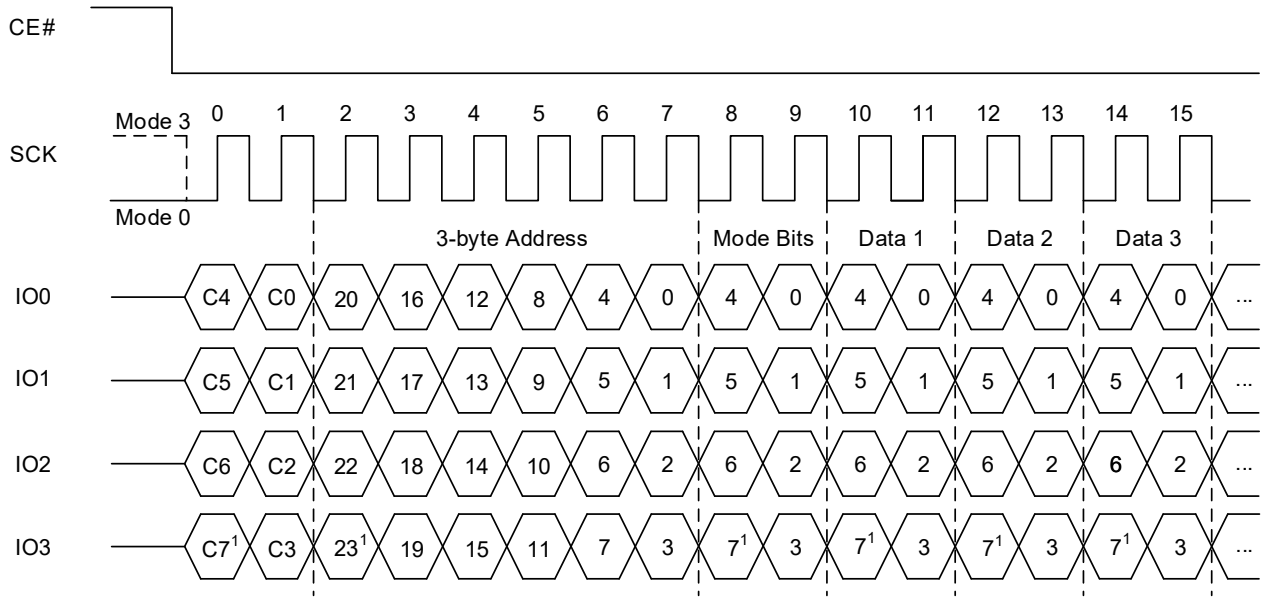


Figure 4.3 QPI Mode Support



Note1: MSB (Most Significant Bit)

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5. SYSTEM CONFIGURATION

The memory array is divided into uniform 4 Kbyte sectors or uniform 32/64 Kbyte blocks (a block consists of eight/sixteen adjacent sectors respectively).

Table 5.1 illustrates the memory map of the device. The Status Register controls how the memory is protected.

5.1 BLOCK/SECTOR ADDRESSES

Table 5.1 Block/Sector Addresses

Memory Density	Block No. (64Kbyte)	Block No. (32Kbyte)	Sector No.	Sector Size (Kbyte)	Address Range
128Mb	Block 0	Block 0	Sector 0	4	000000h – 000FFFh
			:	:	:
		Block 1	:	:	:
			Sector 15	4	00F000h – 00FFFFh
	Block 1	Block 2	Sector 16	4	010000h – 010FFFh
			:	:	:
		Block 3	:	:	:
			Sector 31	4	01F000h – 01FFFFh
	Block 2	Block 4	Sector 32	4	020000h – 020FFFh
			:	:	:
		Block 5	:	:	:
			Sector 47	4	02F000h – 02FFFFh
	:	:	:	:	:
	Block 15	Block 30	Sector 240	4	0F0000h – 0F0FFFh
			:	:	:
		Block 31	:	:	:
			Sector 255	4	0FF000h – 0FFFFFh
	:	:	:	:	:
	Block 31	Block 62	Sector 496	4	1F0000h – 1F0FFFh
			:	:	:
		Block 63	:	:	:
			Sector 511	4	1FF000h – 1FFFFFh
	:	:	:	:	:
	Block 254	Block 508	Sector 4054	4	FE0000h – FE0FFFh
			:	:	:
		Block 509	:	:	:
			Sector 4069	4	FEF000h – FEFFFFh
	Block 255	Block 510	Sector 4070	4	FF0000h – FF0FFFh
			:	:	:
		Block 511	:	:	:
			Sector 4095	4	FFF000h – FFFFFFh

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5.2 SERIAL FLASH DISCOVERABLE PARAMETERS

The Serial Flash Discoverable Parameters (SFDP) standard defines the structure of the SFDP database within the memory device. SFDP is the standard of JEDEC JESD216.
The JEDEC-defined header with Parameter ID FF00h and related Basic Parameter Table is mandatory. Additional parameter headers and tables are optional.

Table 5.2 Signature and Parameter Identification Data Values

Description		Address (Byte)	Address (Bit)	Data
SFDP Signature		00h	7:0	53h
		01h	15:8	46h
		02h	23:16	44h
		03h	31:24	50h
SFDP Revision	Minor	04h	7:0	06h
	Major	05h	15:8	01h
Number of Parameter Headers (NPH)		06h	23:16	00h
Unused		07h	31:24	FFh
Parameter ID LSB		08h	7:0	00h
Parameter Minor Revision		09h	15:8	06h
Parameter Major Revision		0Ah	23:16	01h
Parameter Table Length (in DWPRDs)		0Bh	31:24	10h
Basic Flash Parameter Table Pointer (PTP)		0Ch	7:0	30h
		0Dh	15:8	00h
		0Eh	23:16	00h
Parameter ID MSB		0Fh	31:24	FFh

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Table 5.3 JEDEC Basic Flash Parameter Table

Description	Address (Byte)	Address (Bit)	Data
Minimum Sector Erase Sizes	30h	1:0	01b
Write Granularity		2	1b
Volatile Status Register Block Protect bits		3	0b
Write Enable Command Select for writing to Volatile Status Register		4	0b
Unused		7:5	111b
4KB Erase Command	31h	15:8	20h
Supports (1-1-2) Fast Read	32h	16	1b
Address Bytes		18:17	00b
Supports Double Transfer Rate (DTR) Clocking		19	1b
Supports (1-2-2) Fast Read		20	1b
Supports (1-4-4) Fast Read		21	1b
Supports (1-1-4) Fast Read		22	1b
Unused		23	1b
Unused	33h	31:24	FFh
Flash memory Density (bits)	34h	7:0	FFh
	35h	15:8	FFh
	36h	23:16	FFh
	37h	31:24	07h
1-4-4 Fast Read Wait Cycle Count	38h	4:0	00100b
1-4-4 Fast Read Mode bit Cycle Count		7:5	010b
1-4-4 Fast Read Command	39h	15:8	EBh
1-1-4 Fast Read Wait Cycle Count	3Ah	20:16	01000b
1-1-4 Fast Read Mode bit Cycle Count		23:21	000b
1-1-4 Fast Read Command	3Bh	31:24	6Bh
1-1-2 Fast Read Wait Cycle Count	3Ch	4:0	01000b
1-1-2 Fast Read Mode bit Cycle Count		7:5	000b
1-1-2 Fast Read Command	3Dh	15:8	3Bh
1-2-2 Fast Read Wait Cycle Count	3Eh	20:16	00000b
1-2-2 Fast Read Mode bit Cycle Count		23:21	100b
1-2-2 Fast Read Command	3Fh	31:24	BBh

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Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description	Address (Byte)	Address (Bit)	Data
Supports (2-2-2) Fast Read	40h	0	0b
Reserved		3:1	111b
Supports (4-4-4) Fast Read		4	1b
Reserved		7:5	111b
Reserved	43:41h	31:8	FFFFFFh
Reserved	45:44h	15:0	FFFFh
2-2-2 Fast Read Wait Cycle Count	46h	20:16	00000b
2-2-2 Fast Read Mode bit Cycle Count		23:21	000b
2-2-2 Fast Read Command	47h	31:24	FFh
Reserved	49:48h	15:0	FFFFh
4-4-4 Fast Read Quad I/O Wait Cycle Count at QPI mode	4Ah	20:16	00010b
4-4-4 Fast Read Quad I/O Mode bit Cycle Count at QPI mode		23:21	010b
4-4-4 Fast Read Quad I/O Command at QPI mode	4Bh	31:24	EBh
Erase Type 1 Size (4KB)	4Ch	7:0	0Ch
Erase Type 1 Command	4Dh	15:8	20h
Erase Type 2 Size (32KB)	4Eh	23:16	0Fh
Erase Type 2 Command	4Fh	31:24	52h
Erase Type 3 Size (64KB)	50h	7:0	10h
Erase Type 3 Command	51h	15:8	D8h
Erase Type 4 Size (256KB)	52h	23:16	00h
Erase Type 4 Command	53h	31:24	FFh
Multiplier from typical erase time to maximum erase time, 2*(Count+1), 6.0	57:54h	3:0	0010b
Sector Type 1 ERASE time (typ), (Count+1) * units, 90/300ms		8:4	00101b
Units (00b:1ms, 01b:16ms, 10b:128ms, 11b:1s)		10:9	01b
Sector Type 2 ERASE time (typ), (Count+1) * units, 150/800ms		15:11	01001b
Units (00b:1ms, 01b:16ms, 10b:128ms, 11b:1s)		17:16	01b
Sector Type 3 ERASE time (typ), (Count+1) * units, 200/1200ms		22:18	01100b
Units (00b:1ms, 01b:16ms, 10b:128ms, 11b:1s)		24:23	01b
Sector Type 4 ERASE time (typ), (Count+1) * units		29:25	00000b
Units (00b:1ms, 01b:16ms, 10b:128ms, 11b:1s)		31:30	00b

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Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description	Address (Byte)	Address (Bit)	Data
Multiplier from typical time to maximum time for page or byte PROGRAM, 2* (Count+1), 6.0	58h	3:0	0010b
Page size		7:4	1000b
Page Program Typical time, (Count+1) * units, 400/2400us	5Ah:59h	12:8	00110b
Units (0b:8us, 1b:64us)		13	1b
Byte Program Typical time, first byte, (Count+1) * units, 15/50us		17:14	0001b
Units, 0b:1us, 1b:8us		18	1b
Byte Program Typical time, additional byte, (Count+1) * units, (tPP-tBP)/255, 1.51us		22:19	0001b
Units (0b:1us, 1b:8us)		23	0b
Chip Erase, Typical time, (Count+1) * units, 32/80s	5Bh	28:24	00111b
Units (00b:16ms, 01b:256ms, 10b:4s, 11b:64s)		30:29	10b
Reserved		31	1b
Prohibited Operations During Program Suspend	5Ch	3:0	1100b
Prohibited Operations During Erase Suspend		7:4	1110b
Reserved	5Eh:5Dh	8	1b
Program Resume to Suspend Interval, (Couint+1) * 64us, 100us		12:9	0001b
Suspend in-progress program max latency, (Count+1) * units, 20us		17:13	00010b
Units (00b:128ns, 01b:1us, 10b:8us, 11b:64us)		19:18	10b
Erase Resume to Suspend Interval, (Couint+1) * 64us, 100us		23:20	0001b
Suspend in-progress erase max latency, (Count+1) * units, 20us	5Fh	28:24	00010b
Units (00b:128ns, 01b:1us, 10b:8us, 11b:64us)		30:29	10b
Suspend /Resume supported		31	0b
Program Resume Command	60h	7:0	7Ah
Program Suspend Command	61h	15:8	75h
Resume Command	62h	23:16	7Ah
Suspend Command	63h	31:24	75h
Reserved	64h	1:0	11b
Status Register Polling Device Busy		7:2	111101b

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Table 5.3 JEDEC Basic Flash Parameter Table (Continued)

Description	Address (Byte)	Address (Bit)	Data
Exit Deep Power-down to next operation delay, (Couint+1) * units, 5 us	67h:65h	12:8	00100b
Units (00b:128ns, 01b:1us, 10b:8us, 11b:64us)		14:13	01b
Exit Deep Power-down Command		22:15	ABh
Enter Deep Power-down Command		30:23	B9h
Deep Power-down Supported		31	0b
4-4-4 mode disable sequences (QPIDI)	69h:68h	3:0	1001b
4-4-4 mode enable sequences (QPIEN)		8:4	00001b
0-4-4 Mode Supported		9	1b
0-4-4 Mode Exit Method		15:10	110101b
0-4-4 Mode Entry Method:	6Ah	19:16	1100b
Quad Enable Requirements (QER)		22:20	101b
Hold or RESET Disable		23	0b
Reserved	6Bh	31:24	FFh
Volatile or Non-Volatile Register and Write Enable (WREN) Command for Status Register 1	6Ch	6:0	1101001b
Reserved		7	1b
Soft Reset and Rescue Sequence Support	6Eh:6Dh	13:8	110000b
Exit 4-Byte Addressing		23:14	1100000000b
Enter 4-Byte Addressing	6Fh	31:24	10000000b

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6. STATUS REGISTERS

The device has 3 Status Registers: Status Register-1/ Status Register-2/ Status Register-3
Status Register Format and Bit Definitions are described in Table 6.1, Table 6.2, Table 6.3, Table 6.4.

The device blocks repeated status writes from being written to the internal register when the write data is identical.

Table 6.1 Status Register-1

	S7	S6	S5	S4	S3	S2	S1	S0
	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Default	0	0	0	0	0	0	0	0

Table 6.2 Status Register-2

	S15	S14	S13	S12	S11	S10	S9	S8
	ESUS	CMP	IRL3	IRL2	IRL1	PSUS	QE	SRP1
Default	0	0	0	0	0	0	0	0

Table 6.3 Status Register-3

	S23	S22	S21	S20	S19	S18	S17	S16
	HOLD/RST	ODS1	ODS0	Reserve	PE_ERR	PROT_ERR	DC1	DC0
Default	0	1	0	0	0	0	0	0

Table 6.4 Status Register Bit Definition

Bit	Name	Definition	Read-/Write	Type
S0	WIP	Write In Progress Bit: "0" indicates the device is ready(default) "1" indicates a write cycle is in progress and the device is busy	R	Volatile
S1	WEL	Write Enable Latch: "0" indicates the device is not write enabled (default) "1" indicates the device is write enabled	R/W[1]	Volatile
S2	BP0	Block Protection Bit: (See Table 7.2&Table 7.3 for details)	R/W	Non-Volatile and Volatile
S3	BP1			
S4	BP2			
S5	BP3			
S6	BP4			
S7	SRP0	Status Register Protect 0	R/W	Non-Volatile
S8	SRP1	Status Register Protect 1	R/W	Non-Volatile
S9	QE	Quad Enable bit: "0" indicates the Quad output function disable (default) "1" indicates the Quad output function enable	R/W	Non-Volatile and Volatile
S10	PSUS	Program suspend bit: "0" indicates program is not suspend "1" indicates program is suspend	R	Volatile
S11	IRL1	Lock the Information Register 1: "0" indicates the Information Register can be programmed "1" indicates the Information Register cannot be programmed	R/W	OTP
S12	IRL2	Lock the Information Register 2: "0" indicates the Information Register can be programmed "1" indicates the Information Register cannot be programmed	R/W	OTP
S13	IRL3	Lock the Information Register 3: "0" indicates the Information Register can be programmed "1" indicates the Information Register cannot be programmed	R/W	OTP

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S14	CMP	Complement Protect Bit	R/W	Non-Volatile
S15	ESUS	Erase suspend bit: "0" indicates Erase is not suspend "1" indicates Erase is suspend	R	Volatile
S16	DC0	Dummy Cycle Configuration Bit0	R/W	Non-Volatile
S17	DC1	Dummy Cycle Configuration Bit0	R/W	Non-Volatile
S18	PROT_ERR	"0" indicates no error "1" indicates Program or Erase to a protected sector/block	R	Volatile
S19	PE_ERR	Program Error Bit: "0" indicates no error "1" indicates an Program or Erase operation failure	R	Volatile
S20	Reserved	Reserved	R	Reserved
S21	ODS0	Output Driver Strength: Output Drive Strength can be selected according to Table 6.6	R/W	Non-Volatile
S22	ODS1			
S23	HOLD#/ RESET#	HOLD#/RESET# pin selection Bit: "0" indicates the HOLD# pin is selected (default) "1" indicates the RESET# pin is selected	R/W	Non-Volatile

Note1: WEL bit can be written by WREN and WRDI commands, but cannot by WRSR command.

The BP0, BP1, BP2, BP3, BP4, SRP0, SRP1 are non-volatile and volatile memory cells that can be written by a Write Status Register (WRSR) command. The default value of the BP0, BP1, BP2, BP3, BP4 bits were set to "0" at factory. Only volatile Status Register is readable with Read Status Register Operation (RDSR, 05h)

The function of Status Register bits are described as follows:

WIP bit: Write In Progress (WIP) is read-only, and can be used to detect the progress or completion of a Program, Erase, or Write/Set Non-Volatile/OTP Register operation. WIP is set to "1" (busy state) when the device is executing the operation. During this time the device will ignore further commands except for Read Status Register and Software/Hardware Reset commands. In addition to the commands, an Erase/Program Suspend command also can be executed during a Program or an Erase operation. When an operation has completed, WIP is cleared to "0" (ready state) whether the operation is successful or not and the device is ready for further commands.

WEL bit: Write Enable Latch (WEL) bit indicates the status of the internal write enable latch. When WEL bit is "0", the internal write enable latch is disabled and the Write operations described in Table 6.5 are inhibited. When WEL bit is "1", the Write operations are allowed. WEL bit is set by a Write Enable (WREN, 06h) command. Most of Write Non-Volatile/Volatile Register, Program and Erase command must be preceded by a WREN command.

But Write Volatile Status Register does not require to set WEL bit to "1" by WREN (06h) command. Instead it requires a Volatile Status Register Write Enable (50h) command prior to Write Status Register (01h) command. Volatile Status Register Write Enable (50h) command does not set the Write Enable Latch (WEL) bit to "1".

WEL bit can be reset by a Write Disable (WRDI) command. It will automatically reset after the completion of any Write Non-Volatile Register, Program and Erase operation.

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Table 6.5 Commands requiring WREN command ahead

Commands must be preceded by the WREN command		
Name	**Hex Code**	**Operation**
PP	02h	Serial Input Page Program
PPQ	32h	Quad Input Page Program
SER	20h	Sector Erase 4KB
BER32 (32KB)	52h	Block Erase 32KB
BER64 (64KB)	D8h	Block Erase 64KB
CER	C7h/60h	Chip Erase
WRSR(1)	01h/31h/11h	Write Non-Volatile Status Register-1/2/3
IRER	44h	Erase Information Registers
IRP	42h	Program Information Registers

Notes:
1. **Volatile Status Register Write Enable (50h) command is required for Write Volatile Status Register operation with WRSR(01) command.**
2. **C0h command for SRPV operation does not require WREN command ahead.**

BP4, BP3, BP2, BP1, BP0 bits

The Block Protection (BP4, BP3, BP2, BP1 and BP0) bits are used to define the portion of the memory area to be protected. Refer to Table 7.2&Table 7.3 for the Block Write Protection (BP) bit settings. When a defined combination of BP4, BP3, BP2, BP1 and BP0 bits are set, the corresponding memory area is protected. Any program or erase operation to that area will be inhibited.

Note: A Chip Erase (CER) command will be ignored unless all the Block Protection Bits are "0"s.

SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRPx bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

QE bit

The Quad Enable (QE) is a non-volatile bit in the Status Register that allows quad operation. When the QE bit is set to "0", the pin WP# and HOLD#/RESET# are enabled. When the QE bit is set to "1", the IO2 and IO3 pins are enabled.

WARNING: The QE bit must be set to 0 if WP# or HOLD#/RESET# pin is tied directly to the power supply.

PSUS bit

The Program Suspend Status bit indicates when a Program operation has been suspended. The PSUS changes to "1" after a suspend command is issued during the program operation. Once the suspended Program resumes, the PSUS bit is reset to "0".

ESUS bit

The Erase Suspend Status bit indicates when an Erase operation has been suspended. The ESUS bit is "1" after a suspend command is issued during an Erase operation. Once the suspended Erase resumes, the ESUS bit is reset to "0".

IR Lock bit [1:3]

The default is "0" so that the Information Register can be programmed. If the bit set to "1", the Information Register can't be programmed. Once it sets to "1", it cannot be changed back to "0" since IR Lock bits are OTP.

CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (bit14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status Registers Memory Protection table for details. The default setting is CMP=0.

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DC0/DC1 bitS

DC0/DC1 bits are Non-Volatile registers which can be used to configure Dummy Cycle for EBh and EDh. Configurable Dummy Cycle can reduce read command overhead or support higher read speed for above two commands.

DC[1:0]	EBh		EDh	
	Dummy cycles	Maximum Read Freq.	Dummy cycles	Maximum Read Freq.
00	6	120 MHz	10	80 MHz
01	4	80 MHz	8	80 MHz
10	8	133 MHz	4	40 MHz
11	10	133MHz	6	60MHz

PROT_ERR bit

The Protection Error bit indicates whether an Erase or Program operation has attempted to modify a protected array sector or block. When the bit is set to “1”, it indicates that there was an error or errors in previous Erase or Program operations. PROT_E bit is cleared by POR(Power On Reset) or HW/SW reset

PE_ERR bit

The Program and Erase Error bit indicates whether a Program or Erase operation has succeeded or failed. When the bit is set to “1” it indicates that there was an error or errors in previous Program or Erase operation.

Output Drive Strength (ODS1, ODS0)

The ODS1 and ODS0 bits are used to configure the output driver strength for the Read operations

Table 6.6 Output Drive Strength Configuration

ODS1, ODS0	Drive Strength
0, 0	100%
0, 1	75%
1,0	50% (default for Package part)
1,1	25%

HOLD#／ RESET# bit

HOLD#/RESET# pin selection (23) bit in the Status Register-3 is used to determine whether HOLD# or RESET# function should be implemented on the hardware pin for 8-pin packages. When HOLD#/RESET#=0, the pin acts as #HOLD; when HOLD#/RESET#=1, the pin acts as RESET#. However, HOLD# or RESET# functions are only available when QE=0. If QE is set to 1, the HOLD# and RESET# functions are disabled, the pin acts as a dedicated data I/O pin.

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7. PROTECTION MODE

The device supports hardware and software write-protection mechanisms.

7.1 STATUS REGISTER PROTECTION (SRP0, SRP1)

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRPx bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 7.1 Status Register Protection

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. (1) (2)
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Note:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact ISSI for details.

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7.2 DATA PROTECTION

Table 7.2 Status Register Memory Protection (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	None	None	None	None
0	0	0	0	1	252 to 255	FC0000H-FFFFFFH	256KB	Upper 1/64
0	0	0	1	0	248 to 255	F80000H-FFFFFFH	512KB	Upper 1/32
0	0	0	1	1	240 to 255	F00000H-FFFFFFH	1MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000H-FFFFFFH	2MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000H-FFFFFFH	4MB	Upper 1/4
0	0	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
0	1	0	0	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/64
0	1	0	1	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/32
0	1	0	1	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/16
0	1	1	0	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/8
0	1	1	0	1	0 to 63	000000H-3FFFFFH	4MB	Lower 1/4
0	1	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
X	X	1	1	1	0 to 255	000000H-FFFFFFH	16MB	All
1	0	0	0	1	255	FFF000H-FFFFFFH	4KB	Top Block
1	0	0	1	0	255	FFE000H-FFFFFFH	8KB	Top Block
1	0	0	1	1	255	FFC000H-FFFFFFH	16KB	Top Block
1	0	1	0	X	255	FF8000H-FFFFFFH	32KB	Top Block
1	0	1	1	0	255	FF8000H-FFFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

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Table 7.3 Status Register Memory Protection (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H-FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 251	000000H-FBFFFFH	16128KB	Lower 63/64
0	0	0	1	0	0 to 247	000000H-F7FFFFH	15872KB	Lower 31/32
0	0	0	1	1	0 to 239	000000H-EFFFFFH	15MB	Lower 15/16
0	0	1	0	0	0 to 223	000000H-DFFFFFH	14MB	Lower 7/8
0	0	1	0	1	0 to 191	000000H-BFFFFFH	12MB	Lower 3/4
0	0	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
0	1	0	0	1	4 to 255	040000H-FFFFFFH	16128KB	Upper 63/64
0	1	0	1	0	8 to 255	080000H-FFFFFFH	15872KB	Upper 31/32
0	1	0	1	1	16 to 255	100000H-FFFFFFH	15MB	Upper15/16
0	1	1	0	0	32to 255	200000H-FFFFFFH	14MB	Upper7/8
0	1	1	0	1	64 to 255	400000H-FFFFFFH	12MB	Upper3/4
0	1	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper1/2
X	X	1	1	1	None	None	None	None
1	0	0	0	1	0 to 255	000000H-FFEFFFH	16380KB	Lower-4095/4096
1	0	0	1	0	0 to 255	000000H-FFDFFFH	16376KB	Lower-2047/2048
1	0	0	1	1	0 to 255	000000H-FFBFFFH	16368KB	Lower-1023/1024
1	0	1	0	X	0 to 255	000000H-FF7FFFH	16352KB	Lower-511/512
1	0	1	1	0	0 to 255	000000H-FF7FFFH	16352KB	Lower -511/512
1	1	0	0	1	0 to 255	001000H-FFFFFFH	16380KB	Upper-4095/4096
1	1	0	1	0	0 to 255	002000H-FFFFFFH	16376KB	Upper-2047/2048
1	1	0	1	1	0 to 255	004000H-FFFFFFH	16368KB	Upper -1023/1024
1	1	1	0	X	0 to 255	008000H-FFFFFFH	16352KB	Upper -511/512
1	1	1	1	0	0 to 255	008000H-FFFFFFH	16352KB	Upper -511/512

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8. DEVICE OPERATION

The device utilizes an 8-bit command register. Refer to Table 8.1. Command Set for details on commands and command codes. All commands, addresses, and data are shifted in with the most significant bit (MSB) first_on Serial Data Input (SI) or Serial Data IOs (IO0, IO1, IO2, IO3). The input data on SI or IOs is latched on the rising edge of Serial Clock (SCK) for normal mode and both of rising and falling edges for DTR mode after Chip Enable (CE#) is driven low (V_{IL}). Every command sequence starts with a one-byte command code and is followed by address bytes, data bytes, or both address bytes and data bytes, depending on the type of command. CE# must be driven high (V_{IH}) after the last bit of the command sequence has been shifted in to end the operation.

Table 8.1 Command Set

Command Name	Operation	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
NORD	Normal Read Mode	SPI	03h	A <23:16>	A <15:8>	A <7:0>	Data out		
FRD	Fast Read Mode	SPI QPI	0Bh	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Byte	Data out	
FRDIO	Fast Read Dual I/O	SPI	BBh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	M7-M0 (2)	Dual Data out	
FRDO	Fast Read Dual Output	SPI	3Bh	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Dual Data out	
FRQIO	Fast Read Quad I/O	SPI QPI	EBh	A <23:16> Quad	A <15:8> Quad	A <7:0> Quad	M7-M0 (1,2)	Quad Data out	
FRQO	Fast Read Quad Output	SPI	6Bh	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Quad Data out	
FRDTR	Fast Read DTR Mode	SPI QPI	0Dh	A <23:16>	A <15:8>	A <7:0>	Dummy Byte	Dual Data out	
FRDDTR	Fast Read Dual I/O DTR	SPI	BDh	A <23:16> Dual	A <15:8> Dual	A <7:0> Dual	M7-M0 (2)	Dual Data out	
FRQDTR	Fast Read Quad I/O DTR	SPI QPI	EDh	A <23:16>	A <15:8>	A <7:0>	M7-M0 (2)	Quad Data out	
PP	Input Page Program	SPI QPI	02h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
PPQ	Quad Input Page Program	SPI	32h	A <23:16>	A <15:8>	A <7:0>	Quad PD (256byte)		
SER	Sector Erase	SPI QPI	20h	A <23:16>	A <15:8>	A <7:0>			
BER32 (32KB)	Block Erase 32Kbyte	SPI QPI	52h	A <23:16>	A <15:8>	A <7:0>			
BER64 (64KB)	Block Erase 64Kbyte	SPI QPI	D8h	A <23:16>	A <15:8>	A <7:0>			
CER	Chip Erase	SPI QPI	C7h 60h						
WREN	Write Enable	SPI QPI	06h						
VSRWREN	Volatile Status Register Write Enable	SPI QPI	50h						
WRDI	Write Disable	SPI QPI	04h						
RDSR1	Read Status Register-1	SPI QPI	05h	SR1					
RDSR2	Read Status Register-2	SPI QPI	35h	SR2					
RDSR3	Read Status Register-3	SPI QPI	15h	SR3					
WRSR1	Write Status Register	SPI QPI	01h	SR1	SR2				

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WRSR2	Write Status Register	SPI QPI	31h	SR2					
WRSR3	Write Status Register	SPI QPI	11h	SR3					
SRDP	Set Read Parameters	QPI	C0h	P7-P0					
BRWW	Burst Read with Wrap	QPI	0Ch	A <23:16>	A <15:8>	A <7:0>	Dummy(1) Clock	Data out	
SBWW	Set Burst with Wrap	SPI	77h	dummy	dummy	dummy	Wrap bit		

Command Name	Operation	Mode	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
QPIEN	Enter QPI mode	SPI	38h						
QPIDI	Exit QPI mode	QPI	FFh						
PERSUS	Suspend during program/erase	SPI QPI	75h						
PERRSM	Resume program/erase	SPI QPI	7Ah						
DP	Deep Power Down	SPI QPI	B9h						
RDID, RDPD	Read ID / Release Power Down	SPI QPI	ABh	XXh(3)	XXh(3)	XXh(3)	ID7-ID0		
RDJDID	Read JEDEC ID Command	SPI QPI	9Fh	MF7-MF0	ID15-ID8	ID7-ID0			
RDMDID	Read Manufacturer & Device ID	SPI QPI	90h	XXh(3)	XXh(3)	00h	MF7-MF0	ID7-ID0	
RDUID	Read Unique ID	SPI QPI	4Bh	A(4) <23:16>	A(4) <15:8>	A(4) <7:0>	Dummy Byte(5)	Data out	
RDSFDP	SFDP Read	SPI QPI	5Ah	A <23:16>	A <15:8>	A <7:0>	Dummy Byte(5)	Data out	
RSTEN	Software Reset Enable	SPI QPI	66h						
RST	Software Reset	SPI QPI	99h						
ERSRR	Erase Information Registers	SPI QPI	44h	A <23:16>	A <15:8>	A <7:0>			
PGSRR	Program Information Registers	SPI QPI	42h	A <23:16>	A <15:8>	A <7:0>	PD (256byte)		
RDSRR	Read Information Registers	SPI QPI	48h	A <23:16>	A <15:8>	A <7:0>	Dummy Byte(5)	Data out	

Notes:
1. **The number of dummy cycles depends on C0h**
2. **Mode bits (M7-M0) are considered as a part of dummy cycles.**
3. **XX means "don't care".**
4. **A<23:9> are "don't care" and A<8:4> are always "0".**
5. **8 dummy clocks in QPI mode.**

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8.1 HOLD OPERATION

HOLD# is used in conjunction with CE# to select the device. When the device is selected and a serial sequence is underway, HOLD# can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, HOLD# is brought low while the SCK signal is low. To resume serial communication, HOLD# is brought high while the SCK signal is low (SCK may still toggle during HOLD). Inputs to SI will be ignored while SO is in the high impedance state, during HOLD.

Note: HOLD# is not supported in DTR mode or with QE=1 or when RESET# is selected for the HOLD# or RESET# pin.

Timing graph can be referenced in AC Parameters Figure 9.4.

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8.2 NORMAL READ OPERATION (NORD, 03h)

The NORMAL READ (NORD) command is used to read memory contents at a maximum frequency of 80MHz.

The NORD command code is transmitted via the SI line, followed by three address bytes (A23 - A0) of the first memory location to be read. A total of 24 address bits are shifted in, but only A_{VMSB} (Valid Most Significant Bit) - A_0 are decoded. The remaining bits (A23 – A_{VMSB+1}) are ignored. The first byte addressed can be at any memory location. Upon completion, any data on the SI will be ignored. Refer to Table 8.2 for the related Address Key.

The first byte data (D7 - D0) is shifted out on the SO line, MSB first. A single byte of data, or up to the whole memory array, can be read out in one NORMAL READ command. The address is automatically incremented by one after each byte of data is shifted out. The read operation can be terminated at any time by driving CE# high (VIH) after the data comes out. When the highest address of the device is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read in one continuous READ command.

If the NORMAL READ command is issued while an Erase, Program or Write operation is in process (WIP=1) the command is ignored and will not have any effects on the current operation.

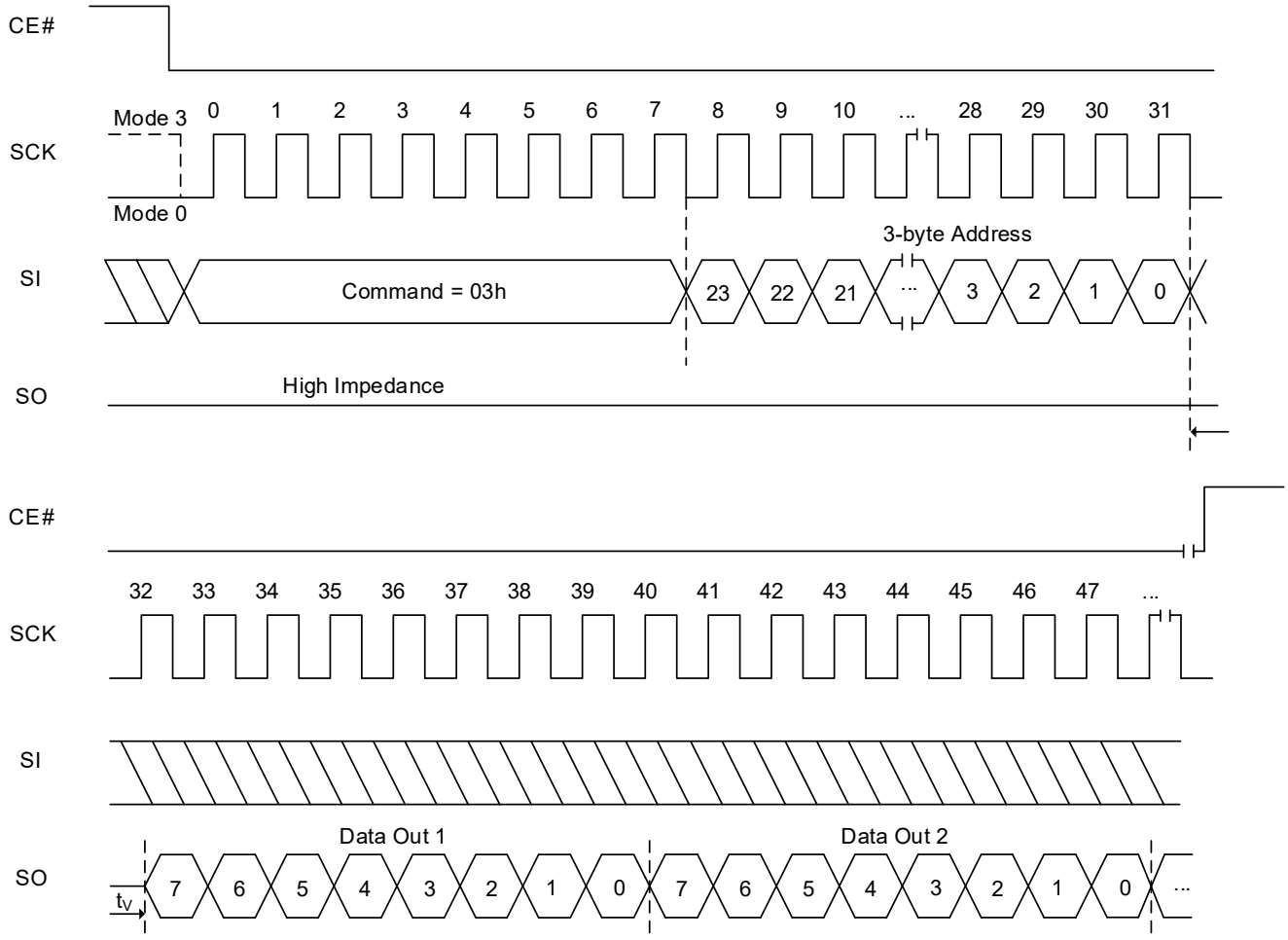
Table 8.2 Address Key

Valid Address	128Mb
A_{VMSB}–A_0	A22-A0 (A23 =X)

Note: X=Don't Care

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Figure 8.1 **Normal Read Sequence**



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8.3 FAST READ OPERATION (FRD, 0Bh)

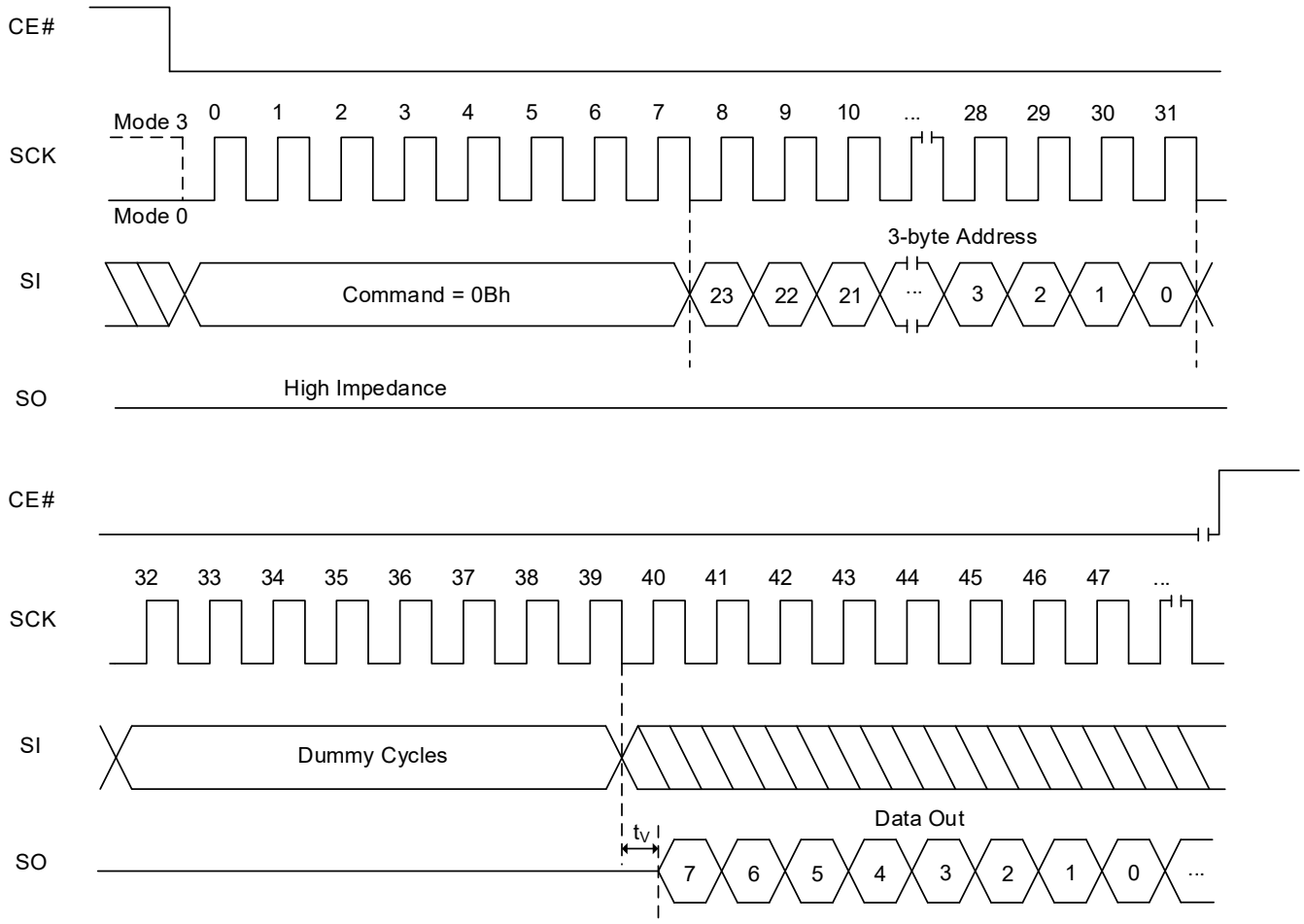
The FAST READ (FRD) command is used to read memory data.

The FAST READ command code is followed by three address bytes (A23 - A0) and a dummy byte , transmitted via the SI line, with each bit latched-in during the rising edge of SCK. Then the first data byte from the address is shifted out on the SO line, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ command. The FAST READ command is terminated by driving CE# high (VIH).

If the FAST READ command is issued while an Erase, Program or Write cycle is in process (WIP=1) the command is ignored without affecting the current cycle.

Figure 8.2 **Fast Read Sequence**



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FAST READ OPERATION IN QPI MODE (FRD, 0Bh)

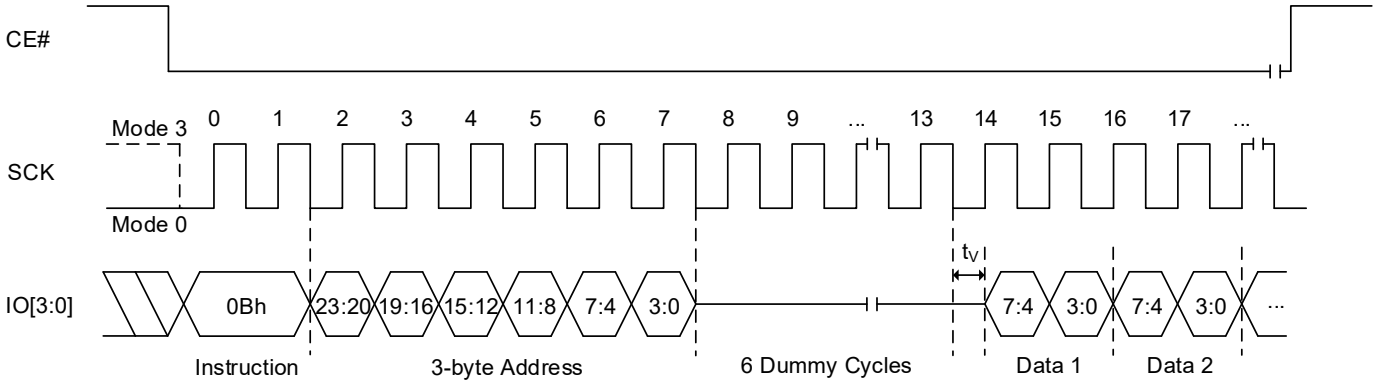
The FAST READ (FRD) command is used also in QPI mode to read memory data.

The FAST READ command code (2 clocks) is followed by three address bytes (A23-A0 — 6 clocks) and dummy cycles (configurable by C0h, default is 6 cycles), transmitted via the IO3, IO2, IO1 and IO0 lines, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each bit shifted out at a maximum frequency f_{CT}, during the falling edge of SCK.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FAST READ command. The FAST READ command in QPI mode is terminated by driving CE# high (VIH).

If the FAST READ command is issued while an Erase, Program or Write cycle is in process (WIP=1) the command is ignored without affecting the current cycle.

Figure 8.3 **Fast Read Sequence In QPI Mode**



Note: Number of dummy cycles can be configured by C0h command

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8.4 FAST READ DUAL I/O OPERATION (FRDIO, BBh)

The FRDIO allows the address bits to be input two bits at a time. This may allow for code to be executed directly from the SPI in some applications.

The FRDIO command code is followed by three address bytes (A23 – A0) and fixed 4 dummy cycles transmitted via the IO1 and IO0 lines, with each pair of bits latched-in during the rising edge of SCK. The address MSB is input on IO1, the next bit on IO0, and this shift pattern continues to alternate between the two lines. Depending on the usage of continuous read mode, a mode byte may be located after address input.

The first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency f_{CT}, during the falling edge of SCK. The MSB is output on IO1, while simultaneously the second bit is output on IO0. Figure 8.4 illustrates the timing sequence.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDIO command. FRDIO command is terminated by driving CE# high (V_{IH}).

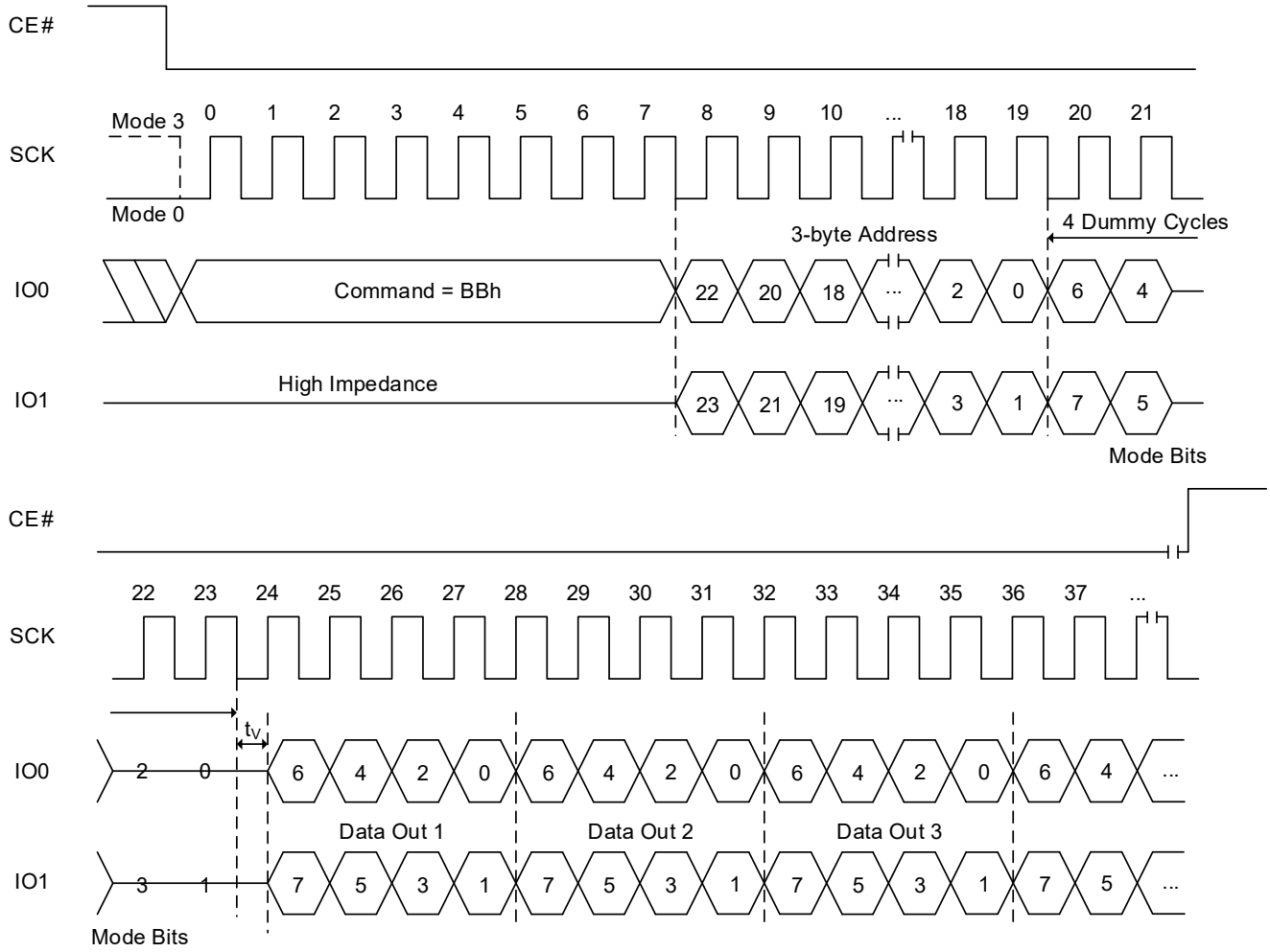
The device supports “continuous read mode”, which can reduce instruction overhead in the following read operation, by applying mode bits during dummy period. mode bits consist of 8 bits such as M7 to M0. Four cycles after address input are reserved for mode bits in FRDIO execution. M5 bit and M4 bit value determines continuous read mode. The rest of 6 bits become don’t care for future use.
When mode bits are XX10XXXXb (where X is don’t care), it enables the “continuous read mode” and subsequent FRDIO execution skips command code. It saves cycles as described in Figure 8.5.

When the mode bits are different from XX10XXXXb (where X is don’t care), the device exits the “continuous read mode”. After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting. mode bit must be applied during dummy cycles. Number of dummy cycles includes same number of mode bits, data output will start right after mode bit is applied.

If the FRDIO command is issued while an Erase, Program or Write cycle is in process (WIP=1) the command is ignored and will not affect the current cycle.

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Figure 8.4 **Fast Read Dual I/O Sequence (with command decode cycles)**

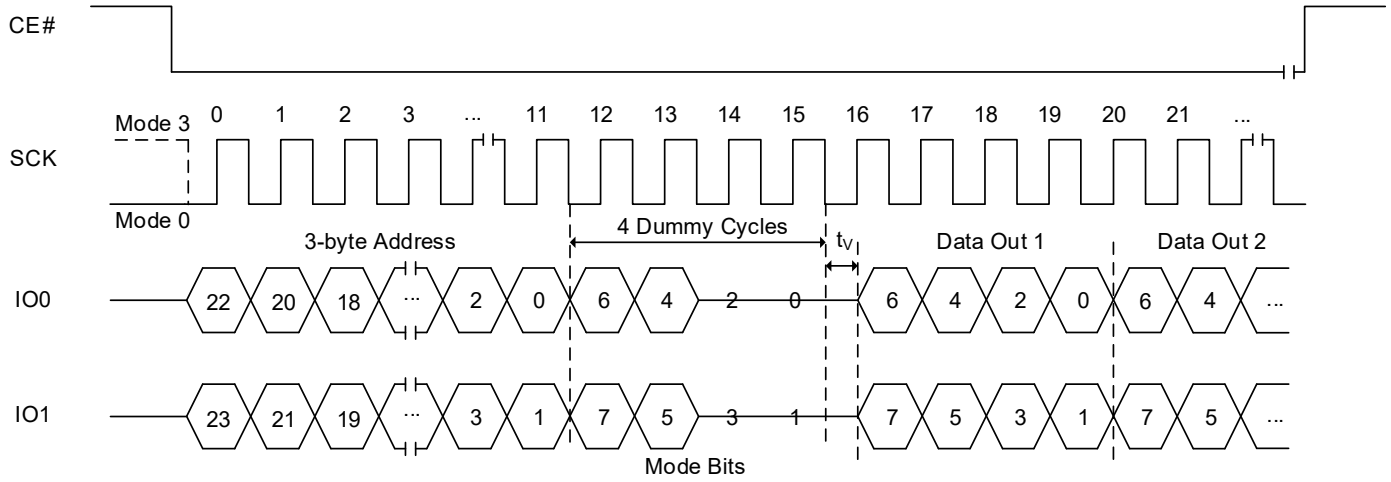


Notes:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without instruction). When mode bits are different from XX10XXb, the device exits the continuous read mode operation.**
2. **Sufficient dummy cycles are required to avoid I/O contention. If the number of dummy cycles and mode bit cycles are same, then X should be Hi-Z.**

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Figure 8.5 **Fast Read Dual I/O 2X read Sequence (without command decode cycles)**



Notes:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without instruction). When mode bits are different from XX10XXb, the device exits the continuous read mode operation.**
2. **Sufficient dummy cycles are required to avoid I/O contention. I/O pins should be Hi-Z prior to the falling edge of the first data out clock.**

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8.5 FAST READ DUAL OUTPUT OPERATION (FRDO, 3Bh)

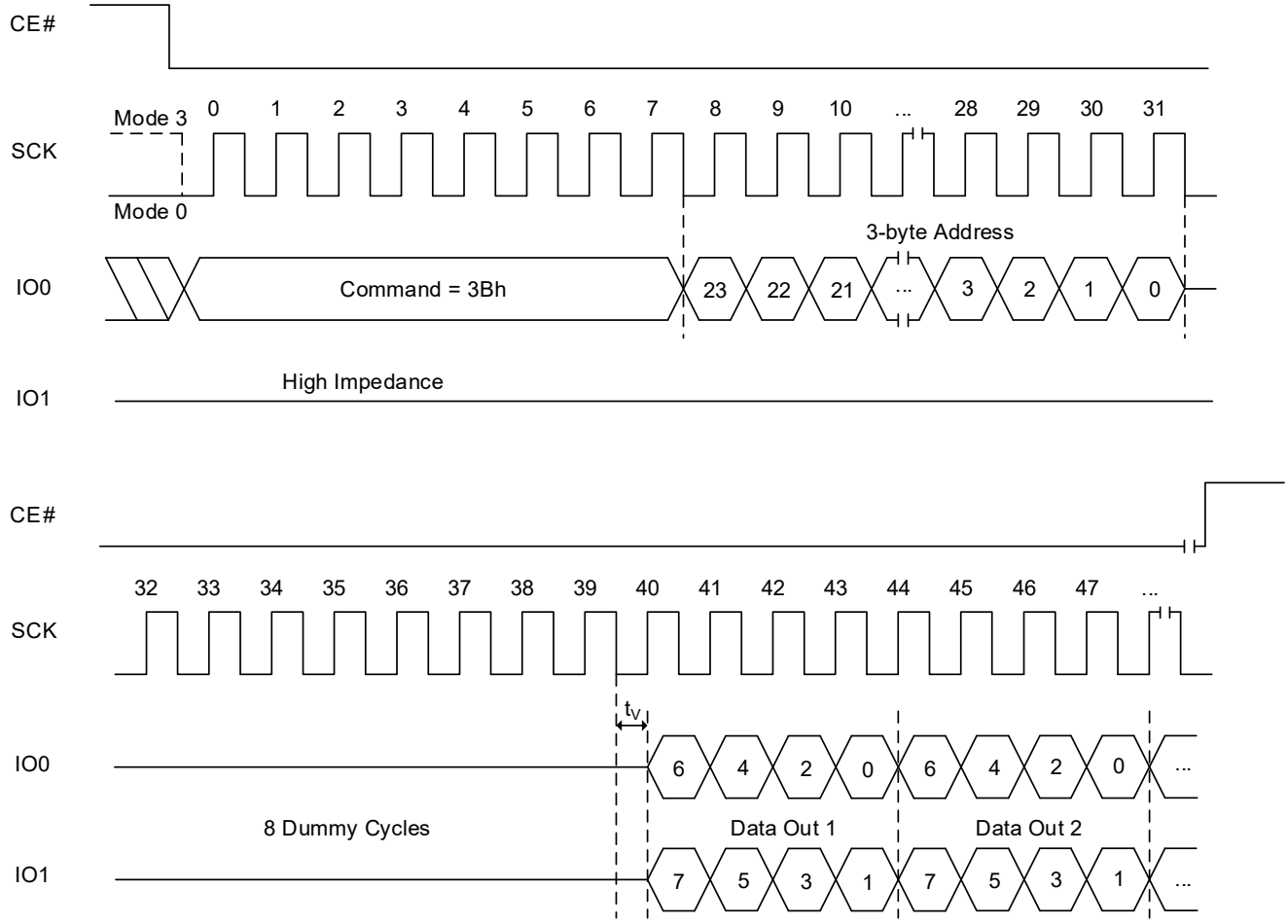
The FRDO command is used to read memory data on two output pins.

The FRDO command code is followed by three address bytes (A23 – A0) and 8 dummy cycles transmitted via the IO0 line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO1 and IO0 lines, with each pair of bits shifted out at a maximum frequency fCT, during the falling edge of SCK. The first bit (MSB) is output on IO1. Simultaneously, the second bit is output on IO0.

The first byte addressed can be at any memory location. The address is automatically incremented by one after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRDO command. The FRDO command is terminated by driving CE# high (VIH).

If the FRDO command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle.

Figure 8.6 **Fast Read Dual Output Sequence**



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8.6 FAST READ QUAD OUTPUT OPERATION (FRQO, 6Bh)

The FRQO command is used to read memory data on four output pins.
A Quad Enable (QE) bit of Status Register must be set to "1" before sending the Fast Read Quad Output command.

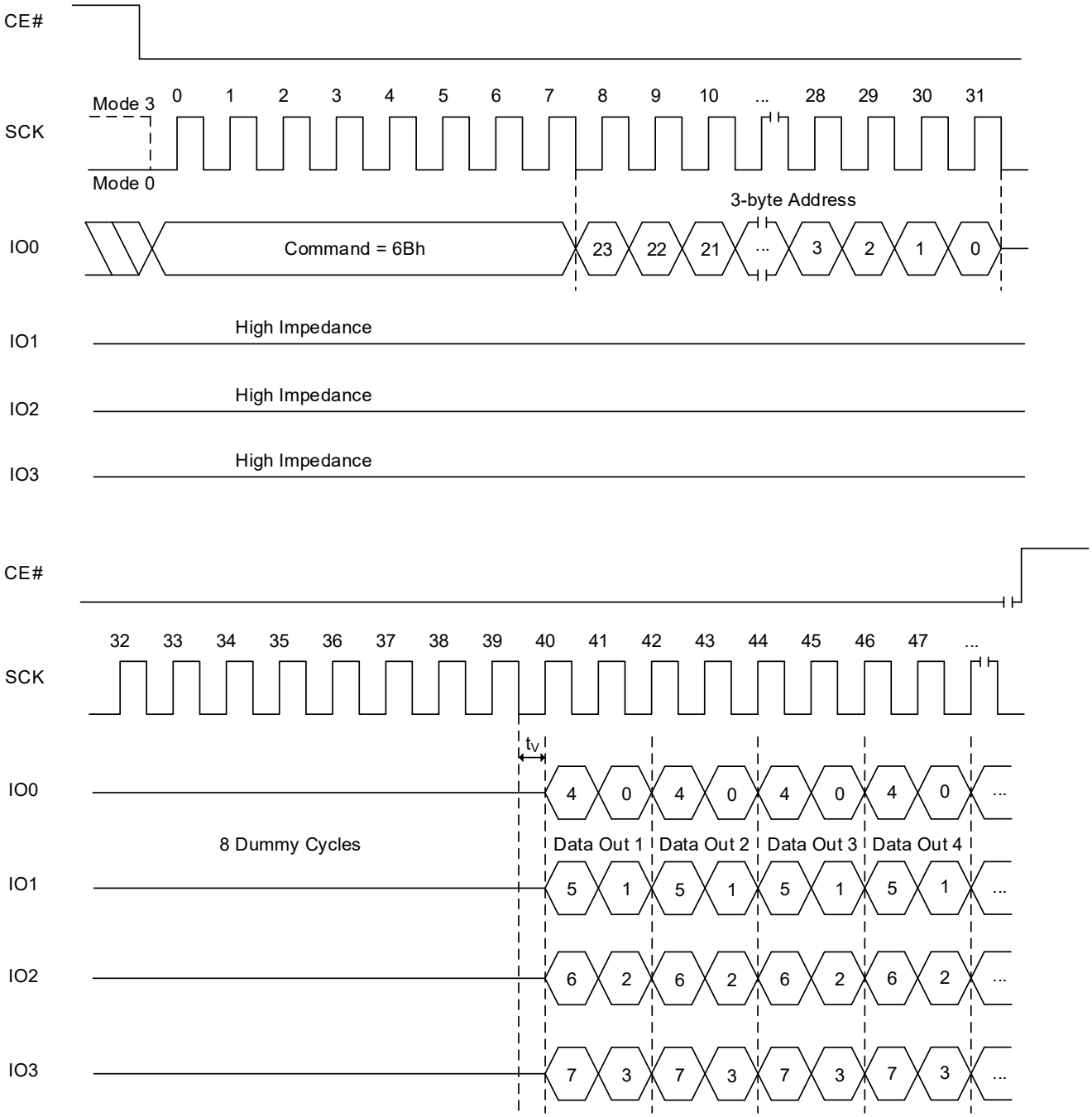
The FRQO command code is followed by three address bytes (A23 – A0) and 8 dummy cycles, transmitted via the IO0 line, with each bit latched-in during the rising edge of SCK. Then the first data byte addressed is shifted out on the IO3, IO2, IO1 and IO0 lines, with each group of four bits shifted out at a maximum frequency fCT, during the falling edge of SCK. The first bit (MSB) is output on IO3, while simultaneously the second bit is output on IO2, the third bit is output on IO1, etc.

The first byte addressed can be at any memory location. The address is automatically incremented after each byte of data is shifted out. When the highest address is reached, the address counter will roll over to the 000000h address, allowing the entire memory to be read with a single FRQO command. FRQO command is terminated by driving CE# high (VIH).

If a FRQO command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle.

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Figure 8.7 **Fast Read Quad Output Sequence**



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8.7 FAST READ QUAD I/O OPERATION (FRQIO, EBh)

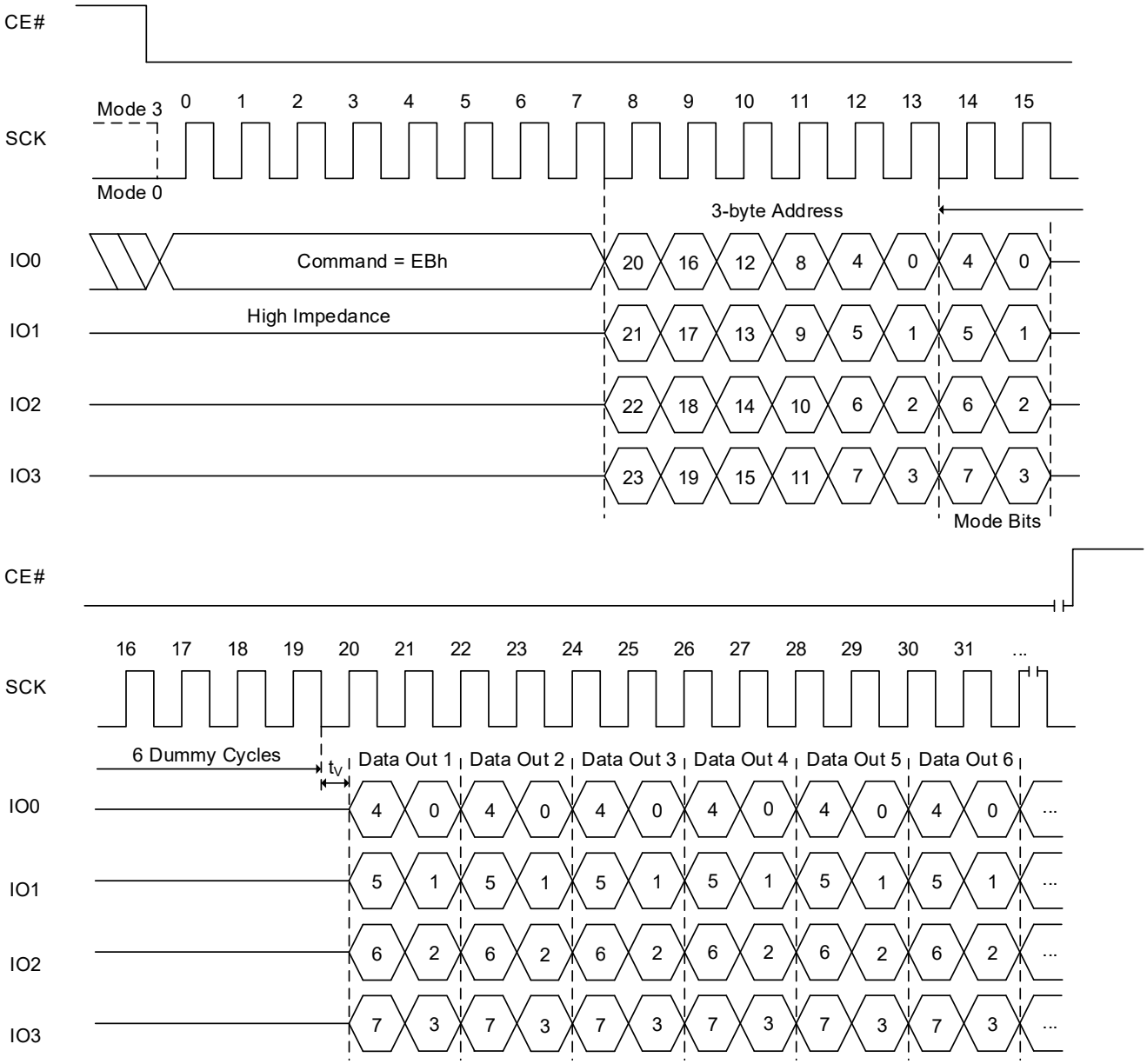
The Fast Read Quad I/O command is similar to the Dual I/O Fast Read command except address and data are transferred on 4-bit mode. 3-byte address (A23-0) is followed by a “continuous read mode” byte and 4-dummy cycle, it equals 6 dummy clock. 4-bit addresses are transferred per clock by IO0, IO1, IO3, IO4, and each bit is latched in on the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte address can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The device supports “continuous read mode”, which can reduce instruction overhead in the following read operation, by applying mode bits during dummy period. Mode bits consist of 8 bits such as M7 to M0. Four cycles after address input are reserved for mode bits in FRDIO execution. M5 bit and M4 bit value determines continuous read mode. The rest of 6 bits become don’t care for future use.
When mode bits are XX10XXXXb (where X is don’t care), it enables the “continuous read mode” and subsequent FRDIO execution skips command code. It saves cycles as described in Figure 8.9.

When the mode bits are different from XX10XXXXb (where X is don’t care), the device exits the “continuous read mode”. After finishing the read operation, device becomes ready to receive a new command. SPI or QPI mode configuration retains the prior setting. Mode bit must be applied during dummy cycles. Number of dummy cycles includes same number of mode bit cycles, data output will start right after mode bit is applied

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Figure 8.8 **Fast Read Quad I/O "continuous read mode" Sequence (with command decode cycles)**

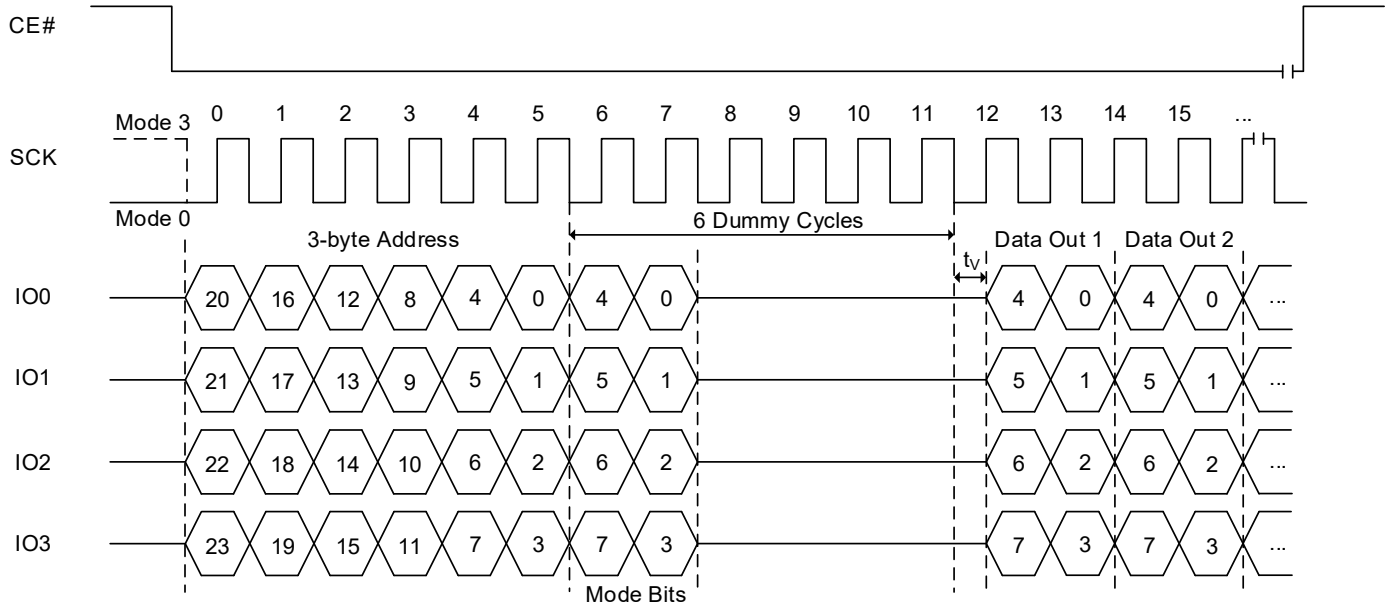


Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

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Figure 8.9 **Fast Read Quad I/O "continuous read mode" Sequence (without command decode cycles)**



Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

FAST READ QUAD I/O WITH "8/16/32/64-BYTE WRAP AROUND" IN STANDARD SPI MODE

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CE# be driven high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

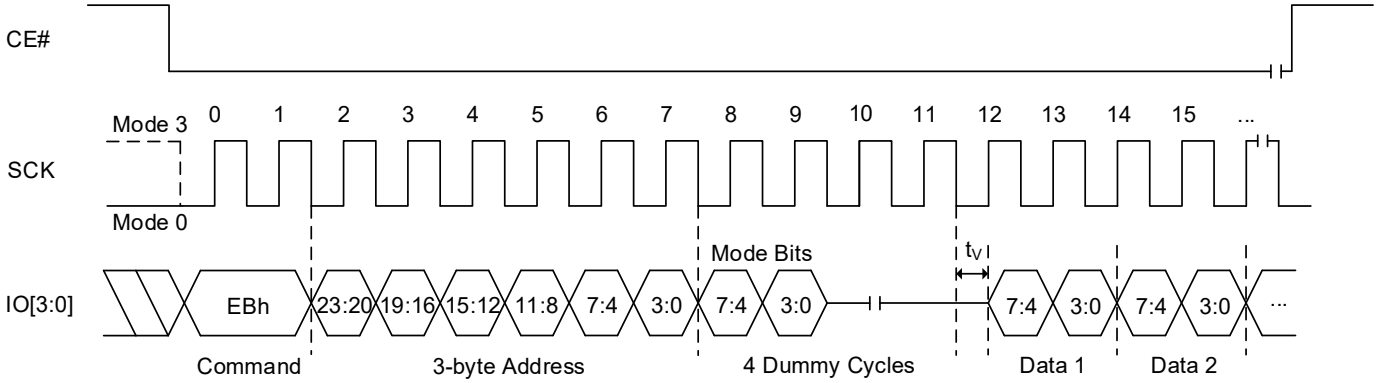
FAST READ QUAD I/O OPERATION (FRQIO, EBH) IN QPI MODE

The Fast Read Quad I/O command is also supported in QPI mode. When QPI mode is enabled, the number of dummy cycles is configured by the "Set Read Parameters (C0h)" command to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy cycles can be configured as either 2, 4, 6 or 8. The default number of dummy cycles upon power up or after a Reset command is 4. In QPI mode, the "Continuous read mode" bits M7-0 are also considered as dummy cycles.

"Continuous read mode" feature is also available in QPI mode for Fast Read Quad I/O command.
Please refer to the description on previous pages.

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Figure 8.10 **Fast Read Quad I/O Sequence (QPI Mode)**



"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) command must be used.

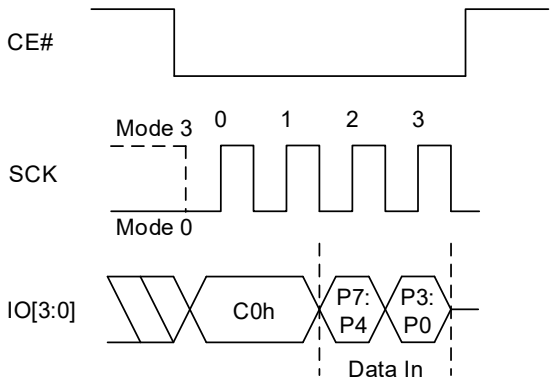
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8.8 SET READ PARAMETERS (C0H)

In QPI mode the “Set Read Parameters (C0h)” command can be used to configure the number of dummy cycles for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)”, “Fast Read DTR Mode(0Dh)” , “Fast Read Quad I/O DTR (EDh)” and “Burst Read with Wrap (0Ch)” command, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” command. C0h is not accepted in standard SPI mode.
In standard SPI mode, the “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77h)” command. This wrap setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.
The default “Wrap Length” after a power up or a Reset command is 8 bytes, the default number of dummy cycles are 6. Whenever the device is switched from SPI mode to QPI mode, the number of dummy cycles should be set again, prior to any 0Bh, EBh or 0Ch commands.

	0Bh/0Ch/EBh		0Dh/EDh			
P5-P4	Dummy cycles	Maximum Read Freq.	Dummy cycles	Maximum Read Freq.	P1-P0	Wrap Length
00	6	120 MHz	10	80MHz	00	8-Byte
01	4	80 MHz	8	80 MHz	01	16-Byte
10	8	133 MHz	4	40 MHz	10	32-Byte
11	10	133MHz	6	60MHz	11	64-Byte

Figure 8.11 **Set Read Parameters command**

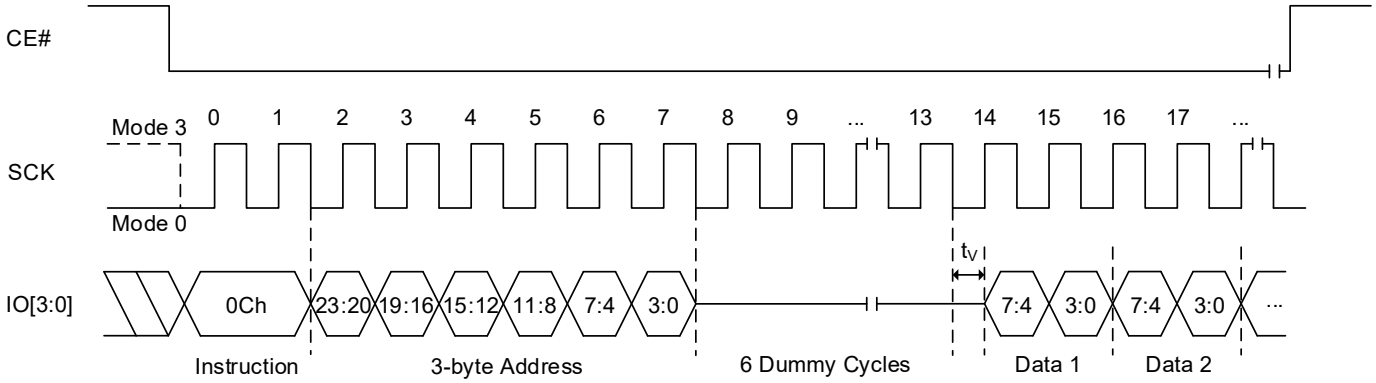


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8.9 BURST READ WITH WRAP (0CH)

The “Burst Read with Wrap (0Ch)” command provides a way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0Bh)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy cycles can be configured by the “Set Read Parameters (C0h)” command, the default is 6 dummy cycle with 8-Byte wrap length.

Figure 8.12 **BURST READ WITH WRAP**



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8.10 SET BURST WITH WRAP (77h)

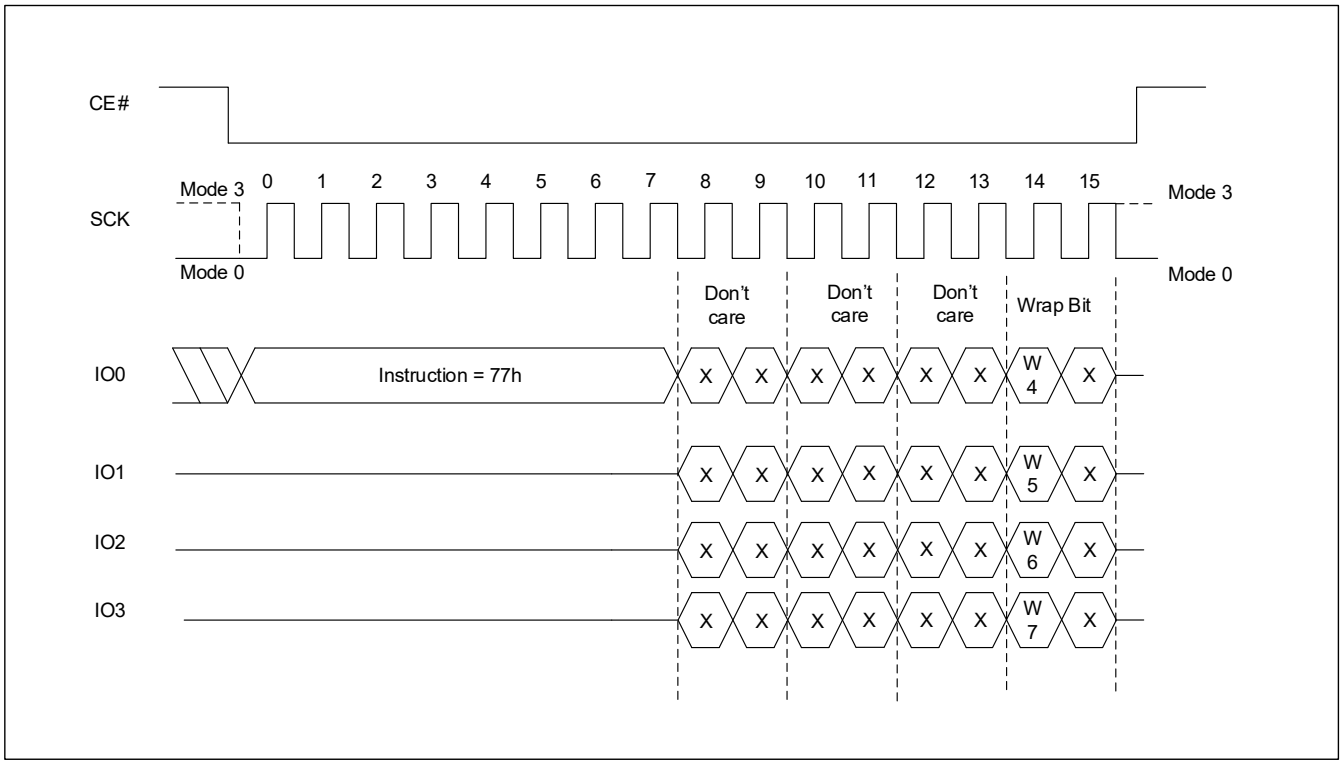
In Standard SPI mode, the Set Burst with Wrap (77h) command is used in conjunction with “Fast Read Quad I/O (EBh)” or “Fast Read Quad I/O DTR (EDh)” commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain pplications can benefit from this feature and improve the overall system code execution performance. Similar to a Quad I/O command, the Set Burst with Wrap command is initiated by driving the CE# pin low and then shifting the command code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7 -0. The command sequence is shown in
Figure 8.13. Wrap bit W7 and the lower nibble W3-0 are not used. QE bit should be set to ‘1’ before executing ‘77h’ command

W6, W5	W4 = 0		W4 = 1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap command, the following “Fast Read Quad I/O” commands will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on or after a software/hardware reset is 1.

In QPI mode, the “Burst Read with Wrap (0Ch)” command should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0h)” command.

Figure 8.13 **SET BURST WITH WRAP**



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8.11 PAGE PROGRAM OPERATION (PP, 02h)

The Page Program (PP) command allows up to 256 bytes data to be programmed into memory in a single operation. The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A PP command which attempts to program into a page that is write-protected will be ignored. Before the execution of PP command, the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) command.

The PP command code, three address bytes and program data (1 to 256 bytes) are input via the SI line. Program operation will start immediately after the CE# is brought high, otherwise the PP command will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all commands will be ignored except the RDSR command. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR command. If the WIP bit is “1”, the program operation is still in progress. If WIP bit is “0”, the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter “1”s into “0”s. The same byte location or page may be programmed more than once, to incrementally change “1”s to “0”s. An erase operation is required to change “0”s to “1”s.

Figure 8.14 **Page Program Sequence In SPI Mode**

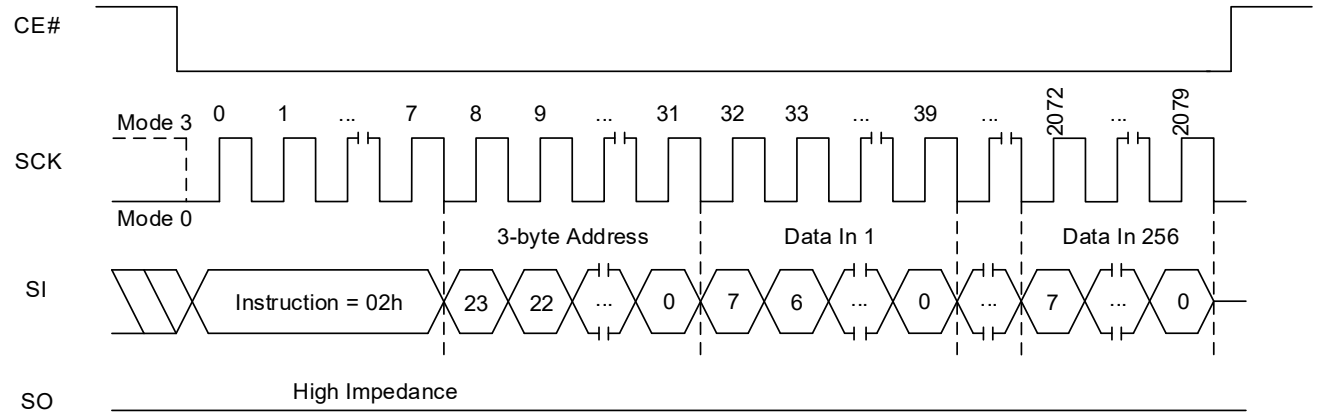
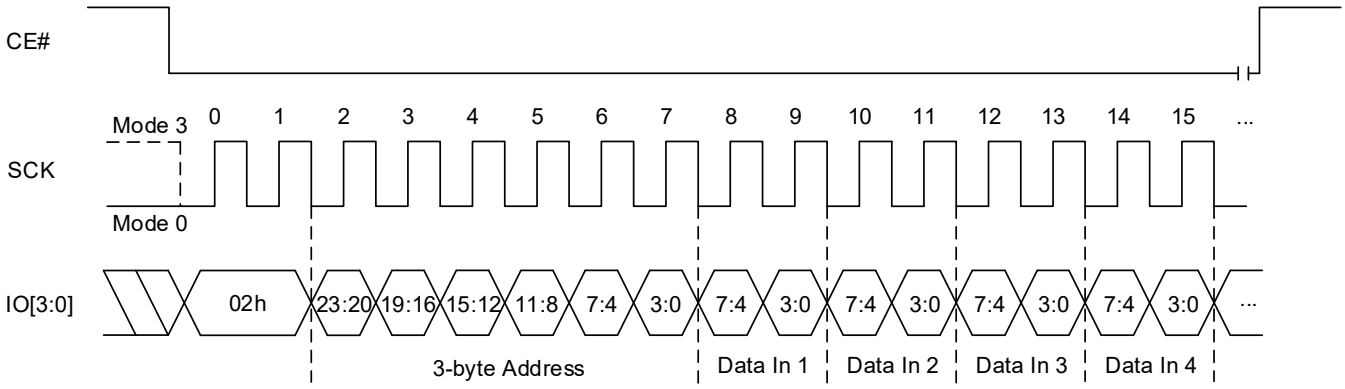


Figure 8.15 **Page Program Sequence In QPI Mode**



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8.12 QUAD INPUT PAGE PROGRAM OPERATION (PPQ, 32h)

The Quad Input Page Program command allows up to 256 bytes data to be programmed into memory in a single operation with four pins (IO0, IO1, IO2 and IO3). The destination of the memory to be programmed must be outside the protected memory area set by the Block Protection (BP3, BP2, BP1, BP0) bits. A Quad Input Page Program command which attempts to program into a page that is write-protected will be ignored.

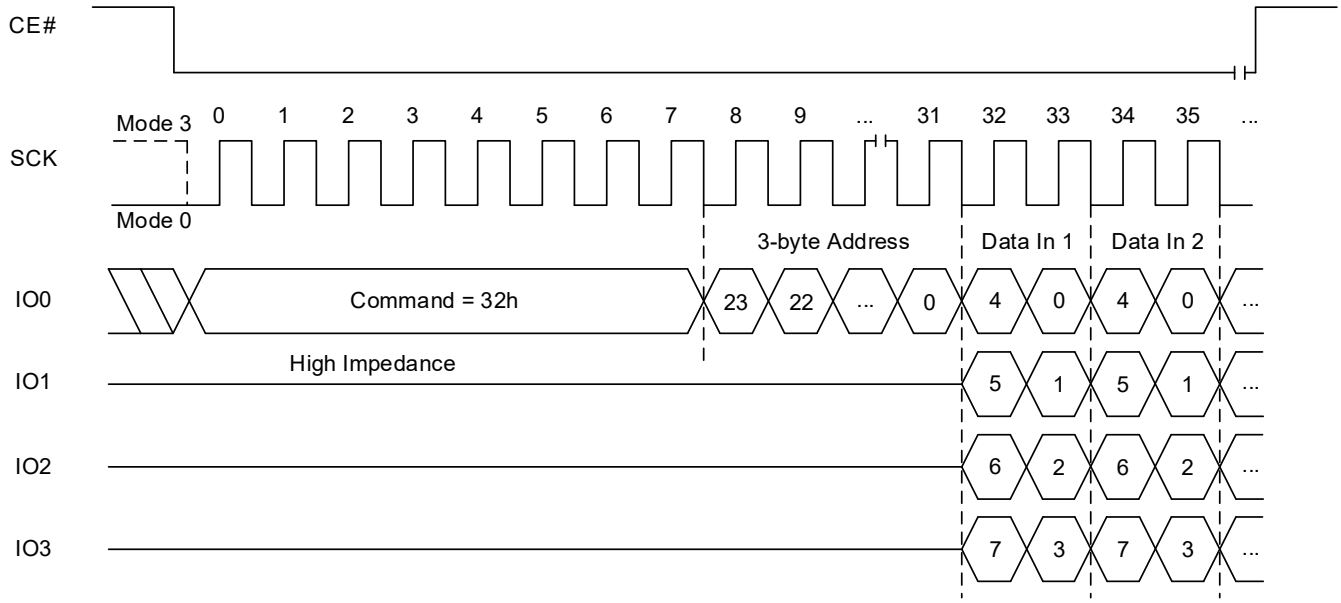
Before the execution of Quad Input Page Program command, the QE bit in the Status Register must be set to "1" and the Write Enable Latch (WEL) must be enabled through a Write Enable (WREN) command.

Program operation will start immediately after the CE# is brought high, otherwise the Quad Input Page Program command will not be executed. The internal control logic automatically handles the programming voltages and timing. During a program operation, all commands will be ignored except the RDSR command. The progress or completion of the program operation can be determined by reading the WIP bit in Status Register via a RDSR command. If the WIP bit is "1", the program operation is still in progress. If WIP bit is "0", the program operation has completed.

If more than 256 bytes data are sent to a device, the address counter rolls over within the same page, the previously latched data are discarded, and the last 256 bytes data are kept to be programmed into the page. The starting byte can be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged.

Note: A program operation can alter "1"s into "0"s. The same byte location or page may be programmed more than once, to incrementally change "1"s to "0"s. An erase operation is required to change "0"s to "1"s.

Figure 8.16 **Quad Input Page Program Sequence**



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8.13 ERASE OPERATION

The Erase command sets all bits in the addressed sector or block to “1”s.

The memory array of the device is organized into uniform 4 Kbyte sectors or 32/64 Kbyte uniform blocks (a block consists of eight/sixteen adjacent sectors respectively).

Before a byte is reprogrammed, the sector or block that contains the byte must be erased (erasing sets bits to “1”). In order to erase the device, there are three erase commands available: Sector Erase (SER), Block Erase (BER) and Chip Erase (CER). A sector erase operation allows any individual sector to be erased without affecting the data in other sectors. A block erase operation erases any individual block. A chip erase operation erases the whole memory array of a device. A sector erase, block erase, or chip erase operation can be executed prior to any programming operation.

SECTOR ERASE OPERATION (SER, 20h)

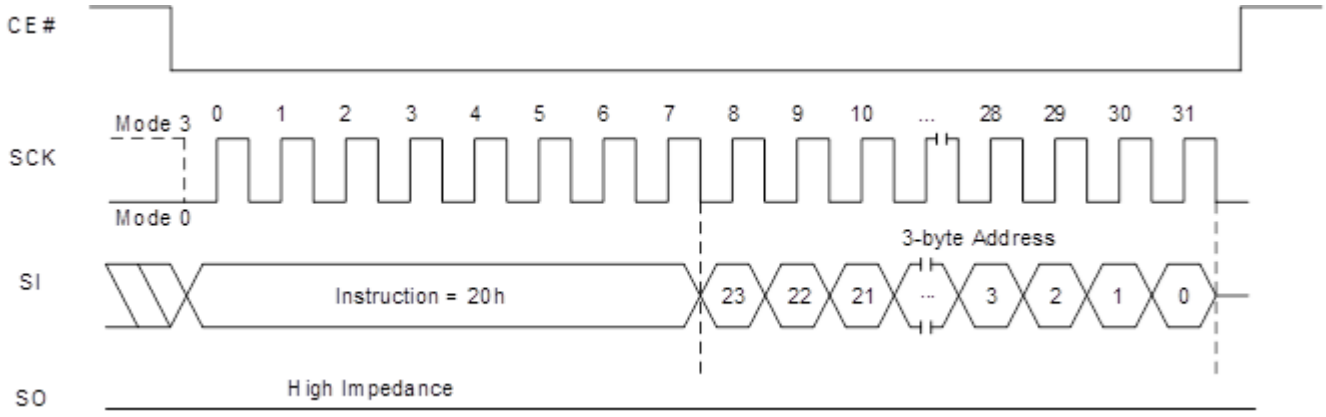
A Sector Erase (SER) command erases a 4 Kbyte sector before the execution of a SER command, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) command. The WEL bit is automatically reset after the completion of Sector Erase operation.

A SER command is entered, after CE# is pulled low to select the device and stays low during the entire command sequence The SER command code, and three address bytes are input via SI. Erase operation will start immediately after CE# is pulled high. The internal control logic automatically handles the erase voltage and timing.

The progress or completion of the erase operation can be determined by reading the WIP bit in the Status Register using a RDSR command.

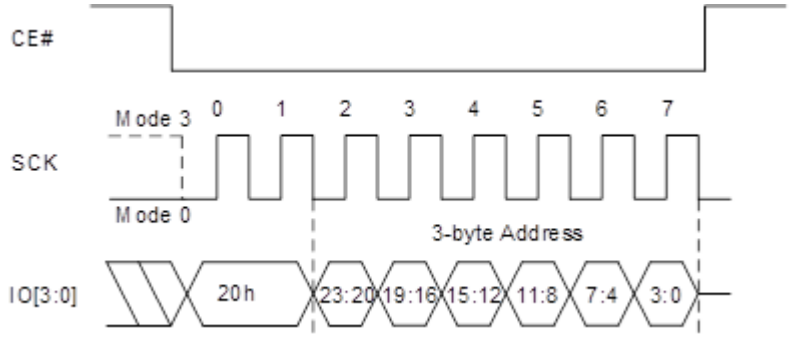
If the WIP bit is “1”, the erase operation is still in progress. If the WIP bit is “0”, the erase operation has been completed.

Figure 8.17 **Sector Erase Sequence in SPI mode**



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Figure 8.18 **Sector Erase Sequence in QPI Mode**



BLOCK ERASE OPERATION (BER32K:52h, BER64K:D8h)
A Block Erase (BER) command erases a 32/64Kbyte block. Before the execution of a BER command, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) command. The WEL is reset automatically after the completion of a block erase operation.

The BER command code and three address bytes are input via SI. Erase operation will start immediately after the CE# is pulled high, otherwise the BER command will not be executed. The internal control logic automatically handles the erase voltage and timing.

Figure 8.19 **Block Erase (64K) Sequence In SPI Mode**

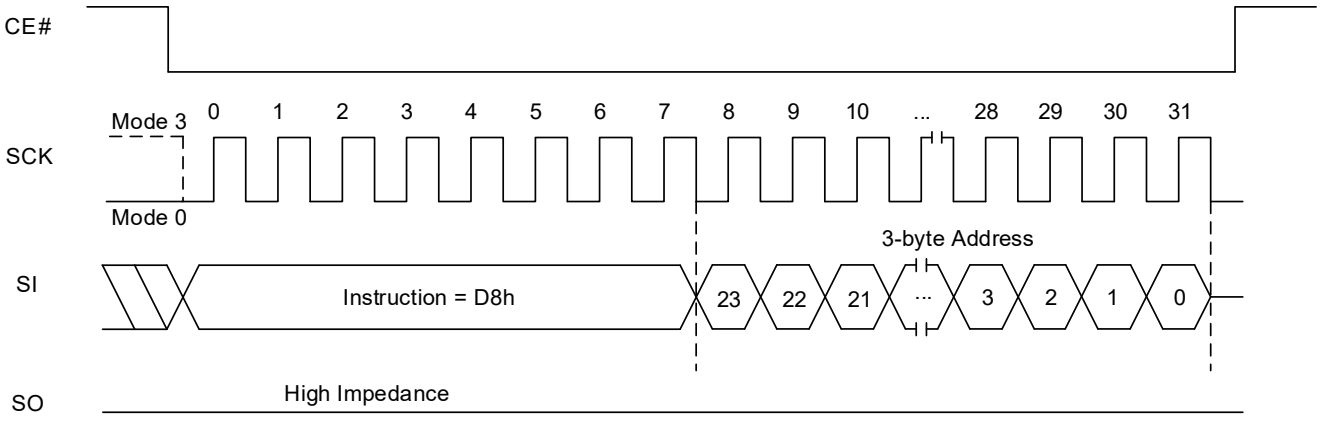
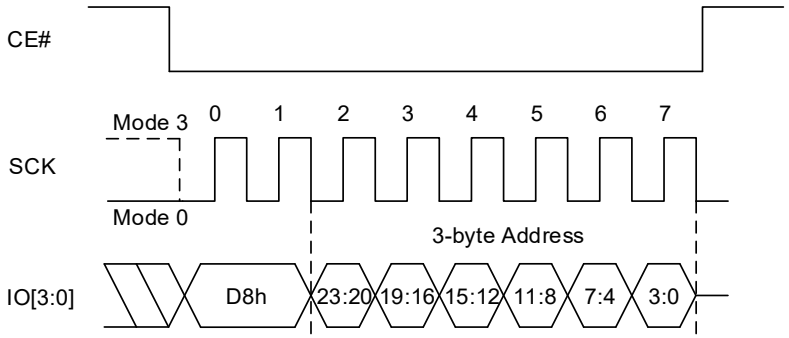


Figure 8.20 **Block Erase (64K) Sequence In QPI Mode**



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Figure 8.21 **Block Erase (32K) Sequence In SPI Mode**

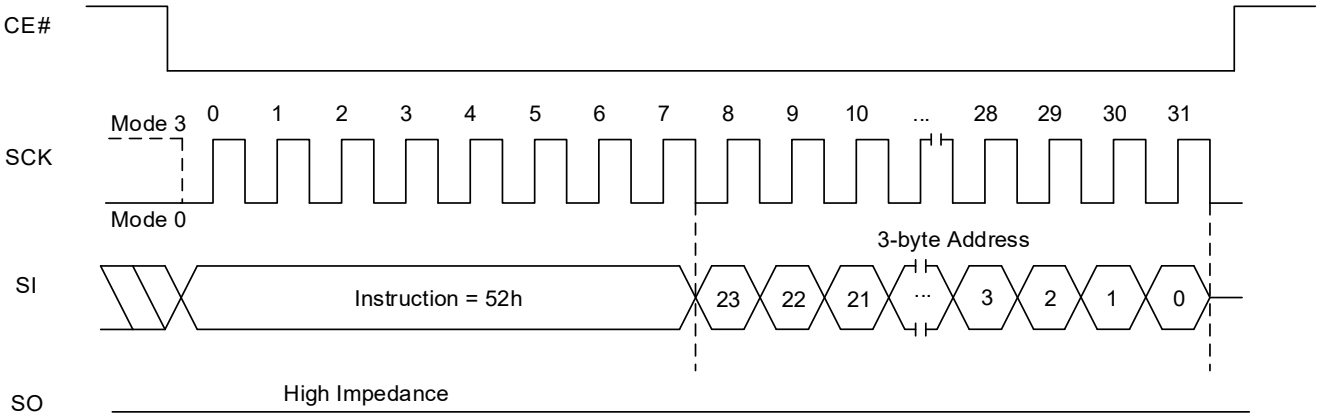
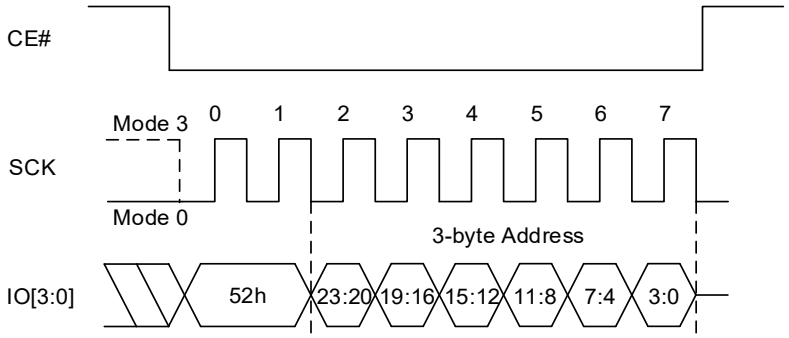


Figure 8.22 **Block Erase (32K) Sequence In QPI Mode**



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CHIP ERASE OPERATION (CER, C7H/60H)

A Chip Erase (CER) command erases the entire memory array. Before the execution of CER command, the Write Enable Latch (WEL) must be set via a Write Enable (WREN) command. The WEL is automatically reset after completion of a chip erase operation.

The CER command code is input via the SI. Erase operation will start immediately after CE# is pulled high, otherwise the CER command will not be executed. The internal control logic automatically handles the erase voltage and timing.

Chip Erase (CER) command can be executed only when all sectors are unprotected. If one or more sectors are protected, the CER command is not executed and E_ERR and PROT_E are set.

Figure 8.23 **Chip Erase Sequence In SPI Mode**

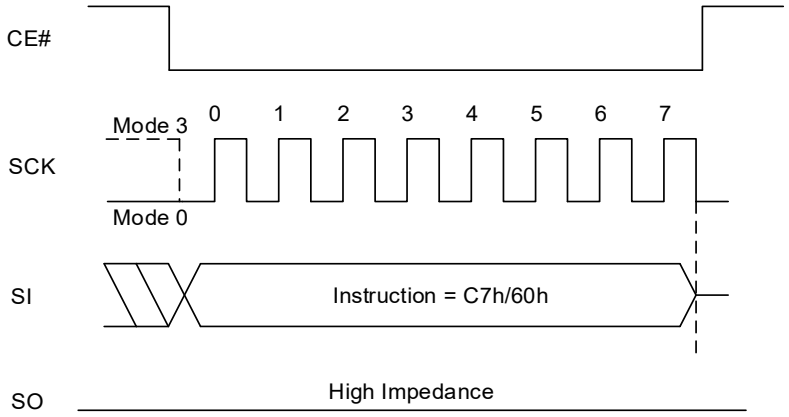
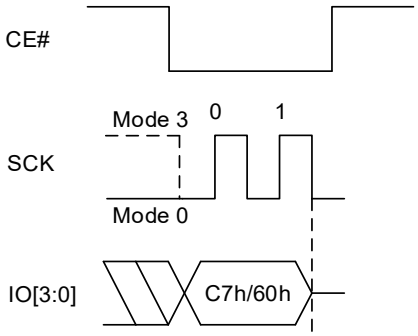


Figure 8.24 **Chip Erase Sequence In QPI Mode**



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8.14 WRITE ENABLE OPERATION (WREN, 06h)

The Write Enable command is used to set the Write Enable Latch (WEL) bit. The WEL bit is reset to the write-protected state after power-up. The WEL bit must be write enabled before any write operation, including Sector Erase, Block Erase, Chip Erase, Page Program, Program Information Row, Write non-volatile Status Register, except for Set volatile Status Register. The WEL bit will be reset to the write-protected state automatically upon completion of a write operation. The WREN command is required before any above operation is executed.

Figure 8.25 **Write Enable Sequence In SPI Mode**

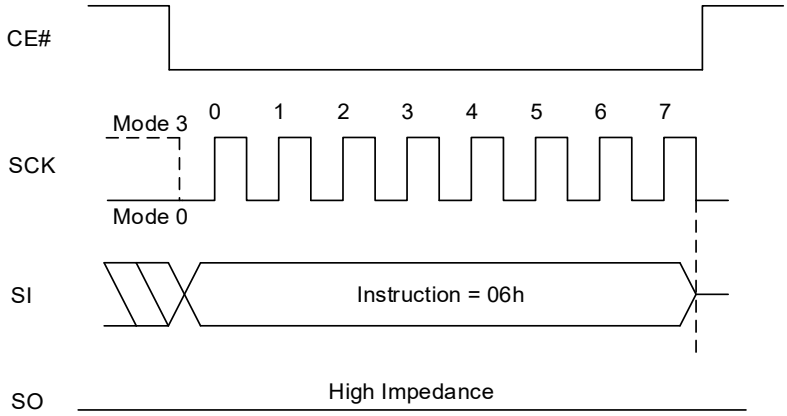
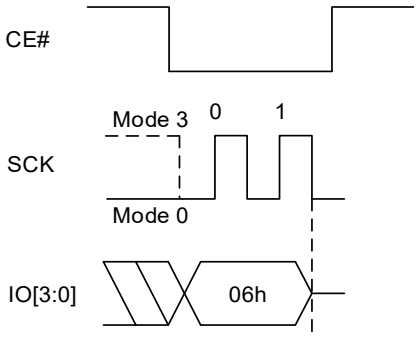


Figure 8.26 **Write Enable Sequence In QPI Mode**



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8.15 WRITE DISABLE OPERATION (WRDI, 04h)

The Write Disable (WRDI) command resets the WEL bit and disables all write commands. The WRDI command is not required after the execution of a write command, since the WEL bit is automatically reset.

Figure 8.27 **Write Disable Sequence In SPI Mode**

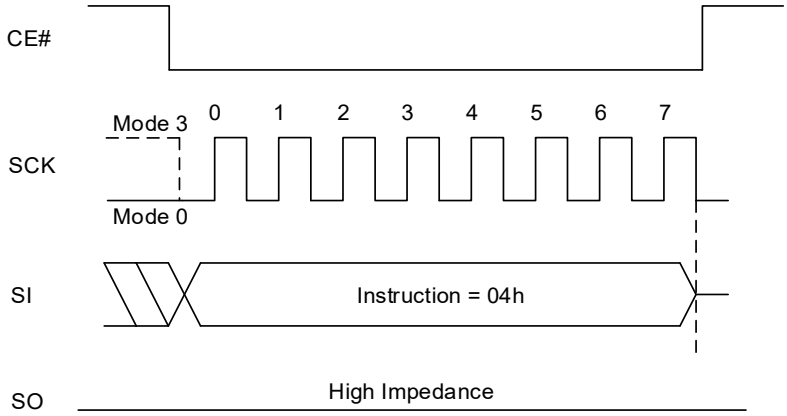
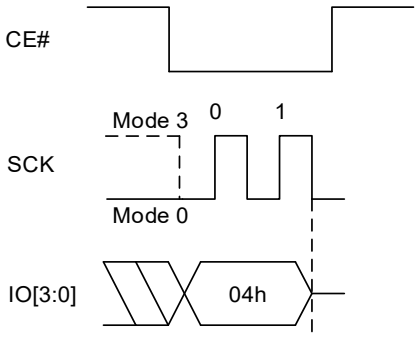


Figure 8.28 **Write Disable Sequence In QPI Mode**



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8.16 VOLATILE STATUS REGISTER WRITE ENABLE OPERATION (VSRWREN, 50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

The Volatile Status Register Write Enable (50h) command does not set the Write Enable Latch (WEL) bit to "1".

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Figure 8.29 **Write Enable for Volatile Status Registers Sequence In SPI Mode**

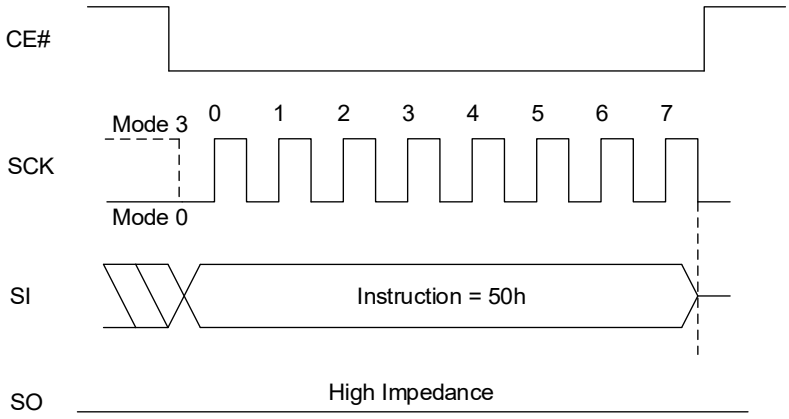
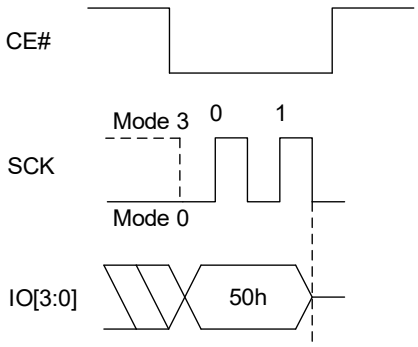


Figure 8.30 **Write Enable for Volatile Status Registers Sequence In QPI Mode**



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8.17 READ STATUS REGISTER-1/2/3 (RDSR1/2/3, 05h/35h/15h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by driving CE# low and shifting the command code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 8.31 and Figure 8.32. Refer to section 7.1 for Status Register descriptions.
The Read Status Register command may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another command. The Status Register can be read continuously, as shown in Figure 8.31 and Figure 8.32. The command is completed by driving CE# high.

Figure 8.31 **Read Status Register Sequence In SPI Mode**

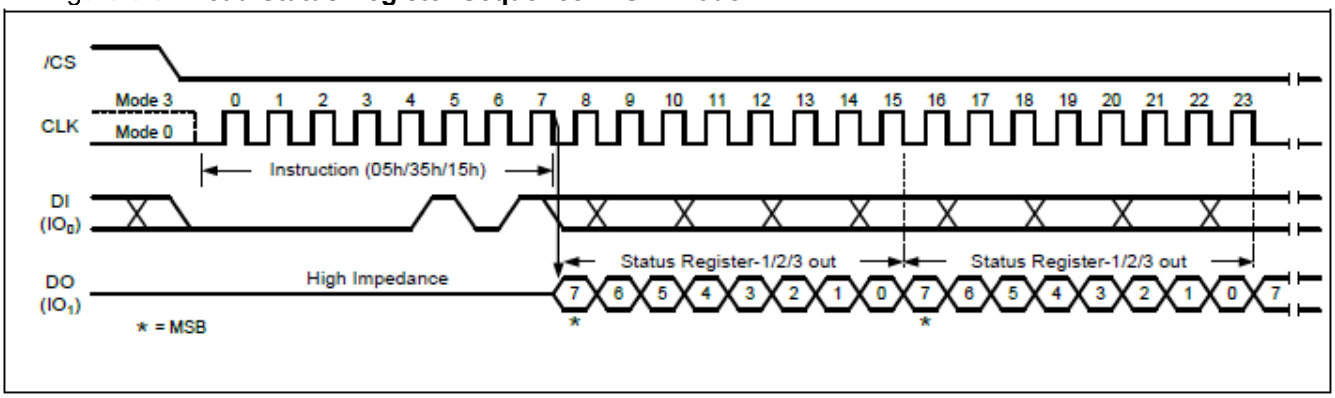
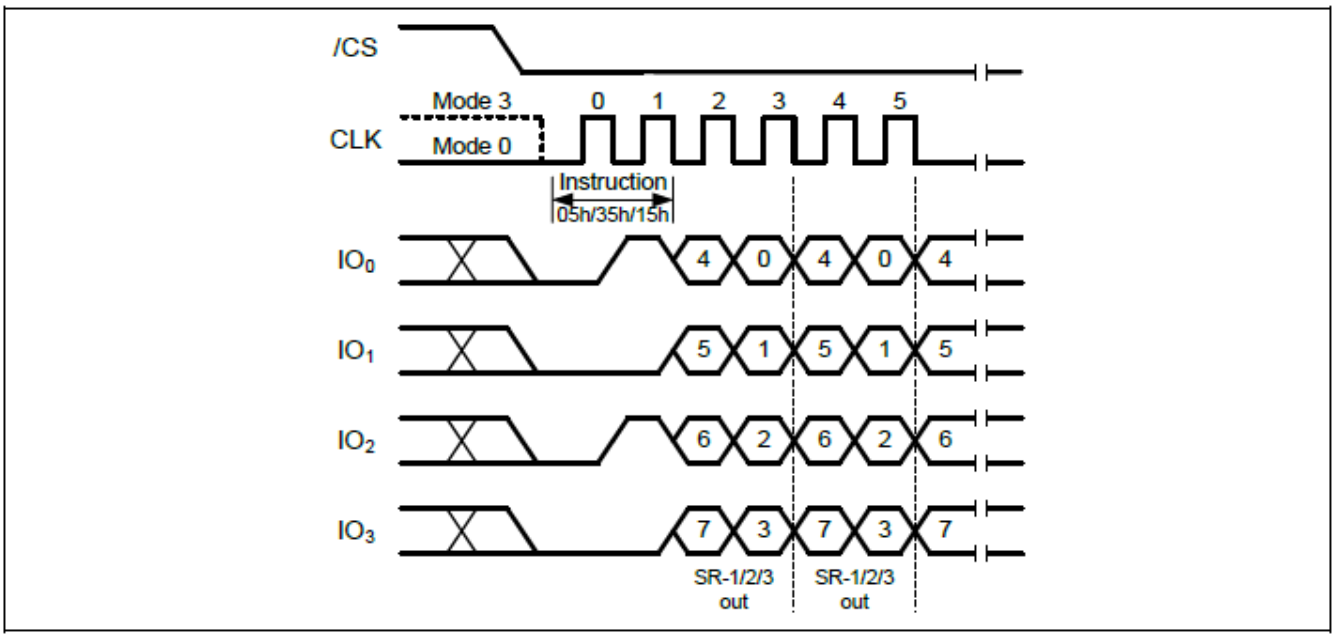


Figure 8.32 **Read Status Register Sequence In QPI Mode**



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8.18 WRITE STATUS REGISTER-1/2/3 (WRSR1/2/3, 01h/31h/11h)

The Write Status Register command allows the Status Registers to be written. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, IRL[3:1], QE, SRP1 in Status Register-2; HOLD/RST, ODS1, ODS0, PE_ERR, PROT_ERR in Status Register-3.
All other Status Register bit locations are read-only and will not be affected by the Write Status Register command. IRL[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write non-volatile Status Register bits, a standard Write Enable (06h) command must previously have been executed for the device to accept the Write Status Register command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CE# low, sending the command code "01h/31h/11h", and then writing the status register data byte as illustrated in Figure 8.33 and 8.34.

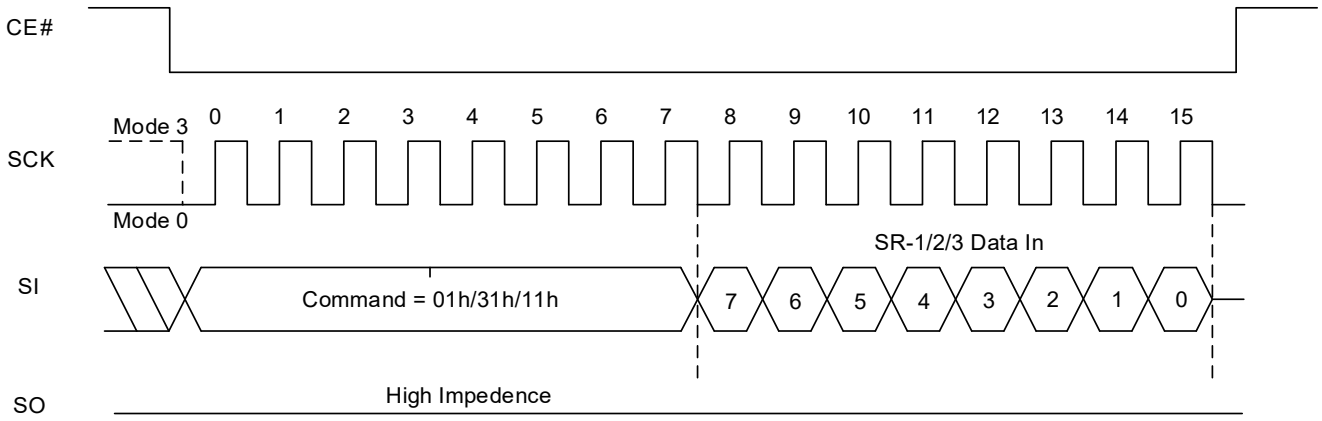
To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) command must have been executed prior to the Write Status Register command (Status Register bit WEL remains 0). However, SRP1 and IRL[3:1] cannot be changed from "1" to "0" because of the OTP protection for these bits. Upon power off or the execution of a Software/Hardware Reset command, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

During non-volatile Status Register write operation (06h combined with 01h/31h/11h), after CE# is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other commands again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after CE# is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (See AC Characteristics). BUSY bit will remain 0 during the Status Register bit refresh period.

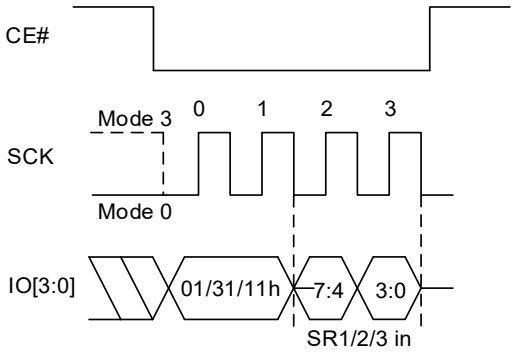
The Write Status Register command can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

Figure 8.33 **Write Status Register Sequence In SPI Mode**



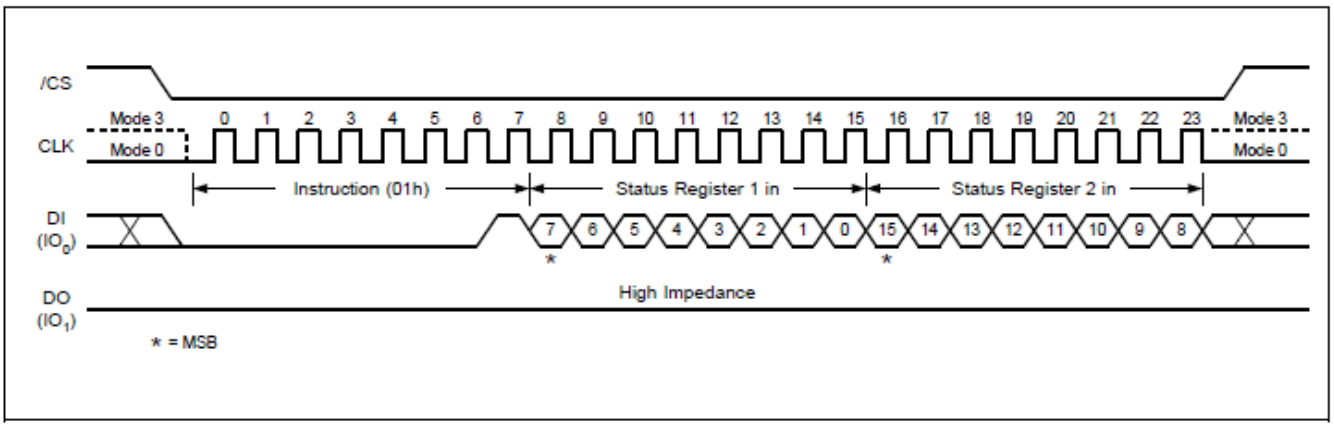
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Figure 8.34 **Write Status Register Sequence In QPI Mode**



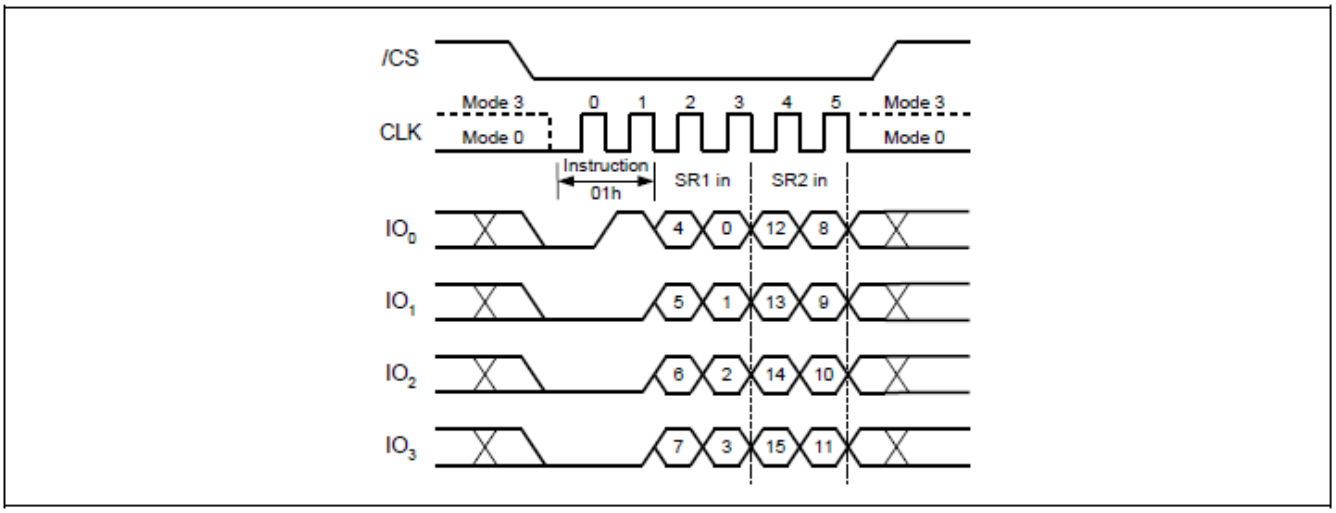
01h command also supports two byte writing, in which the Status Register-1&2 can be written using a single “Write Status Register-1 (01h)” command. To complete the Write Status Register-1&2 command, the CE# pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 8.35 and Figure 8.36. If CE# is driven high after the eighth clock, the Write Status Register-1 (01h) command will only program the Status Register-1, the Status Register-2 will not be affected (some parts from other suppliers may clear CMP and QE bits).

Figure 8.35 **Two Byte Write Status Register Sequence In SPI Mode**



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Figure 8.36 **Two Byte Write Status Register Sequence In QPI Mode**



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8.19 ENTER QUAD PERIPHERAL INTERFACE (QPI) MODE OPERATION (QPIEN, 38h; QPIDI, FFh)

The Enter Quad Peripheral Interface (QPIEN) command, 38h, enables the Flash device for QPI bus operation. Upon completion of the command, all commands thereafter will be 4-bit multiplexed input/output until a power cycle or an Exit Quad Peripheral Interface command is sent to device.

The Exit Quad Peripheral Interface (QPIDI) command, FFh, resets the device to 1-bit SPI protocol operation. To execute an Exit Quad Peripheral Interface operation, the host drives CE# low, sends the QPIDI command, then drives CE# high. The device just accepts QPI (2 clocks) command cycles.

Figure 8.37 **Enter Quad Peripheral Interface (QPI) Mode Sequence**

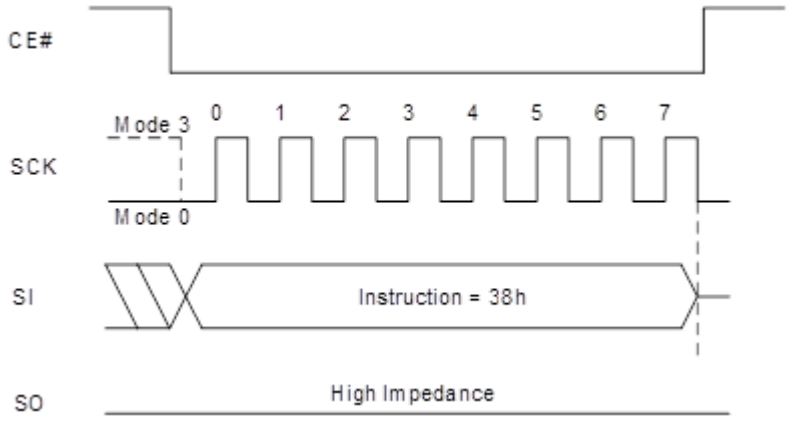
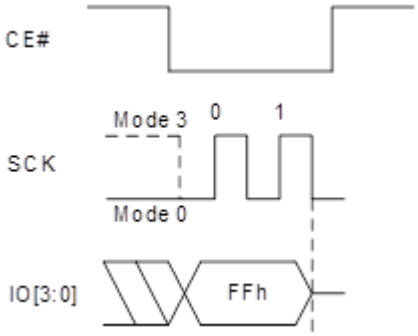


Figure 8.1 **Exit Quad Peripheral Interface (QPI) Mode Sequence**



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8.20 PROGRAM/ERASE SUSPEND & RESUME (PERSUS 75H, PERRSM 7AH)

The device allows the interruption of Sector Erase, Block Erase, or Page Program operations to conduct other operations. 75h command for suspend and 7Ah for resume will be used. (SPI/QPI all acceptable) Status Register bit10 (PSUS) and bit15 (ESUS) are used to check whether or not the device is in suspend mode.

Suspend to read ready timing (t_{SUS}): 20µs (MAX)
Resume to another suspend timing (t_{RS}): 100µs (TYP)

SUSPEND DURING SECTOR-ERASE OR BLOCK-ERASE (PERSUS 75h)
The Suspend command allows the interruption of Sector Erase and Block Erase operations. But Suspend command will be ignored during Chip Erase operation. After the Suspend command, other commands include array read operation can be accepted.

But Write Status Register command (01h) and Erase commands are not allowed during Erase Suspend. Also, array read for being erased sector/block is not allowed.

To execute Erase Suspend operation, the host drives CE# low, sends the Suspend command cycle (75h), then drives CE# high. The Status Register indicates that the Erase has been suspended by setting the ESUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit or wait the specified time t_{SUS}. When ESUS bit is set to "1", the Write Enable Latch (WEL) bit clears to "0".

SUSPEND DURING PAGE PROGRAMMING (PERSUS 75h)
The Suspend command also allows the interruption of all array Program operations. After the Suspend command, other commands include array read operation can be accepted.

But Write Status Register command (01h) and Program commands are not allowed during Program Suspend. Also, array read for being programmed page is not allowed.

To execute the Program Suspend operation, the host drives CE# low, sends the Suspend command cycle (75h), then drives CE# high. The Status Register indicates that the programming has been suspended by setting the PSUS bit from "0" to "1", but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the WIP bit or wait the specified time t_{SUS}. When PSUS bit is set to "1", the Write Enable Latch (WEL) bit clears to "0".

PROGRAM/ERASE RESUME (PERRSM 7Ah)
The Program/Erase Resume restarts the Program or Erase command that was suspended, and clears the suspend status bit in the Status Register (ESUS or PSUS bits) to "0". To execute the Program/Erase Resume operation, the host drives CE# low, sends the Program/Erase Resume command cycle (7Ah), then drives CE# high. A cycle is two nibbles long, most significant nibble first. To issue another Erase Suspend operation after Erase Resume operation, Erase Resume to another Erase Suspend delay (t_{RS}) is required, but it could require longer Erase time to complete Erase operation.

To determine if the internal, self-timed Write operation completed, poll the WIP bit.

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Table 8.3 Commands accepted during Suspend

Operation Suspended	Command Allowed		
	Name	Hex Code	Operation
Program or Erase	NORD	03h	Read Data Bytes from Memory at Normal Read Mode
Program or Erase	FRD	0Bh	Read Data Bytes from Memory at Fast Read Mode
Program or Erase	FRDIO	BBh	Fast Read Dual I/O
Program or Erase	FRDO	3Bh	Fast Read Dual Output
Program or Erase	FRQIO	EBh	Fast Read Quad I/O
Program or Erase	FRQO	6Bh	Fast Read Quad Output
Program or Erase	FRDTR	0Dh	Fast Read DTR Mode
Program or Erase	FRDDTR	BDh	Fast Read Dual I/O DTR
Program or Erase	FRQDTR	EDh	Fast Read Quad I/O DTR
Erase	PP	02h	Serial Input Page Program
Erase	PPQ	32h	Quad Input Page Program
Erase	WREN	06h	Write Enable
Program or Erase	RDSR	05h	Read Status Register
Program or Erase	PERRSM	7Ah	Resume program/erase
Erase	PERSUS	75h	Program/Erase Suspend
Program or Erase	RDID	ABh	Read Manufacturer and Product ID
Program or Erase	SRPV	C0h	Set Read Parameters (Volatile)
Program or Erase	RDJDID	9Fh	Read Manufacturer and Product ID by JEDEC ID Command
Program or Erase	RDMDID	90h	Read Manufacturer and Device ID
Program or Erase	RDUID	4Bh	Read Unique ID Number
Program or Erase	RDSFDP	5Ah	SFDP Read
Program or Erase	RSTEN	66h	Software reset enable
Program or Erase	RST	99h	Reset (Only along with 66h)
Program or Erase	IRRD	48h	Read Information Row
Erase	PSR	42h	Program Information Registers

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8.21 ENTER DEEP POWER DOWN (DP, B9h)

The Deep Power-down (DP) command is for setting the device on the minimizing the power consumption (enter into Power-down mode). During this mode, standby current is reduced from I_{sb1} to I_{sb2}. While in the Power-down mode, the device is not active and all Write/Program/Erase commands are ignored. The command is initiated by driving the CE# pin low and shifting the command code into the device. The CE# pin must be driven high after the command has been latched, or Power-down mode will not engage. Once CE# pin driven high, the Power-down mode will be entered within the time duration of t_{DP}. While in the Power-down mode only the Release from Power-down/RDID command, which restores the device to normal operation, will be recognized. All other commands are ignored, including the Read Status Register command which is always available during normal operation. Ignoring all but one command makes the Power Down state a useful condition for securing maximum write protection. It is available in both SPI and QPI mode.

Figure 8.38 **Enter Deep Power Down Mode Sequence In SPI Mode**

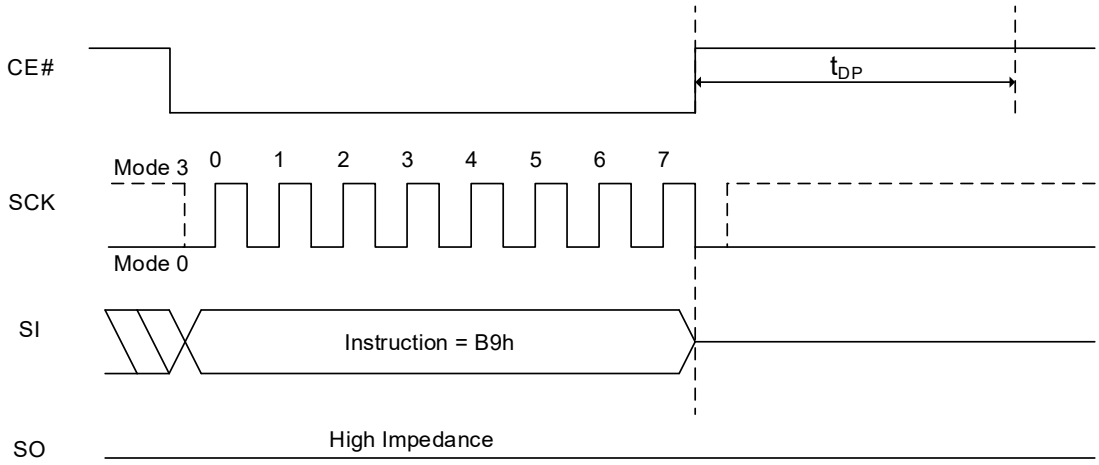
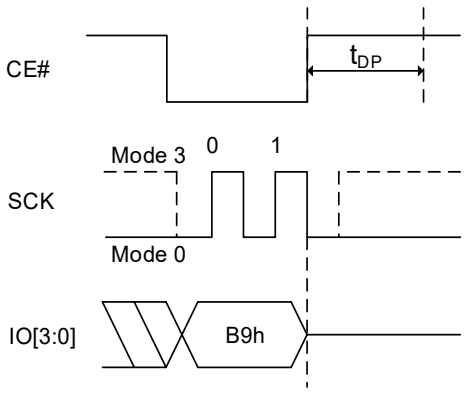


Figure 8.39 **Enter Deep Power Down Mode Sequence In QPI Mode**



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8.22 RELEASE DEEP POWER DOWN (RDPD, ABh)

The Release Deep Power-down/Read Device ID command is a multi-purpose command. To release the device from the Power-down mode, the command is issued by driving the CE# pin low, shifting the command code “ABh” and driving CE# high.

Releasing the device from Power-down mode will take the time duration of t_{RES1} before normal operation is restored and other commands are accepted. The CE# pin must remain high during the t_{RES1} time duration. If the Release Deep Power-down/RDID command is issued while an Erase, Program or Write cycle is in progress (WIP=1) the command is ignored and will not have any effects on the current cycle.

Figure 8.40 **Release Deep Power Down Mode Sequence In SPI Mode**

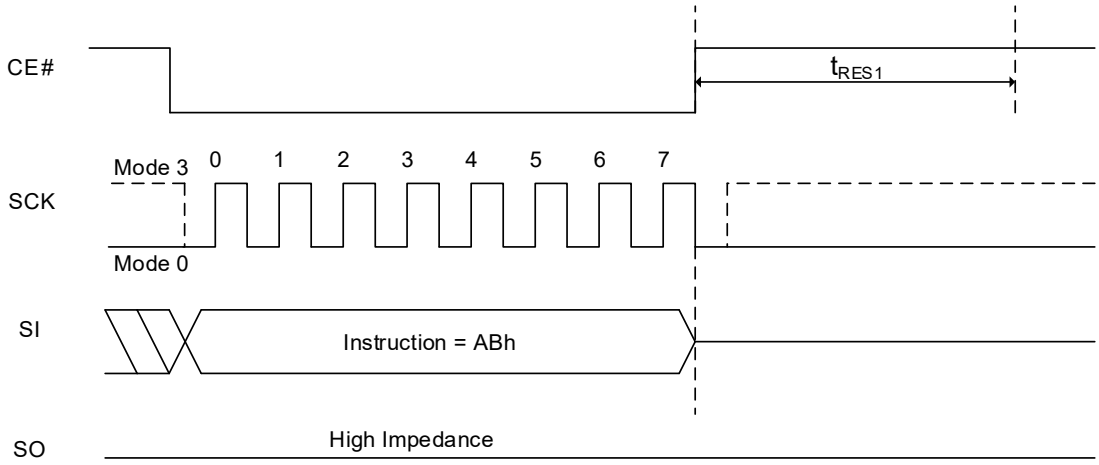
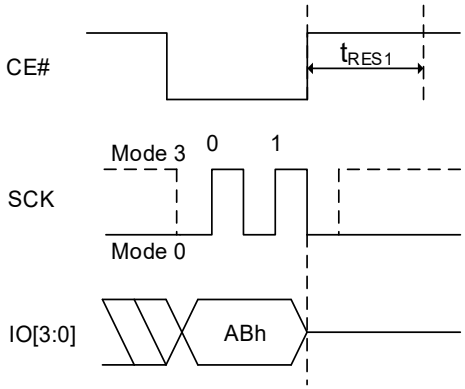


Figure 8.41 **Release Deep Power Down Mode Sequence In QPI Mode**



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8.23 READ PRODUCT IDENTIFICATION (RDID, ABh)

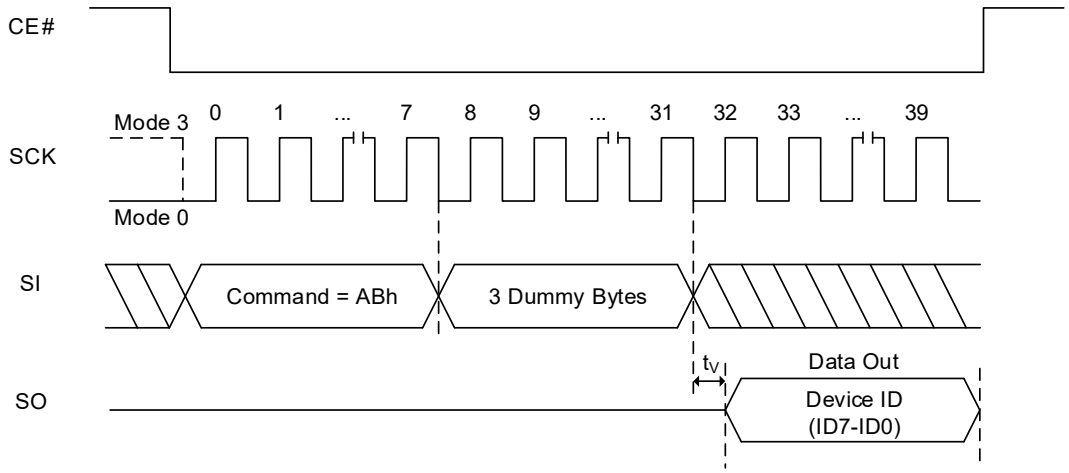
The Release from Power-down/Read Device ID command is a multi-purpose command. It can support both SPI and QPI modes. The Read Product Identification (RDID) command is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of Product Identification.

The RDID command code is followed by three dummy bytes, each bit being latched-in on SI during the rising SCK edge. Then the Device ID is shifted out on SO with the MSB first, each bit been shifted out during the falling edge of SCK. The RDID command is ended by driving CE# high. The Device ID (ID7-ID0) outputs repeatedly if additional clock cycles are continuously sent to SCK while CE# is at low.

Table 8.4 Product Identification

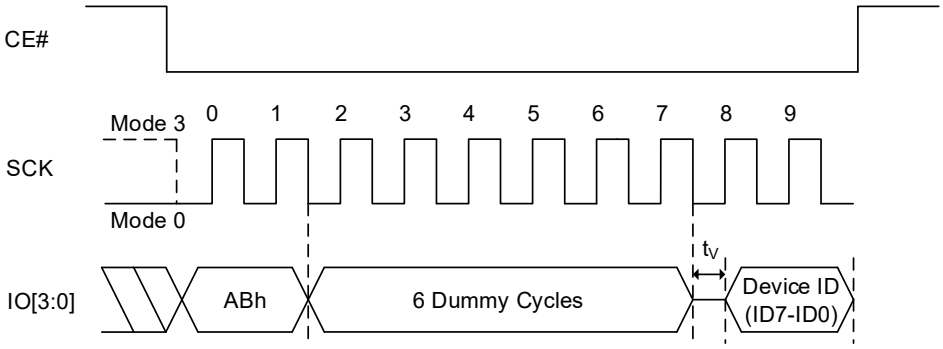
Command	Manufacturer ID	Device ID(ID15-ID8)	Device ID(ID7-ID0)
90h	9Dh		17h
9Fh	9Dh	71h	18h
ABh			17h

Figure 8.42 **Read Product Identification Sequence In SPI Mode**



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Figure 8.43 **Read Product Identification Sequence In QPI Mode**



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8.24 READ PRODUCT IDENTIFICATION BY JEDEC ID OPERATION (RDJDID, 9Fh)

The JEDEC ID READ command allows the user to read the manufacturer and product ID of devices. Refer to Table 8.4 Product Identification for Manufacturer ID and Device ID. After the JEDEC ID READ command (9Fh in SPI mode and QPI mode) is input, the Manufacturer ID is shifted out MSB first followed by the 2-byte electronic ID (ID15-ID0) that indicates Memory Type and Capacity, one bit at a time. Each bit is shifted out during the falling edge of SCK. If CE# stays low after the last bit of the 2-byte electronic ID, the Manufacturer ID and 2-byte electronic ID will loop until CE# is pulled high.

Figure 8.44 **RDJDID (Read JEDEC ID) Sequence In SPI Mode**

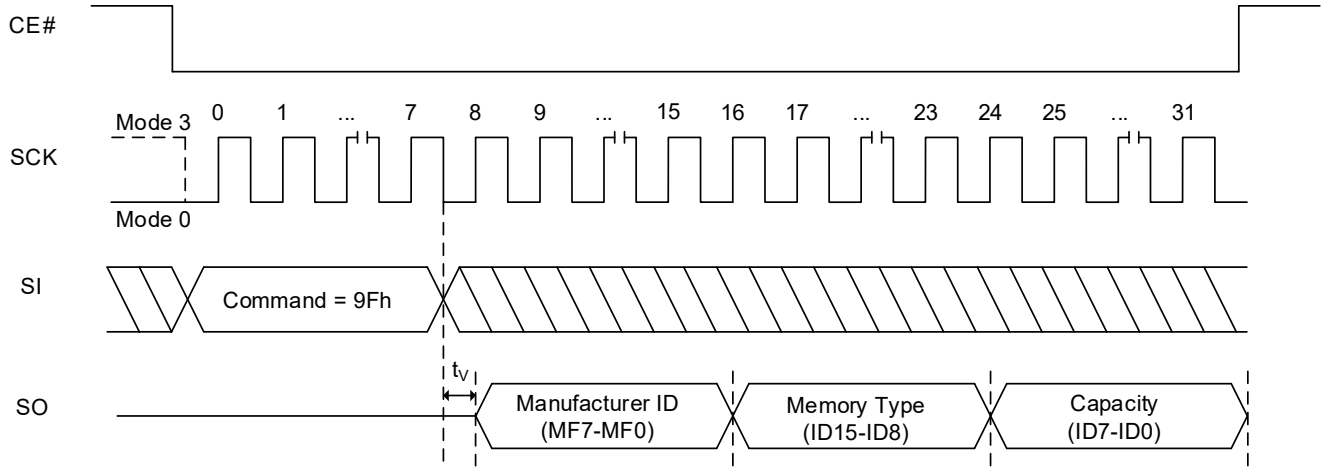
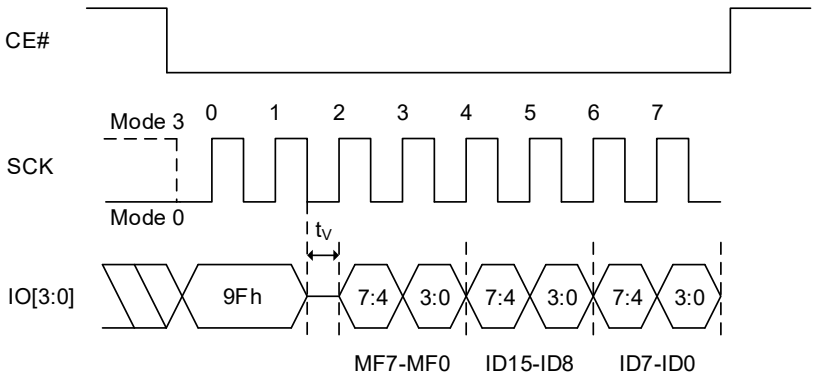


Figure 8.45 **RDJDID and RDJDIDQ (Read JEDEC ID) Sequence In QPI Mode**

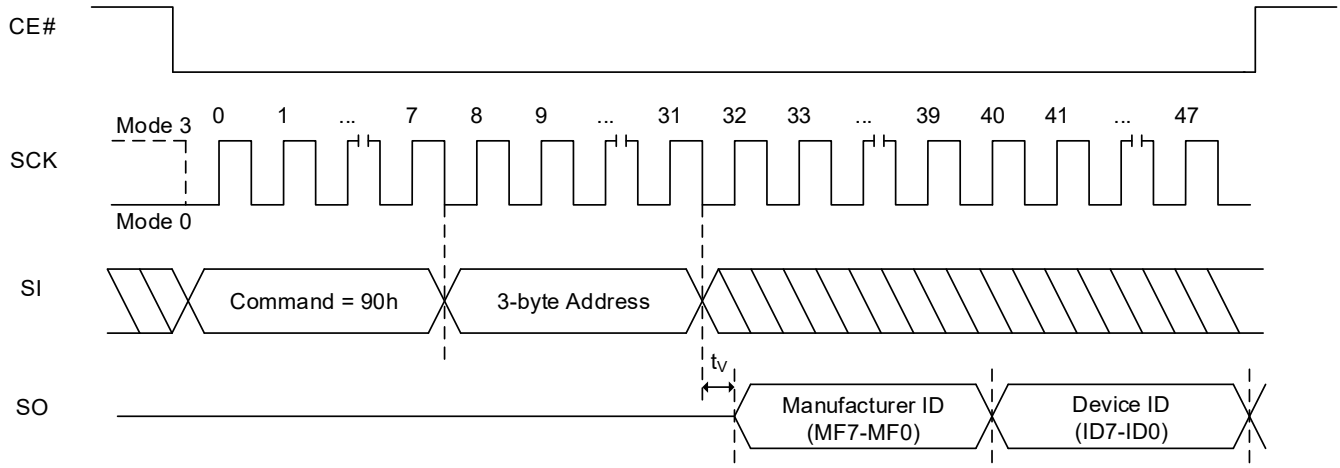


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8.25 READ DEVICE MANUFACTURER AND DEVICE ID OPERATION (RDMDID, 90h)

The Read Device Manufacturer and Device ID (RDMDID) command allows the user to read the Manufacturer and product ID of devices. Refer to Table 8.4 Product Identification for Manufacturer ID and Device ID. The RDMDID command code is followed by 3 byte address (A23~A0)=000000h, each bit being latched-in on SI during the rising edge of SCK. Manufacturer ID is shifted out on SO with the MSB first followed by the Device ID (ID7- ID0). Each bit is shifted out during the falling edge of SCK.

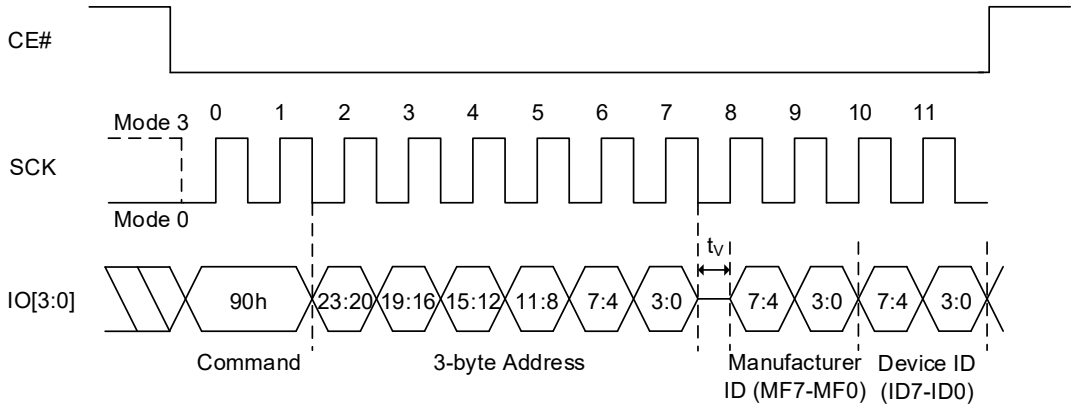
Figure 8.46 **Read Product Identification by RDMDID Sequence In SPI Mode**



Notes:

1. **The Manufacturer and Device ID can be read continuously and will alternate from one to the other until CE# pin is pulled high.**

Figure 8.47 **Read Product Identification by RDMDID Sequence In QPI Mode**



Notes:

1. **The Manufacturer and Device ID can be read continuously and will alternate from one to the other until CE# pin is pulled high.**

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8.26 READ UNIQUE ID NUMBER (RDUID, 4BH)

The Read Unique ID Number (RDUID) command accesses a factory-set read-only 16-byte number that is unique to the device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The RDUID command is instated by driving the CE# pin low and shifting the command code (4Bh) followed by 3 address bytes and a dummy byte. After which, the 16-byte ID is shifted out on the falling edge of SCK as shown below.
As a result, the sequence of RDUID command is same as FAST READ.

RDUID (4Bh) command is also supported in QPI mode with fixed 8 dummy cycles.

Note: 16 bytes of data will repeat as long as CE# is low and SCK is toggling.

Figure 8.48 **RDUID Sequence In SPI Mode**

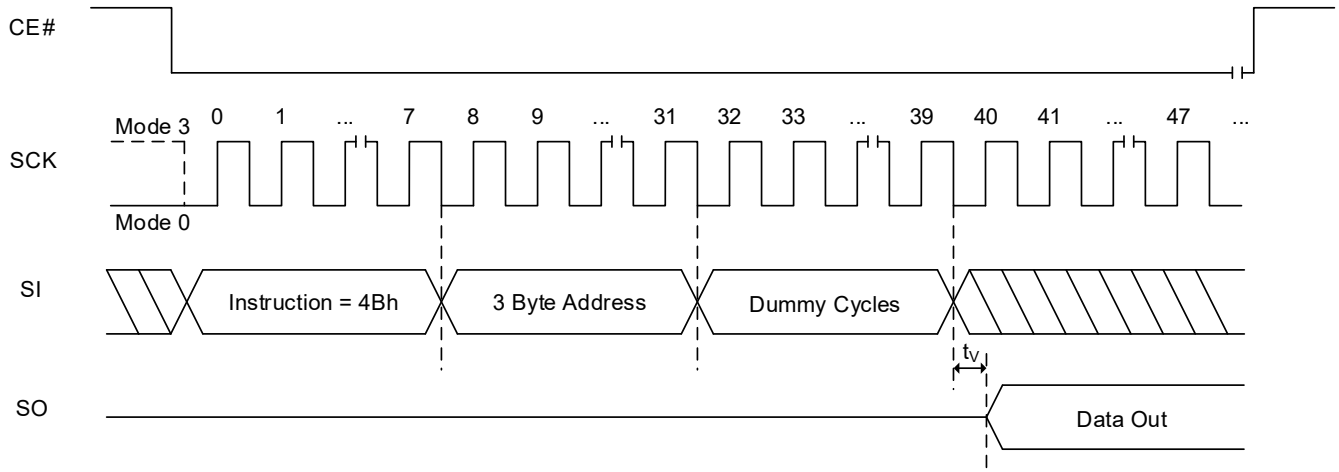


Table 8.5 Unique ID Addressing

A[23:16]	A[15:9]	A[8:4]	A[3:0]
XXh	XXh	00h	0h Byte address
XXh	XXh	00h	1h Byte address
XXh	XXh	00h	2h Byte address
XXh	XXh	00h	⋮
XXh	XXh	00h	Fh Byte address

Note: XX means "don't care".

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8.27 READ SFDP OPERATION (RDSFDP, 5AH)

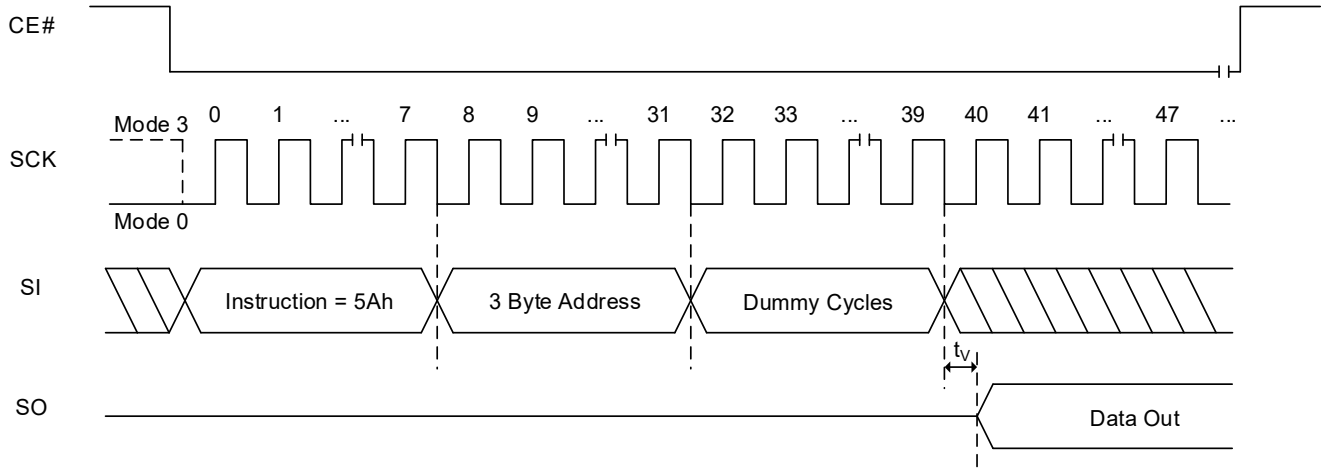
The Serial Flash Discoverable Parameters (SFDP) standard provides a consistent method of describing the functions and features of serial Flash devices in a standard set of internal parameter tables. These parameters can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. For more details, please refer to the JEDEC Standard JESD216 (Serial Flash Discoverable Parameters).

The sequence of issuing RDSFDP command in SPI mode is:

CE# goes low → Send RDSFDP command (5Ah) → Send 3 address bytes on SI pin → 8 dummy cycles on SI pin → Read SFDP code on SO → End RDSFDP operation by driving CE# high at any time during data out. Refer to ISSI's Application note for SFDP table. The data at the addresses that are not specified in SFDP table are undefined.

RDSFDP (5Ah) command is also supported in QPI mode with fixed 8 dummy cycles.

Figure 8.49 **RDSFDP (Read SFDP) Sequence in SPI mode**



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8.28 SOFTWARE RESET (RESET-ENABLE (RSTEN, 66H) AND RESET (RST, 99H)) AND HARDWARE RESET

The Software Reset operation is used as a system reset that puts the device in normal operating mode. During the Reset operation, the value of volatile registers will default back to the value in the corresponding non-volatile register. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST). The operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

Execute the CE# pin low → sends the Reset-Enable command (66h), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99h), and pulls CE# high.

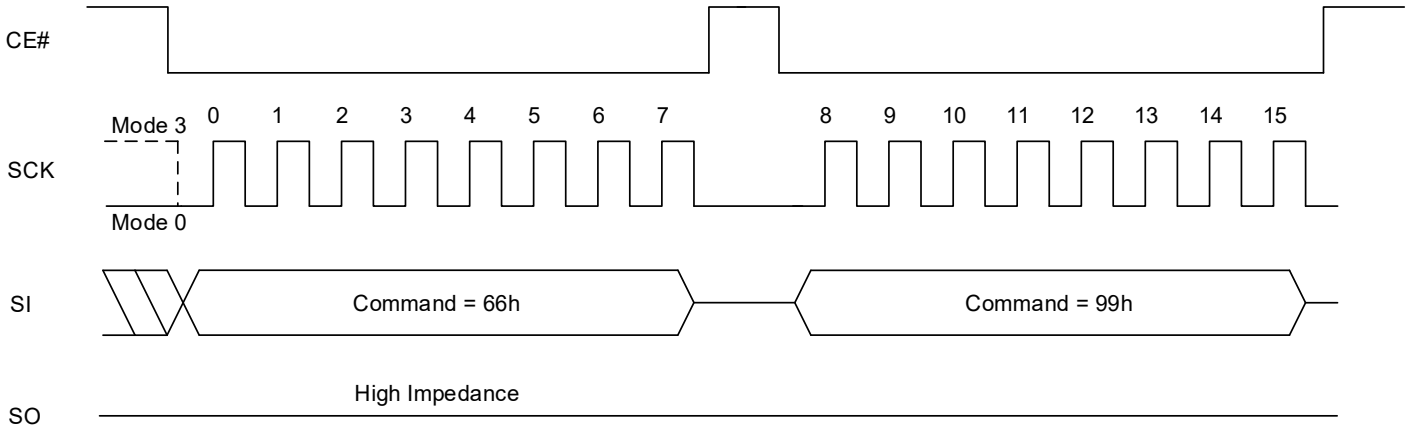
Only if the RESET# pin is enabled, Hardware Reset function is available.
For the device with HOLD#/RESET#, the RESET# pin will be solely applicable in SPI mode and when the QE bit = "0". For the device with dedicated RESET# (Dedicated RESET# Disable bit is "0" in Status Register), the RESET# pin is always applicable regardless of the QE bit value in Status Register and HOLD#/RESET# selection bit (Bit23) in Status Register in SPI/QPI mode.

In order to activate Hardware Reset, the RESET# pin (or ball) must be driven low for a minimum period of t_{RESET} (100ns). Drive RESET# low for a minimum period of t_{RESET} will interrupt any on-going internal and external operations, release the device from deep power down mode[1], disable all input signals, force the output pin enter a state of high impedance, and reset all the read parameters.

The Software/Hardware Reset during an active Program or Erase operation aborts the operation, which can result in corrupting or losing the data of the targeted address range. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation will require more latency than recovery from other operations.

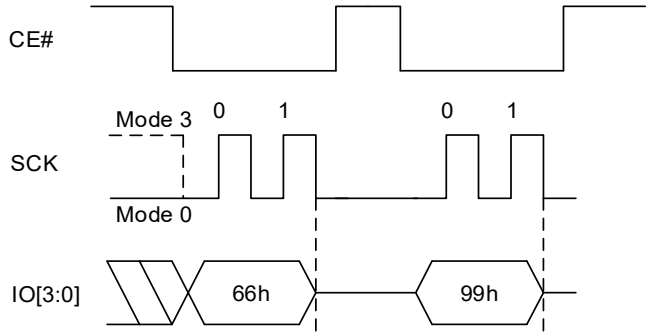
Note1: The Status Registers remain unaffected.

Figure 8.50 **Software Reset Enable and Software Reset Sequence In SPI Mode (RSTEN, 66h + RST, 99h)**



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Figure 8.51 **Software Reset Enable and Software Reset Sequence In QPI Mode (RSTEN, 66h + RST, 99h)**



8.29 SECURITY INFORMATION REGISTER

The Security Information Register is comprised of an additional 3 x 1024 bytes of programmable information. The security bits can be reprogrammed by the user. Any program security command issued while an erase, program or write cycle is in progress is rejected without having any effect on the cycle that is in progress.

Table 8.6 Information Register Valid Address Range

Address Assignment	A[23:16]	A[15:12]	A[11:10]	A[9:0]
IRL1 (Information Register Lock1)	00h	0001b	00b	Don't care
IRL2 (Information Register Lock2)	00h	0010b	00b	Don't care
IRL3 (Information Register Lock3)	00h	0011b	00b	Don't care

Bit 13~11 of the Status Register-2 is used to permanently lock the programmable memory array.

When STATUS REGISTERS-2 bit IRLx = "0", the 1024 bytes of the programmable memory array can be programmed.
When STATUS REGISTERS-2 bit IRLx = "1", the 1024 bytes of the programmable memory array function as read only.

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8.30 ERASE INFORMATION REGISTERS (44h)

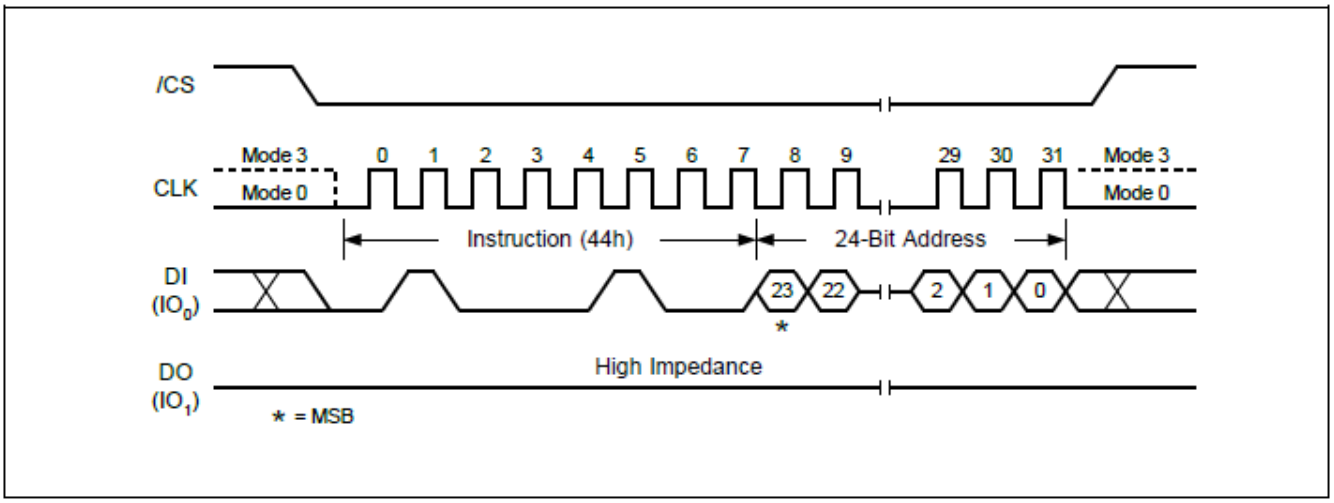
The IS25WJ128F provides 3x1024-Byte Information Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Information Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Information Registers command sequence: CS# goes low→sending Erase Information Registers command→3-byte address on SI→CS# goes high. The command sequence is shown below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Erase Information Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Information Registers cycle (whose duration is tSE) is initiated. While the Erase Information Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Information Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Information Registers Lock Bit (IRL1, IRL2, IRL3) in the Status Register-2 can be used to OTP protect the Information Registers . Once the LB bit is set to 1, the Information Registers will be permanently locked; the Erase Information Registers command will be ignored.

Address	A23-16	A15-12	A11-10	A9-0
Information Register 1	00h	0001b	00b	Don't care
Information Register 2	00h	0010b	00b	Don't care
Information Register 3	00h	0011b	00b	Don't care

Figure 8.52 **IRER (Information Register Erase) Sequence**



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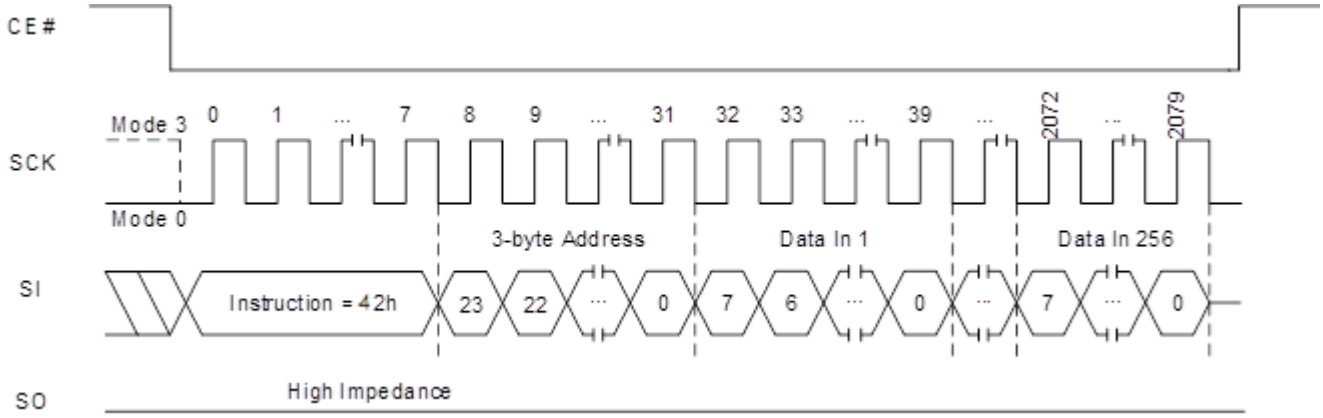
8.31 PROGRAM INFORMATION REGISTERS (42h)

The Program Information Registers command is similar to the Page Program command. Each Information Registers contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Information Registers command. The Program Information Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Information Registers cycle (whose duration is tPP) is initiated. While the Program Information Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Information Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
If the Information Registers Lock Bit (IRL1, IRL2, IRL3) is set to 1, the Information Registers will be permanently locked. Program Information Registers command will be ignored.

Note: A program operation can alter "1" s into "0"s, The same byte location or Information Register array may be programmed more than once to incrementally change "1" to "0"s. An erase operation is required to change "0" s back to "1"s.

Address	A23-16	A15-12	A11-10	A9-0
Information Registers 1	00h	0001b	00b	Byte Address
Information Registers 2	00h	0010b	00b	Byte Address
Information Registers 3	00h	0011b	000b	Byte Address

Figure 8.53 **IRP (Information Register Program) Sequence**



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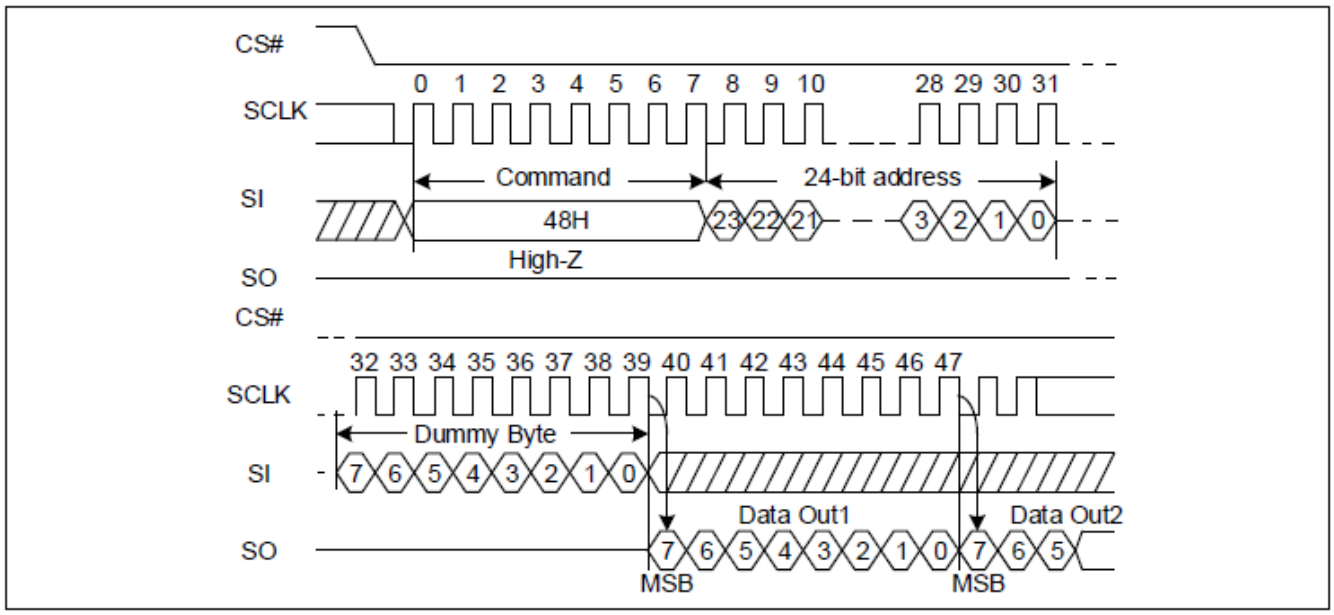
8.32 READ INFORMATION REGISTERS (48H)

The Read Information Registers command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the four Information Registers . The command is initiated by driving the CE# pin low and then shifting the command code “48h” followed by a 24-bit address (A23-A0) and eight ‘dummy’ clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The command is completed by driving CE# high. The Read Information Registers command sequence is shown in Figure 47. If a Read Information Registers command is issued while an Erase, Program or Write cycle is in process (BUSY=1) the command is ignored and will not have any effects on the current cycle. The Read Information Registers command allows clock rates from D.C. to a maximum of FR
(see AC Electrical Characteristics).

48h command is also supported in QPI mode with fixed 8 dummy cycles.

Address	A23-16	A15-12	A11-10	A9-0
Information Registers 1	00h	0001b	00b	Byte Address
Information Registers 2	00h	0010b	00b	Byte Address
Information Registers 3	00h	0011b	00b	Byte Address

Figure 8.54 **Read Information Registers Command (SPI Mode)**



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8.33 FAST READ DTR MODE OPERATION IN SPI MODE (FRDTR, 0DH)

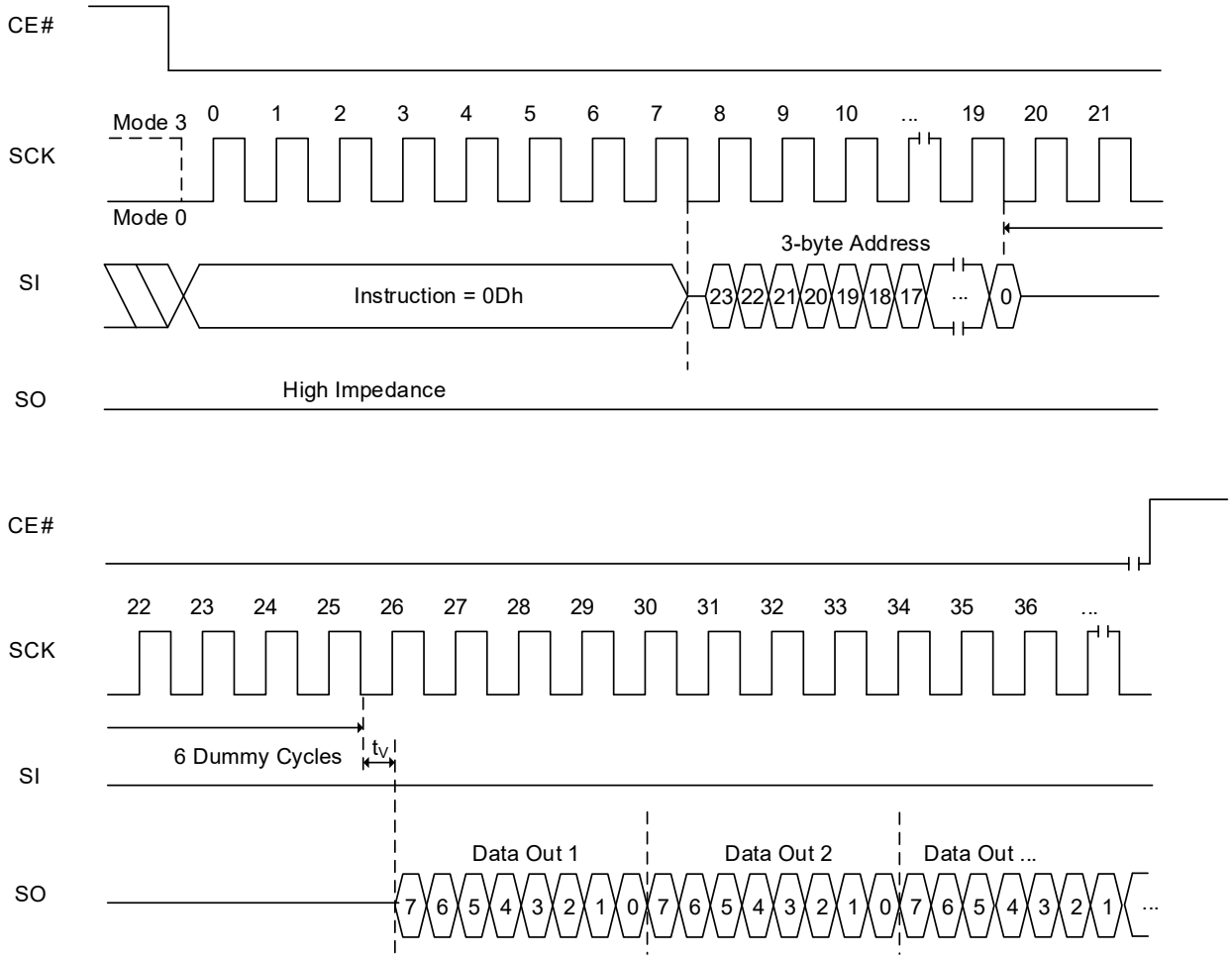
The FRDTR command is for doubling the data in and out. Signals are triggered on both rising and falling edge of clock. The address is latched on both rising and falling edge of SCK, and data of each bit shifts out on both rising and falling edge of SCK at a maximum frequency f_{C2}. The 2-bit address can be latched-in at one clock, and 2-bit data can be read out at one clock, which means one bit at the rising edge of clock, the other bit at the falling edge of clock.

The first address byte can be at any location. The address is automatically increased to the next higher address after each byte of data is shifted out, so the whole memory can be read out in a single FRDTR command. The address counter rolls over to 0 when the highest address is reached.

The sequence of issuing FRDTR command is: CE# goes low → Sending FRDTR command code (1bit per clock) → 3-byte address on SI (2-bit per clock) → 6 dummy cycles on SI → Data out on SO (2-bit per clock) → End FRDTR operation via driving CE# high at any time during data out.

While a Program/Erase/Write Status Register cycle is in progress, FRDTR command will be rejected without any effect on the current cycle.

Figure 8.55 **FRDTR Sequence In SPI Mode**



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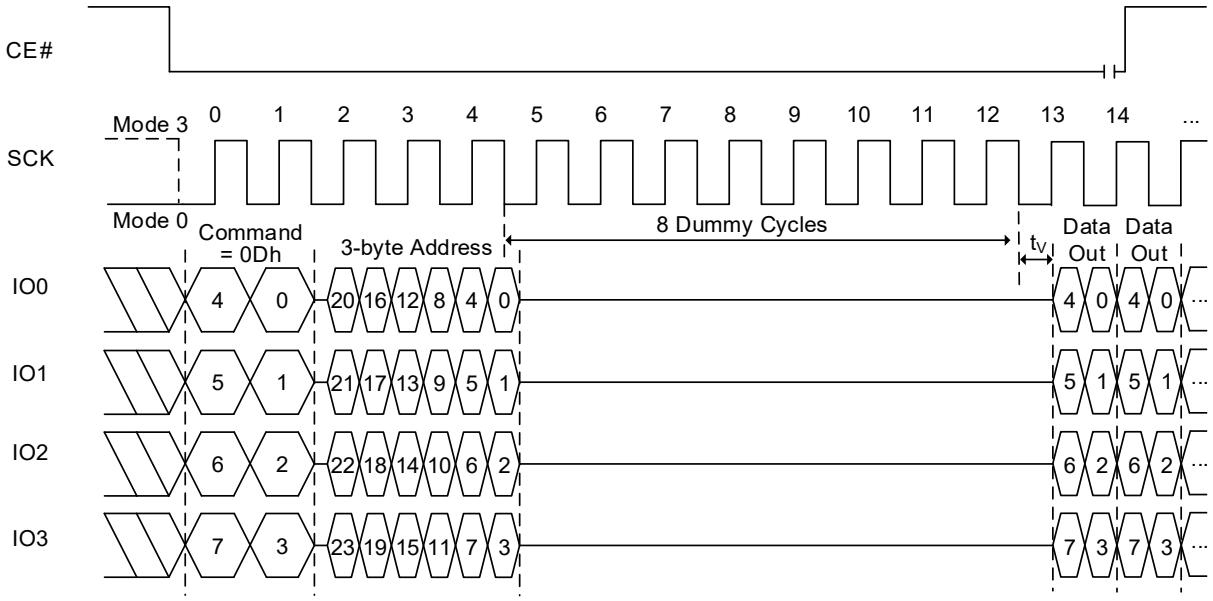
FAST READ DTR MODE OPERATION IN QPI MODE (FRDTR, 0Dh)

The FRDTR command in QPI mode utilizes all four IO lines to input the command code so that only two clocks are required, while the FRDTR command requires that the byte-long command code is shifted into the device only via IO0 line in eight clocks. In addition, subsequent address and data out are shifted in/out via all four IO lines unlike the FRDTR command. Eventually this operation is same as the FRQDTR in QPI mode, but the only different thing is that AX mode is not available in the FRDTR operation in QPI mode.

The sequence of issuing FRDTR command in QPI mode is: CE# goes low → Sending FRDTR command (4-bit per clock) → 24-bit address interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → 8 dummy cycles → Data out interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → End FRDTR operation in QPI mode by driving CE# high at any time during data out.

If the FRDTR command in QPI mode is issued while a Program/Erase/Write Status Register cycle is in progress (WIP=1), the command will be rejected without any effect on the current cycle.

Figure 8.56 **FRDTR Sequence In QPI Mode**



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8.34 FAST READ DUAL IO DTR MODE OPERATION (FRDDTR, BDH)

The FRDDTR command enables Double Transfer Rate throughput on dual I/O of the device in read mode. The address (interleave on dual I/O pins) is latched on both rising and falling edge of SCK, and the data (interleave on dual I/O pins) shift out on both rising and falling edge of SCK at a maximum frequency f_{T2}. The 4-bit address can be latched-in at one clock, and 4-bit data can be read out at one clock, which means two bits at the rising edge of clock, the other two bits at the falling edge of clock.

The first address byte can be at any location. The address is automatically increased to the next higher address after each byte of data is shifted out, so the whole memory can be read out with a single FRDDTR command. The address counter rolls over to 0 when the highest address is reached. Once writing FRDDTR command, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing FRDDTR command is: CE# goes low → Sending FRDDTR command (1-bit per clock) → 24-bit address interleave on IO1 & IO0 (4-bit per clock) → 6 dummy cycles on IO1 & IO0 → Data out interleave on IO1 & IO0 (4-bit per clock) → End FRDDTR operation via pulling CE# high at any time during data out (Please refer to Figure 8.22 for 2 x I/O Double Transfer Rate Read Mode Timing Waveform).

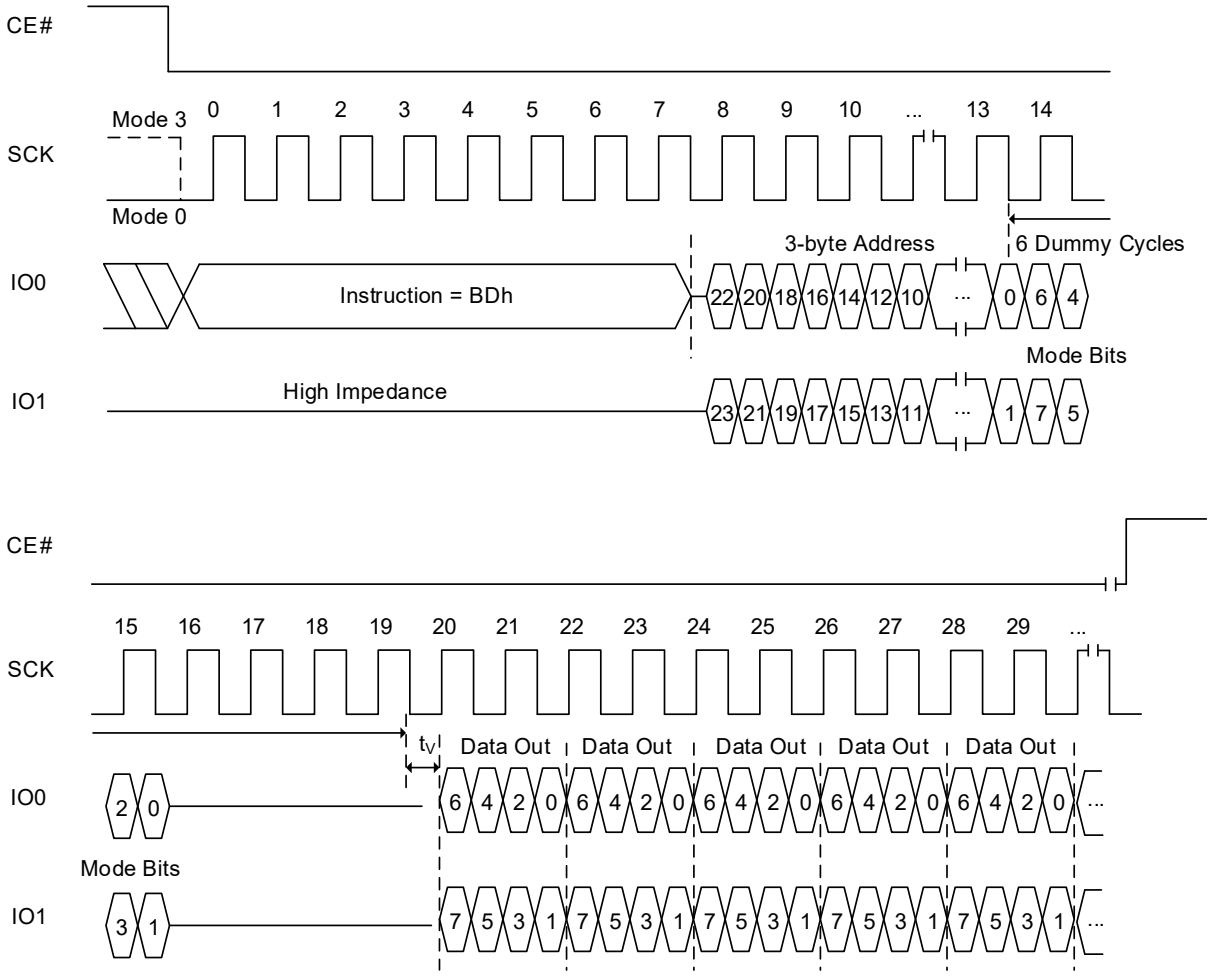
If mode bits=XX10XXXXb (where X is don't care) is input for the mode bits during dummy cycles, the device will enter "continuous read mode", which enables subsequent FRDDTR execution without command cycles.

When the mode bits are different from XX10XXXXb (where X is don't care), the device exits the "continuous read mode". After finishing the read operation, device becomes ready to receive a new command.

If the FRDDTR command is issued while a Program/Erase/Write Status Register cycle is in progress (WIP=1), the command will be rejected without any effect on the current cycle.

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Figure 8.57 **FRDDTR Sequence (with command decode cycles)**

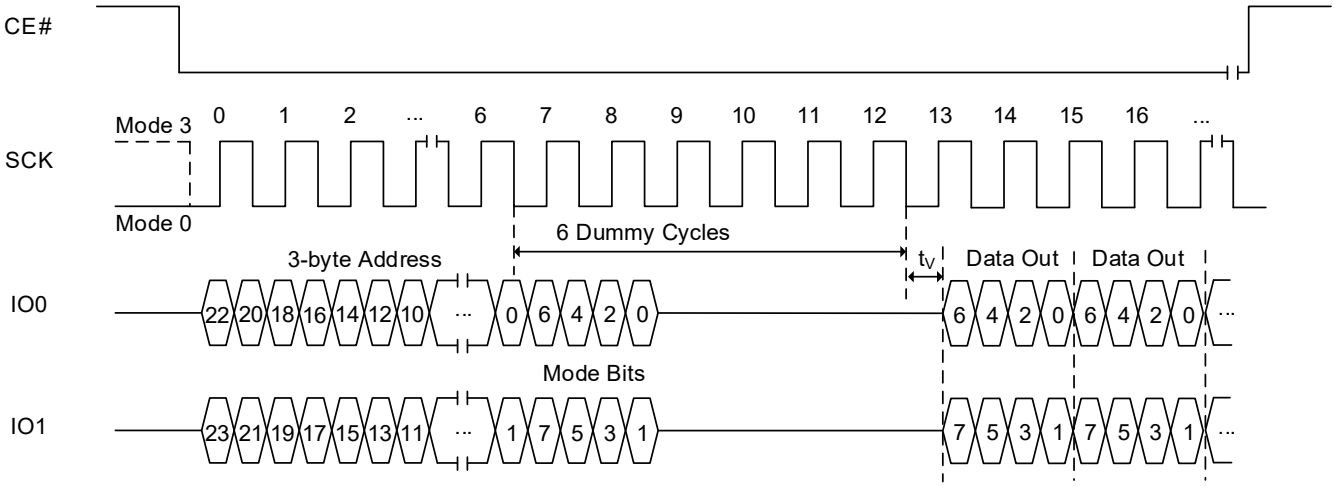


Notes:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

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Figure 8.58 **FRDDTR 2X read Sequence (without command decode cycles)**



Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

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8.35 FAST READ QUAD I/O DTR MODE OPERATION IN SPI MODE (FRQDTR, EDH)

The FRQDTR command enables Double Transfer Rate throughput on quad I/O of the device in read mode.
A Quad Enable (QE) bit of Status Register must be set to "1" before sending the Fast Read Quad I/O command.

The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCK at a maximum frequency f_{Q2}. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at the rising edge of clock, the other four bits at the falling edge of clock.

The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out with a single FRQDTR command. The address counter rolls over to 0 when the highest address is reached. Once writing FRQDTR command, the following address/dummy/data out will perform as 8-bit instead of previous 1-bit.

The sequence of issuing FRQDTR command is: CE# goes low → Sending FRQDTR command (1-bit per clock) → 24-bit address interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → 8 dummy cycles→ Data out interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → End FRQDTR operation by driving CE# high at any time during data out.

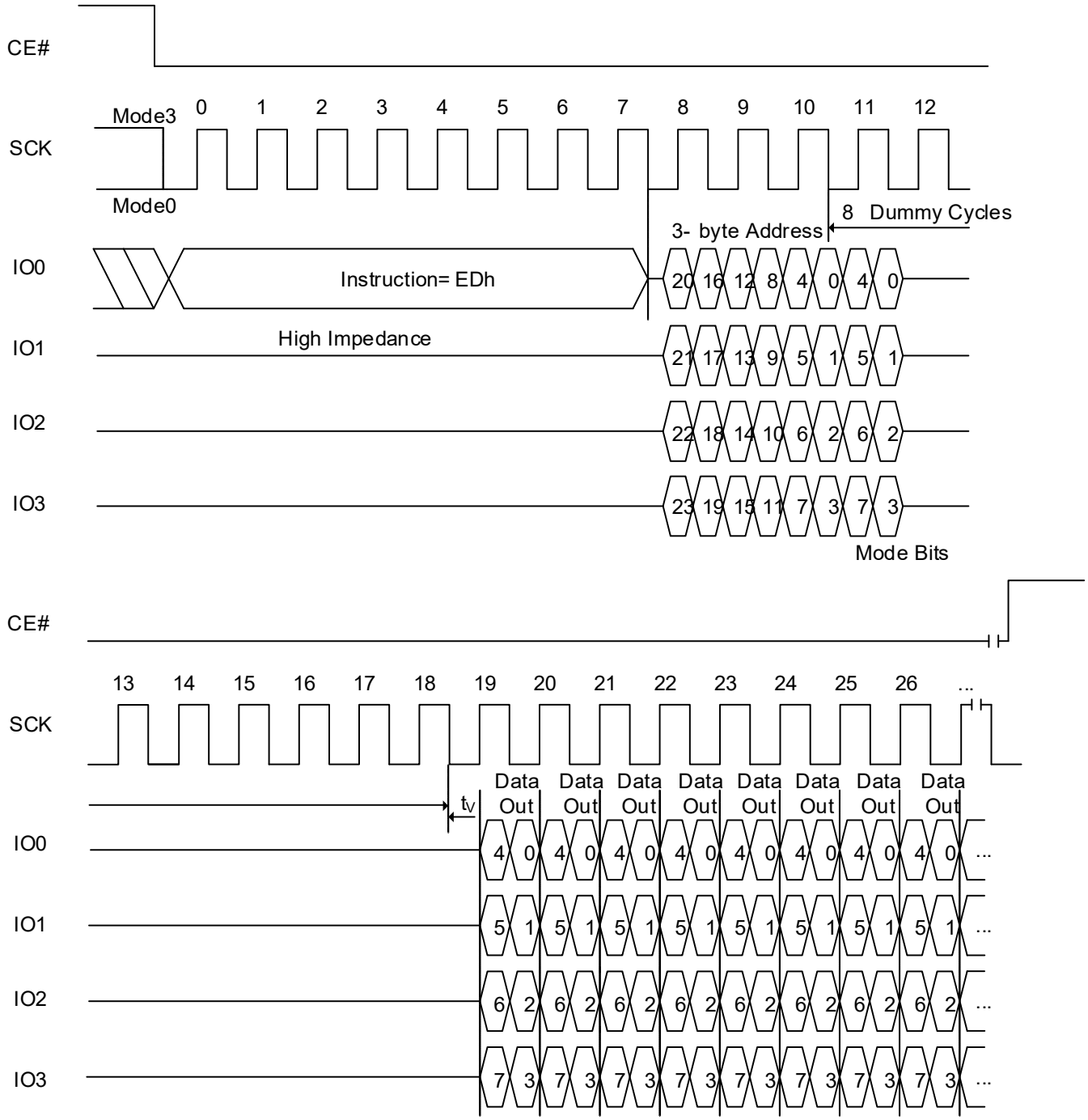
If mode bits=XX10XXXXb (where X is don't care) is input for the mode bits during dummy cycles, the device will enter "continuous read mode", which enables subsequent FRDDTR execution without command cycles.

When the mode bits are different from XX10XXXXb (where X is don't care), the device exits the "continuous read mode". After finishing the read operation, device becomes ready to receive a new command.

If the FRQDTR command is issued while a Program/Erase/Write Status Register cycle is in progress (WIP=1), the command will be rejected without any effect on the current cycle.

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Figure 8.59 **FRQDTR Sequence (with command decode cycles)**

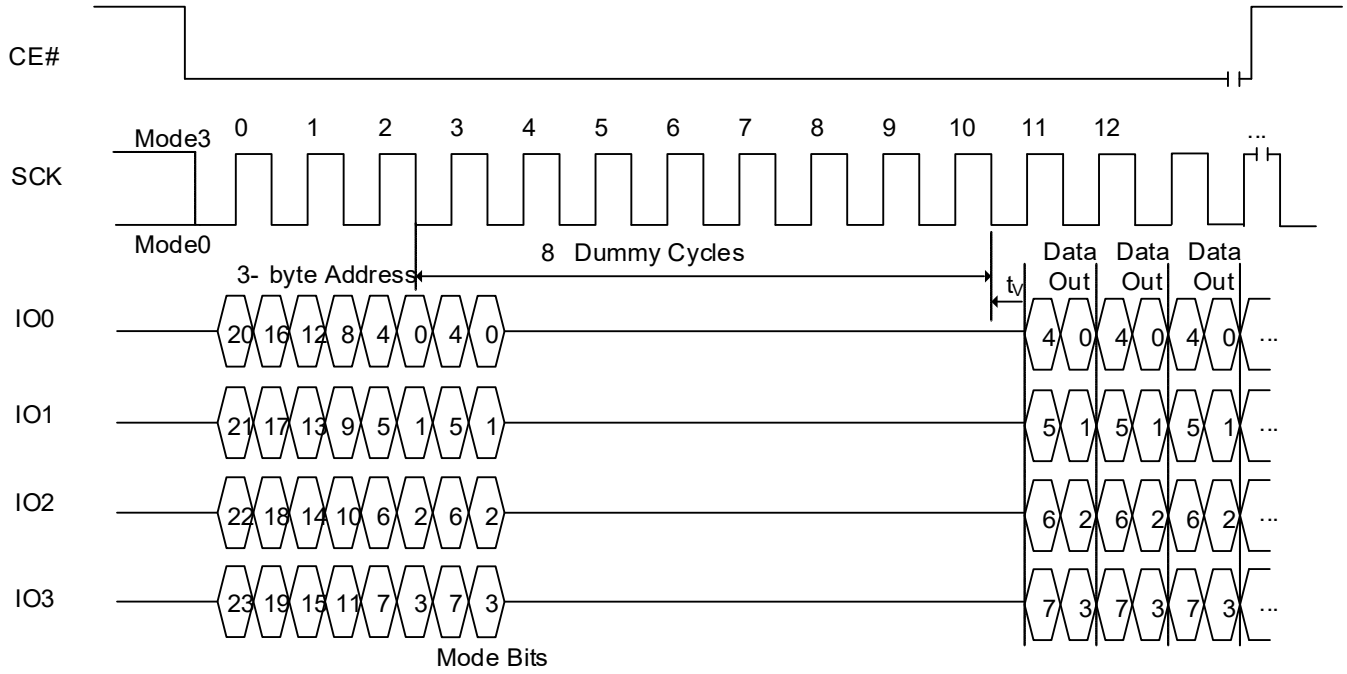


Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

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Figure 8.60 **FRQDTR Sequence continuous read mode (without command decode cycles)**



Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation.**

Fast Read Quad I/O DTR with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EDh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EDh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CE# be driven high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

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FAST READ QUAD IO DTR MODE OPERATION IN QPI MODE (FRQDTR, EDh)

The FRQDTR command in QPI mode utilizes all four IO lines to input the command code so that only two clocks are required, while the FRQDTR command requires that the byte-long command code is shifted into the device only via IO0 line in eight clocks. As a result, 6 command cycles will be reduced by the FRQDTR command in QPI mode. In addition, subsequent address and data out are shifted in/out via all four IO lines like the FRQDTR command. In fact, except for the command cycle, the FRQDTR operation in QPI mode is exactly same as the FRQDTR operation in SPI mode.

It is not required to set QE bit to "1".before Fast Read Quad I/O DTR command in QPI mode.

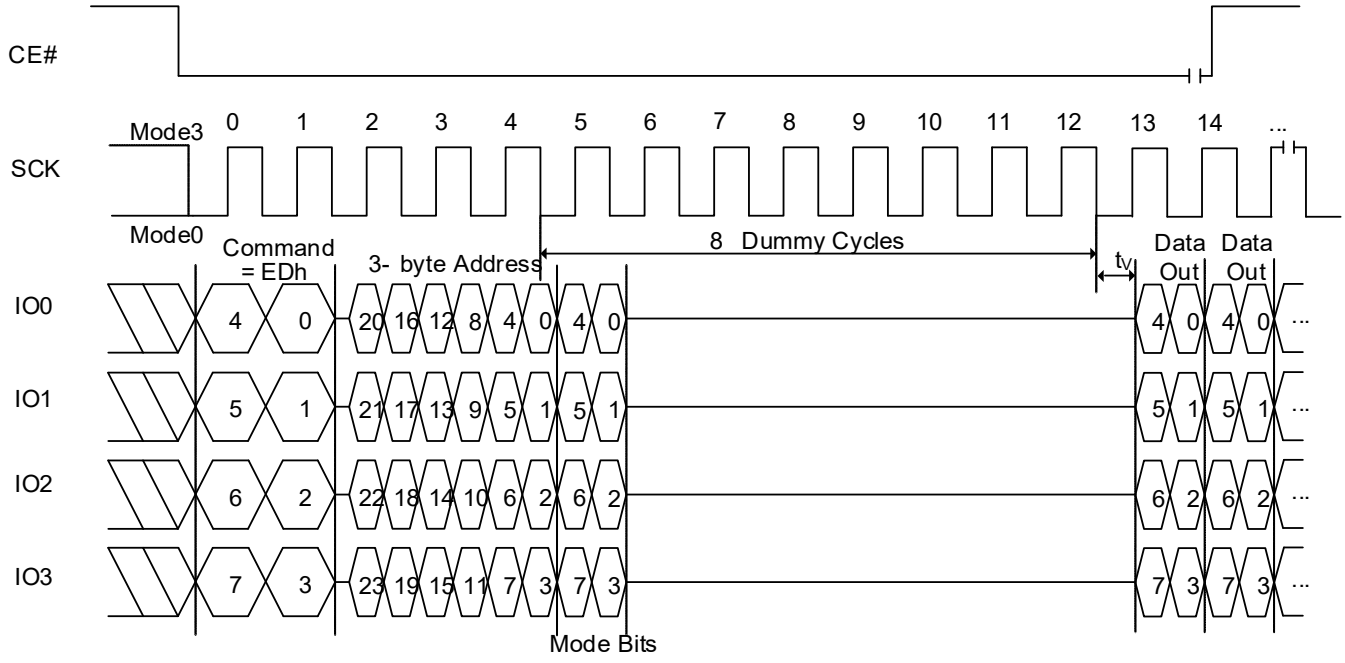
The sequence of issuing FRQDTR command in QPI mode is: CE# goes low → Sending FRQDTR command (4-bit per clock) → 24-bit address interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → 8 dummy cycles → Data out interleave on IO3, IO2, IO1 & IO0 (8-bit per clock) → End FRQDTR operation by driving CE# high at any time during data out.

If mode bits=XX10XXXXb (where X is don't care) is input for the mode bits during dummy cycles, the device will enter "continuous read mode", which enables subsequent FRDDTR execution without command cycles.

When the mode bits are different from XX10XXXXb (where X is don't care), the device exits the "continuous read mode". After finishing the read operation, device becomes ready to receive a new command.

If the FRQDTR command in QPI mode is issued while a Program/Erase/Write Status Register cycle is in progress (WIP=1), the command will be rejected without any effect on the current cycle.

Figure 8.61 **FRQDTR Sequence In QPI Mode (with command decode cycles)**



Note:

1. **If the mode bits=XX10XXb (M5 bit and M4 bit are 10b, other bits are don't care), it can execute the continuous read mode (without command). When mode bits are different from XX10XXb, the device exits the continuous read operation**.

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9. ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature	-65°C to +150°C
Input Voltage with Respect to Ground on All Pins	-0.6V to V_{CC} + 0.5V
All Output Voltage with Respect to Ground	-0.6V to V_{CC} + 0.5V
V_{CC}	-0.5V to +2.5V
Electrostatic Discharge Voltage (Human Body Model)(2)	-2000V to +2000V

Notes:
1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

9.2 OPERATING RANGE

Operating Temperature	Extended Grade E	-40°C to 105°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Power Supply		1.65V (VMIN) –2.0V (VMAX); 1.8V (Typ)

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9.3 DC CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ(2)	Max	Units
I_{CC1}	V_{CC} Active Read current(3)	NORD Single at 66MHz		1.5	3.0	mA
		FRD Single at 80MHz		2.0	4.0	
		FRD Quad at 80MHz		3.0	6.0	
		FRD Quad at 104MHz		3.5	7.0	
		FRD Quad at 133MHz		4.5	9.0	
		FRD DTR Quad at 80MHz		3.5	7.0	
I_{CC2}	V_{CC} Program Current	CE# = V_{CC}		13	15	mA
I_{CC3}	V_{CC} WRSR Current	CE# = V_{CC}		13	15	
I_{CC4}	V_{CC} Erase Current (SER/BER32/BER64)	CE# = V_{CC}		13	15	
I_{CC5}	V_{CC} Erase Current (CE)	CE# = V_{CC}		13	15	
I_{SB1}	V_{CC} Standby Current CMOS	CE# = V_{CC}		15	35	µA
I_{SB2}	Deep power down current	CE# = V_{CC}		0.1	8	µA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}			±2	µA
I_{LO}	Output Leakage Current	V_{IN} = 0V to V_{CC}			±2	µA
V_{IL}(1)	Input Low Voltage		-0.5		$0.3V_{CC}$	V
V_{IH}(1)	Input High Voltage		$0.7V_{CC}$		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA			0.2	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2			V

Notes:

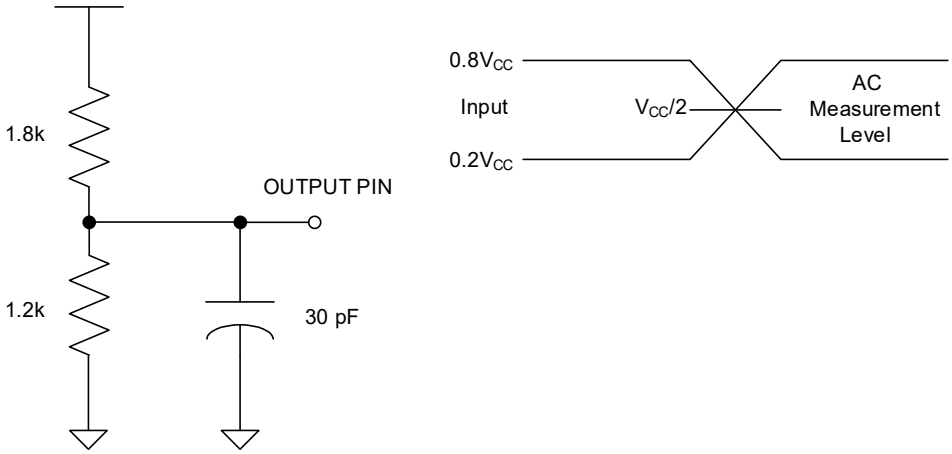
1. **Maximum DC voltage on input or I/O pins is VCC + 0.5V. During voltage transitions, input or I/O pins may overshoot VCC by + 1.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -1.0V for a period of time not to exceed 20ns.**
2. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ), TA=25°C.**
3. **Outputs are unconnected during reading data so that output switching current is not included.**

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9.4 AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Load Capacitance		30	pF
TR,TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
VREFI	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		V

Figure 9.1 Output test load & AC measurement I/O Waveform



9.5 PIN CAPACITANCE

(TA = 25°C, VCC=1.8V, 1MHz)

Symbol	Parameter	Test Condition	IS25WJ128F		Units
			Min	Max	
C_{IN}	Input Capacitance (CE#, SCK)	V_{IN} = 0V	-	6	pF
$C_{IN/OUT}$	Input/Output Capacitance (other pins)	$V_{IN/OUT}$ = 0V	-	8	pF

Notes:
1. These parameters are characterized and are not 100% tested.

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9.6 AC CHARACTERISTICS

Symbol	Parameter		Min	Typ(2)	Max	Units
f_{CT}	Clock Frequency except for fast read DTR and read (03h)		0		133	MHz
	Clock Frequency for fast read DTR: SPI DTR, Dual DTR, Dual I/O DTR, Quad I/O DTR and QPI DTR.		0		80	MHz
f_C	Clock Frequency for read (03h)		0		66	MHz
t_{CLCH}(1)	SCK Rise Time (peak to peak)		0.1			V/ns
t_{CHCL}(1)	SCK Fall Time (peak to peak)		0.1			V/ns
t_{CKH}	SCK High Time	For read (03h)	0.45 x 1/f_{Cmax}			ns
		For others	0.45 x 1/f_{CTmax}			
t_{CKL}	SCK Low Time	For read (03h)	0.45 x 1/f_{Cmax}			ns
		For others	0.45 x 1/f_{CTmax}			
t_{CEH}	CE# High Time		7			ns
t_{CS}	CE# Active Setup Time		5			ns
t_{CH}	CE# Active Hold Time		5			ns
t_{CHSL}	CE# Not Active Hold Time		2.7			ns
t_{SHCH}	CE# Not Active Setup Time		2.7			ns
t_{DS}	Data In Setup Time	STR	2			ns
		DTR	1.5			
t_{DH}	Data in Hold Time	STR	2			ns
		DTR	1.5			
t_V	Output Valid	CL = 10pF			4.8	ns
		CL = 15pF			6	
		CL = 30pF			7	
t_{OH}	Output Hold Time		1.2			ns
t_{DIS}(1)	Output Disable Time				6.0	ns
t_{WHSL}(3)	Write Protect Setup Time		20			ns
t_{SHWL}(3)	Write Protect Hold Time		100			ns
t_{HLCH}	HOLD Active Setup Time relative to SCK		5			ns
t_{CHHH}	HOLD Active Hold Time relative to SCK		5			ns
t_{HHCH}	HOLD Not Active Setup Time relative to SCK		5			ns
t_{CHHL}	HOLD Not Active Hold Time relative to SCK		5			ns
t_{LZ}(1)	HOLD to Output Low Z				6	ns
t_{HZ}(1)	HOLD to Output High Z				6	ns
t_{RES1}(1)	Release deep power down				5	µs
t_{DP}(1)	Deep power down				3	µs
t_W	Write Status Register time			2	15	ms
t_{SUS}	Suspend to read ready				20	µs
t_{RS}	Resume to next suspend			100		µs
t_{RST}	Reset recovery time				30	µs
t_{SRST}(1)	Software Reset recovery time				30	µs
t_{RESET}(1)	RESET# pin low pulse width		100			ns
t_{HWRST}(1)	Hardware Reset recovery time				30	µs

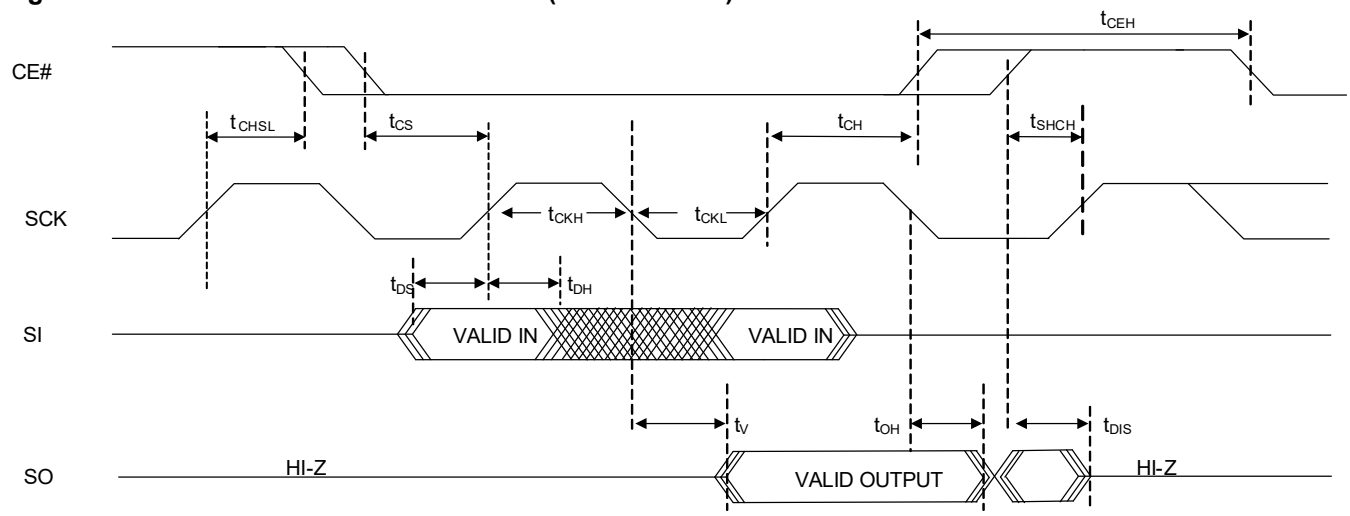
Downloaded from Arrow.com.

Notes:
1. These parameters are characterized and not 100% tested.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ), TA=25°C.
3. Only applicable as a constraint for a WRITE STATUS REGISTER command when SRP0 is set at 1.

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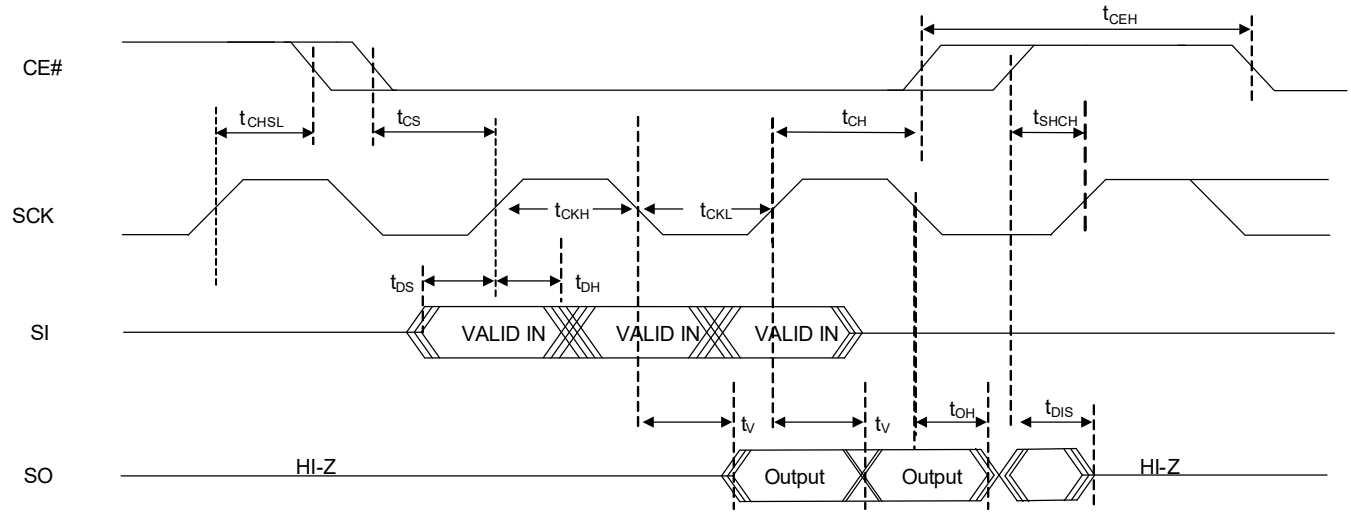
9.7 SERIAL INPUT/OUTPUT TIMING

Figure 9.2 SERIAL INPUT/OUTPUT TIMING (Normal Mode) (1)



Note1: For SPI Mode 0 (0, 0)

Figure 9.3 SERIAL INPUT/OUTPUT TIMING (DTR Mode) (1)



Note1: For SPI Mode 0 (0, 0)

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Figure 9.4 HOLD TIMING

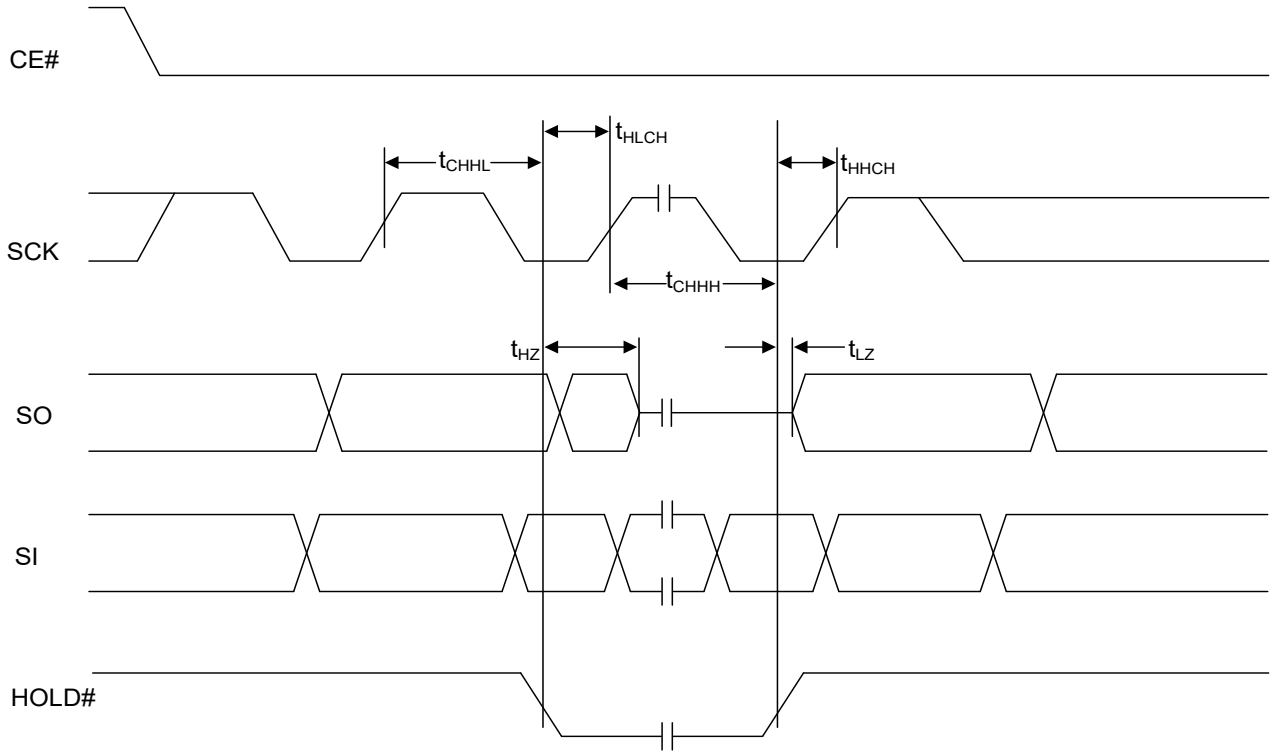
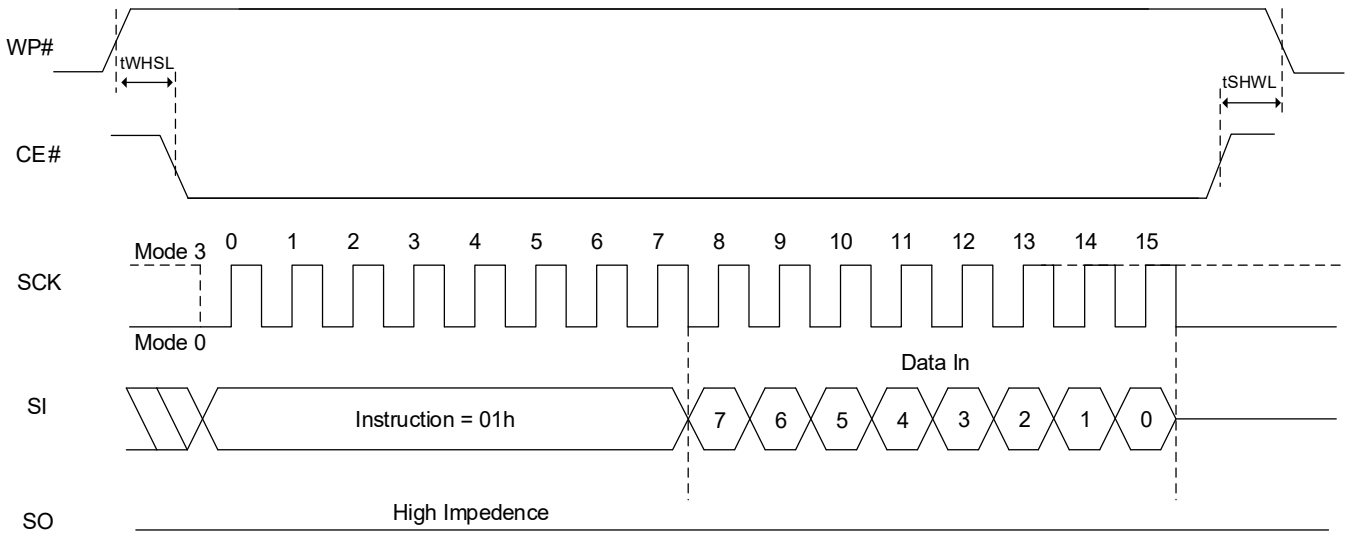


Figure 9.5 WRITE PROTECT SETUP AND HOLD TIMIMNG DURING WRITE STATUS REGISTER (SRWD=1)



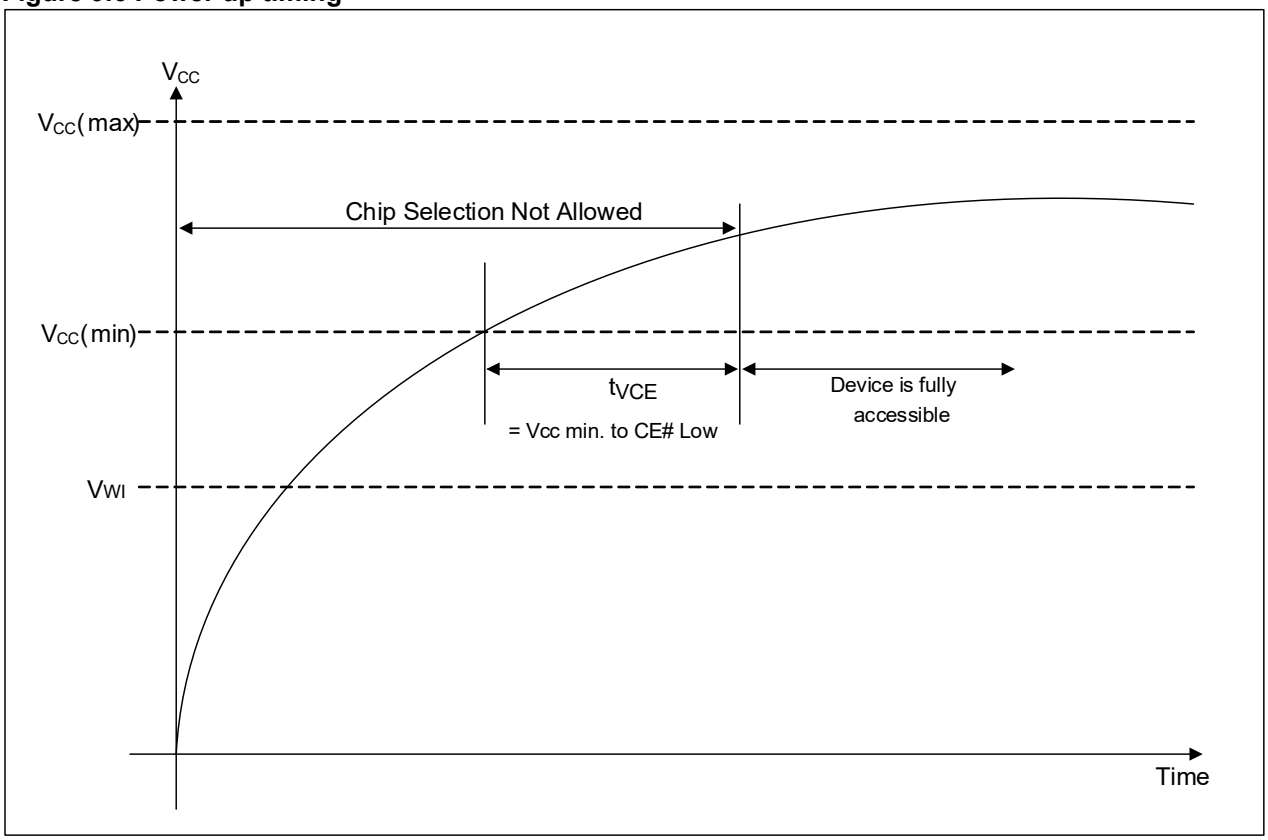
Note: WP# must be kept high until the embedded operation finish.

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9.8 POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level. (Adding a simple pull-up resistor on CE# is recommended.)

Figure 9.6 Power up timing



Symbol	Parameter	Min.	Max	Unit
tVCE(1)	Vcc(min) to CE# Low	100		us
V_{WI}(1)	Write Inhibit Voltage		1.4	V

Note: These parameters are characterized and not 100% tested.

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9.9 PROGRAM/ERASE PERFORMANCE

Parameter	Typ	Max	Unit
Sector Erase Time (4Kbyte)	90	300	ms
Block Erase Time (32Kbyte)	0.15	0.8	s
Block Erase Time (64Kbyte)	0.2	1.2	s
Chip Erase Time	32	80	s
Page Programming Time	0.4	2.4	ms
Byte Program (First Byte)	15	50	µs

Note: These parameters are characterized and not 100% tested.

9.10 RELIABILITY CHARACTERISTICS

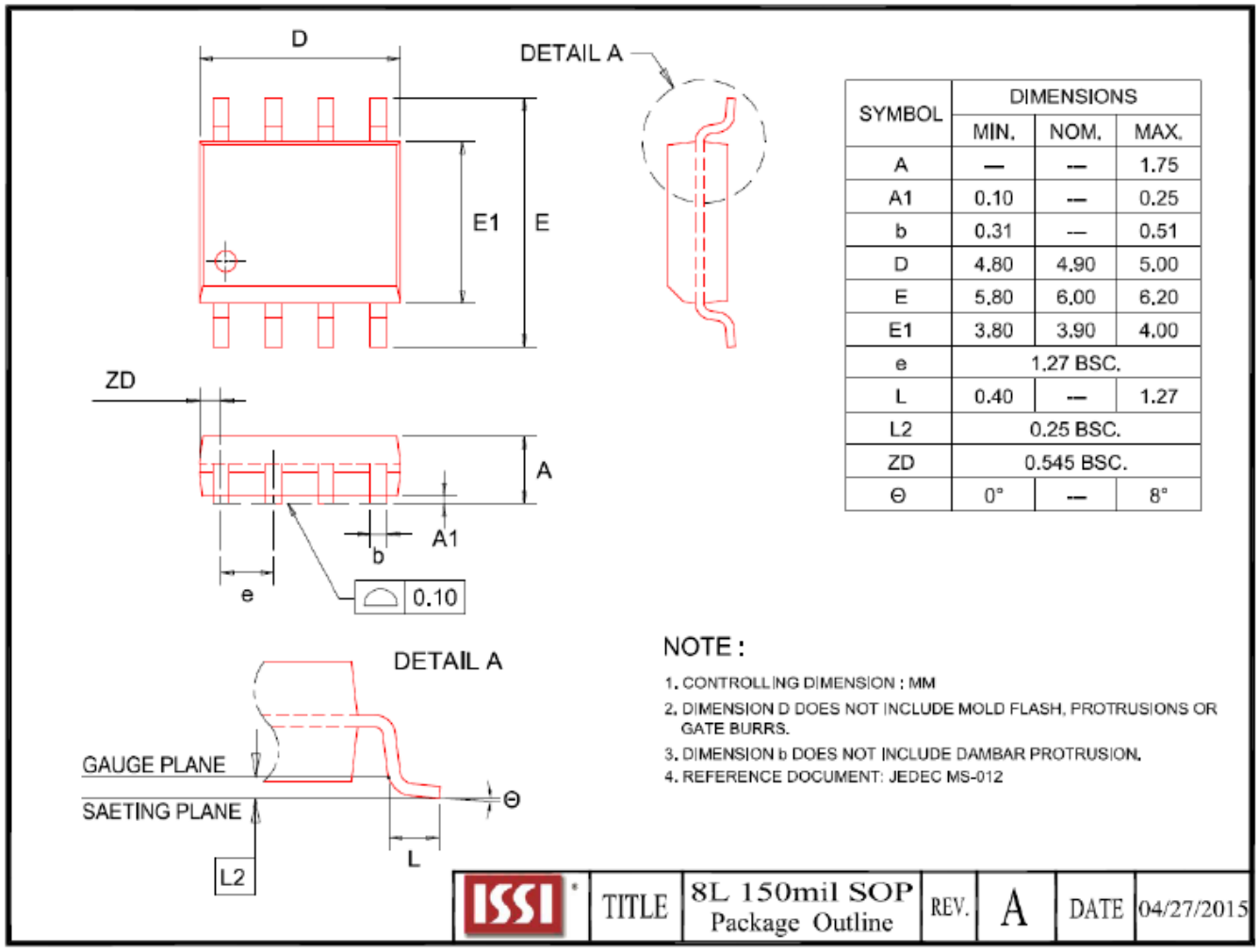
Parameter	Min	Max	Unit	Test Method
Endurance	100,000	-	Cycles	JEDEC Standard A117
Data Retention	20	-	Years	JEDEC Standard A117
Latch-Up	-100	+100	mA	JEDEC Standard 78

Note: These parameters are characterized and not 100% tested.

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10. PACKAGE TYPE INFORMATION

10.1 8-PIN JEDEC 150MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (N)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
b	0.31	—	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC.		
L	0.40	—	1.27
L2	0.25 BSC.		
ZD	0.545 BSC.		
Θ	0°	—	8°

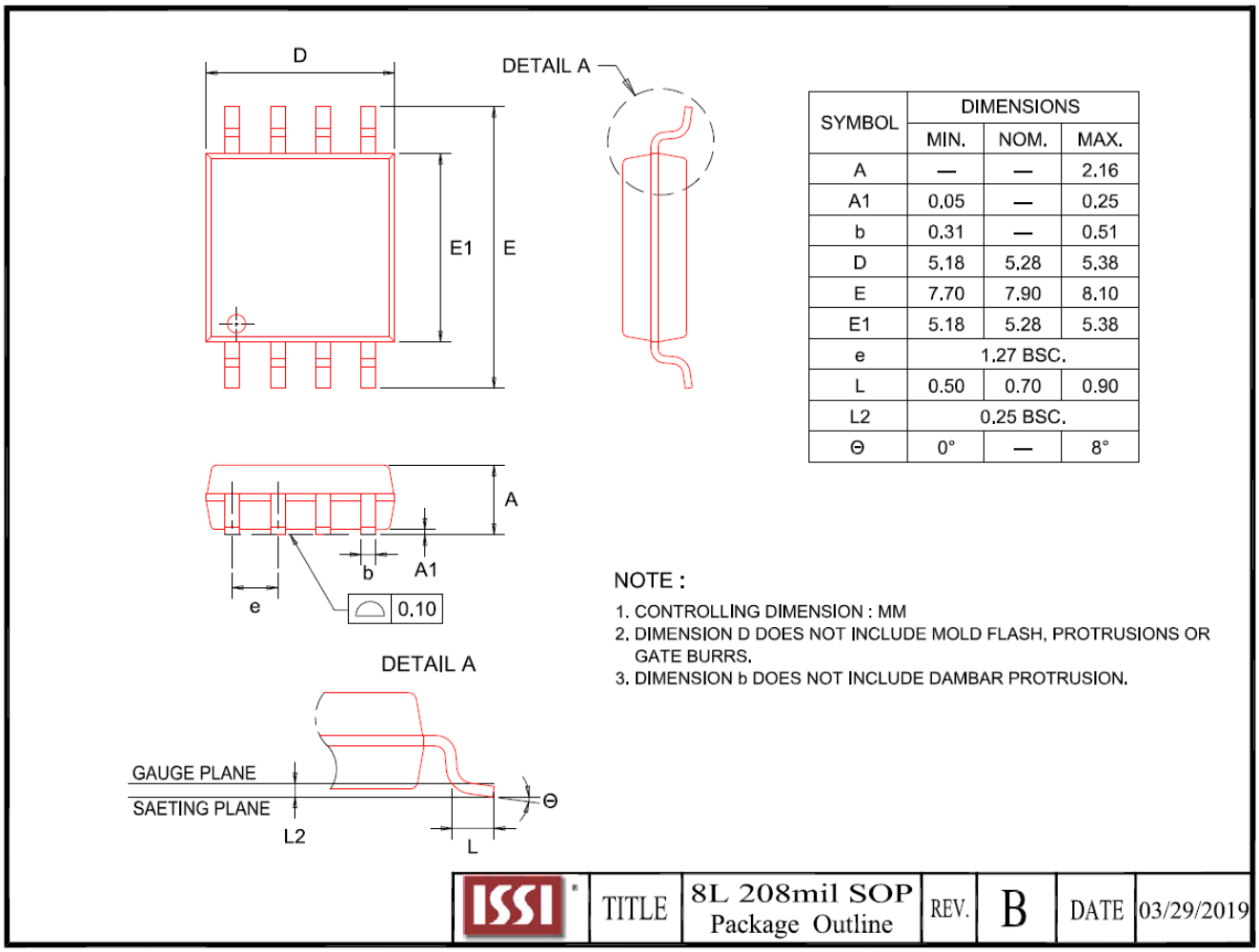
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012

TITLE	8L 150mil SOP Package Outline	REV.	A	DATE	04/27/2015

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10.2 8-PIN JEDEC 208MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (B)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.16
A1	0.05	—	0.25
b	0.31	—	0.51
D	5.18	5.28	5.38
E	7.70	7.90	8.10
E1	5.18	5.28	5.38
e	1.27 BSC.		
L	0.50	0.70	0.90
L2	0.25 BSC.		
Θ	0°	—	8°

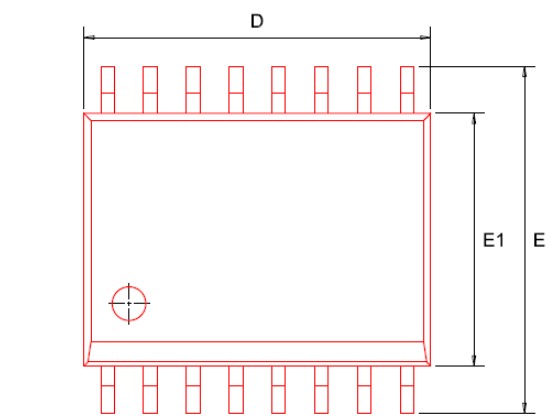
NOTE :

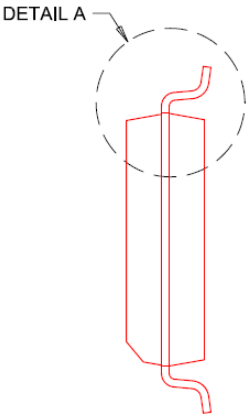
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

ISSI	TITLE	8L 208mil SOP Package Outline	REV.	B	DATE	03/29/2019

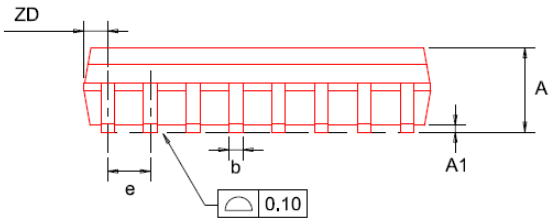
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10.3 16-LEAD PLASTIC SMALL OUTLINE PACKAGE (300 MILS BODY WIDTH) (M)



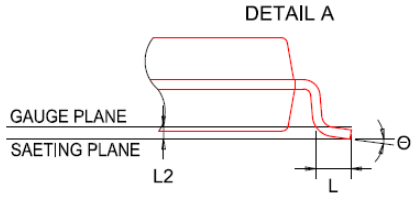


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
b	0.31	—	0.51
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC.		
L	0.38	0.81	1.27
L2	0.25 BSC.		
ZD	0.705 BSC.		
Θ	0°	—	8°



NOTE :

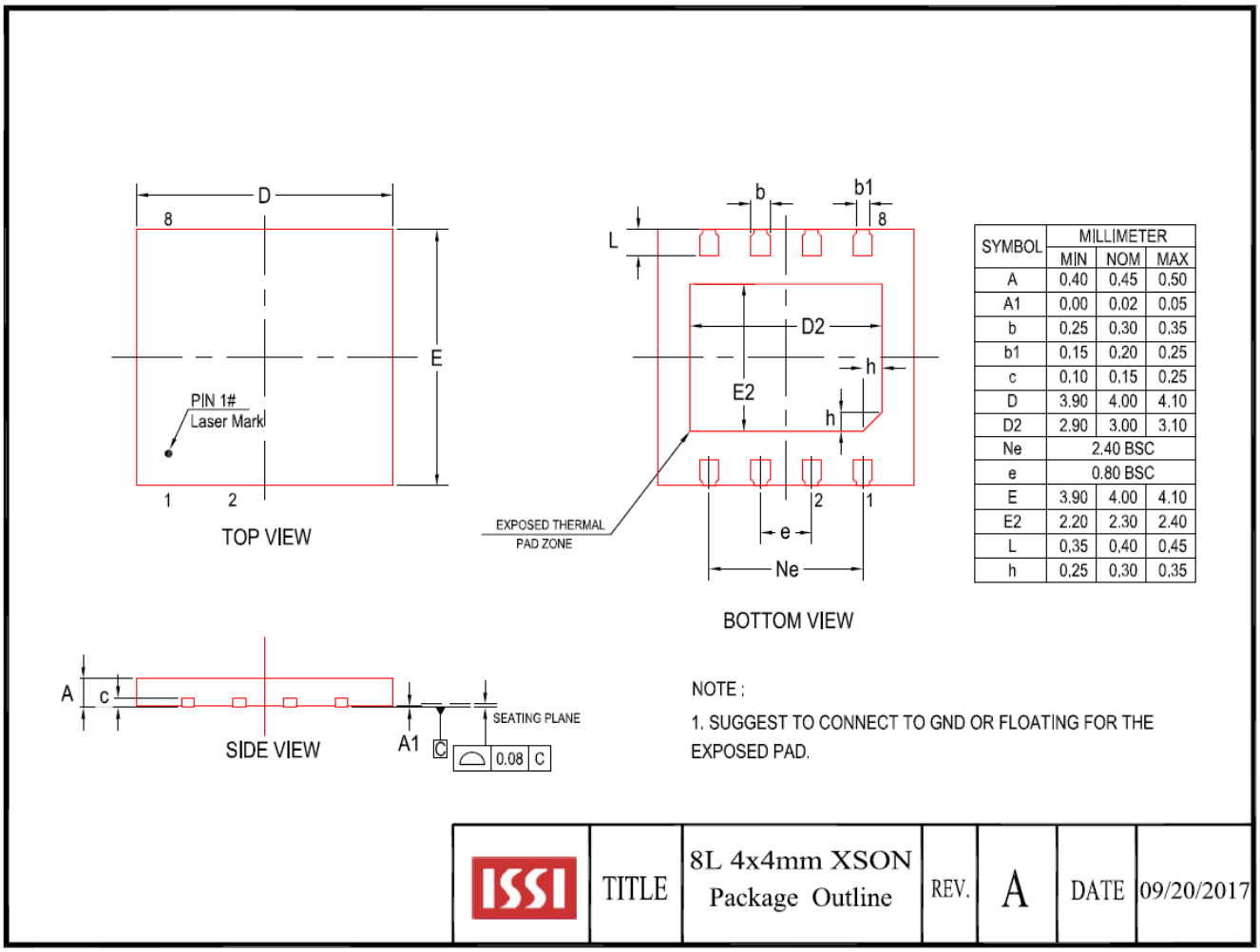
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.



ISSI	TITLE	16L 300mil SOP Package Outline	REV.	A	DATE	06/26/2015

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10.4 8-CONTACT EXTREMELY-THIN SMALL OUTLINE NO-LEAD (XSON) PACKAGE 4X4MM (E)



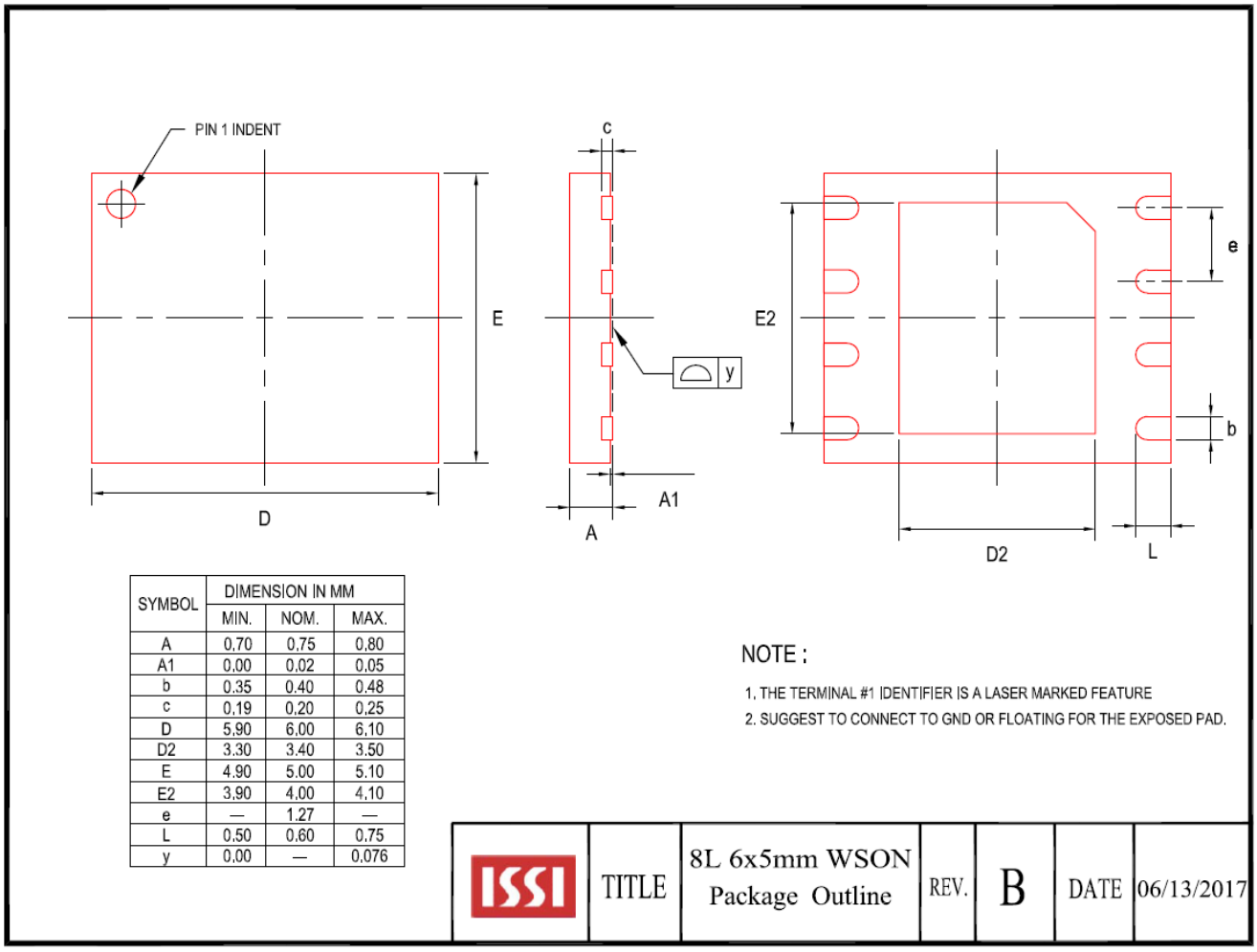
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
c	0.10	0.15	0.25
D	3.90	4.00	4.10
D2	2.90	3.00	3.10
Ne	2.40 BSC		
e	0.80 BSC		
E	3.90	4.00	4.10
E2	2.20	2.30	2.40
L	0.35	0.40	0.45
h	0.25	0.30	0.35

Note:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.

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10.5 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 6X5MM (K)



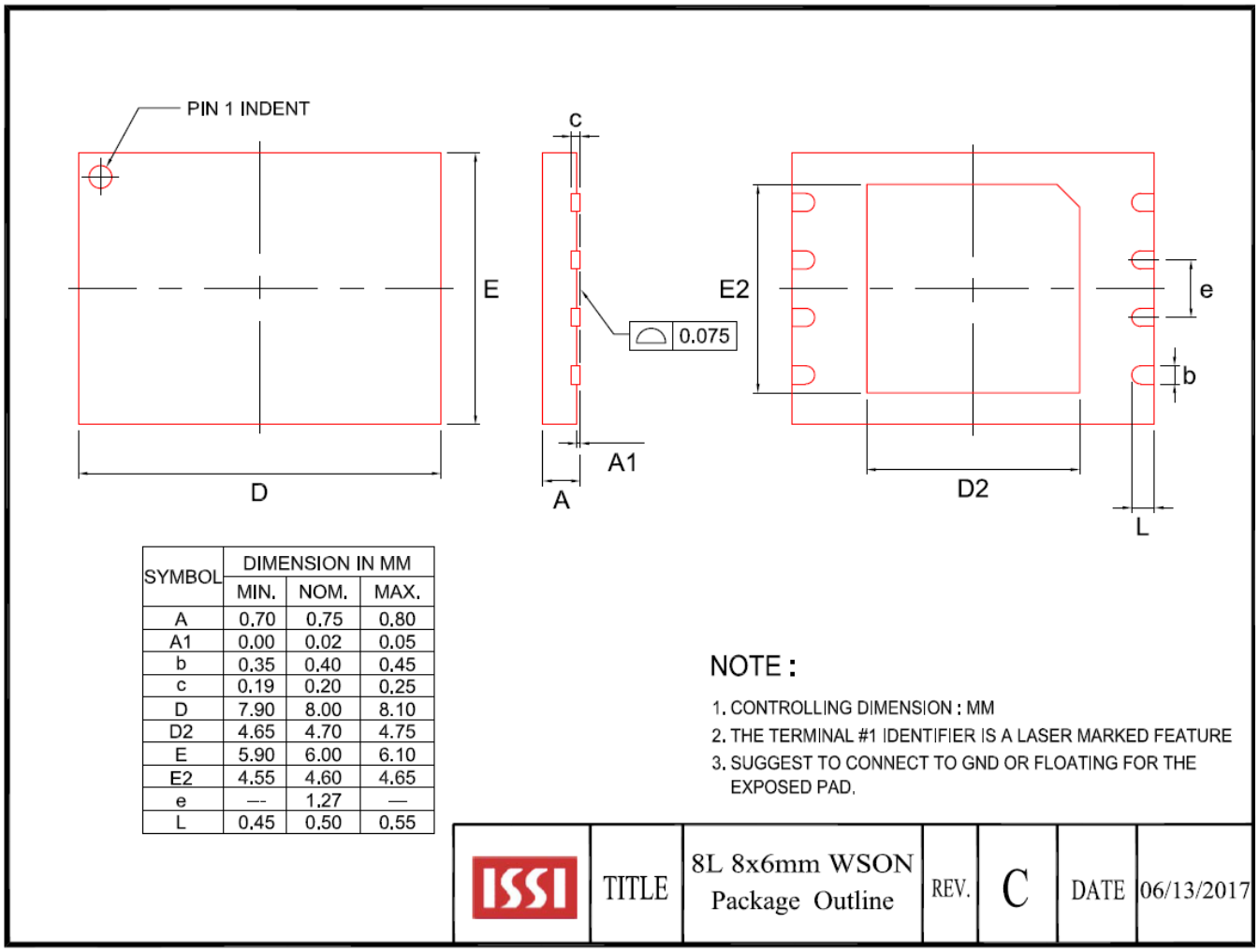
SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.48
c	0.19	0.20	0.25
D	5.90	6.00	6.10
D2	3.30	3.40	3.50
E	4.90	5.00	5.10
E2	3.90	4.00	4.10
e	—	1.27	—
L	0.50	0.60	0.75
y	0.00	—	0.076

Note:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.

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10.6 8-CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 8X6MM (L)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
c	0.19	0.20	0.25
D	7.90	8.00	8.10
D2	4.65	4.70	4.75
E	5.90	6.00	6.10
E2	4.55	4.60	4.65
e	---	1.27	---
L	0.45	0.50	0.55

NOTE :

1. CONTROLLING DIMENSION : MM
2. THE TERMINAL #1 IDENTIFIER IS A LASER MARKED FEATURE
3. SUGGEST TO CONNECT TO GND OR FLOATING FOR THE EXPOSED PAD.

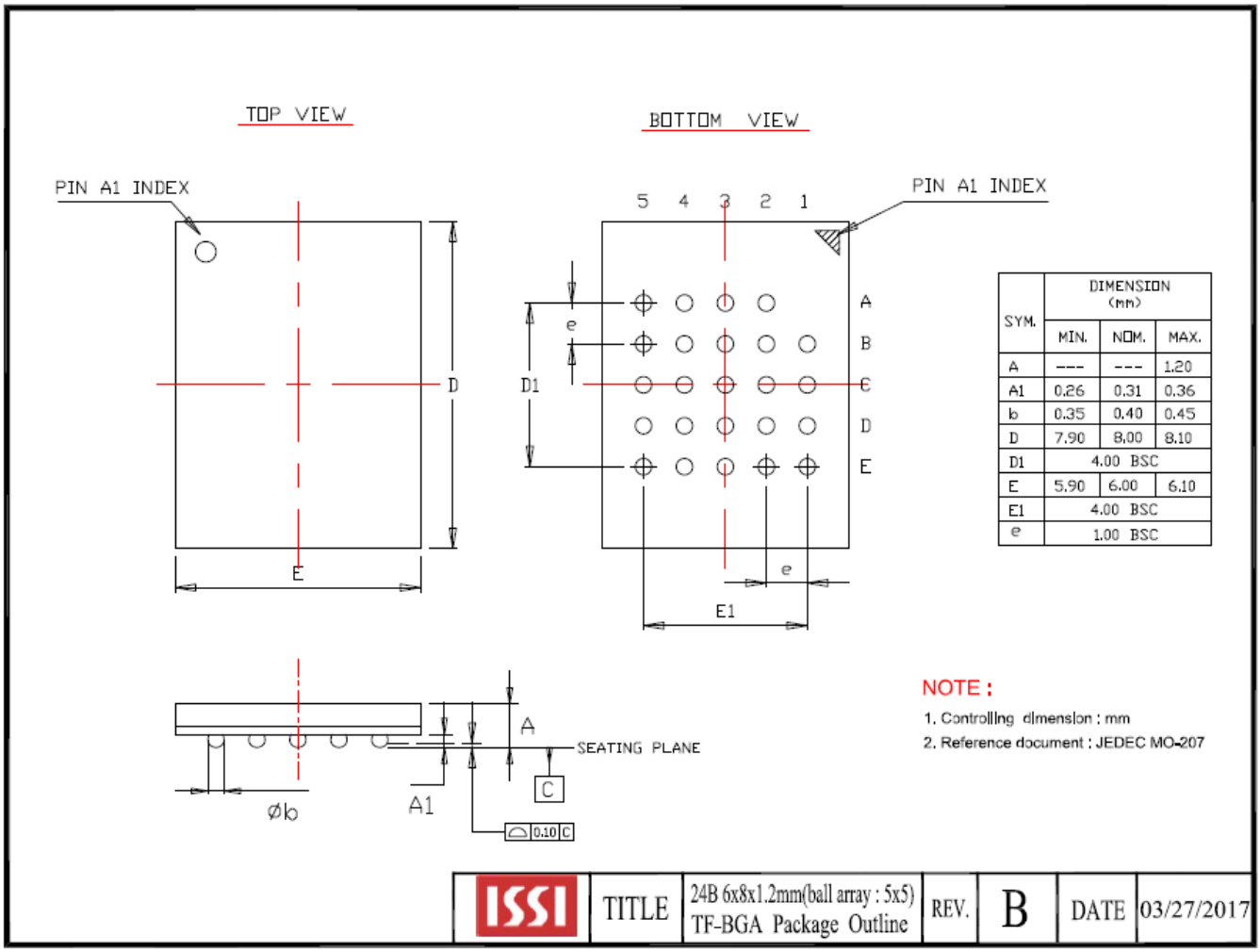
	TITLE	8L 8x6mm WSON Package Outline	REV.	C	DATE	06/13/2017

Note:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XSON package handling precautions) for assembly guidelines.

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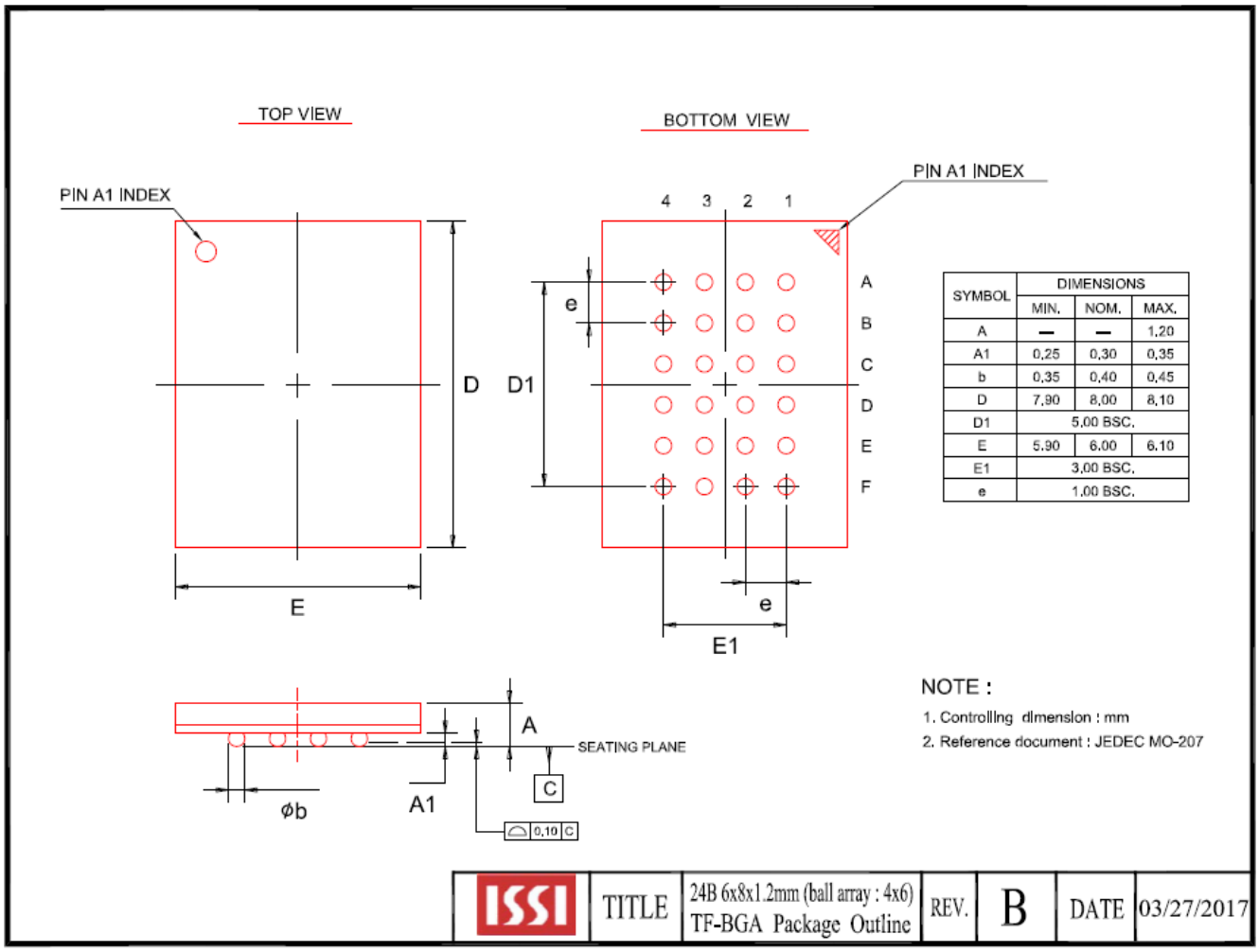
10.7 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 BALL ARRAY (H)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

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10.8 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 4X6 BALL ARRAY (G)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.25	0.30	0.35
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1		5.00 BSC.	
E	5.90	6.00	6.10
E1		3.00 BSC.	
e		1.00 BSC.	

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11. ORDERING INFORMATION - Valid Part Numbers



PACKING
TR = Tape and Reel
TY = Tray
Blank = Bulk

TEMPERATURE RANGE
E=Industrial (-40°C to +105°C)
A2=Automotive (-40°C to +105°C)

PACKAGING CONTENT
L = Green Package **(**RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type
N = 8-pin SOIC 150mil (Call Factory)
B = 8-pin SOIC 208mil
E = 8-contact XSON 4x4mm
K = 8-contact WSON 6x5mm
L = 8-contact WSON 8x6mm
M = 16-pin SOIC 300mil (Call Factory)
H = 24-ball TFBGA 5x5 ball array
W = KGD (Call Factory)

Option
J = Standard
R = Dedicated RESET# for 16-pin SOIC/24-ball BGA

Die Revision
F = Revision F

Density
128 = 128 Megabit

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
25WJ = FLASH, 1.65V ~ 2.0V, Volatile & Non-Volatile Status Register

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Density, Voltage	Frequency (MHz)	Order Part Number	Package
128Mb, 1.8V	STR 133, DTR 80	IS25WJ128F-JELE	8-contact XSON 4x4mm
		IS25WJ128F-JKLE	8-contact WSON 6x5mm
		IS25WJ128F-JLLE	8-contact WSON 8x6mm
		IS25WJ128F-JBLE	8-pin SOIC 208mil
		IS25WJ128F-RHLE	24-ball TFBGA 6x8mm 5x5 ball array
		IS25WJ128F-JELA2	8-contact XSON 4x4mm
		IS25WJ128F-JKLA2	8-contact WSON 6x5mm
		IS25WJ128F-JLLA2	8-contact WSON 8x6mm
		IS25WJ128F-JBLA2	8-pin SOIC 208mil
		IS25WJ128F-RHLA2	24-ball TFBGA 6x8mm 5x5 ball array

Note:
1. A2: Meets AEC-Q100 requirements with PPAP
Temp Grades: E= -40 to 105°C, A2= -40 to 105°C

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