MP2724

2.2A, Single-Cell, I²C-Controlled Buck Charger with USB Type-C Sink Mode and 15mA Termination Current

DESCRIPTION

The MP2724 is a highly integrated, 2.2A, switch-mode battery management device for single-cell Li-ion or Li-polymer batteries. The narrow-voltage DC (NVDC) power management structure provides a low-impedance power path that optimizes charging efficiency, reduces battery charging time, and extends battery life during discharging.

The MP2724 supports USB Type-C sink mode to detect the current capability of a USB Type-C adapter. Its input source type identification algorithm also supports USB Battery Charging Specification 1.2 (BC1.2) and non-standard adapter detection.

The I^2C interface offers complete operating control, including charging parameter configurations and status/interrupt monitoring.

The MP2724 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The MP2724 is available in a QFN-22 (2.5mmx3.5mm) package.

FEATURES

- 2.2A Switching Charger with NVDC Power Path Management
- Integrated CC Controller for USB Type-C Sink Mode
- Supports USB BC1.2 and Non-Standard Adapters
- 26V Sustainable Input Voltage (V_{IN})
- Configurable 40mA to 2.2A Charge Current (I_{CC}) and 100mA to 3.2A Input Current Limit (I_{IN_LIM}) via the I^2C
- Minimum V_{IN} Loop for Maximum Adapter Power Tracking
- Comprehensive Safety Features:
    - Fully Customizable JEITA Profile
    - Additional Negative Temperature Coefficient (NTC) Thermistor Input
    - Configurable Die Temperature Regulation from 60°C to 120°C

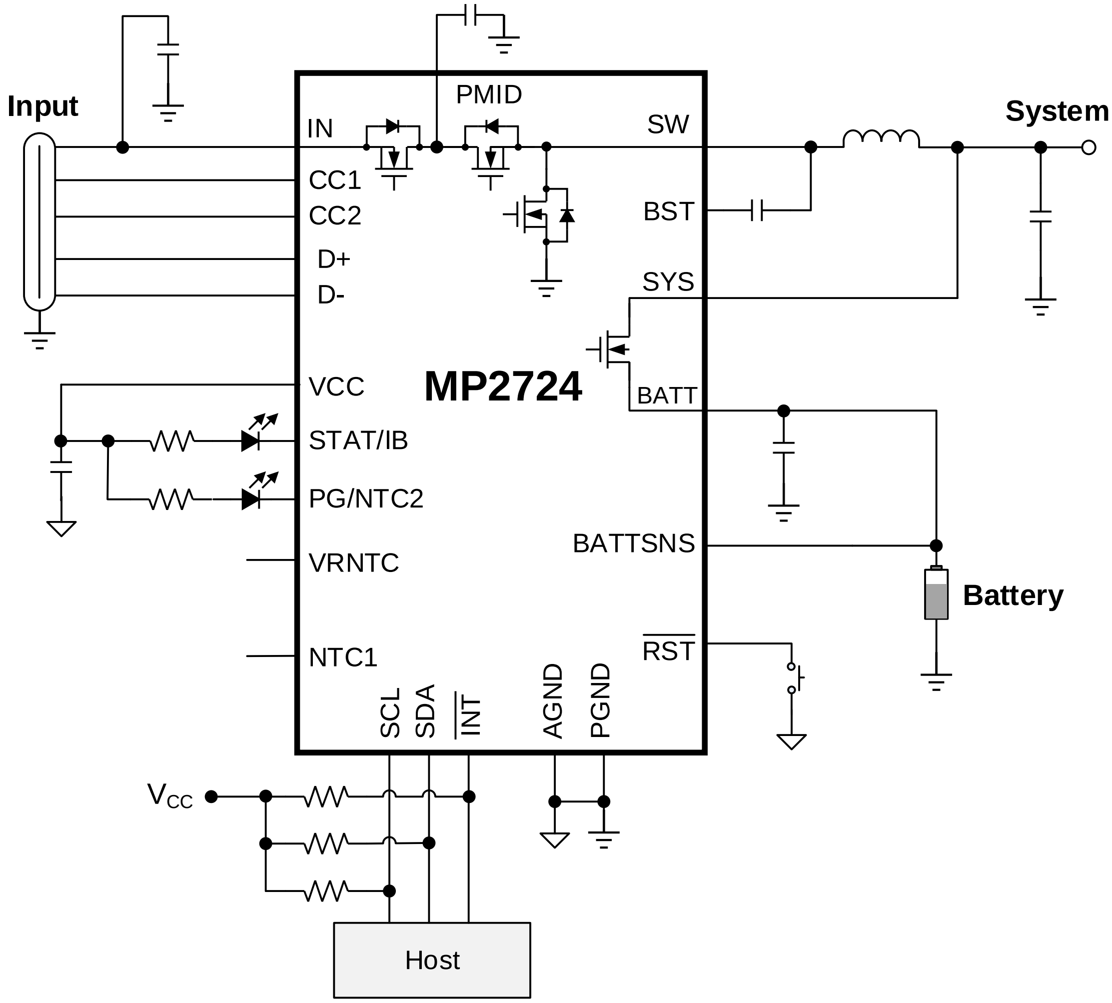
FEATURES *(continued)*

    - Complete Charge and Pre-Charge Safety Timers
    - Watchdog Safety Timer
    - Lockable Registers for Charging Parameters
- Configurable 750kHz to 1.5MHz Switching Frequency (f_{SW})
- Integrated 30mΩ Low-$R_{DS(ON)}$ Battery MOSFET with Shipping and Reset Modes
- Ultra-Low 8.5µA Battery Discharge Current in Shipping Mode
- Down to 15mA Termination Current Settings for Wearable Applications
- I^2C Port for Flexible System Parameter Setting and Status Reporting
- Configurable Boost Converter for Source Mode and USB On-The-Go (OTG):
    - Configurable Output Current Limit Loop Up to 3A
    - Output Over-Current Protection (OCP)
    - Configurable 5V to 5.35V Output Voltage
- Accuracy:
    - ±0.5% Battery Regulation Voltage (V_{BATT_REG})
    - ±5% I_{CC}
    - ±5% I_{IN_LIM}
    - Remote Battery Sensing for Fast Charge
    - ±2% Output Regulation in Boost Mode
- Available in a Small QFN-22 (2.5mmx3.5mm) Package

APPLICATIONS

- General ≤15W USB Applications
- Bluetooth Headphones
- Bluetooth Speakers
- Point-of-Sale (POS) Terminals
- Portable Cameras

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2724GRH-xxxx**	QFN-22 (2.5mmx3.5mm)	*See Below*	1
EVKT-MP2724	Evaluation Kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP2724GRH-xxxx-Z).

** “xxxx” is the register setting option. The factory default code is “0000.” This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING

CDH
YWW
LLL

CDH: Product code of MP2724GRH-xxxx
Y: Year code
WW: Week code
LLL: Lot number

EVALUATION KIT EVKT-MP2724

EVKT-MP2724 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2724-RH-00A	MP2724 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB-to-I²C communication interface device, one USB cable, and one ribbon cable	1
3	Online resources	Includes the datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

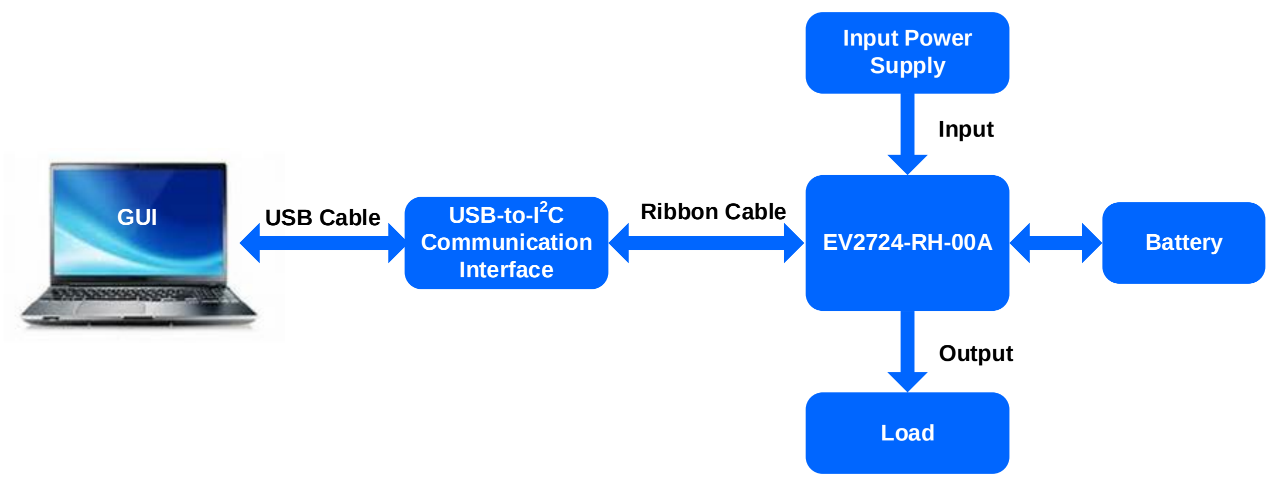
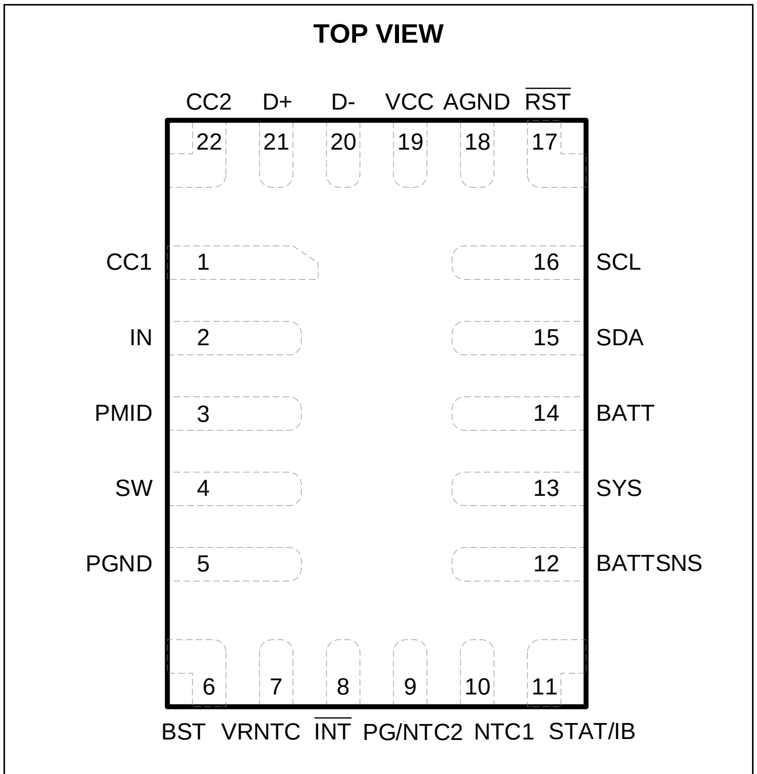


Figure 1: EVKT-MP2724 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-22 (2.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Type (1)	Description
2	IN	P	**Power input.** Connect a 1µF ceramic capacitor from the IN pin to PGND.
3	PMID	P	**Decoupling node for the power stage.** Bypass the PMID pin with a minimum 10µF ceramic capacitor connected from PMID to PGND, and placed as close to the IC as possible with the shortest possible route.
4	SW	P	**Switching node.** Connect the SW pin to the inductor.
6	BST	P	**Bootstrap power.** Connect a 22nF capacitor between the BST and SW pins to form a floating supply for the high-side MOSFET (HS-FET) driver.
13	SYS	P	**System power output.** Connect a minimum 20µF ceramic capacitor from the SYS pin to PGND.
14	BATT	P	**Battery positive terminal.** The internal narrow-voltage DC (NVDC) battery MOSFET is connected between the SYS and BATT pins. Place a minimum 20µF ceramic capacitor from BATT to PGND.
5	PGND	P	**Power ground.** Short the PGND pin to AGND on the PCB.
18	AGND	P	**Analog ground.** Short the AGND pin to PGND on the PCB.
19	VCC	P	**Internal circuit power supply.** Connect a 4.7µF ceramic capacitor from the VCC pin to AGND, placed as close to the IC as possible.
12	BATTSNS	AI	**Battery voltage-sense pin for battery voltage regulation.** Connect the BATTSNS pin as close as possible to the battery pack's positive terminal.
8	$\overline{\text{INT}}$	DO	**Open-drain interrupt output.** This pin generates an active low 256µs pulse when the IC has a status or fault report. Pull this pin up to VCC or another logic rail with a 10kΩ resistor.
16	SCL	DI	**I2C interface clock.** Pull the SCL pin up to VCC or another logic rail with a 10kΩ resistor.
15	SDA	DIO	**I2C interface data.** Pull the SDA pin up to VCC or another logic rail with a 10kΩ resistor.
1	CC1	AI	**USB Type-C CC1 pin.**
22	CC2	AI	**USB Type-C CC2 pin.**
21	D+	AIO	**Positive line of the USB data line pair.** USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
20	D-	AIO	**Negative line of the USB data line pair.** USB charger type detection is based on BC1.2. Non-standard adapter detection can also be implemented.
17	$\overline{\text{RST}}$	DI	**Battery MOSFET reset input.** During shipping mode, pull this pin to logic low for a set time ($t_{SHIPMODE}$) to wake up the IC from shipping mode. When the input voltage (V_{IN}) is not present, setting this pin to logic low for a set time (t_{RST}) resets the SYS power by turning the battery MOSFET off for a set time (t_{SYS_RST}). Then the battery MOSFET is re-enabled. This pin is internally pulled up by a 200kΩ resistor. Float this pin if it is not used.
7	VRNTC	AO	**Voltage output for powering up the NTC.** The VRNTC pin is powered up to the same voltage as VCC when the buck or boost converter operates.
10	NTC1	AI	**Temperature-sense input 1.** Connect the NTC1 pin to a negative temperature coefficient (NTC) thermistor. Connect a resistor divider from VRNTC to NTC1 to AGND. NTC1 supports a JEITA profile.
9	PG/NTC2	DO/AI	**Open-drain power good indicator.** Pull the PG/NTC2 pin up with a 10kΩ resistor. This pin is active low when the VIN_GD bit is 1, and it can be configured to act as temperature-sense input 2.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type [(1)]	Description
11	STAT/IB	DO/AO	**Charge status open-drain output or battery current indication.** This pin can be configured for the following functions: • Charge status (STAT): Pull up the STAT/IB pin with a 10kΩ resistor. STAT/IB goes low to indicate when charging is in progress; it goes high to indicate when charging is complete or not in progress. If a fault occurs, STAT/IB blinks at a frequency of 1Hz. • Battery current indication (IB): STAT/IB can source a current that is proportional to the battery's charge or discharge current. Connect a resistor from STAT/IB to AGND to obtain the battery current information.

Note:

1) AI = analog input, AO = analog output, AIO = analog input output, DI = digital input, DO = digital output, DIO = digital input output, P = power.

ABSOLUTE MAXIMUM RATINGS [(2)]

IN to PGND ....-0.3V to +26V
PMID to PGND ....-0.3V to +26V
SW to PGND..........-0.3V (-2V for 20ns) to +24V
PMID to IN ....-0.3V to +12V
BATT, BATTSNS, SYS to PGND.-0.3V to +6.5V
BST to SW…………..................-0.3V to +4V
VCC to AGND…………..................-0.3V to +4V
CC1, CC2 to AGND………….......-0.3V to +22V
All other pins to AGND.........-0.3V to VCC+0.3V
Continuous power dissipation (T_A = 25°C) [(3)] 2W
Junction temperature (T_J) ....150°C
Lead temperature (solder) ....260°C
Storage temperature .... -65°C to +150°C

ESD Ratings

Human body model (HBM) [(4)]................... 2000V
Charged-device model (CDM) [(5)] 250V

Recommended Operating Conditions [(7)]

Supply voltage (V_{IN}) ....3.9V to 6.3V
Input current (I_{IN}) ....Up to 3.2A
System current (I_{SYS})............................Up to 5A
Charge current (I_{CC}) ....Up to 2.2A
Discharge current (I_{DISCHG}) ....Up to 4A
Battery voltage (V_{BATT}) ....Up to 4.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance [(6)]	θ_{JA}	θ_{JC}	
QFN-22 (2.5mmx3.5mm)......	50	12....	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per ANSI/ESDA/JEDEC JS-001, all pins.
5) Per ANSI/ESDA/JEDEC JS-002, all pins.
6) Measured on a JESD51-7, 4-layer PCB.
7) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in shipping mode	I_{BATT_SHIP}	V_{BATT} = 4V, V_{IN} = 0V, BATTFET disabled, T_A = -40°C to +85°C		8.5	12	µA
Battery discharge current in idle mode	I_{BATT_IDLE}	V_{BATT} = 4V, V_{IN} = 0V, BATTFET enabled, USB Type-C is disabled, T_A = -40°C to +85°C		44	64	µA
Battery discharge current in sink mode	I_{BATT_SINK}	V_{BATT} = 4V, V_{IN} = 0V, BATTFET enabled, T_A = -40°C to 85°C		46	65	µA
USB suspend mode current	I_{IN_SUSP}	V_{IN} = 5V, EN_BUCK = 0		0.8		mA
Power-On/-Off						
Input operating range	V_{IN_OP}		3.9		6.3	V
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling, V_{BATT} = 0V	3.1	3.25	3.45	V
Input UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$	V_{IN} rising, V_{BATT} = 0V		250		mV
Input debounce time	t_{DEB}	V_{IN} debounce to set VIN_GD		15		ms
Hold-off timer	t_{HOLD}	VIN_GD = 1 to D+ and D- detection starts		250		ms
Input vs. battery voltage headroom threshold	V_{HDRM}	V_{IN} - V_{BATT}, V_{BATT} = 4V, V_{IN} rising	135	240	340	mV
		V_{IN} - V_{BATT}, V_{BATT} = 4V, V_{IN} falling	10	80	175	mV
Input over-voltage protection (OVP) threshold	V_{IN_OVP}	V_{IN} rising	6.1	6.3	6.55	V
Input OVP hysteresis	$V_{IN\_OVP\_HYS}$	V_{IN} falling		250		mV
V_{BATT} UVLO threshold	V_{BATT_UVLO}	V_{IN} = 0, V_{BATT} falling	2.4	2.5	2.6	V
V_{BATT} UVLO hysteresis	$V_{BATT\_UVLO\_HYS}$	V_{IN} = 0, V_{BATT} rising		400		mV
Power Path						
System regulation voltage	V_{SYS_REG}	$V_{BATT} < V_{SYS\_MIN}$, SYS_MIN = 100	3.7	3.82	3.94	V
Blocking FET on resistance	$R_{DS(ON)\_RBFET}$	T_A = 25°C		15		mΩ
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	T_A = 25°C		25		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	T_A = 25°C		25		mΩ
Battery MOSFET on resistance	$R_{DS(ON)\_BFET}$	T_A = 25°C		30		mΩ
Battery MOSFET forward voltage in supplement mode	V_{FWD}			30		mV
Charge (T_A = 0°C to 70°C)						
Charge voltage configuration range	V_{BATT_RANGE}		3.6		4.6	V
Charge voltage step	V_{BATT_STEP}			25		mV
Battery charge voltage regulation	V_{BATT_REG}	VBATT = 4.2V	4.179	4.2	4.221	V
		VBATT = 4.35V	4.328	4.35	4.372	V
Charge current regulation range	I_{CC_RANGE}		0		2200	mA

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge current step	I_{CC_STEP}			40		mA
Fast charge current	I_{CC}	ICC = 520mA, V_{BATT} = 3.8V	0.46	0.52	0.58	A
		ICC = 1000mA, V_{BATT} = 3.8V	0.95	1	1.05	A
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, VPRE = 3.2V	3.1	3.2	3.3	V
Pre-charge to fast charge threshold hysteresis		V_{BATT} falling, VPRE = 3.2V		250		mV
Pre-charge current	I_{PRE}	IPRE = 20mA, V_{BATT} = 2.5V, T_A = 25°C	13	20	28	mA
		IPRE = 20mA, V_{BATT} = 2.5V	10	20	32	mA
		IPRE = 40mA, V_{BATT} = 2.5V	31	40	50	mA
		IPRE = 120mA, V_{BATT} = 2.5V	102	120	142	mA
Charge termination current threshold	I_{TERM}	ITERM = 15mA, T_A = 25°C	10	15	22	mA
		ITERM = 15mA	9	15	23	mA
		ITERM = 30mA	21	30	41	mA
		ITERM = 135mA	102	135	168	mA
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2	2.1	V
Trickle charge to pre-charge threshold hysteresis		V_{BATT} falling		200		mV
Trickle charge current	I_{TC}	ITRICKLE = 16mA, V_{BATT} = 1V, T_A = 25°C	10	16	25	mA
		ITRICKLE = 16mA, V_{BATT} = 1V	8.5	16	26.5	mA
		ITRICKLE = 32mA, V_{BATT} = 1V	23	32	43	mA
		ITRICKLE = 64mA, V_{BATT} = 1V	44	64	88	mA
Automatic recharge battery voltage threshold	V_{RECH}	V_{BATT} falling, VRECHG = 100mV	45	90	130	mV
		V_{BATT} falling, VRECHG = 200mV	135	190	240	mV
Input Regulation (T_A = 0°C to 70°C)						
Input minimum voltage regulation	V_{IN_LIM}	VIN_LIM = 3.88V, V_{BATT} = 3.3V	3.758	3.88	4.002	V
		VIN_LIM = 4.36V, V_{BATT} = 3.3V	4.236	4.36	4.484	V
Input minimum voltage regulation tracking battery	$V_{IN\_LIM\_BATT}$	VIN_LIM = 3.88V, V_{BATT} = 4V	70	165	285	mV
Input current limit	I_{IN_LIM}	IIN_LIM = 500mA	415	450	500	mA
		IIN_LIM = 1.5A	1.34	1.41	1.5	A
		IIN_LIM = 3A	2.7	2.84	3	A
BATT Over-Voltage Protection (OVP)						
Battery over-voltage protection (OVP) threshold	V_{BATT_OVP}	V_{BATT} rising, percentage of V_{BATT_REG}	103	105	106.5	%
Battery OVP hysteresis				1.7		%

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal						
Junction temperature regulation (8)	T_{J_REG}	TREG = 80°C		80		°C
		TREG = 120°C		120		°C
Thermal shutdown threshold (8)	T_{J_SHDN}	Temperature rising		150		°C
Thermal shutdown hysteresis (8)	T_{SHDN_HYS}			30		°C
JEITA NTC Monitor (T_A = 0°C to 70°C)						
NTC cold temperature rising threshold	V_{COLD}	As a percentage of V_{RNTC}, VCOLD = 74.2% (0°C)	73.9	74.5	75.1	%
NTC cold temperature rising threshold hysteresis		As a percentage of V_{RNTC}		1.4		%
NTC cool temperature rising threshold	V_{COOL}	As a percentage of V_{RNTC}, VCOOL = 64.8% (10°C)	64.3	64.9	65.5	%
NTC cool temperature rising threshold hysteresis		As a percentage of V_{RNTC}		1.4		%
NTC warm temperature falling threshold	V_{WARM}	As a percentage of V_{RNTC}, VWARM = 32.6% (45°C)	31.9	32.5	33.1	%
NTC warm temperature falling threshold hysteresis		As a percentage of V_{RNTC}		1.4		%
NTC hot temperature falling threshold	V_{HOT}	As a percentage of V_{RNTC}, VHOT = 23% (60°C)	22.7	23.3	23.9	%
NTC hot temperature falling threshold hysteresis		As a percentage of V_{RNTC}		1.4		%
BATTFET Over-Current Protection (OCP)						
BATTFET over-current protection (OCP) threshold	I_{BATT_OCP}		3.5	4		A
PWM Converter						
Switching frequency	f_{SW}	SW_FREQ = 750kHz	630	750	895	kHz
		SW_FREQ = 1000kHz	900	1050	1280	kHz
		SW_FREQ = 1250kHz	1060	1250	1450	kHz
		SW_FREQ = 1500kHz	1260	1475	1680	kHz
Boosts						
Boost regulation voltage	V_{PMID_REG}	VBOOST = 5.15V, T_A = -40°C to +85°C	5.08	5.15	5.22	V
BATT_LOW comparator falling threshold	V_{BATT_LOW}	BATT_LOW = 3V	2.88	3	3.12	V
		BATT_LOW = 3.3V	3.20	3.33	3.46	V
BATT_LOW comparator hysteresis				200		mV
Battery low comparator debounce time	$t_{D\_BATT\_LOW}$			10		ms
Boost output current limit	I_{BST_LIM}	OLIM = 500mA, T_A = 0°C to 70°C	500		615	mA
		OLIM = 1.5A, T_A = 0°C to 70°C	1500		1700	mA
Boost OVP threshold	V_{BST_OVP}	Boost mode, V_{IN} rising	5.5	5.8	6.1	V

Note:

8) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Low-Dropout (LDO) Regulator						
VCC output voltage	V_{CC}	V_{IN} = 5V, I_{VCC} = 5mA		3.65		V
IB Output (T_A = 0°C to 70°C)						
IB current output gain	I_B	I_B, charging, I_{BATT} = 50mA, BFET_STAT = 0	1.1	2	2.8	µA
		I_B, charging, I_{BATT} = 500mA, BFET_STAT = 0	18.2	20	22.1	µA
		I_B, discharging, I_{BATT} = 50mA, BFET_STAT = 1	1.1	2	2.8	µA
		I_B, discharging, I_{BATT} = 500mA, BFET_STAT = 1	18.2	20	22.1	µA
Impedance Test						
Input impedance test current	I_{VIN_SRC}	IVIN_SRC = 10µA	6	10	14	µA
		IVIN_SRC = 40µA	28	40	52	µA
		IVIN_SRC = 320µA	240	320	405	µA
Input impedance test voltage threshold	V_{IN_TEST}	VIN_TEST = 0.5V	0.46	0.5	0.54	V
		VIN_TEST = 1.5V	1.4	1.5	1.6	V
Logic I/O for SCL, SDA, INT, RST, STAT						
Logic input low voltage	V_{IL}				0.4	V
Logic input high voltage	V_{IH}		1.3			V
Open-drain output low voltage	V_{OL}	I_{SINK} = 10mA			0.2	V
RST pull-up resistor	R_{PULL_UP}			200		kΩ
D+/D- Detection						
DCD D+ pull-up current	I_{DP_SRC}		7	10	13	µA
DCD D- pull-low resistance	R_{DM_DWN}		16	20	24	kΩ
D+/D- source voltage low	V_{SRC_L}		550	600	650	mV
D+/D- source voltage high	V_{SRC_H}		3.1	3.3	3.5	V
D+/D- sink current	I_{SNK}		50	100	150	µA
Data detection voltage	V_{DAT_REF}		300	350	400	mV
Non-standard 1.2V window	V_{1P2_TH}	Low threshold	0.95	1	1.05	V
		High threshold	1.33	1.4	1.47	V
Non-standard 2V window	V_{2P0_TH}	Low threshold	1.73	1.8	1.87	V
		High threshold	2.17	2.25	2.33	V
Non-standard 2.7V window	V_{2P7_TH}	Low threshold	2.3	2.4	2.5	V
		High threshold	2.9	3	3.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

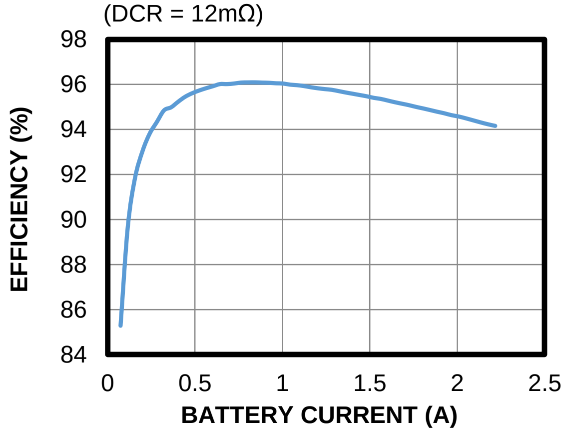
T_A = -40°C to +125°C, T_A = 25°C, and V_{BATT} = 4V for typical values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
USB Type-C CC Detection						
CC1 and CC2 pull-down resistance	R_D		4.6	5.1	5.6	kΩ
Sink port vRd-Connect threshold	V_{RD_CNCT}		0.17	0.2	0.23	V
Sink port vRd-USB threshold	V_{RD_USB}		0.63	0.66	0.69	V
Sink port vRd-1.5 threshold	V_{RD_1P5}		1.22	1.26	1.3	V
USB Type-C attachment debounce time	$t_{CC\_DEBOUNCE}$		120	150	180	ms
CC pin debounce time for PD	$t_{PD\_DEBOUNCE}$		12	15	18	ms
USB Type-C resistance (Rp) change debounce time	t_{RP_CHANGE}		12	15	18	ms
Timing						
Battery Charger						
Charge termination deglitch time	t_{TERM_DGL}			250		ms
Charge timer	t_{CHG_TMR}	CHG_TIMER = 10hrs	8	10	12	hr
Top-off timer	t_{TOP_OFF}	TOPOFF_TMR = 30min	24	30	36	min
Battery auto-recharge deglitch time	t_{RECH_DGL}			100		ms
RST Timing						
RST low time to exit shipping mode	$t_{SHIPMODE}$		0.9	1.1	1.3	s
RST low time to reset BATTFET	t_{RST}		8	10	12	s
BATTFET reset time	t_{SYS_RST}		250	330	400	ms
Enter shipping mode delay	t_{SHIP_DLY}		10	12	15	s
Watchdog and Clock						
Watchdog timer	t_{WDT}	WATCHDOG = 40s		40		s
I²C clock	f_{SCL}				400	kHz

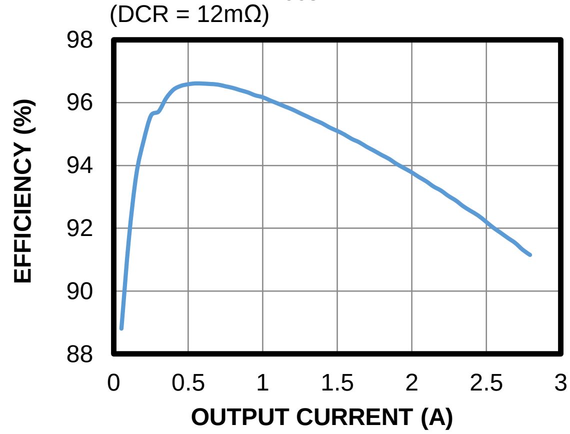
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1A, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

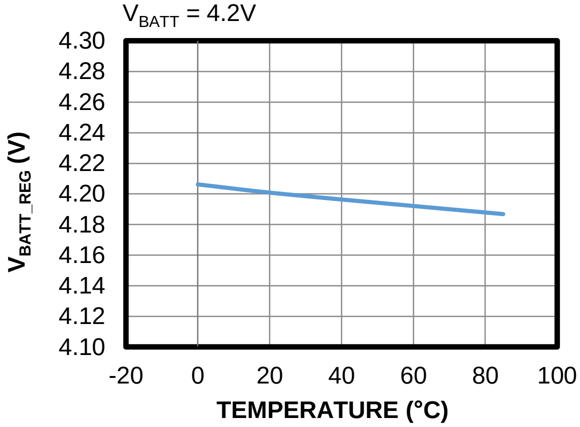
Charge Efficiency
V_{IN} = 5V, V_{BATT} = 3.8V, L = 1µH (DCR = 12mΩ)



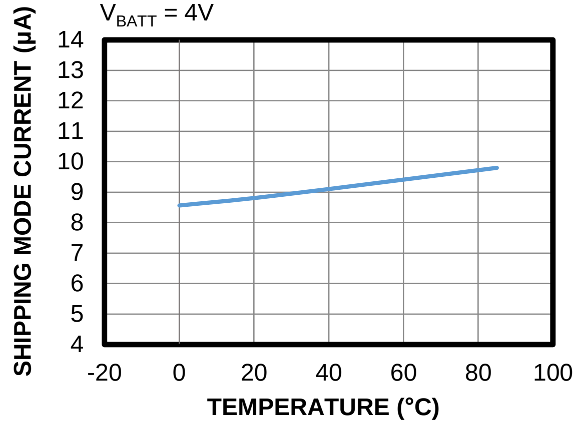
Boost Efficiency
V_{BATT} = 4.2V, V_{BOOST} = 5.15V, L = 1µH (DCR = 12mΩ)



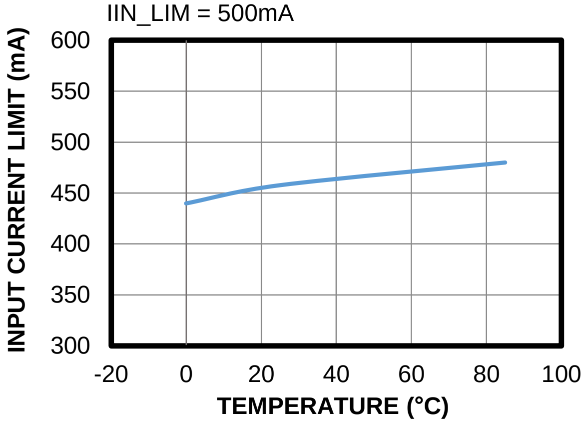
Battery Regulation Voltage vs.Temperature
V_{BATT} = 4.2V



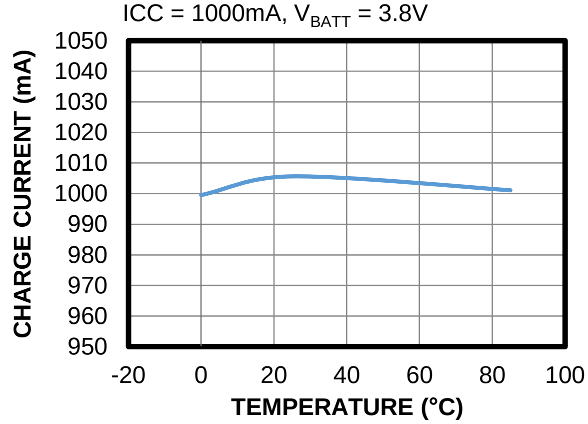
Shipping Mode Current vs. Temperature
V_{BATT} = 4V



Input Current Limit vs. Temperature
IIN_LIM = 500mA



Charge Current vs. Temperature
ICC = 1000mA, V_{BATT} = 3.8V

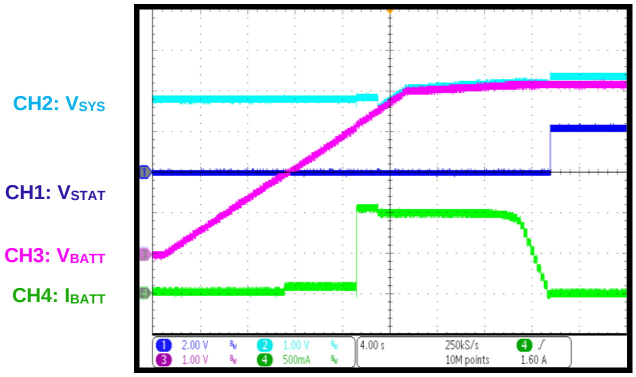


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1A, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

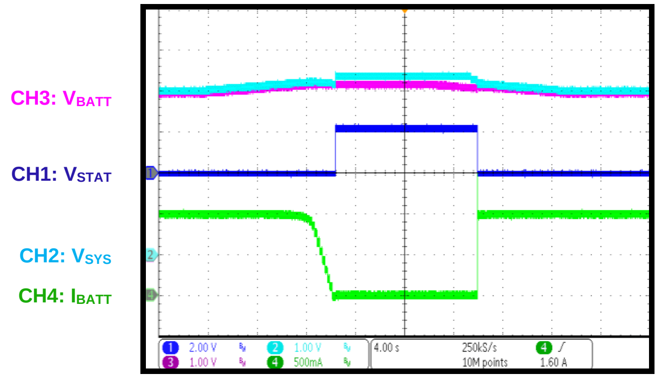
Battery Charge Profile

V_{IN} = 5V, I_{PRE} = 80mA, I_{CC} = 1A, I_{SYS} = 0A



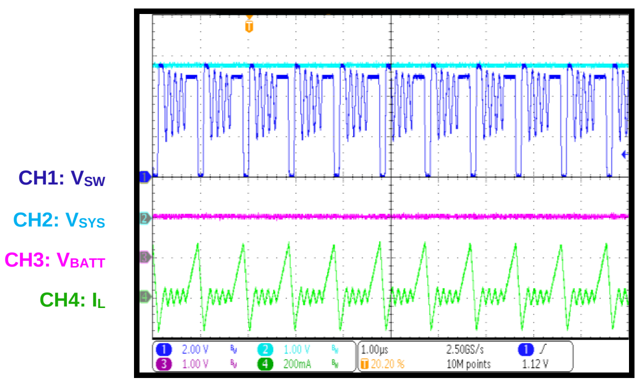
Automatic Recharge

V_{IN} = 5V, I_{CC} = 1A, I_{SYS} = 0A



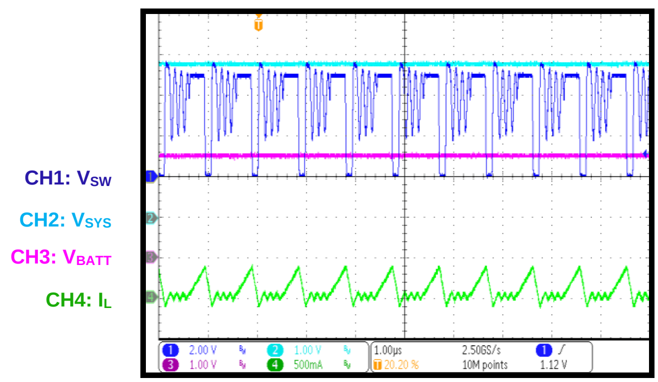
Trickle Charge

V_{IN} = 5V, V_{BATT} = 1V, I_{TC} = 32mA, I_{SYS} = 0A



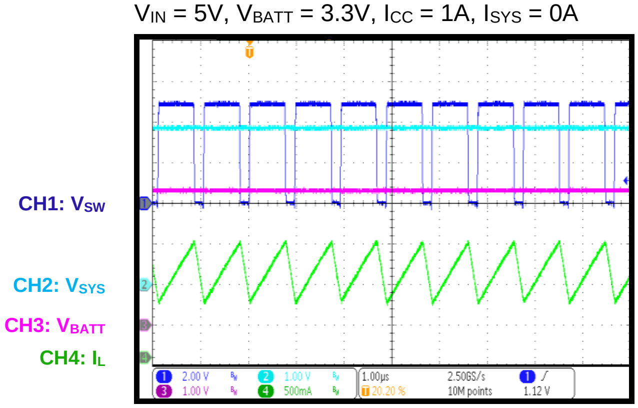
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2.5V, I_{PRE} = 80mA, I_{SYS} = 0A



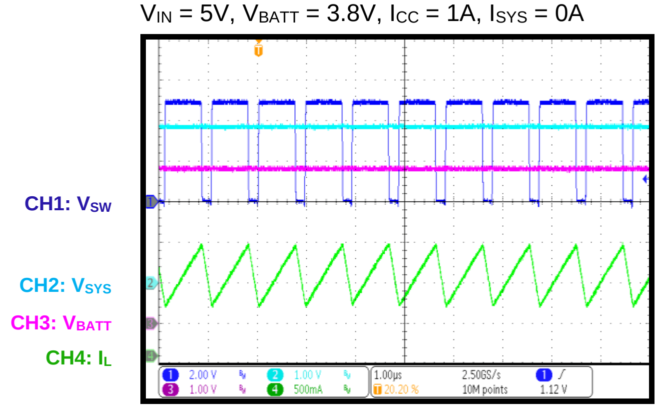
Linear CC Charge

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1A, I_{SYS} = 0A



Switching CC Charge

V_{IN} = 5V, V_{BATT} = 3.8V, I_{CC} = 1A, I_{SYS} = 0A

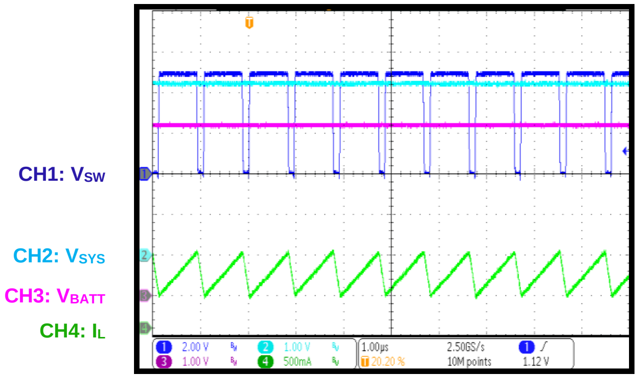


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1A, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

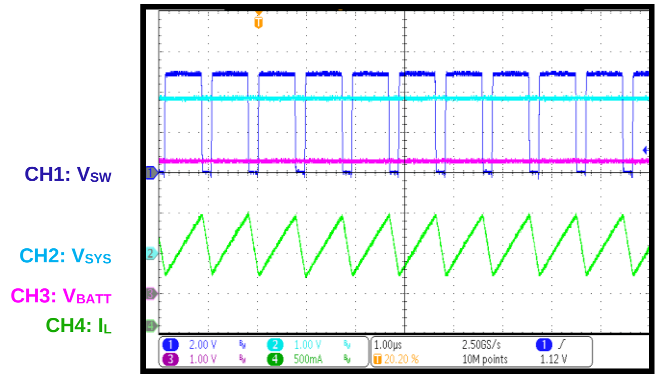
Constant-Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.185V, I_{SYS} = 0A



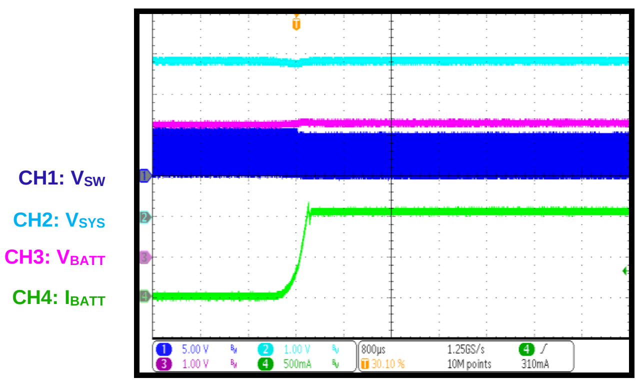
Charge Disabled Steady State

V_{IN} = 5V, V_{BATT} = 3.3V, I_{SYS} = 1A



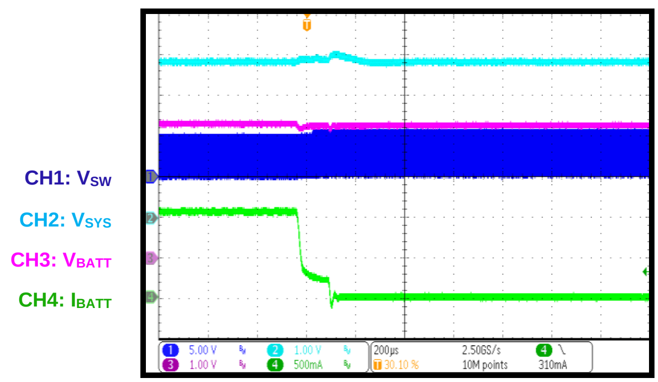
Charging Enabled

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1A, I_{SYS} = 0A



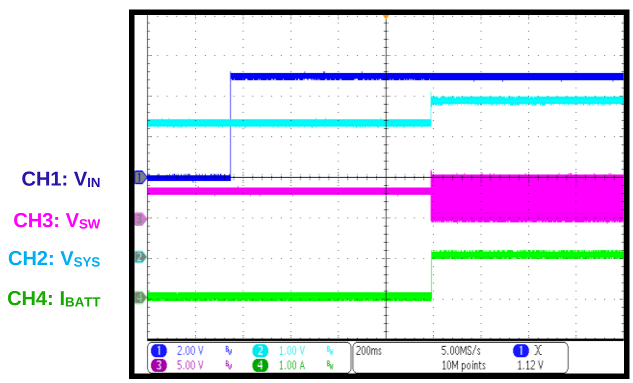
Charging Disabled

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1A, I_{SYS} = 0A



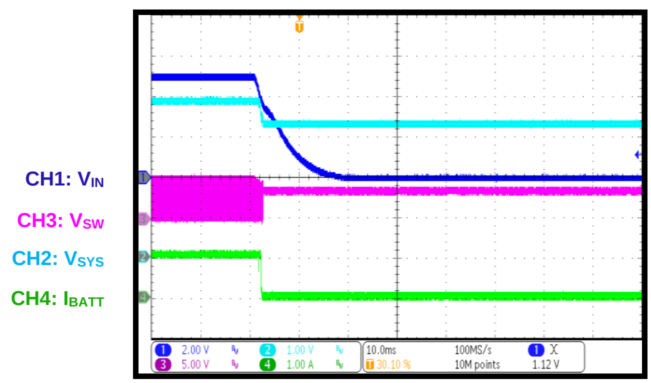
Start-Up

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1A, I_{SYS} = 0A



Shutdown

V_{IN} = 5V, V_{BATT} = 3.3V, I_{CC} = 1A, I_{SYS} = 0A

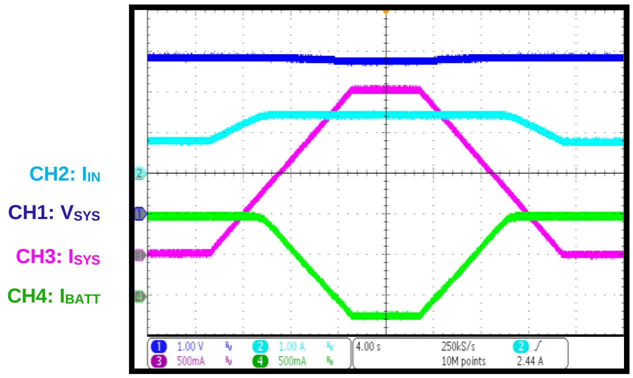


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1A, I_{IN_LIM} = 3A, V_{IN_MIN} = 4.36V, L = 1µH (DCR = 12mΩ), T_A = 25°C, unless otherwise noted.

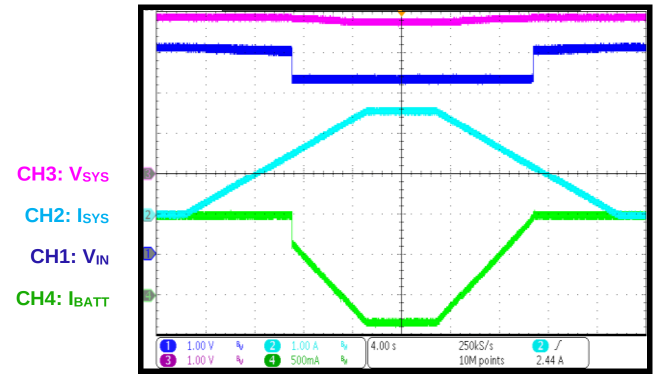
Input Current Limit

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 3.8V, I_{CC} = 1A



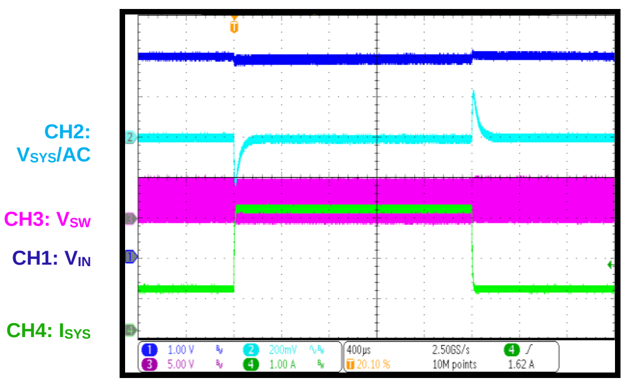
Input Voltage Limit

V_{IN} = 5V (2A), I_{IN_LIM} = 3A, V_{BATT} = 3.8V, I_{CC} = 1A



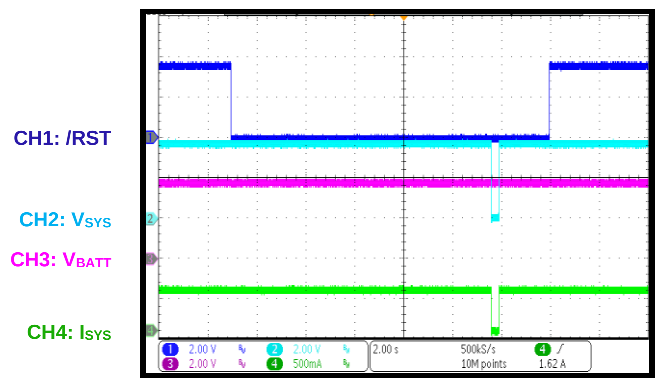
SYS Load Transient Response

V_{IN} = 5V, V_{BATT} = 3.3V, charge disabled, I_{SYS} = 1A to 3A



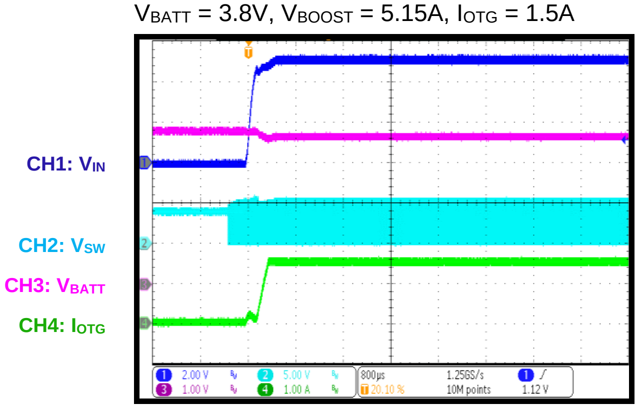
BATTFET Reset

V_{BATT} = 3.8V, I_{SYS} = 0.5A



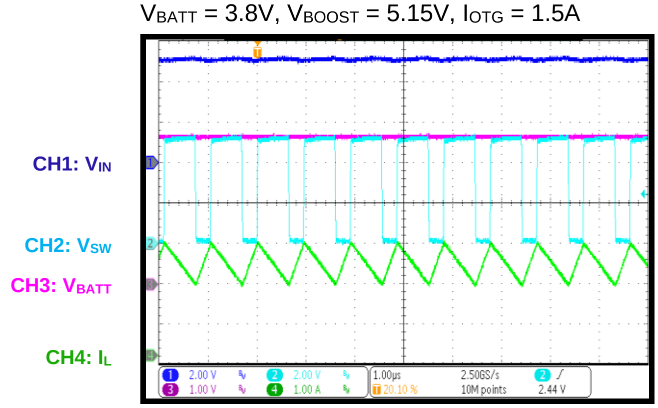
OTG Mode Enabled

V_{BATT} = 3.8V, V_{BOOST} = 5.15A, I_{OTG} = 1.5A



OTG Steady State Operation

V_{BATT} = 3.8V, V_{BOOST} = 5.15V, I_{OTG} = 1.5A



FUNCTIONAL BLOCK DIAGRAM

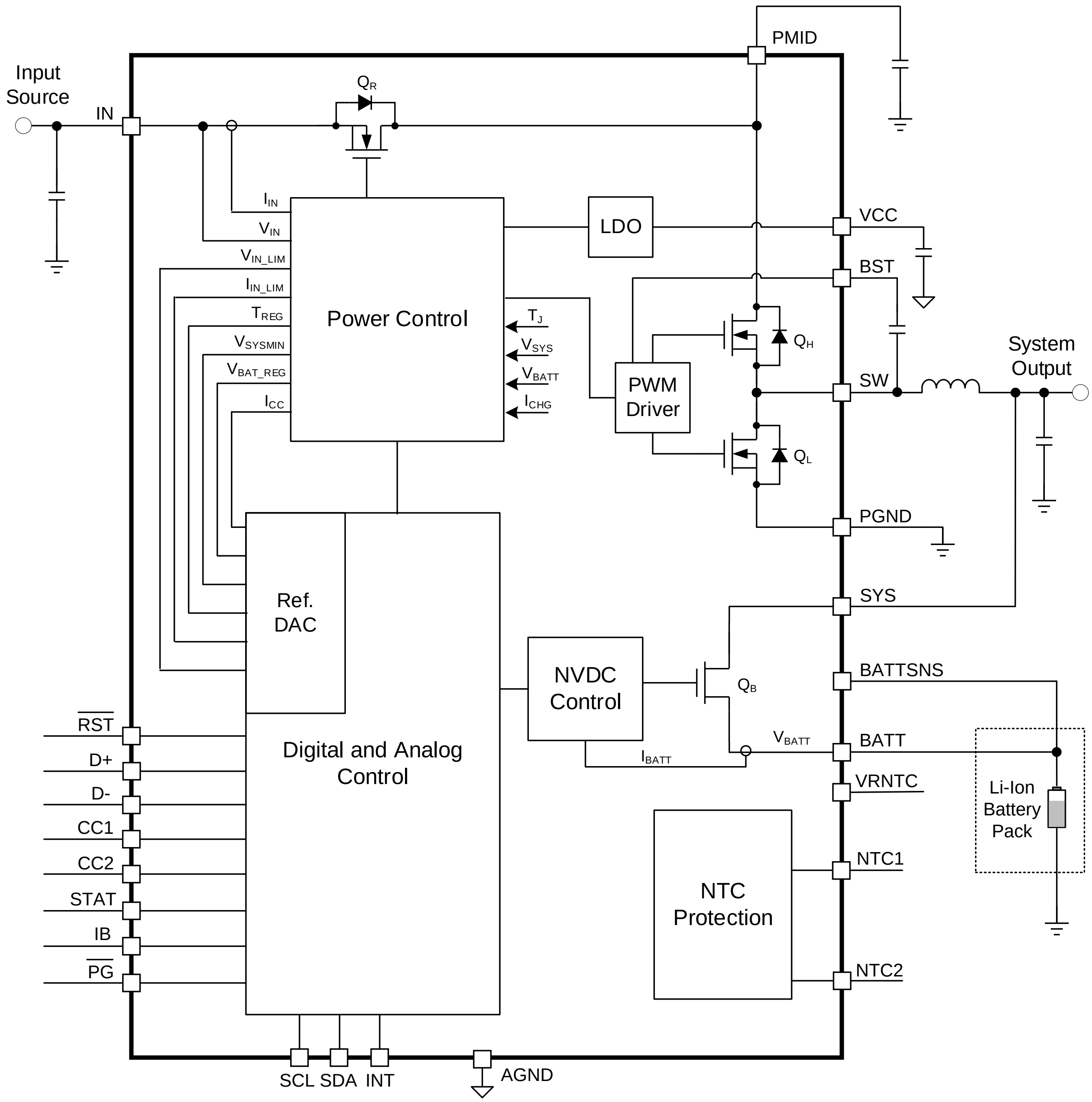


Figure 2: Functional Block Diagram

OPERATION

The MP2724 is a highly integrated, I²C-controlled, switch-mode battery charger IC with narrow-voltage DC (NVDC) power path management for single-cell lithium-ion or lithium-polymer battery applications. The MP2724 integrates the reverse blocking MOSFET (RB-FET, Q_R), high-side switching MOSFET (HS-FET, Q_H), low-side switching MOSFET (LS-FET, Q_L), battery MOSFET (BATTFET, Q_B), and a USB Type-C sink mode CC controller.

VCC Regulator

The VCC regulator is powered from the higher voltage between the IN, BATT, and PMID pins. The VCC pin requires an external 4.7µF bypass capacitor. VCC provides power for the internal circuits and the gate drivers. When the VCC pin voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) threshold (V_{CC_UVLO}), the I²C interface is ready for communication, and all the registers are reset to their default values. VCC can be used for external logic pull-up, but it is not recommended for excess loads.

Battery Power-On

If an input source is not available, the battery is connected, and the battery voltage (V_{BATT}) exceeds its UVLO threshold (V_{BATT_UVLO}), then the BATTFET turns on and powers up the system. The low quiescent current (I_Q) and low voltage drop on the BATTFET minimize battery consumption and maximize the battery runtime. The BATTFET's discharge current is monitored. If the system is overloaded or shorted to ground (I_{BATT} > I_{BATT_OCP}), then the device turns off BATTFET immediately and sets the BATTFET_DIS bit to 1. The BATTFET can be re-enabled following the methods described in the Exiting Shipping Mode section on page 22.

Input Power-On

When an input source is plugged in, the IC detects the input source type and sets the input current limit (I_{IN_LIM}) before the buck converter starts. The start-up sequence from the input source is described in detail below:

1. The input voltage (V_{IN}) is detected.
2. The hold-off timer (about 250ms) runs.
3. Input source type detection starts.
4. I_{IN_LIM} is set.
5. If EN_BUCK = 1, the buck converter starts.
6. If EN_CHG = 1, charging starts.

Hold-Off Timer

When a valid input source is detected, the IC runs a hold-off timer (t_{HOLD}, typically about 250ms) before detecting the input source type. t_{HOLD} can be bypassed by setting the HOLDOFF_TMR bit to 0.

Input Source Type Detection

The IC runs D+/D- detection when the following conditions are met:

- V_{IN} exceeds its UVLO threshold (V_{IN_UVLO})
- V_{IN} is below the input over-voltage protection (OVP) threshold (V_{IN_OVP})
- VIN_GD = 1
- t_{HOLD} ends
- AUTODPDM = 1, or FORCEDPDM is set

D+/D- detection includes the USB Battery Charging Specification 1.2 (BC1.2) and non-standard adapter detection. BC1.2 detection begins with data contact detection (DCD). If DCD is successful, the standard downstream port (SDP), dedicated charging port (DCP), and charging downstream port (CDP) are distinguished by primary and secondary detection. If the DCD timer expires, then non-standard adapter detection is initiated. Table 1 shows the criteria for non-standard adapter detection.

Table 1: Non-Standard Adapter Detection

Adapter Type	D+ Voltage (V_{D+})	D- Voltage (V_{D-})
Divider 1	V_{D+} within V_{2P0_TH}	V_{D-} within V_{2P7_TH}
Divider 2	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P0_TH}
Divider 3	V_{D+} within V_{2P7_TH}	V_{D-} within V_{2P7_TH}
Divider 4	V_{D+} within V_{1P2_TH}	V_{D-} within V_{1P2_TH}
Divider 5	V_{D+} within V_{2P7_TH}	V_{D-} > V_{2P7_TH}

If AUTODPDM = 0, then D+/D- detection is bypassed, and the DPDM_STAT bits remain set to 0000.

Table 2 shows the I_{IN_LIM} settings from D+/D- detection.

Table 2: Input Current Limit Setting by D+/D- Detection

D+/D- Detection	Input Current Limit
Not started	500mA
USB SDP	500mA
USB DCP	2A
USB CDP	1.5A
Divider 1	1A
Divider 2	2.1A
Divider 3	2.4A
Divider 4	2A
Divider 5	3A
Unknown	500mA

USB Type-C Sink Detection

In USB Type-C sink mode, the CC1 and CC2 pins are connected to AGND via a 5.1kΩ resistor (Rd). The CC1 and CC2 voltages are monitored. The sink power sub-state is determined by the monitored CC pin voltage (see Table 3).

Table 3: USB-C Sink Power Sub-States by the CC Voltage

CC Detection Result	CC Voltage	Min	Max
Type-C default USB	vRd-USB	0.25V	0.61V
Type-C 1.5A current	vRd-1.5	0.70V	1.16V
Type-C 3A current	vRd-3	1.31V	2.04V

Input Current Limit (I_{IN_LIM}) Setting

After input source type detection finishes, the following actions are executed:

- The CC1_SNK_STAT or CC2_SNK_STAT bits are updated
- The DPDM_STAT bits are updated
- I_{IN_LIM} is updated
- VIN_RDY = 1

When the VIN_RDY bit is set, an INT pulse asserts and I_{IN_LIM} is updated (see Table 4). The host can overwrite the IIN_LIM registers to modify I_{IN_LIM}.

If the FORCEDPDM bit is written to 1, then D+/D- detection restarts. After D+/D- detection finishes, the DPDM_STAT bits and I_{IN_LIM} update. An INT pulse follows this action.

If the monitored CC pin changes after the USB Type-C resistance (Rp) change debounce time (t_{RP_CHANGE}) (typically 15ms), then I_{IN_LIM} updates. An INT pulse follows this action.

Table 4: Input Current Limit Setting

CC Detection Result	Input Current Limit
Type-C default USB or CC_CFG is disabled	D+/D- detection result (500mA if AUTODPDM = 0)
Type-C 1.5A current	1.5A
Type-C 3A current	3A
vRa (V_{IN} is present, but no voltage is detected on the CC pin)	500mA

Input Voltage Limit (V_{IN_LIM}) Setting

The MP2724 supports a configurable input voltage limit (V_{IN_LIM}). If V_{IN} drops to V_{IN_LIM} due to the input source capability or a cable voltage drop, then the duty cycle is limited to prevent V_{IN} from dropping further. This reduces the converter's total output current.

If the EN_VIN_TRK bit is set to 0, then the absolute V_{IN_LIM} is set by the VIN_LIM register. If the EN_VIN_TRK bit is set to 1, then V_{IN_LIM} is the maximum value between the VIN_LIM register's setting and (V_{BATT} + 165mV).

Buck Converter and Charger Start-Up

After the VIN_RDY bit is set to 1, the buck converter soft starts if EN_BUCK = 1. The buck converter's switching frequency (f_{SW}) can be set between 750kHz and 1.5MHz.

Peak current mode control is adopted to regulate the system voltage (V_{SYS}), battery charge current, battery regulation voltage (V_{BATT_REG}), I_{IN_LIM}, V_{IN_LIM}, and the device's die temperature loops.

If the EN_CHG bit is set to 1, the device automatically starts charging.

NVDC Battery MOSFET (BATTFET)

Using the NVDC structure, the BATTFET separates the system from the battery and controls the battery charging and discharging.

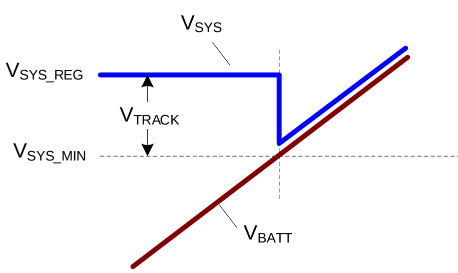
With power path management, the device prioritizes the system (SYS) output by utilizing the input source, battery, or both.

When the input source is absent, the BATTFET turns fully on to pass the battery power to the system via the ultra-low impedance path. When the input source is present and the buck converter has started up, the system output is related to V_{BATT} in the following ways:

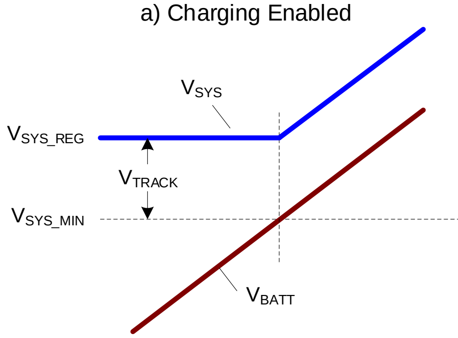
1. When V_{BATT} is below the minimum system voltage setting (V_{SYS_MIN}), V_{SYS} is regulated to (V_{SYS_MIN} + V_{TRACK}), where V_{TRACK} is typically 200mV. Depending on V_{BATT}, the BATTFET works in linear mode to charge the battery with a trickle-charge, pre-charge, or fast charge current.
2. Once V_{BATT} exceeds V_{SYS_MIN}, the BATTFET turns on fully, and the voltage difference between V_{SYS} and V_{BATT} is the BATTFET's resistive voltage drop.
3. When charging is disabled or terminated, V_{SYS} is always regulated to V_{TRACK} plus the higher value between V_{SYS_MIN} and V_{BATT}. In this scenario, V_{TRACK} is typically 150mV.

The status register VSYS_STAT indicates whether the system is in V_{SYS_MIN} regulation.

Figure 3 shows V_{SYS} regulation as VBATT changes.



a) Charging Enabled



b) Charging Disabled

Figure 3: V_{SYS} Regulation with V_{BATT}

Dynamic Power Management

During the buck converter's operation, the MP2724 continuously monitors the input current (I_{IN}) and V_{IN}. If I_{IN_LIM} or V_{IN_LIM} is reached, the charge current is reduced to prevent the input source from being overloaded.

If the battery current (I_{BATT}) drops to 0A, V_{SYS} starts to drop due to the input power limit. Once V_{SYS} falls below V_{BATT}, the IC automatically enters supplement mode.

If the converter operates in the input current loop or input voltage limit loop, the IINDPM_STAT or VINDPM_STAT bit is set to 1, respectively. This is followed by a maskable INT pulse.

Supplement Mode

Once V_{SYS} falls below V_{BATT}, the BATTFET turns on to prevent V_{SYS} from dropping further. In this scenario, the buck converter and the battery work together to provide power for the system.

Battery Charging

The MP2724 can autonomously run a charging cycle without host involvement. The host can also control the charging operations and parameters via the registers.

A new charge cycle starts when the following conditions are met:

- The buck converter has started up
- The NTC pin voltages (V_{NTC1} and V_{NTC2}) are within the acceptable ranges
- The BATTFET is on (BATTFET_DIS = 0)
- Charging is enabled (EN_CHG = 1)

Charging Profile

The MP2724 detects V_{BATT} to provide four main charging phases: trickle-charge, pre-charge, constant-current (CC) charge, and constant-voltage charge (see Table 5 on page 20).

Table 5: Charge Current Setting

Battery Voltage (V_{BATT})	Charge Current	Default Value	CHG_ STAT
$V_{BATT} < V_{BATT\_TC}$	$I_{TRICKLE}$	16mA	001
$V_{BATT\_TC} \leq V_{BATT} < V_{BATT\_PRE}$	I_{PRE}	20mA	010
$V_{BATT\_PRE} \leq V_{BATT} < V_{BATT\_REG}$	I_{CC}	40mA	011
$V_{BATT} = V_{BATT\_REG}$	$<I_{CC}$	-	100

Throughout the charging process, the actual charge current may be below the register setting due to other regulation loops, such as the input current loop, input voltage loop, or thermal regulation. In this scenario, charge termination is blocked, and the charge timer counts at half of its usual speed if EN_TMR2X = 1. Figure 4 shows the battery charge profile.

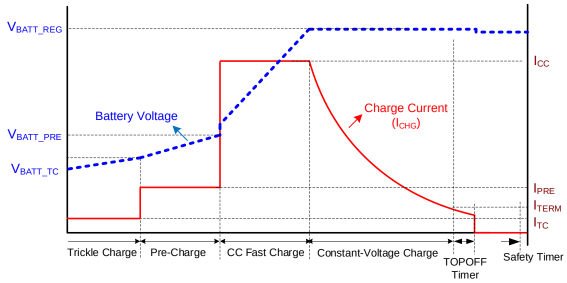


Figure 4: Battery Charging Profile

Charge Termination

If the following conditions are met, charging is terminated:

- Termination is enabled (EN_TERM = 1)
- I_{BATT} is below the termination threshold for t_{TEC_DGL} (about 250ms)
- The device is charging in the constant-voltage phase
- The device is not in an input current loop or input voltage loop
- The device is not in thermal regulation

After termination, the status register CHG_STAT is set to 101, the STAT pin indicator goes high, and an INT pulse is generated.

To restart a new charge cycle once charging terminates, re-plug in the input source or toggle the EN_CHG bit.

To fully charge the battery, a top-off timer can be applied after termination is detected. The TOPOFF_TMR bits set the top-off timer. The TOPOFF_ACTIVE bit is 1 when the top-off timer is active. A maskable INT pulse is generated when entering and exiting the top-off time. During top-off timer operation, charging continues, while the CHG_STAT bits and the STAT pin both indicate that charging is done.

The top-off timer can be reset by any of the following conditions:

- Charging changes from disabled to enabled
- Recharging begins
- The REG_RST bit is set

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system supplement mode or self-discharge. When V_{BATT} discharges to the recharge threshold, the MP2724 automatically starts a new charging cycle without requiring a manual charge cycle restart, as long as the input power is valid. There is a deglitch timer (t_{RECH_DGL}, about 100ms) to detect whether V_{BATT} is below the recharge threshold. An INT pulse asserts when automatic recharging starts.

JEITA Thermistor Qualification

The MP2724 supports the JEITA profile to manage the charging parameters by continuously monitoring V_{NTC1} and V_{NTC2}. Two independent negative temperature coefficient (NTC) thermistors with temperature sensing and flexible configurations are provided. The NTC1 and NTC2 pins can be enabled and disabled by setting the NTC1_ACTION and NTC2_ACTION bits, respectively.

The EN_PG_NTC2 bit should be set to 1 to enable the NTC2 channel. When the EN_PG_NTC2 bit is set to 0, there is only one NTC monitor.

If the corresponding NTC channel is enabled, then V_{NTC1} or V_{NTC2} must be within the V_{HOT} to V_{COLD} range to initiate a charge cycle. If V_{NTC1} or V_{NTC2} is outside the V_{HOT} to V_{COLD} range, then the MP2724 suspends charging and waits for V_{NTC1} or V_{NTC2} to return to the standard range.

In the cool temperature range (V_{COLD} to V_{COOL}), the charge current and/or charge voltage are reduced according to the COOL_ACT, JEITA_ISET, and JEITA_VSET settings.

In the warm temperature range (V_{WARM} to V_{HOT}), the charge voltage and/or charge current are reduced according to the WARM_ACT, JEITA_ISET, and JEITA_VSET settings.

The V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds all have four configurable percentage levels.

The temperature conditions can be read in the NTC1_FAULT and/or NTC2_FAULT bits. An INT pulse is generated when the NTC1 or NTC2 condition changes.

The NTC1 and NTC2 pins share the same configurable thresholds. Table 6 shows the detection priority when the detection results between the two NTC inputs are different.

Table 6: JEITA Detection Priority

NTC2 \ NTC1	Hot	Warm	Normal	Cool	Cold
Hot	Hot	Hot	Hot	Hot	Hot
Warm	Hot	Warm	Warm	Warm	Cold
Normal	Hot	Warm	Normal	Cool	Cold
Cool	Hot	Warm	Cool	Cool	Cold
Cold	Hot	Cold	Cold	Cold	Cold

For battery temperature protection during boost mode, if the NTC1_ACTION or NTC2_ACTION bit is set to 1, the device compares V_{NTC1} and/or V_{NTC2} with the V_{COLD} and V_{HOT} thresholds. If V_{NTC1} or V_{NTC2} is outside the V_{COLD} to V_{HOT} range, then boost mode is suspended. The NTC1_FAULT or NTC2_FAULT bit is also set to report the condition.

The preset V_{HOT}, V_{COLD}, V_{WARM}, and V_{COOL} thresholds are defined for a β = 3435 thermistor. It is recommended to use a pull-up resistance that matches the thermistor's resistance at 25°C.

Figure 5 shows the JEITA voltage/current regulations with the following set-up: NTC1_ACTION = 1, NTC2_ACTION = 0, WARM_ACT = 01, COOL_ACT = 10, JEITA_VSET = 00, and JEITA_ISET = 00.

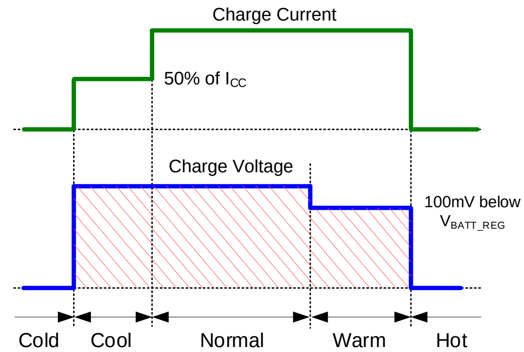


Figure 5: NTC Window under JEITA Control

Charging Safety Timer

The MP2724 has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. When V_{BATT} is below the V_{BATT_PRE} threshold, the safety timer is fixed to 2 hours. When V_{BATT} exceeds the V_{BATT_PRE} threshold, the safety timer is configured by the CHG_TIMER bits. When the CHG_TIMER bits are set to 00, both the pre-charge timer and the fast-charge timer are disabled.

Charging is disabled after the safety timer expires. Then the fault register's CHG_FAULT bit is set to 10, and an INT pulse is generated.

During an I_{IN}, V_{IN}, thermal regulation, or JEITA cool/warm condition (when the charge current (I_{CC}) reduction is enabled), the charge timer counts at half of its usual rate. This halved clock rate function can be disabled by setting the EN_TMR2X bit to 0.

The charging safety timer resets if any of the following conditions are met:

- The input source is unplugged
- EN_BUCK or EN_CHG is toggled
- The REG_RST bit is set

Remote Battery Voltage Sense

To minimize the parasitic trace resistance during charging, the BATTSNS pin can be connected to the actual battery pack's positive terminal. Remote sensing of the battery voltage accelerates the charging speed by helping the charger stay in CC charge mode for longer.

Shipping Mode

Entering Shipping Mode

When the host sets the BATTFET_DIS bit to 1, the MP2724 turns off the BATTFET immediately or after a set delay time (t_{SHIP_DLY}), configured by the BATTFET_DLY bit.

Exiting Shipping Mode

When the MP2724 is in shipping mode (BATTFET_DIS = 1), either of the following events can wake up the BATTFET:

- An input source is applied
- The $\overline{RST}$ pin pulls low for $t_{SHIPMODE}$

BATTFET Reset

When the input source is absent, the system is powered by the battery through the BATTFET. The system can be forced to have a hardware power-on reset (POR) by changing the BATTFET status from on to off, then back to on.

For this function, the $\overline{RST}$ pin can be connected to the device's push-button. The $\overline{RST}$ pin is pulled up internally.

If the $\overline{RST}$ pin is driven low for t_{RST} while the input source is not plugged in, and BATTFET_DIS = 0, the BATTFET turns off for t_{SYS_RST}, then it is enabled again (see Figure 6).

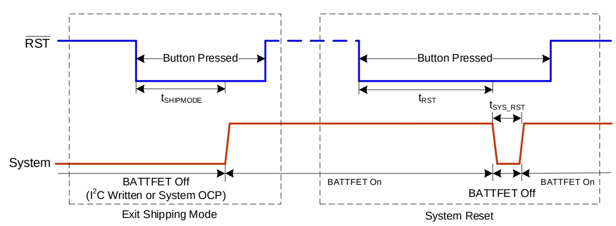


Figure 6: $\overline{RST}$ Timing

This function can be disabled by setting the BATTFET_RST_EN bit to 0.

Power Good (PG) Indication

When EN_PG_NTC2 is set to 0, the PG/NTC2 pin acts as the power good (PG) indicator. This pin goes low to indicate a good input source when the following conditions are met:

- V_{IN} exceeds V_{IN_UVLO}
- V_{IN} is below V_{IN_OVP}
- The 15ms debounce timer has passed

STAT/IB Indication

When the EN_STAT_IB bit is set to 0, the charging status is indicated on the open-drain STAT/IB pin (see Table 7).

Table 7: STAT Indication

Charging State	STAT
Charging	Low
Charging is complete, top-off timer, boost mode, and charging is disabled	High
Charging is suspended (due to battery OVP, input OVP, timer fault, or an NTC fault), and boost mode is suspended (due to an NTC fault, OTP, or BATT_LOW)	Blinks at 1Hz

When EN_STAT_IB is set to 1, the STAT/IB pin acts as an analog current source output that indicates the value of the battery current flowing into or out of the battery. The current's direction can be read via the BFET_STAT bit. Connect a resistor load between the STAT/IB pin and AGND to sense the IB current. If IB_EN is set to 1, the IB output is always on. If IB_EN is set to 0, the IB output is only on when the device is switching.

The IB output voltage ranges between 0V and V_{CC}. The host can measure the IB voltage to make a software fuel gauge or monitor the peak discharge current.

Interrupts (INT)

A 256µs interrupt pulse is generated on the open-drain INT pin if any of the interrupt events occur. See the Interrupt List section on page 39 for more details.

Watchdog Functions (Bark and Bite)

After the first battery or V_{IN} start-up, the MP2724 operates with the default set-up. The watchdog timer is expired by default when WATCHDOG_FAULT = 1. Writing 1 to WATCHDOG_RST starts the watchdog timer.

The watchdog timer has a bark function that generates an INT pulse when the watchdog timer is 3/4 of the way through its timer. The host can distinguish this condition by reading the WATCHDOG_BARK bit.

To maintain custom settings after the watchdog timer starts, write 1 to the WATCHDOG_RST bit before the watchdog timer expires. If the watchdog timer expires, the registers are reset according to the register table. After the watchdog timer expires, an INT pulse is sent, and the WATCHDOG_FAULT bit is set to 1.

The watchdog timer can be disabled by setting the WATCHDOG bit to 00. If the watchdog timer is disabled, the registers keep their values until a POR occurs.

Boost Mode

By boosting from the battery, the MP2724 can supply a regulated output at the IN pin. Boost mode starts once the following conditions are met:

- V_{IN} is below V_{IN_UVLO}
- EN_BOOST = 1
- V_{NTC1} and V_{NTC2} are within the acceptable range
- V_{BATT} exceeds V_{BATT_UVLO}
- If BOOST_STP = 1, V_{BATT} must exceed V_{BATT_LOW}

The boost PWM's switching frequency is the same as the buck converter's setting. The boost voltage loop regulates the PMID pin voltage (V_{PMID}) at the value set by the VBOOST bits. The boost output current loop limits the output current at the value set by the OLIM bits for the $V_{IN} > V_{BATT} + V_{HDRM}$ range.

The boost mode start-up sequence follows the steps below:

1. The converter soft starts and regulates V_{PMID}.
2. The blocking FET (Q_R) soft starts and regulates the discharge current from PMID to IN.
3. Once the IN pin starts up successfully, the boost is controlled to regulate V_{PMID} and the output current sensed through Q_R.

The boost converter's soft-start (SS) function allows the device to power into large capacitive loads on the IN pin.

USB Type-C Sink Mode

The MP2724 integrates a USB Type-C sink mode CC controller. This function is configured by the CC_CFG bits.

The MP2724 can present Rd to AGND on the CC1 and CC2 pins to sink power from the input source. Set the CC_CFG bits to 000 to enable the MP2724 to act as a charger only port, where the battery is charged once the input source is detected by the IN pin.

The VIN_GD bit indicates whether a valid input source is detected. The CC1_SNK_STAT or CC2_SNK_STAT bits indicate the input source power advertisement.

Forced Input Current Limit

When an input source is plugged in, the MP2724 runs the start-up sequence and initiates input source type detection. After detection finishes, I_{IN_LIM} is automatically generated. The I_{IN_LIM} result is returned by the IIN_LIM bits.

If the host does not want to use the automatically generated I_{IN_LIM}, I_{IN_LIM} can be set to different values by configuring either the IIN_MODE or IIN_LIM bits.

If the IIN_MODE bits are set to 000, the MP2724 runs with the automatically generated I_{IN_LIM} (returned by the IIN_LIM bits). However, once the VIN_RDY bit is set, the host can override the IIN_LIM bits to set I_{IN_LIM} to any value. This requires host involvement every time the converter starts up.

If the IIN_MODE bits are set to other values, I_{IN_LIM} is forced and fixed. For example, if the IIN_MODE bits are set to 101, the device always runs with a fixed 2000mA I_{IN_LIM}, ignoring the input source type detection.

Legacy Cable Detection

The MP2724 supports a legacy cable detection function. If the input source is plugged in through a Type-C to Type-C (C-C) cable, then V_{IN} is available after the CC1 and CC2 pins make contact for ≥100ms. The adapter's Type-C port requires a debounce time ($t_{CC\_DEBOUNCE}$)

(between 100ms and 200ms) before it can turn on the bus voltage (V_{BUS}) output. If a legacy Type-A to Type-C (A-C) cable is used, there is no debounce time.

A legacy cable timer (t_{LEGACY}, 75ms) starts once the CC1 or CC2 pin detects a vRd connect voltage (>0.2V). If an input source provides V_{BUS} before $t_{CC\_DEBOUNCE}$ expires, or V_{IN} is available before the CC1 and CC2 pins make contact, then the LEGACYCABLE bit is set to 1 once a valid input source is detected (e.g. V_{IN} is between V_{IN_UVLO} and V_{IN_OVP} after 15ms). The LEGACYCABLE bit is reset to 0 if V_{IN} drops below V_{IN_UVLO} or exceeds V_{IN_OVP}.

With legacy cable detection, the host can know the cable type. An advantage of this function is that if the legacy cable is non-compliant with the specification (e.g. if the CC pin is shorted to V_{BUS} or Rp is incorrect), then the host can adjust the device's I_{IN_LIM} with the DPDM detection results.

Input Impedance Test

The MP2724 supports an input impedance testing function. By sourcing a current on the IN pin, the device can detect the impedance on the connecter receptacle (water detection).

The host can write 1 to the VIN_SRC_EN bit to turn on the input impedance test by sourcing a current to IN pin. The testing current can be configured via the IVIN_SRC bits. If V_{IN} rises to the threshold configured via the VIN_TEST bit, then VIN_TEST_HIGH is set to 1 and latched. This is followed by an INT pulse.

The host can write 0 to the VIN_SRC_EN bit to turn off the test current source and clear the VIN_TEST_HIGH bit.

The VIN_SRC_EN bit can only be effective when neither the buck nor boost is operating, and the current source's maximum pull-up voltage is 2.5V. If $V_{IN} > V_{IN\_UVLO}$ is detected during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0, and the test ends immediately. If boost mode is enabled during the test, then the VIN_SRC_EN and VIN_TEST_HIGH bits are reset to 0, and the test ends immediately.

Lock Function

The MP2724 supports a lock function that limits the value of some key parameters (prevents accidental I²C writing). The battery regulation voltage, CC charge current, pre-charge current, and JEITA voltage/current settings are some of these parameters.

To enable the lock function, the host can set the above parameters to a target value, then write the LOCK_CHG bit to 1. After this operation, these parameters can only be written to values below the previously set value.

Any of the following events can unlock the parameters:

- The host writes the LOCK_CHG bit to 0
- The host writes the REG_RST bit to 0
- The device shuts down

Protections

Battery Under-Voltage Protection (UVP)

If the battery is discharged below V_{BATT_UVLO} when the input source is absent, then the BATTFET turns off, and all registers are reset.

BATTFET Over-Current Protection (OCP)

The MP2724 monitor the BATTFET's current. If SYS is overloaded or experiences a short, and the battery discharge current reaches the I_{BATT_OCP} threshold, then the BATTFET turns off and latches. In addition, the BATTFET_DIS bit is set to 1. To release the latch, apply one of the methods described in the Exiting Shipping Mode section on page 22.

Input Over-Voltage Protection (OVP)

The MP2724 provides input OVP with a 6.3V rising threshold. If the IN pin senses a voltage above the V_{IN_OVP} threshold, then the buck converter stops working, the CHG_FAULT bits are set to 01, and an INT pulse is generated.

When V_{IN} returns to the normal range, the device runs the start-up sequence again and resumes normal operation. The CHG_FAULT bits are also cleared.

Battery Over-Voltage Protection (OVP)

The battery OVP threshold is 104% of V_{BATT_REG}. If a battery over-voltage (OV) condition is detected, charging is disabled. The fault register's CHG_FAULT bits are set to 11, and an INT pulse asserts.

Thermal Regulation and Thermal Shutdown

If the internal junction temperature reaches to the thermal regulation limit (T_{J_REG}) configured via the TREG bits (60°C to 120°C) during battery charging, then the charge current is reduced, charge termination is blocked, and the charge timer runs at half rate. The status register's THERM_STAT bit is set to 1, followed by a maskable INT pulse.

If the internal junction temperature rises to the shutdown threshold (T_{J_SHDN}, about 150°C) at any time, then both the converter and BATTFET turn off. Once the junction temperature is below T_{J_SHDN} (150°C) by T_{SHDN_HYS} (about 30°C), the MP2724 resumes normal operation.

Boost Over-Voltage Protection (OVP)

If V_{IN} exceeds the regulation target and the boost OVP threshold (V_{BST_OVP}) during boost operation, then the device stops switching immediately. The BOOST_FAULT bits are set to 010, and an INT pulse is generated. Boost operation recovers once V_{IN} returns to its normal range.

Boost Overload Protection (OLP)

If V_{IN} drops below the (V_{BATT} + V_{HDRM}) or V_{IN_UVLO} threshold due to a heavy load or short during boost operation, the blocking FET turns off and restarts after 500ms. If a total of 8 restarts are not successful, the boost converter stops and latches off. Then the BOOST_FAULT bits are set to 001, and an INT pulse is generated.

If the IN pin is shorted to ground before the boost converter starts, the blocking FET also restarts 8 times. If this is not successful, the boost converter stops and latches off.

Set the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Battery Low Protection

The MP2724 can protect the battery from being over-drained and prevent a system shutdown during boost operation.

If the BOOST_STP_EN bit is set to 1 and V_{BATT} falls below the BATT_LOW setting, boost operation automatically turns off and the MP2724 latches. The BOOST_FAULT bits are set to 100 and generate a maskable INT pulse. The BATTFET continues operating to provide power to SYS.

The battery low comparator has a 10ms de-bounce time. Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Boost Over-Temperature Protection

The MP2724 provides protection from over-temperature conditions in boost mode. If the BOOST_OTP_EN bit is set to 1 and the internal junction temperature rises to the thermal regulation limit (T_{J_REG}, configured via the TREG bits), then boost operation stops and the MP2724 latches. The BOOST_FAULT bits are set to 011, followed by an INT pulse. In this scenario, the BATTFET continues operating to provide power to SYS.

Change the EN_BOOST bit to 0 to clear the BOOST_FAULT bits.

Serial Interface

The MP2724 uses an I²C-compatible interface to flexibly set charging parameters and instantaneously report the device status. The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage with a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller unit (MCU). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high to low transition on the SDA line while SCL is high. A stop command is defined as a low to high transition on the SDA line when the SCL is high (see Figure 7).

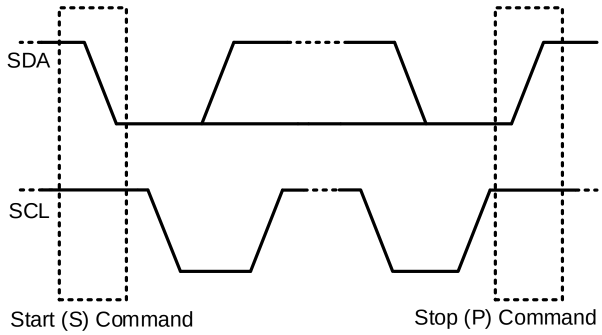


Figure 7: Start and Stop Commands

For data validity, data on the SDA line must be stable during the clock's high period. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 8).

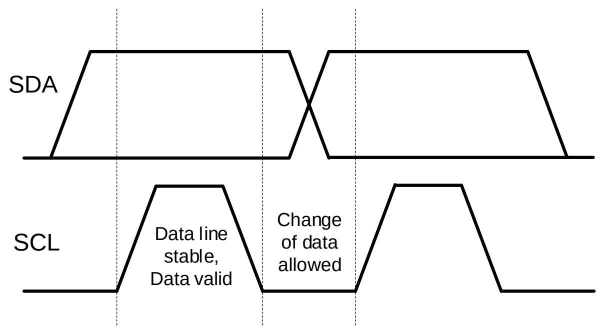


Figure 8: Bit Transfer on the I²C Bus

Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

Each byte must be followed by an acknowledge (ACK) bit. The ACK bit is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low, which remains low during the high period of the 9th clock.

If the SDA line is high during the 9th clock pulse, this is considered a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer or a repeated start (Sr) command to start a new transfer.

A slave address is sent after the start command. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 9 shows the address bit arrangement.

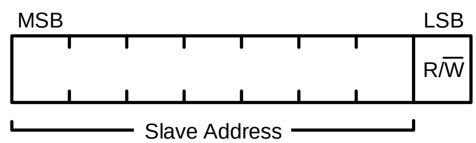


Figure 9: 7-Bit Address

Figure 10 shows a data transfer on the I²C bus. Figure 11 on page 27 shows a single write sequence. Figure 12 on page 27 shows a single read sequence. Figure 13 on page 27 shows a multi-write sequence. Figure 14 on page 27 shows a multi-read sequence.

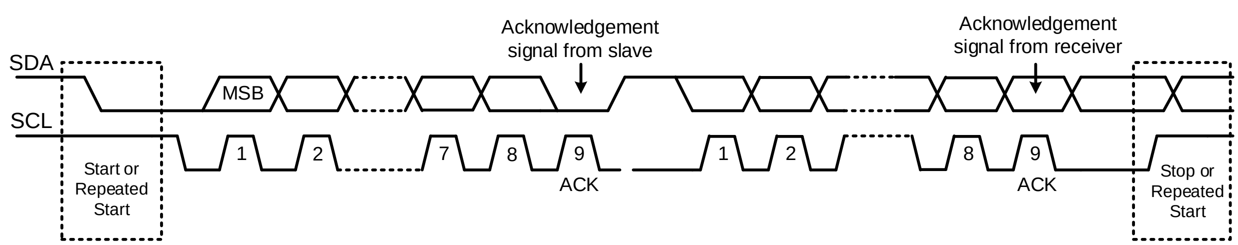


Figure 10: Data Transfer on the I²C Bus

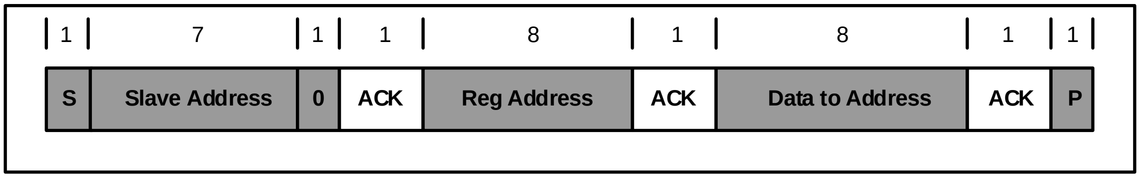


Figure 11: Single Write Sequence

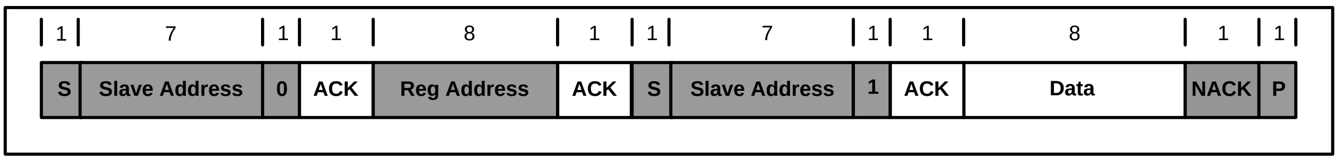


Figure 12: Single Read Sequence

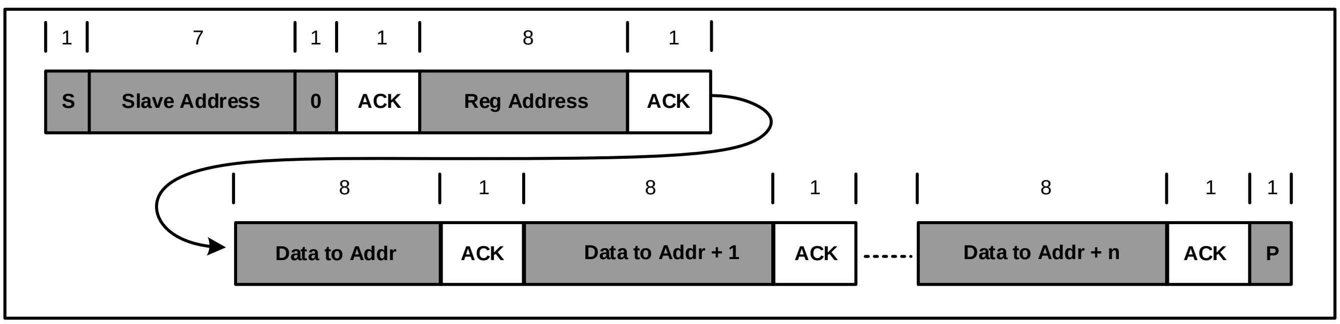


Figure 13: Multi-Write Sequence

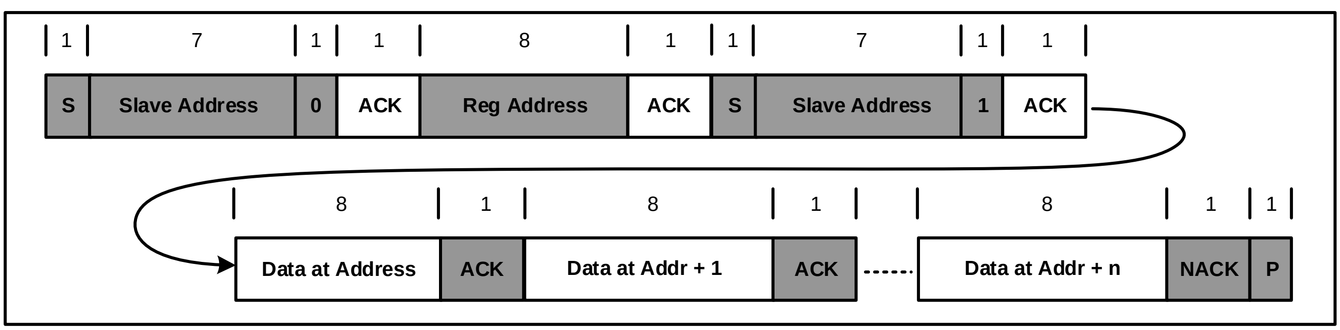


Figure 14: Multi-Read Sequence

REGISTER MAP

I²C Slave Address: 3Fh

Configuration Bytes: 00h~10h

Status Bytes: 11h~16h

CONFIGURATION BYTES (00h~10h)

Legend: POR = default value; WTD = watchdog; R/W = read/write; R = read-only, OTP-configurable = the register's default value can be configured via the OTP

CHG_CTRL0 (00h)

The CHG_CTRL0 command sets the function of the STAT/IB and PG/NTC2 pins, switching frequency (f_{SW}), enable/disable of the hold-off timer, and the input voltage (V_{IN}) tracking function.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R/W	REG_RST	1'b0	-	Resets the register. This bit returns to 0 after it is written to 1. 0: Keeps the current setting (default) 1: Resets the registers to their default values
6	R/W	EN_STAT_IB	1'b0	No	This bit is one-time programmable (OTP) memory-configurable. 0: The STAT/IB pin is configured as an open-drain status indicator (STAT) (default) 1: The STAT/IB pin is configured as a battery current indicator (IB)
5	R/W	EN_PG_NTC2	1'b0	No	To enable the NTC2 channel, this bit must be set to 1. OTP-configurable. 0: The PG/NTC2 pin is configured as an open-drain power good indicator (PG) (default) 1: The PG/NTC2 pin is configured as a second thermistor input (NTC2)
4	R/W	LOCK_CHG	1'b0	No	After this bit is set to 1, any future writes to VBATT, ICC, IPRE, JEITA_VSET, and JEITA_ISET can only reduce the set values. 0: Not locked (default) 1: The VBATT, ICC, IPRE, JEITA_VSET, and JEITA_ISET values are locked
3	R/W	HOLDOFF_TMR	1'b1	Yes	This bit is OTP-configurable. 0: Disables the hold-off timer 1: Enables the hold-off timer (default)
2:1	R/W	SW_FREQ	2'b01	No	Configures both the buck and boost operating frequencies. OTP-configurable. 00: 750kHz 01: 1MHz (default) 10: 1.25MHz 11: 1.5MHz
0	R/W	EN_VIN_TRK	1'b1	No	When this bit is set to 0, the VIN_LIM register sets the absolute input voltage limit (V_{IN_LIM}) value. When this bit is set to 1, V_{IN_LIM} is the maximum value between VIN_LIM and (V_{BATT} + 165mV). 0: V_{IN_LIM} is fixed 1: V_{IN_LIM} also tracks V_{BATT} (default)

IIN (01h)

The IIN command sets the input current limit (I_{IN_LIM}).

Bits	Access	Bit Name	Default	WTD Reset	Description
7:5	R/W	IIN_MODE	3'b000	No	When setting these bits to 000, I_{IN_LIM} follows the automatically generated I_{IN_LIM} value in bits[4:0] of this command. OTP-configurable. When setting these bits to other values, I_{IN_LIM} is fixed. 000: Follows the setting of bits[4:0] of this command (default) 001: Forces I_{IN_LIM} to 100mA 010: Forces I_{IN_LIM} to 500mA 011: Forces I_{IN_LIM} to 900mA 100: Forces I_{IN_LIM} to 1500mA 101: Forces I_{IN_LIM} to 2000mA 110: Forces I_{IN_LIM} to 3000mA
4:0	R/W	IIN_LIM	5'b00100	No	Sets I_{IN_LIM}. This is automatically updated after input source type detection. The host can overwrite the I_{IN_LIM} value. Range: 100mA (00000) to 3.2A (11111) Offset: 100mA Step: 100mA Default: 500mA (00100)

CHG_PARAMETER0 (02h)

The CHG_PARAMETER0 command sets the pre-charge voltage and fast charge current.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R/W	VPRE	2'b11	No	Sets the pre-charge to fast charge battery voltage threshold. 00: 2.6V 01: 2.8V 10: 3V 11: 3.2V (default)
5:0	R/W	ICC	6'b000001	Yes	Sets the fast charge current. Do not set this value above 2.2A. OTP-configurable. Range: 0mA (000000) to 2.2A (110111) Offset: 0mA Step: 40mA Default: 40mA (000001)

CHG_PARAMETER1 (03h)

The CHG_PARAMETER1 command sets the pre-charge current and termination current.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:4	R/W	IPRE	4'b0001	Yes	Sets the pre-charge current. OTP-configurable. Range: 0mA (0000) to 300mA (1111) Offset: 0mA Step: 20mA Default: 20mA (0001)
3:0	R/W	ITERM	4'b0001	Yes	Sets the termination current. OTP-configurable. Range: 15mA (0000) to 240mA (1111) Offset: 15mA Step: 15mA Default: 30mA (0001)

CHG_PARAMETER2 (04h)

The CHG_PARAMETER2 command sets the recharge threshold, trickle charge current, and V_{IN_LIM}.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R/W	VRECHG	1'b0	Yes	Sets the recharge threshold. 0: 100mV (default) 1: 200mV
6:4	R/W	ITRICKLE	3'b001	Yes	Sets the trickle charge current. OTP-configurable. Range: 0mA (000) to 112mA (111) Offset: 0mA Step: 16mA Default: 16mA (001)
3:0	R/W	VIN_LIM	4'b0110	No	Sets the V_{IN_LIM} threshold. Range: 3.88V (0000) to 5.08V (1111) Offset: 3.88V Step: 80mV Default: 4.36V (0110)

CHG_PARAMETER3 (05h)

The CHG_PARAMETER3 command sets the battery regulation voltage (V_{BATT_REG}) and top-off timer.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R/W	TOPOFF_TMR	2'b00	Yes	Sets the timer to stop charging after charge termination. 00: Disabled (default) 01: 15 minutes 10: 30 minutes 11: 45 minutes
5:0	R/W	VBATT	6'b011000	No	Sets V_{BATT_REG}. Values exceeding 101000 (4.6V) are clamped to 101000. OTP-configurable. Range: 3.6V (000000) to 4.6V (101000) Offset: 3.6V Step: 25mV Default: 4.2V (011000).

CHG_CTRL1 (06h)

The CHG_CTRL1 command sets the system minimum voltage (V_{SYS_MIN}) and thermal regulation threshold.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R	RESERVED	2'b00	No	Reserved.
5:3	R/W	SYS_MIN	3'b100	No	Sets V_{SYS_MIN}. The actual system regulation voltage is this value + V_{TRACK}. OTP-configurable. 000: 2.975V 001: 3.15V 010: 3.325V 011: 3.5V 100: 3.588V (default) 101: 3.675V 110: 3.763V
2:0	R/W	TREG	3'b100	Yes	Sets the thermal regulation threshold for charge mode, as well as the thermal protection threshold for boost mode. 000: 60°C 001: 70°C 010: 80°C 011: 90°C 100: 100°C (default) 101: 110°C 110: 120°C

CHG_CTRL2 (07h)

The CHG_CTRL2 command sets the watchdog timer and charge safety timer.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R/W	IB_EN	1'b0	Yes	Enables IB when only the battery is present, which uses about 3µA of the battery current. 0: IB outputs when the switcher is on (default) 1: IB outputs all the time
6	R/W	WATCHDOG_ RST	1'b0	-	0: No action (default) 1: Resets the watchdog timer
5:4	R/W	WATCHDOG	2'b01	Yes	This bit is OTP-configurable. 00: Disables the timer 01: 40s (default) 10: 80s 11: 160s
3	R/W	EN_TERM	1'b1	Yes	0: Disables termination 1: Enables termination (default)
2	R/W	EN_TMR2X	1'b1	Yes	0: Disables the 2x timer 1: Enables the 2x timer (default)
1:0	R/W	CHG_TIMER	2'b10	Yes	Sets the charge safety timer. 00: Disables the timer 01: 5hrs 10: 10hrs (default) 11: 15hrs

CHG_CTRL3 (08h)

The CHG_CTRL3 command controls the behavior of BATTFET, sets the boost output voltage, and sets the boost current limit.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R/W	BATTFET_DIS	1'b0	No	Shipping mode or over-current protection (OCP). Writing to this bit controls whether the BATTFET is on or off. Reading this bit indicates the BATTFET's status. 0: Allows the BATTFET to remain on (default) 1: Turns off the BATTFET
6	R/W	BATTFET_DLY	1'b1	No	Sets the delay after BATTFET_DIS is set to 1. 0: Turns off the BATTFET immediately 1: Turns off the BATTFET after a 10s delay (default)
5	R/W	BATTFET_ RST_EN	1'b1	Yes	0: Disables the BATTFET reset function 1: Enables the BATTFET reset function (default)
4:3	R/W	OLIM	2'b11	Yes	Sets the boost output current limit. 00: 500mA 01: 1.5A 10: 2.1A 11: 3A (default)
2:0	R/W	VBOOST	3'b111	No	Sets the boost output voltage. OTP-configurable. 011: 5.35V 010: 5.3V 001: 5.25V 000: 5.2V 111: 5.15V (default) 110: 5.1V 101: 5.05V 100: 5V

CHG_CTRL4 (09h)

The CHG_CTRL4 command controls the enable/disable of buck, boost, and charging. It also sets the behavior of the CC1 and CC2 pins.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R	RESERVED	1'b0	No	Reserved.
6:4	R/W	CC_CFG	3'b101	Yes	This bit is OTP-configurable. 000: Enables CC1/CC2 sink mode 101: CC1/CC2 is disabled (default)
3	R	RESERVED	1'b0	Yes	Reserved.
2	R/W	EN_BOOST	1'b0	Yes	0: The boost is disabled (default) 1: The boost is enabled
1	R/W	EN_BUCK	1'b1	Yes	0: The buck is disabled 1: The buck is allowed (default)
0	R/W	EN_CHG	1'b1	Yes	0: Charging is disabled 1: Charging is allowed (default)

VIN_DET (0Ah)

The VIN_DET command controls the behavior of DPDM and CC1/CC2 detection.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R	RESERVED	2'b00	No	Reserved.
5	R/W	AUTODPDM	1'b1	Yes	This bit is OTP-configurable. 0: D+/D- detection starts manually 1: D+/D- detection automatically starts after VIN_GD = 1 and the hold-off timer ends (default)
4	R/W	FORCEDPDM	1'b0	-	This bit returns to 0 after it is written to 1. It is only effective when an input source is applied. 0: Normal (default) 1: Forces D+/D- detection
3:2	R	RESERVED	2'b00	Yes	Reserved.
1:0	R/W	FORCE_CC	2'b11	Yes	This bit is OTP-configurable. 00: The CC1 and CC2 pins are automatically configured via CC_CFG 11: Forces the CC1 and CC2 pins to a high-impedance (Hi-Z) state (default)

CHG_CTRL5 (0Ch)

The CHG_CTRL5 command sets the protection behavior in charge and boost mode.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R	RESERVED	1'b0	No	Reserved.
6	R/W	NTC1_ACTION	1'b0	No	This bit is OTP-configurable. 0: Only generates INT when the NTC1 status changes (default) 1: NTC1 is fully functional
5	R/W	NTC2_ACTION	1'b0	No	This bit is OTP-configurable. 0: Only generates INT when the NTC2 status changes (default) 1: NTC2 is fully functional
4	R/W	BATT_OVP_EN	1'b1	Yes	0: Battery over-voltage protection (OVP) is neglected 1: Battery OVP is enabled (default)
3:2	R/W	BATT_LOW	2'b00	No	If V_{BATT} falls below BATT_LOW, an INT pulse is generated with a 10ms debounce. 00: 3V falling (default) 01: 3.1V falling 10: 3.2V falling 11: 3.3V falling
1	R/W	BOOST_STP_EN	1'b0	Yes	This bit is OTP-configurable. 0: The BATT_LOW comparator only generates INT (default) 1: The BATT_LOW comparator turns off boost operation and latches
0	R/W	BOOST_OTP_EN	1'b1	Yes	This bit is OTP-configurable. 0: Boost over-temperature protection is ignored 1: Boost over-temperature protection occurs at TREG (default)

NTC_ACTION (0Dh)

The NTC_ACTION command sets the NTC protection behavior in the warm and cool windows.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R/W	WARM_ACT	2'b01	No	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 6 on page 21 for more details. 00: No action during an NTC warm condition 01: Reduces V_{BATT_REG} during an NTC warm condition (default) 10: Reduces I_{CC} during an NTC warm condition 11: Reduces both V_{BATT_REG} and I_{CC} during an NTC warm condition
5:4	R/W	COOL_ACT	2'b10	No	If both the NTC1_ACTION and NTC2_ACTION bits are set to 1, see Table 6 on page 21 for more details. 00: No action during an NTC cool condition 01: Reduces V_{BATT_REG} during an NTC cool condition 10: Reduces I_{CC} during an NTC cool condition (default) 11: Reduces both V_{BATT_REG} and I_{CC} during an NTC cool condition
3:2	R/W	JEITA_VSET	2'b00	Yes	00: V_{BATT_REG} - 100mV (default) 01: V_{BATT_REG} - 150mV 10: V_{BATT_REG} - 200mV 11: V_{BATT_REG} - 250mV
1:0	R/W	JEITA_ISET	2'b00	Yes	00: 50% of I_{CC} (default) 01: 33% of I_{CC} 10: 20% of I_{CC}

NTC_TH (0Eh)

The NTC_TH command sets the NTC hot, warm, cool, and cold thresholds.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R/W	VHOT	2'b10	Yes	Sets the hot falling threshold as a percentage of the VRNTC pin voltage (V_{RNTC}). 00: 29.1% (50°C) 01: 25.9% (55°C) 10: 23% (60°C) (default) 11: 20.4% (65°C)
5:4	R/W	VWARM	2'b01	Yes	Sets the warm falling threshold as a percentage of V_{RNTC}. 00: 36.5% (40°C) 01: 32.6% (45°C) (default) 10: 29.1% (50°C) 11: 25.9% (55°C)
3:2	R/W	VCOOL	2'b10	Yes	Sets the cool rising threshold as a percentage of V_{RNTC}. 00: 74.2% (0°C) 01: 69.6% (5°C) 10: 64.8% (10°C) (default) 11: 59.9% (15°C)
1:0	R/W	VCOLD	2'b01	Yes	Sets the cold rising threshold as a percentage of V_{RNTC}. 00: 78.4% (-5°C) 01: 74.2% (0°C) (default) 10: 69.6% (5°C) 11: 64.8% (10°C)

VIN_IMPD (0Fh)

The VIN_IMPD command sets the parameters of the input impedance test.

Bits	Access	Bit Name	Default	WTD Reset	Description
7	R	RESERVED	1'b0	No	Reserved.
6	R/W	VIN_SRC_EN	1'b0	Yes	Enables the input impedance test. 0: Normal (default) 1: Sources current to the IN pin
5:2	R/W	IVIN_SRC	4'b0000	Yes	Configures the input impedance test current source. 0000: 5µA (default) 0001: 10µA 0010: 20µA 0011: 40µA 0100: 80µA 0101: 160µA 0110: 320µA 0111: 640µA 1000: 1280µA
1:0	R/W	VIN_TEST	2'b00	Yes	Configures the input impedance test comparator threshold. 00: 0.3V (default) 01: 0.5V 10: 1V 11: 1.5V

INT_MASK (10h)

The INT_MASK command sets the mask for each interrupt.

Bits	Access	Bit Name	Default	WTD Reset	Description
7:6	R	RESERVED	2'b01	No	Reserved.
5	R/W	MASK_THERM	1'b0	No	This bit is OTP-configurable. 0: Enables the THERM_STAT INT pulse (default) 1: Masks the THERM_STAT INT pulse
4	R/W	MASK_DPM	1'b0	No	0: Enables the VINDPM and IINDPM INT pulses (default) 1: Masks the VINDPM and IINDPM INT pulses
3	R/W	MASK_TOPOFF	1'b0	No	0: Enables the top-off timer INT pulse (default) 1: Masks the top-off timer INT pulse
2	R/W	MASK_CC_INT	1'b1	No	This bit is OTP-configurable. 0: Enables the CC_SNK INT pulse 1: Masks the CC_SNK INT pulse (default)
1	R/W	MASK_BATT_LOW	1'b0	No	0: Enables the BATT_LOW INT pulse (default) 1: Masks the BATT_LOW INT pulse
0	R/W	MASK_DEBUG	1'b0	No	0: Allows the DEBUGACC INT pulse (default) 1: Masks the DEBUGACC INT pulse

STATUS BYTES (11h~16h)

Legend: POR = default value; R/W = read/write; R = read-only; INT = interrupt; YM = the interrupt can be masked

STATUS0 (11h)

The STATUS0 command indicates charger operation status register 0.

Bits	Access	Bit Name	Default	INT	Description
7:4	R	DPDM_STAT	-	No	Returns the input source D+/D- detection result. 0000: Not started (500mA) 0001: USB standard downstream port (SDP) (500mA) 0010: USB dedicated charging port (DCP) (2A) 0011: USB charging downstream port (CDP) (1.5A) 0100: Divider 1 (1A) 0101: Divider 2 (2.1A) 0110: Divider 3 (2.4A) 0111: Divider 4 (2A) 1000: Unknown (500mA) 1001: USB DCP (2A) 1110: Divider 5 (3A)
3:2	R	RESERVED	-	No	Reserved.
1	R	VINDPM_STAT	-	YM	0: Not in VINDPM 1: In VINDPM
0	R	IINDPM_STAT	-	YM	0: Not in IINDPM 1: In IINDPM

STATUS1 (12h)

The STATUS1 command indicates charger operation status register 1.

Bits	Access	Bit Name	Default	INT	Description
7	R	RESERVED	-	No	Reserved.
6	R	VIN_GD	-	Yes	When $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVP}$ in buck mode, this bit is set to 1, and the PG/NTC2 pin is driven low (after a 15ms debounce time). 0: The input source is not valid 1: The input source is good
5	R	VIN_RDY	-	Yes	Indicates whether input source type detection has finished. IIN_LIM is updated. 0: V_{IN} is not ready to charge 1: V_{IN} is ready to charge
4	R	LEGACYCABLE	-	No	0: Normal 1: The legacy cable is detected
3	R	THERM_STAT	-	YM	0: Not in thermal regulation 1: In thermal regulation
2	R	VSYS_STAT	-	No	0: $V_{BATT} < V_{SYS\_MIN}$ 1: $V_{BATT} > V_{SYS\_MIN}$
1	R	WATCHDOG_FAULT	-	Yes	0: Normal 1: The watchdog timer has expired
0	R	WATCHDOG_BARK	-	Yes	0: Normal 1: The 3/4 watchdog timer has expired

STATUS2 (13h)

The STATUS2 command indicates charger operation status register 2.

Bits	Access	Bit Name	Default	INT	Description
7:5	R	CHG_STAT	-	No	000: Not charging 001: Trickle charge 010: Pre-charge 011: Fast charge 100: Constant-voltage charge 101: Charging is done
4:2	R	BOOST_ FAULT	-	Yes	000: Normal 001: An IN overload or short (latch-off) has occurred 010: Boost OVP (not latch) has occurred 011: Boost over-temperature protection (latch-off) has occurred 100: The boost stops due to BATT_LOW (latch-off)
1:0	R	CHG_FAULT	-	Yes	00: Normal 01: Input OVP 10: The charge timer has expired 11: Battery OVP

STATUS3 (14h)

The STATUS3 command indicates charger operation status register 3.

Bits	Access	Bit Name	Default	INT	Description
7	R	NTC_MISSING	-	Yes	0: Normal 1: NTC is missing (V_{NTC} > 95% of V_{RNTC})
6	R	BATT_ MISSING	-	Yes	0: Normal 1: The battery is missing (two terminations detected within 3s)
5:3	R	NTC1_FAULT	-	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot
2:0	R	NTC2_FAULT	-	Yes	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot

STATUS4 (15h)

The STATUS4 command indicates charger operation status register 4.

Bits	Access	Bit Name	Default	INT	Description
7:6	R	CC1_SNK_ STAT	-	YM	A glitch in the CC pin debounce time for PD ($t_{PD\_DEBOUNCE}$) does not affect this result. 00: CC1 detects vRa 01: CC1 detects vRd-USB 10: CC1 detects vRd-1.5 11: CC1 detects vRd-3.0
5:4	R	CC2_SNK_ STAT	-	YM	A glitch in $t_{PD\_DEBOUNCE}$ does not affect this result. 00: CC2 detects vRa 01: CC2 detects vRd-USB 10: CC2 detects vRd-1.5 11: CC2 detects vRd-3.0
3:0	R	RESERVED	-	No	Reserved.

STATUS5 (16h)

The STATUS5 command indicates charger operation status register 5.

Bits	Access	Bit Name	Default	INT	Description
7	R	RESERVED	-	No	Reserved.
6	R	TOPOFF_ ACTIVE	-	YM	0: The top-off timer is not counting 1: The top-off timer is counting
5	R	BFET_STAT	-	No	0: The battery is charging or disabled 1: The battery is discharging
4	R	BATT_LOW_ STAT	-	YM	The hysteresis is 200mV. 0: V_{BATT} exceeds BATT_LOW 1: V_{BATT} is below BATT_LOW
3	R	RESERVED	-	No	Reserved.
2	R	VIN_TEST_ HIGH	-	Yes	0: V_{IN} is below the VIN_TEST threshold 1: V_{IN} has reached the VIN_TEST threshold
1	R	DEBUGACC	-	YM	0: Normal 1: Enters DebugAccessory.SNK state
0	R	RESERVED	-	No	Reserved.

INTERRUPT LIST

INT Name	Related Registers	Can Be Masked	Event
VIN_GD	VIN_GD changes	No	A good input source has been detected.
DPDM_DET_DONE	DPDM_STAT changes	No	DPDM detection is finished.
VIN_RDY	VIN_RDY: 0 to 1	No	I_{IN_LIM} has been updated; the buck converter has started.
CHG_DONE	CHG_STAT: any value to 101	No	Charging has terminated.
RECHARGE	CHG_STAT exits 101 and enters the CC/CV charge	No	Recharging has been initiated.
THERM_STAT	THERM_STAT: 0 to 1	Yes	The IC has entered charge thermal regulation.
WATCHDOG_FAULT	WATCHDOG_FAULT: 0 to 1	No	A watchdog timeout has occurred.
WATCHDOG_BARK	WATCHDOG_BARK: 0 to 1	No	A watchdog bark has occurred.
CHG_FAULT	CHG_FAULT: • 00 to 01 • 00 to 10 • 00 to 11	No	One of the following charge faults has occurred: input OVP, battery OVP, or the charge timer has expired.
NTC_MISSING	NTC_MISSING changes	No	NTC is missing.
BATT_MISSING	BATT_MISSING changes	No	BATT is missing.
BOOST_FAULT	BOOST_FAULT: • 000 to 001 • 000 to 010 • 010 to 000 • 000 to 011 • 000 to 100	No	One of the following boost faults has occurred: IN overloaded or short, boost OVP, boost over-temperature protection, or boost stops due to BATT_LOW.
NTC_FAULT	NTC1_FAULT or NTC2_FAULT changes	No	The NTC status has changed.
VINDPM_STAT	VINDPM_STAT: 0 to 1	Yes	The V_{IN} regulation loop has been entered.
IINDPM_STAT	IINDPM_STAT: 0 to 1		The I_{IN} regulation loop has been entered.
TOPOFF_TMR	TOPOFF_ACTIVE changes	Yes	The top-off timer has started and ended.
CC_SNK	CC1_SNK_STAT or CC2_SNK_STATchanges	Yes	vRd connect has been detected or the source current advertisement has changed.
BATT_LOW	BATT_LOW_STAT: 0 to 1	Yes	V_{BATT} has dropped to the BATT_LOW threshold.
VIN_TEST_HIGH	VIN_TEST_HIGH: 0 to 1	No	V_{IN} has reached the VIN_TEST threshold during the input impedance test.
DEBUGACC	DEBUGACC changes	Yes	DebugAccessory.SNK state entry/exit.

ONE-TIME PROGRAMMABLE (OTP) MAP

The MP2724 provides a one-time programmable (OTP) function to configure the default values for certain registers. The OTP map below shows the OTP-configurable commands.

<table>
<tr><th>Reg #</th><th>Bit[7]</th><th>Bit[6]</th><th>Bit[5]</th><th>Bit[4]</th><th>Bit[3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr>
<tr><td>00h</td><td>N/A</td><td>EN_STAT_IB</td><td>EN_PG_NTC2</td><td>N/A</td><td>HOLDOFF_TMR</td><td colspan="2">SW_FREQ</td><td>N/A</td></tr>
<tr><td>01h</td><td colspan="3">IIN_MODE</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>02h</td><td>N/A</td><td>N/A</td><td colspan="6">ICC</td></tr>
<tr><td>03h</td><td colspan="4">IPRE</td><td colspan="4">ITERM</td></tr>
<tr><td>04h</td><td>N/A</td><td colspan="3">ITRICKLE</td><td colspan="4">N/A</td></tr>
<tr><td>05h</td><td>N/A</td><td>N/A</td><td colspan="6">VBATT</td></tr>
<tr><td>06h</td><td>N/A</td><td>N/A</td><td colspan="3">SYS_MIN</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>07h</td><td>N/A</td><td>N/A</td><td colspan="2">WATCHDOG</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>08h</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="3">VBOOST</td></tr>
<tr><td>09h</td><td>N/A</td><td colspan="3">CC_CFG</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>0Ah</td><td colspan="2">N/A</td><td>AUTODPDM</td><td>N/A</td><td>N/A</td><td>N/A</td><td colspan="2">FORCE_CC</td></tr>
<tr><td>0Ch</td><td>N/A</td><td>NTC1_ACTION</td><td>NTC2_ACTION</td><td>N/A</td><td>N/A</td><td>N/A</td><td>BOOST_STP_EN</td><td>BOOST_OTP_EN</td></tr>
<tr><td>10h</td><td>N/A</td><td>N/A</td><td>MASK_THERM</td><td>N/A</td><td>N/A</td><td>MASK_CC_INT</td><td>N/A</td><td>N/A</td></tr>
</table>

ONE-TIME PROGRAMMABLE (OTP) DEFAULT

OTP Items	Default
EN_STAT_IB	0: STAT
EN_PG_NTC2	0: PG
HOLDOFF_TMR	1: Enables the hold-off timer
SW_FREQ	01: 1MHz
IIN_MODE	000: Follows the IIN_LIM setting
ICC	000001: 40mA
IPRE	0001: 20mA
ITERM	0001: 30mA
ITRICKLE	001: 16mA
VBATT	011000: 4.2V
SYS_MIN	100: 3.588V
WATCHDOG	01: 40s
VBOOST	111: 5.15V
CC_CFG	101: Disabled
AUTODPDM	1: D+/D- detection automatically starts
FORCE_CC	11: Forces CC1/CC2 to Hi-Z
NTC1_ACTION	0: INT only
NTC2_ACTION	0: INT only
BOOST_STP_EN	0: The BATT_LOW comparator only generates INT
BOOST_OTP_EN	1: Boost operation stops when TREG occurs
MASK_THERM	0: Allows INT
MASK_CC_INT	1: Masks INT

APPLICATION INFORMATION

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor corresponds to a smaller size, however, it also results in a higher current ripple, magnetic hysteretic losses, and output capacitances. A higher-value inductor results in a lower ripple current and smaller output filter capacitors; however, it also results in higher inductor DC resistance (DCR) loss.

The required inductance (L) can be estimated with Equation (1):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L\_MAX}} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}} \quad (1)$$

Where V_{SYS} is the converter's output voltage, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is typically designed to be 20% to 40% of the maximum load current.

Choose an inductor that does not saturate under the worst-case load condition, which can be calculated with Equation (2):

$$I_{SAT} > I_{LOAD} + \frac{\Delta I_{L\_MAX}}{2} \quad (2)$$

Where I_{SAT} is the inductor saturation current, and I_{LOAD} is the buck converter's maximum load.

Selecting the PMID Capacitor (C_{PMID})

The PMID capacitor (C_{PMID}) decouples the switching buck converter and absorbs the switching ripple current. Select C_{PMID} based on the demand for the PMID current ripple. The input current ripple (I_{RMS_MAX}) can be calculated with Equation (3):

$$I_{RMS\_MAX} = I_{LOAD} \times \frac{\sqrt{V_{SYS} \times (V_{IN} - V_{SYS})}}{V_{IN}} \quad (3)$$

Use low-ESR ceramic capacitors with an X7R or X5R rating for C_{PMID}. This capacitor should be placed as close to the PMID and PGND pins as possible. The capacitor's voltage rating must exceed V_{IN}, and it is recommended to consider the plug-in overshoot voltage. A capacitor rated for at least 25V is recommended for applications with a 15V V_{IN}. Generally, a capacitance of 10µF is considered a sufficient starting value.

PCB Layout Guidelines

PCB layout is important to meet the specified noise, efficiency, and stability requirements. For the best results, refer to Figure 15 and Figure 16, and follow the guidelines below:

1. Place C_{PMID} as close as possible to the PMID and PGND pins using a short copper plane connection.
2. Place C_{PMID} on the same layer as the IC.
3. Minimize the high-frequency current path loop between C_{PMID} and the buck converter power MOSFETs (from the PMID pin to the capacitor to ground) (see Figure 15).

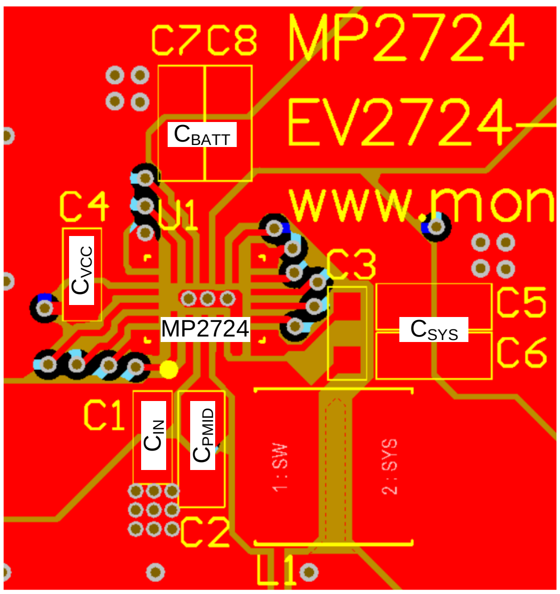


Figure 15: Recommended Layout for Decoupling Capacitors

4. Place the inductor's input terminal as close as possible to the SW pin.
5. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation, and ensure that the trace is wide enough to carry the charging current.
6. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
7. Place decoupling capacitors (e.g. the VCC pin capacitor) as close as possible to the IC pins, and make the connection as short as possible (see Figure 15).
8. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
9. Ensure that the number and physical size of the vias are sufficient for a current path.
10. Figure 16 shows a high-frequency current path, where the high-frequency path (the high-side MOSFET, low-side MOSFET, and C_{PMID}) must be minimized.

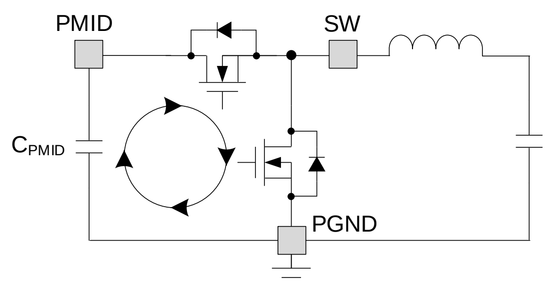


Figure 16: High-Frequency Current Path

TYPICAL APPLICATION CIRCUIT

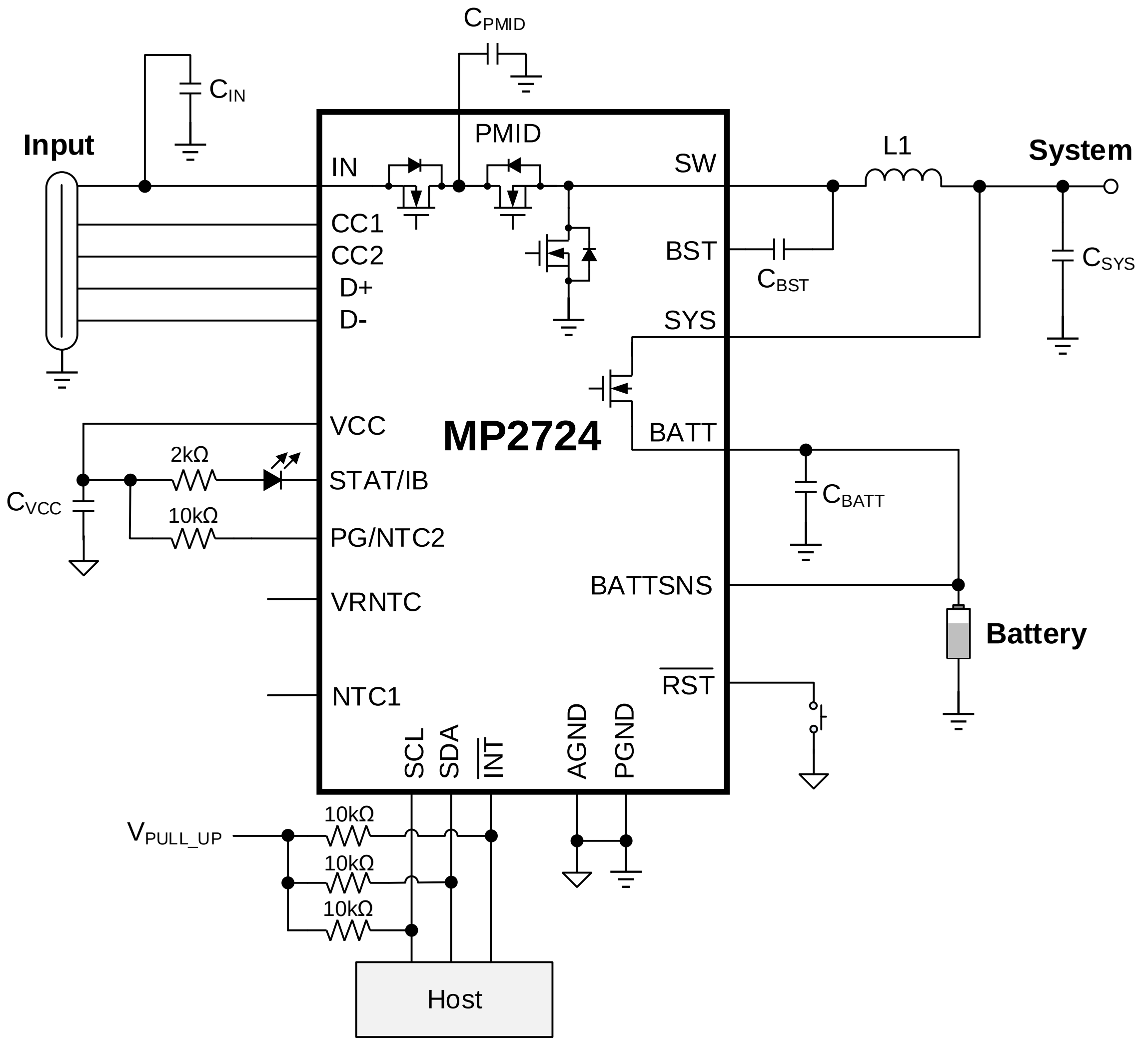


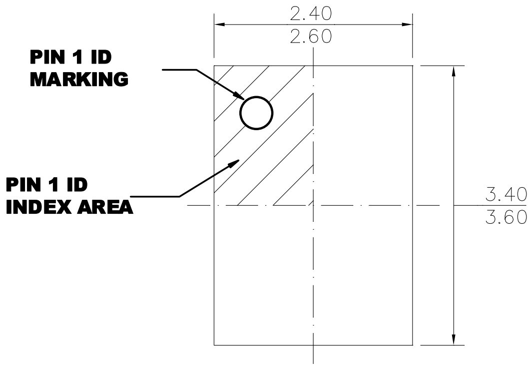
Figure 17: Typical Application Circuit

Table 8: Key BOM for Typical Application Circuit

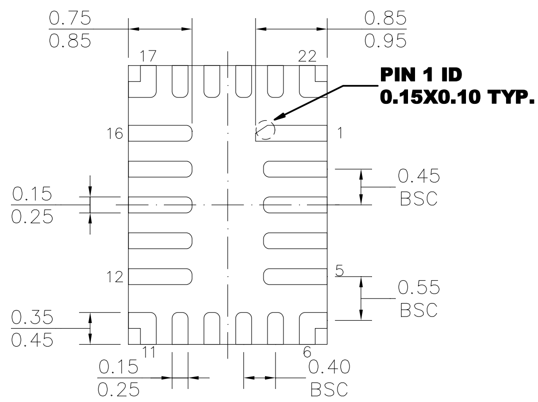
Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C_{PMID}	10µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
2	C_{SYS}	10µF x 2	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	10µF x 2	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{VCC}	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	22nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1µH	Inductor, 1µH, low DCR	SMD	Any

PACKAGE INFORMATION

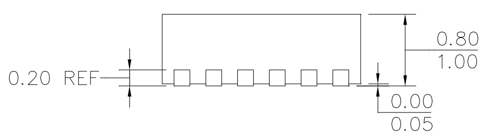
QFN-22 (2.5mmx3.5mm)



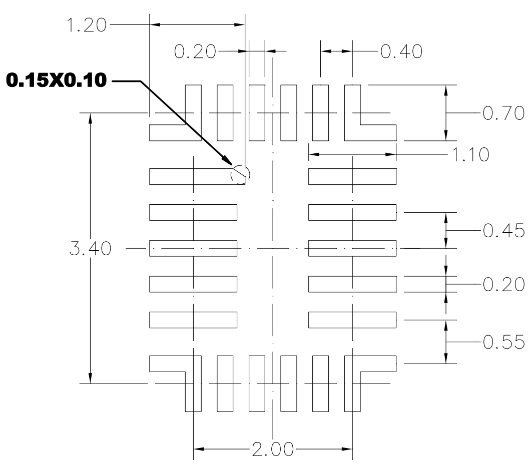
TOP VIEW



BOTTOM VIEW



SIDE VIEW

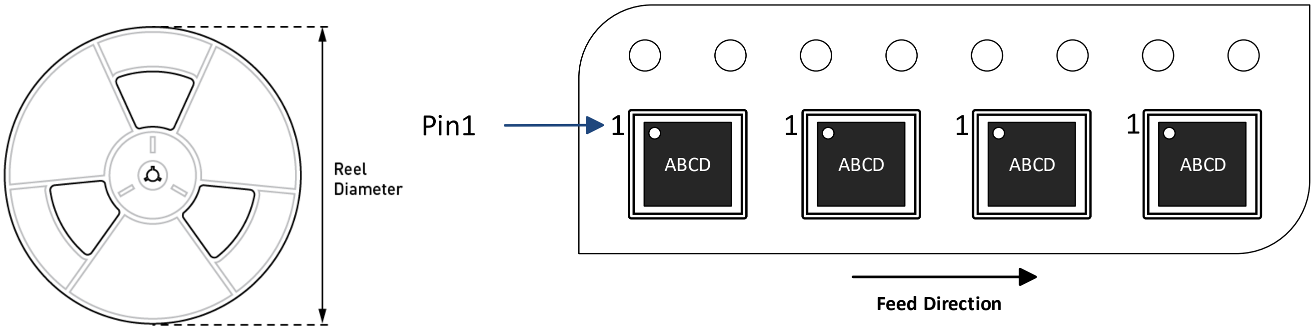


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2724GRH-xxxx-Z	QFN-22 (2.5mmx 3.5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/29/2024	Initial Release	-