SECO-NCD5700-GEVB

NCD5700 mini Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Purpose

This document describes the use and applications for the NCD5700 gate driver mini board. The board is designed on a two layer PCB and includes the NCD5700 driver and all the necessary drive circuitry including isolation as can be seen in Figure 3. The board also includes ability to solder any MOSFET or SiC MOSFET in a TO−247 high voltage package and compatibility with SECO−GDBB−GEVB baseboard for out−of−the−box evaluation. The board does not include a power stage and is generic from the point of view that it is not optimized to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these boards can be configured in a totem pole type drive configuration. The boards can be considered as an isolator+driver+TO−247 discrete module.

NCD5700 Description

The NCD5700 is a high−current, high−performance stand−alone IGBT driver for high power applications that include solar inverters, motor control and uninterruptable power supplies. The device offers a cost−effective solution by eliminating many external components. Device protection features include Active Miller Clamp, accurate

UVLO, EN input, DESAT protection and Active Low FAULT output. The driver also features an accurate 5.0 V output and separate high and low (VOH and VOL) driver outputs for system design convenience. The driver is designed to accommodate a wide voltage range of bias supplies including unipolar and bipolar voltages. It is available in a 16−pin SOIC package. The simplified block diagram is shown in Figure 4.

Collaterals

- SECO−NCD5700−GEVB
- SECO−GDBB−GEVB

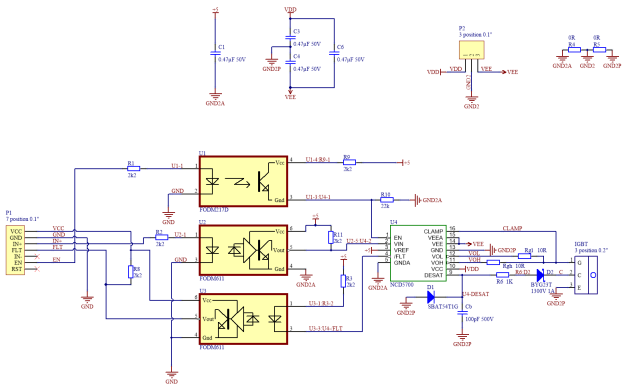


Figure 3. NCD5700 mini Board Schematic



Figure 1. SECO−NCD5700−GEVB

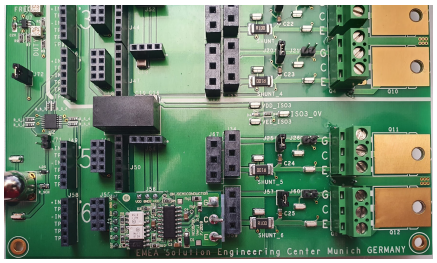


Figure 2. Board Plugged into SECO−GDBB−EVB

Features

- Galvanic Isolated Gate Driver Circuit
- Demonstrates NCD5700 Driver with Advanced Features
- Replaceable Load Capacitor and Gate Resistor for different Load Conditions
- Plug−and−Play Testing with SECO−GDBB−GEVB as seen in Figure 6
- Minimized Form−factor for Embedding and Testing in Application Boards or New Designs
- Custom Voltage Levels with External Power Supply

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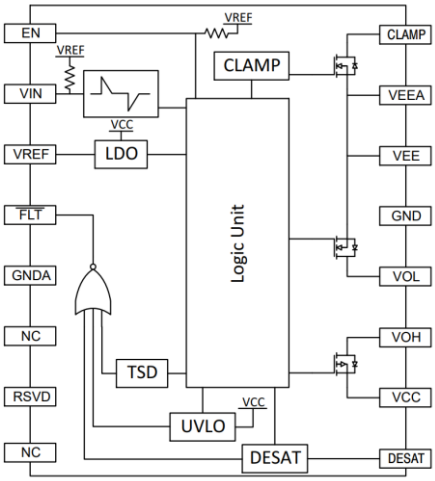


Figure 4. Simplified NCD5700 Block Diagram

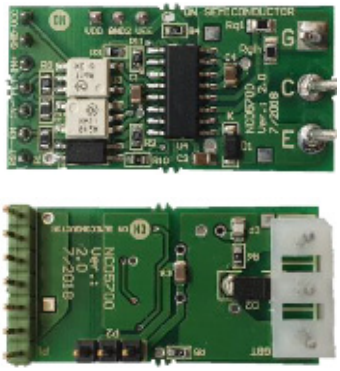


Figure 5. NCD5700 mini Board − Top and Bottom View

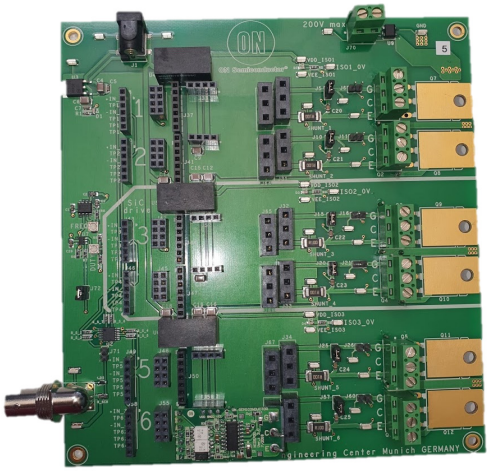


Figure 6. NCD5700 Connected to SECO−GDBB−GEVB Auxiliary Evaluation Board

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Table 1. NCD5700 mini BOARD BOM

Reference Designators	Qty per PCB	Value	Description	Notes
C1, C3, C4, C6	4	0.47 μF 50 V	0.47 μF 50 V Ceramic Capacitor X7R 0805 (2012 Metric) 0.079” L x 0.049” W (2.00 mm x 1.25 mm)	
Cb	1	100 pF 500 V	100 pF 500 V Ceramic Capacitor C0G, NP0 0805 (2012 Metric) 0.079” L x 0.049” W (2.00 mm x 1.25 mm)	
D1	1	SBATS4T1G	Diode Schottky 30 V 200 mA (DC) Surface Mount SOD−123	
D2	1	1300 V 1 A	Diode Avalanche 1300V 1A (DC) Surface Mount DO−214AC (SMA)	
IGBT	1	3 position 0.2”	Connector Header Through Hole 3 position 0.200” (5.08 mm)	Not assembly
P1	1	7 position 0.1”	Connector Header Through Hole 7 position 0.100” (2.54 mm)	Not assembly
P2	1	3 position 0.1”	Connector Header Through Hole 3 position 0.100” (2.54 mm)	Not assembly
R1, R2, R3, R8, R9, R11	6	2k2	2.2 kΩ ±5% 0.25 W, 1/4 W Chip Resistor 0603 (1608 Metric) Automotive AEC−Q200, Pulse Withstanding Thick Film	
R4, R5	2	0R	0 Ω Jumper 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC−Q200 Thick Film	
R6	1	1K	1 kΩ ±5% 0.25 W, 1/4 W Chip Resistor 0603 (1608 Metric) Automotive AEC−Q200, Pulse Withstanding Thick Film	
R10	1	22k	22 kΩ ±5% 0.25 W, 1/4 W Chip Resistor 0603 (1608 Metric) Automotive AEC−Q200, Pulse Withstanding Thick Film	
Rgh, Rgl	2	10R	10 Ω ±1% 0.5 W, 1/2 W Chip Resistor 0805 (2012 Metric) Automotive AEC−Q200, Pulse Withstanding Thick Film	
U1	1	FODM217D	Optoisolator Transistor Output 3750 Vrms 1 Channel 4−SOP	
U2, U3	2	FODM611	Logic Output Optoisolator 10 Mbps Open Collector, Schottky Clamped 3750 Vrms 1 Channel 20 kV/μs CMTI 5−Mini−Flat	
U4	1	NCD5700	High−Side or Low−Side Gate Driver IC 16−SOIC	

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PCB Assembly and Layers

Figure 5 and Figure 7 shows the top and bottom real/assembly view of the PCB. The PCB is 35 mm x 18 mm x 1 mm (length x width x height) where the width of the PCB is approximately the width of a TO − 247 body. As a default two header connectors (P1 and P2) and power connecter we call IGBT are not assembly because of versatility of suggested concept of mainboards. This is depicted within BOM list in Table 1.

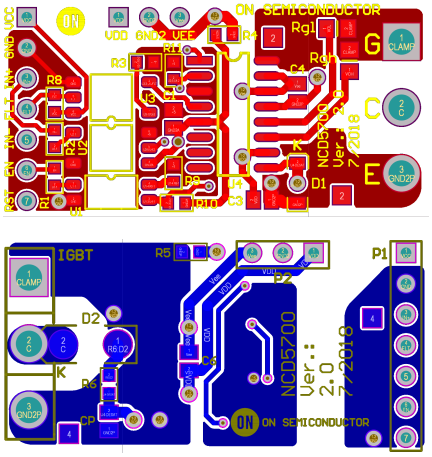


Figure 7. NCD5700 mini Board TOP/BOTTOM Layout Drawing

I/O Connectors

There are 3 I/O connectors including 13 pins described in Table 2 below. The signals on low voltage side are noted as “primary” ground referenced. There is no true “primary” and “secondary” ground but there is galvanic isolation across the isolation boundary. It is especially important to maintain isolation in high−side, high−voltage, switching applications where the “secondary” Vdd (P2.1) above the power supply input voltage (P1.1).

Table 2. I/O CONNECTOR DESCRIPTIONS

Ref Des	Name	I/O	GND Ref	Description	Value [V]
P1.1	VCC	Power	Primary	Positive primary power supply	5
P1.2	GND	Power	Primary	Ground	0
P1.3	IN+	Input	Primary	Non−inverting PWM input	0 − 3.3 (5)
P1.4	FLT	Output	Primary	Fault flag	0 − 5 (3.3)
P1.5	NC	NC	NC	No Connect	NC
P1.6	EN	Input	Primary	Enable signal	0 − 5 (3.3)
P1.7	NA	NA	NA	NA	NA
P2.1	VDD	Power	Secondary	Positive branch power supply	< 20
P2.2	GND2	Power	Secondary	Ground of the power supply	0
P2.3	VEE	Power	Secondary	Negative branch of power supply	> −10
IGBT (G, G)	Gate	Output	Secondary	Gate pin of a power switch	< 20
IGBT (C, D)	Collector	Output	Secondary	Collector (drain) pin of a power switch	≤ 1200
IGBT (E, S)	Emitter	Output	Secondary	Emitter (source) pin of a power switch	0

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Mounting into Existing PCB

The board can be mounted into an existing power board, shown as “Main PCB” in Figure 6. If there are no components or low profile surface mount components only, the mini SMD EVB can be mounted parallel to the main PCB as shown in Figure 6. The TO−247, power device leads would pass through the mini EVB plated thru−holes and into the main PCB. Or, if necessary, the gate lead of the TO−247, power device can be soldered to the plated thru−hole on the EVB and cut so that it does not contact the main PCB. For mechanical strength, it is preferred that the TO−247 gate lead pass through both PCB’s. This configuration is helpful for already existing application with horizontal TO−247 positions.

Recommended procedure for Option 1 Mounting into an existing PCB:

1. On the main PCB, isolate the gate drive to the TO−247. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Place Kapton or non−conductive tape over the main PCB area directly beneath the EVB. This is to avoid the possibility of having any components on the bottom of the mini SMD EVB touch components or conductive surfaces on the main PCB.
5. Solder a flying lead of bus wire to the main PCB, PWM signal and so on. Make sure there is enough length of the PWM input (flying lead) to reach through the EVB.
6. Solder the TO−247 through just the EVB first
7. With the TO−247 installed into the EVB, install and solder the TO−247 leads into the main PCB.
8. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
9. Using the same size bus wire, solder the remaining connections between the EVB to the appropriate locations on the main PCB.
10. Solder flying leads for bias voltage. Note that P2 are across the isolation boundary from.

Mounting into Existing PCB − Option 2

If components mounted on the main PCB interfere with mounting the EVB as described by Option 1 (Figure 8), the TO−247 leads can be formed (lead length may need to be added) with the EVB mounted perpendicular to the main PCB as shown in Figure 9. If required, both mounting options allow the application of a heat sink to the TO−247 package. If high dv/dt is present on the drain of the TO−247, the EVB should be angled, away from being parallel to the TO−247, as much as possible.

1. On the main PCB, isolate the gate drive to the TO−247 power device. If the existing design includes a gate drive resistor, removing it should serve the purpose of isolating the gate drive to the TO−247. If there is no series component between the PWM signal source and the TO−247 gate lead, the gate drive PCB track will need to be cut.
2. Measure the resistance between the PWM source and the TO−247 gate lead (or PWM source to gate drive transformer/isolator if applicable). Verify reading is high impedance (open).
3. If a TO−247 discrete is installed in the main PCB, remove it now.
4. Solder a flying lead of bus wire to the main PCB, PWM signal. Make sure there is enough length of the PWM input (flying lead) to reach through the mini EVB plated thru−hole.
5. After the TO−247 leads have been formed, check for fit through the EVB and down into the main PCB
6. Solder the TO−247 through just the EVB first
7. With the TO−247 installed into the EVB, install and solder the TO−247 leads into the main PCB
8. Solder the other end of the PWM input (flying lead) to IN+ for non−inverting PWM applications or IN− for inverting PWM applications.
9. Using the same size bus wire, solder the remaining connections between EVB to the appropriate locations on the main PCB.
10. Solder flying leads from bias voltage to the EVB. Note that power supply connector is across the isolation boundary.

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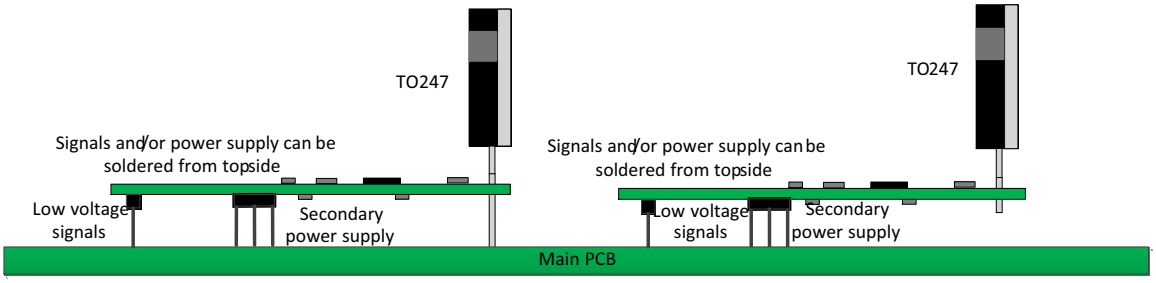


Figure 8. Mounting into Existing PCB

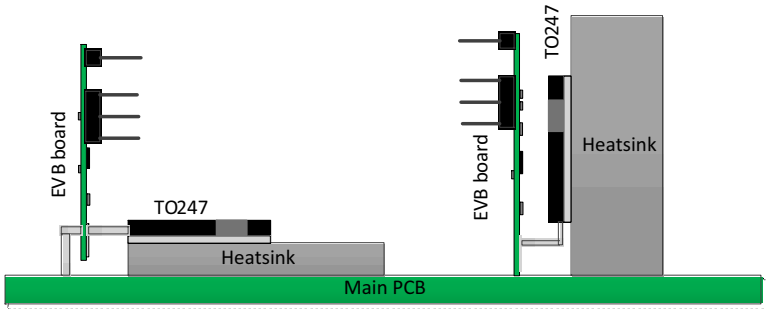


Figure 9. EVB Board Installations

Mounting into New PCB Design

The EVB can also be used as an isolator+driver+TO−247 “driver module” that can be integrated into a new PCB design. The gate lead of the TO−247 between the EVB and the main PCB is for mechanical strength only. For main PCB layout, the gate lead extends down through the main PCB and can be soldered to an isolated plated thru−hole. As shown in Figure 10, shoulder pins with appropriate flange are one option that can be used as mounting pins between mini EVB and the main PCB. In the case new design Figure 11 all needed for footprint design.

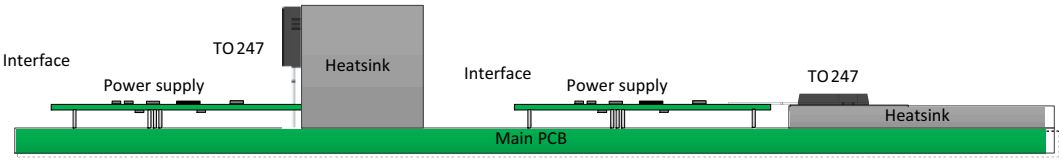


Figure 10. NCD5700 SMD mini Board New Design Installations

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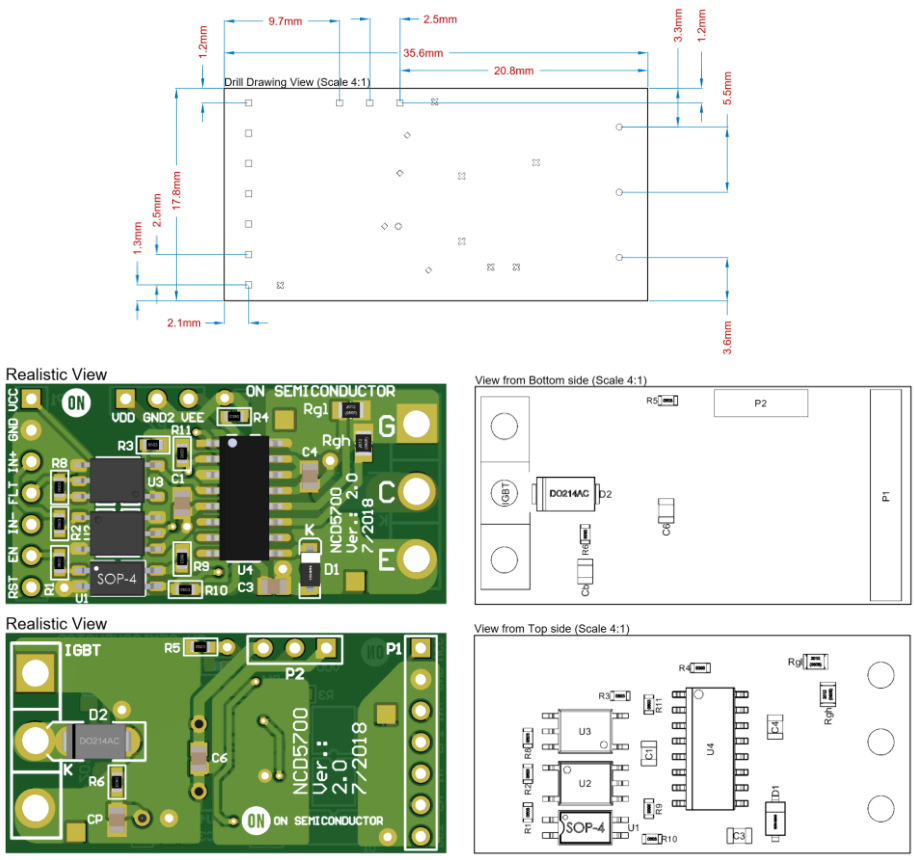


Figure 11. EVB's PCB Mechanical Data

Testing without Installing into a PCB

The EVB can also be tested without installing into a main PCB. However, since this EVB was designed for small form factor there are no test points included for connecting voltage probes. The EVB should be hand probed carefully since the components are very fine pitch or flying leads connected to desired probe points can be attached. The 20 Vdc bias (Vcc2 and Gnd2) is on the secondary side of the isolated gate driver IC and therefore has a separate/isolated return ground from the 5 Vdc bias (Vcc1 and Gnd2). The recommended series load of below 4.7 nF and 4.7 Ω is close to what might be representative of a power switch gate drive input impedance. Leaded passive components can be soldered into the TO−247 holes as shown in Figure 12. Alternatively, a TO−247 power switch can also be soldered in place and used as a load for the gate driver board. Note that testing without installing into a power stage, leaves the DESAT pin open since there is no active drain signal. The effect of operating DESAT this way is explained in section 'DESAT'.

Testing with Gate Driver Base Board

Another very easy way how to test and evaluate more mini boards at same time is to use dedicated base board containing all necessary for easy use. Figure 13 shows typical example where we only need scope for detail waveform analyzing and precise measurement. The base board makes possible connect up to 200 V voltage for power device loading to see impact of non−linear miller capacity to driving performance.

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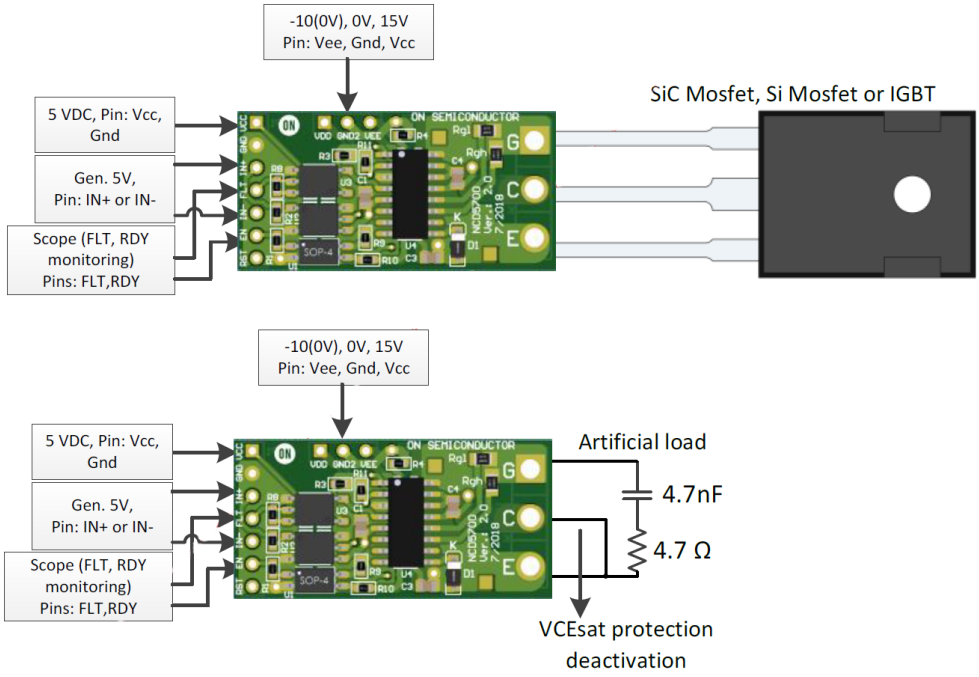
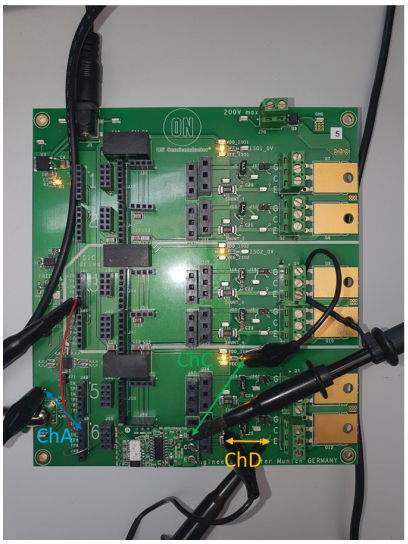


Figure 12. Test Configuration of EVB without Installing into Main or Base PCB



ChA: Measure voltage across J58.1 and GND on test point close to BNC connector

ChC: Measure voltage across G pin on the DUT and ISO GND on test point ISO3_0V

ChD: Measure voltage across shunt resistor SHUNT_6

Figure 13. An Example How to Use Extended Mother Board (SECO−GDBB−EVB) for Gate Drive Mini Boards Testing and Evaluating

DESAT Setup

This feature monitors the collector−emitter voltage of the IGBT in the turned−on state. When the IGBT is fully turned on, it operates in a saturation region. Its collector−emitter voltage (called saturation voltage) is usually low, well below 3 V for most modern IGBTs. It could indicate an overcurrent or similar stress event on the IGBT if the collector−emitter voltage rises above the saturation voltage, after the IGBT is fully turned on. Therefore the DESAT protection circuit compares the collector−emitter voltage with a voltage level $V_{DESAT(TH)}$ to check if the IGBT didn't leave the saturation region. It will activate FLT output and shut down driver output (thus turn−off the IGBT), if the saturation voltage rises above the $V_{DESAT(TH)}$. This protection works on every turn−on phase of the IGBT switching period. At the beginning of turning−on of the IGBT, the collector−emitter voltage is much higher than the saturation voltage level which is present after the IGBT is fully turned on. It takes almost 1 μs between the start of the IGBT turn−on and the moment when the collector−emitter voltage falls to the saturation level. Therefore the comparison is delayed by a configurable time period (blanking time) to prevent false triggering of DESAT protection before the IGBT collector−emitter voltage falls below the saturation level.

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Blanking time is set by the value of the capacitor Cb. At the turned−off output state of the driver, the DESAT pin is shorted to ground via the discharging transistor. Therefore, the inverting input holds the comparator output at low level. At the turned−on output state of the driver, the current IDESAT−CHG from current source starts to flow to the blanking capacitor Cb, connected to DESAT pin. Appropriate value of this capacitor has to be selected to ensure that the DESAT pin voltage does not rise above the threshold level $V_{DESAT(TH)}$ before the IGBT fully turns on.

DESAT is a type of short circuit or/and over−current protection dedicated to monitoring the $I_D \cdot R_{DS}$ of the MOSFET.

The EVB is preconfigured with R6 = 1 kΩ (DESAT resistor). The internal DESAT threshold is fixed at $V_{DESAT(TH)}$ = 6.35 V and the DESAT signal amplitude is adjustable by R6 and HV diode connected in series with R6. R6 = 1 kΩ may not be the correct resistor value for some applications. If V_{DESAT} > 6.35 V during normal operation, decrease R6 to lower the signal amplitude. If DESAT is active, the output is driven low. Further, the /FLT output is activated, please refer to datasheet for more details.

Basic Measurement

Figure 13 shows basic gate driver board connected to base board. Very easily can be evaluated time delays, maximal gate current capability or maximal switch frequency before thermal runaway at given condition and similar. Typically we can measure time between fault event and FLT pin reaction. Typical task is to compare different part numbers at same time and/or same condition to see “online” all, for application, important behaviors. Figure 14 and Figure 15 show typical waveforms helps us to understand any gate driver behavior and optimize gate driving processes.

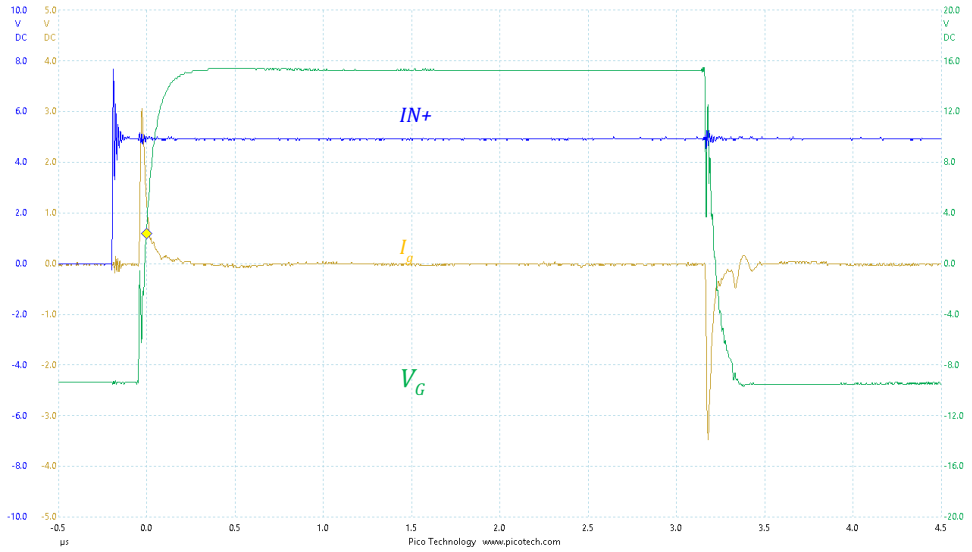


Figure 14. Normal Operation for Turn−on and Turn−off

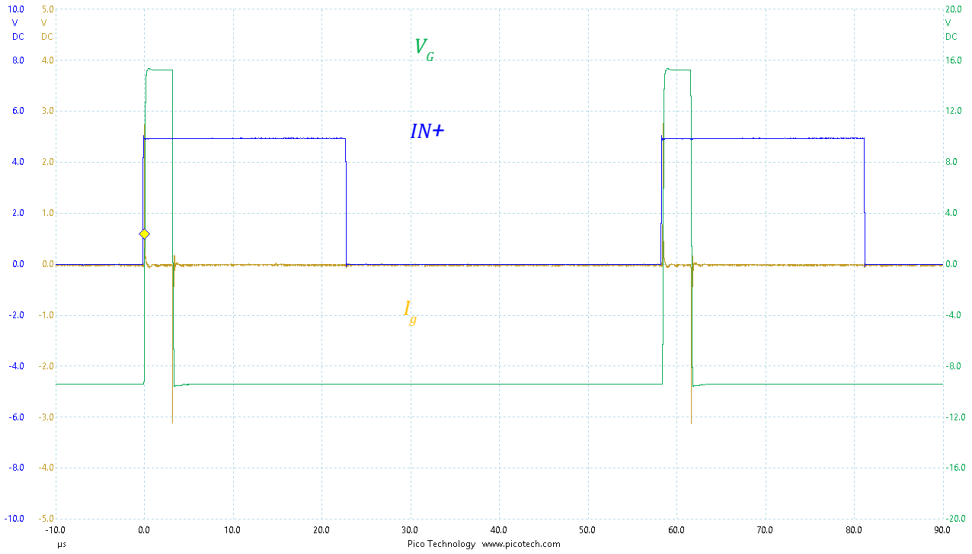


Figure 15. DESAT Function Verification

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