



# 2N7002K-AU

## 60V N-Channel Enhancement Mode MOSFET – ESD Protected

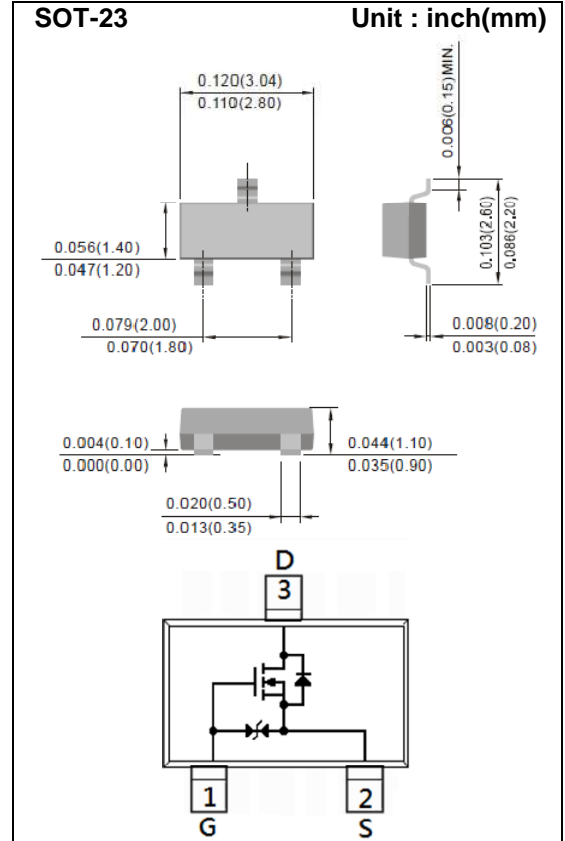
**Voltage** 60 V **Current** 300mA

### Features

- $R_{DS(ON)}$ ,  $V_{GS}@10V$ ,  $I_D@500mA < 3\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@4.5V$ ,  $I_D@200mA < 4\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc
- ESD Protected 2KV HBM
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

### Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0003 ounces, 0.0084 grams



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	$V_{DS}$	60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current (Note 4)	$I_D$	300	mA	
Pulsed Drain Current (Note 1)	$I_{DM}$	2000		
Power Dissipation	$P_D$	$T_A=25^\circ\text{C}$	500	mW
		Derate above $25^\circ\text{C}$	4	mW/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$	
Typical Thermal Resistance	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$	
- Junction to Ambient (Note 3,4)				



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### Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =10uA	60	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	2.5	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA	-	-	3	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =200mA	-	-	4	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±10	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =250mA	100	-	-	mS
<b>Dynamic</b> (Note 5)						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =250mA, V <sub>GS</sub> =5V (Note 1,2)	-	0.8	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.35	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.2	-	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	-	35	-	pF
Output Capacitance	C <sub>oss</sub>		-	13	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	8	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =200mA, V <sub>GS</sub> =10V, R <sub>G</sub> =10Ω (Note 1,2)	-	2.7	-	ns
Turn-On Rise Time	t <sub>r</sub>		-	19	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	15	-	
Turn-Off Fall Time	t <sub>f</sub>		-	23	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>s</sub>	---	-	-	300	mA
Diode Forward Voltage	V <sub>SD</sub>	I <sub>s</sub> =200mA, V <sub>GS</sub> =0V	-	0.82	1.3	V

**NOTES:**

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper.
4. The maximum current rating is package limited.
5. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

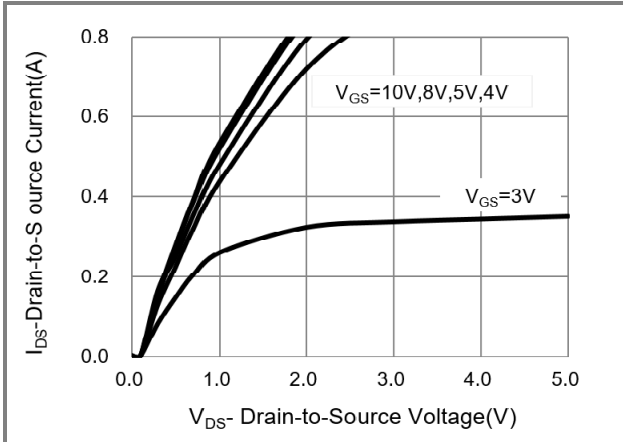


Fig.1 On-Region Characteristics

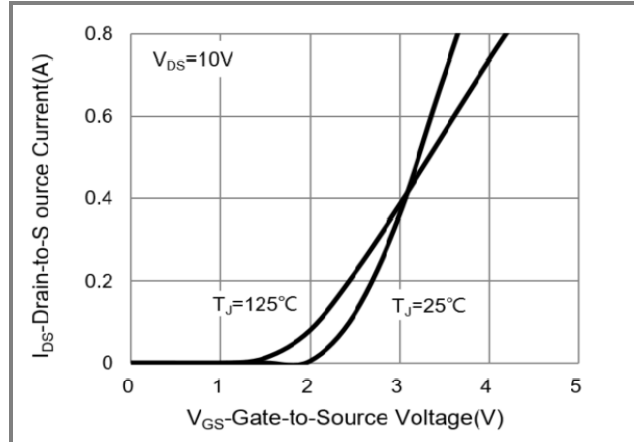


Fig.2 Transfer Characteristics

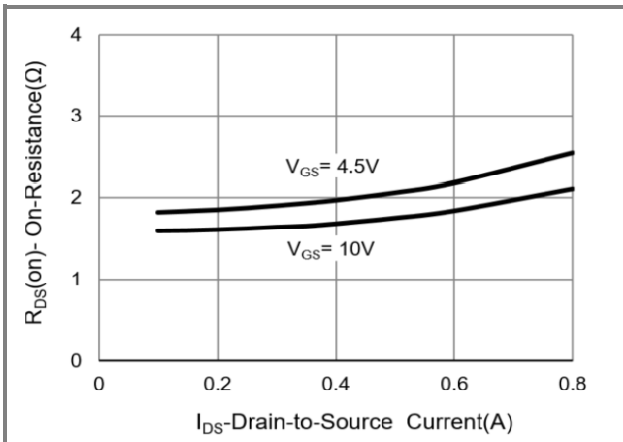


Fig.3 On-Resistance vs. Drain Current

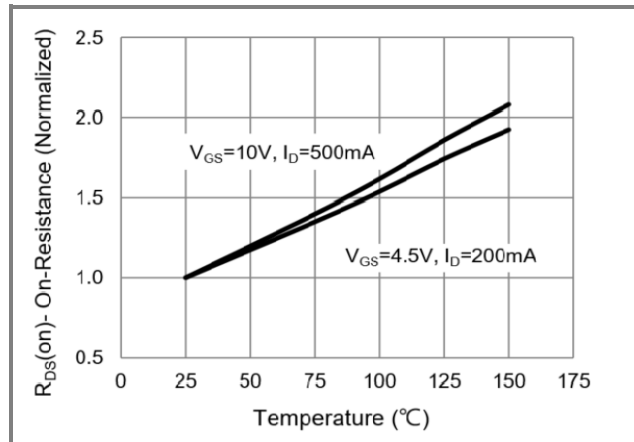


Fig.4 On-Resistance vs. Junction temperature

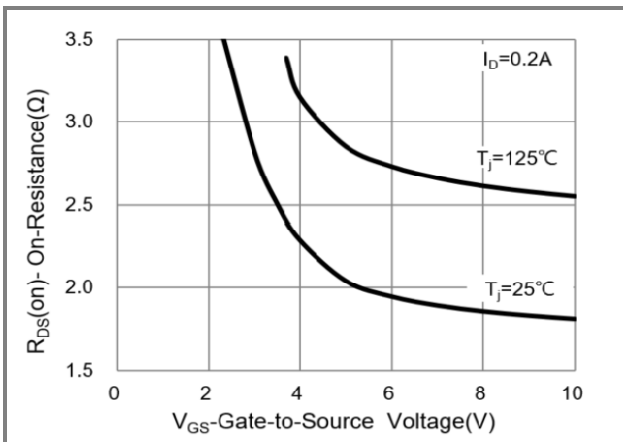


Fig.5 On-Resistance Variation with  $V_{GS}$

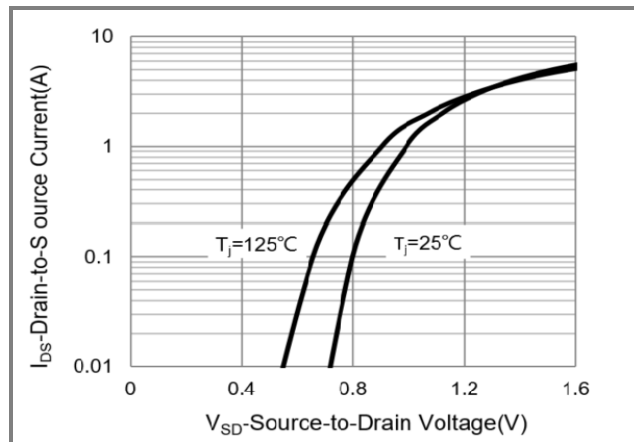


Fig.6 Body Diode Characteristics



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## TYPICAL CHARACTERISTIC CURVES

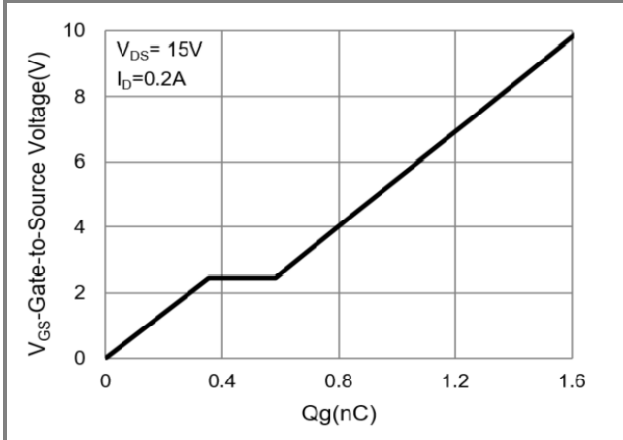


Fig.7 Gate-Charge Characteristics

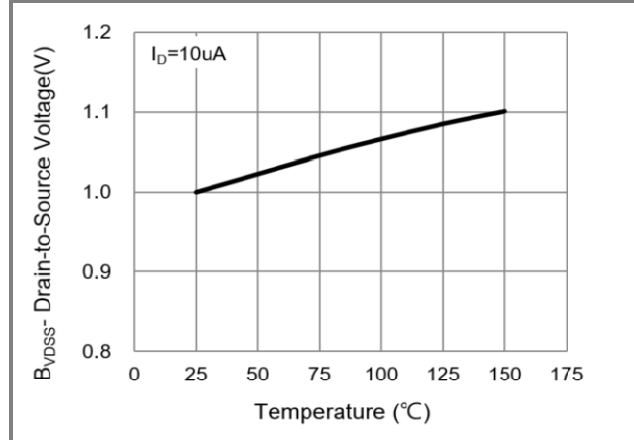


Fig.8 Breakdown Voltage Variation vs. Temperature

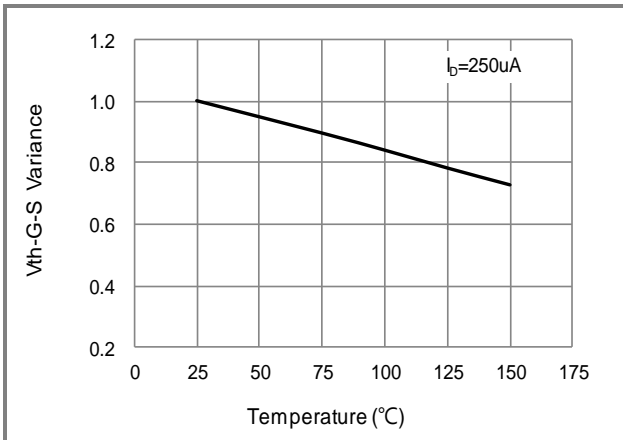


Fig.9 Threshold Voltage Variation with Temperature

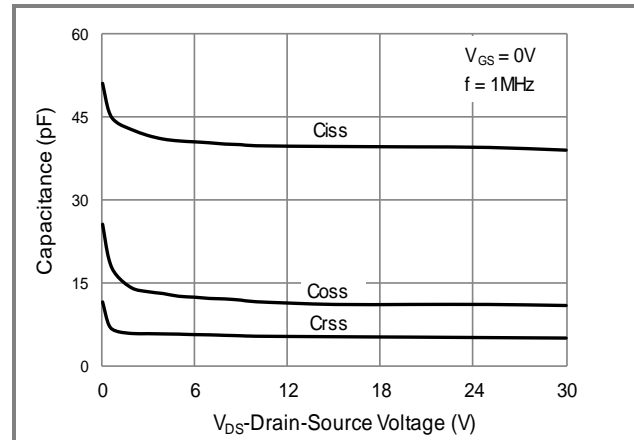


Fig.10 Capacitance vs. Drain-Source Voltage

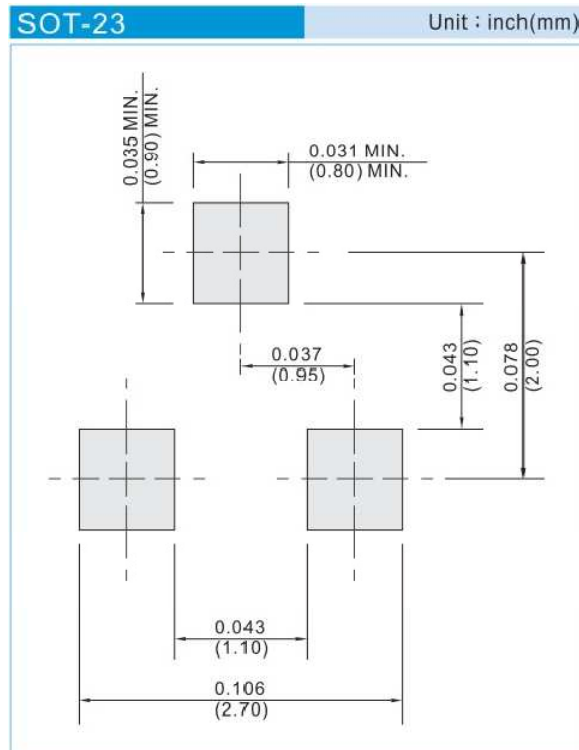


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## Part No. Packing Code Version

Part No. Packing Code	Package Type	Packing Type	Marking	Version
2N7002K-AU_R1_000A2	SOT-23	3K pcs / 7" reel	K72	Halogen free

## Mounting Pad Layout





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