



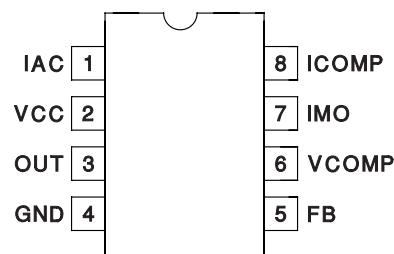
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) . . . . .	40V
Output Drive Current,	
Continuous . . . . .	0.125A
Peak . . . . .	0.5A
Output Minimum Voltage . . . . .	-0.3V
IAC Maximum Input Current . . . . .	1mA
IMO Maximum Output Current . . . . .	-2mA
IMO Minimum Voltage . . . . .	-0.3V
FB Maximum Input Voltage . . . . .	5V
VCOMP Maximum Voltage . . . . .	6.2V
ICOMP Sourcing Current . . . . .	Self-Limiting
ICOMP Sinking Current . . . . .	20mA
ICOMP Maximum Voltage . . . . .	7.2V
Storage Temperature . . . . .	-65°C to +150°C
Junction Temperature . . . . .	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . .	+300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

## CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)  
J or N, D Package



## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1853;  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the 2853; and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3853;  $V_{CC} = 16\text{V}$ ,  $V_{FB} = 3\text{V}$ ,  $I_{AC} = 100\mu\text{A}$ ,  $V_{VCOMP} = 3.75\text{V}$ ,  $V_{ICOMP} = 3\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Undervoltage Lockout Section</b>					
VCC Turn-on Threshold	$V_{VCOMP}$ , $V_{ICOMP}$ Open		11.5	13	V
Hysteresis		1.5	1.8	2.1	V
<b>Supply Current Section</b>					
$I_{VCC}$ Startup	$V_{CC} = 8\text{V}$ , $I_{AC} = 100\mu\text{A}$ ; $V_{VCOMP}$ , $V_{ICOMP}$ Open		250	500	$\mu\text{A}$
$I_{VCC}$	$I_{AC} = 0\mu\text{A}$ , $V_{ICOMP} = 0\text{V}$		10	15	mA
<b>Voltage Loop Error Amplifier Section</b>					
Transconductance	$I_{OUT} = \pm 20\mu\text{A}$ 0-70C	300	450	575	$\mu\text{mho}$
	Temperature	135		640	$\mu\text{mho}$
Input Voltage	0-70C	2.925	3	3.075	V
	Temperature	2.9		3.1	V
AVOL	$V_{VCOMP} = 1\text{V} - 4\text{V}$	50	60		dB
Output Sink Current	$V_{FB} = 3.2\text{V}$ , $V_{VCOMP} = 3.75\text{V}$	20	50		$\mu\text{A}$
Output Source Current	$V_{FB} = 2.8\text{V}$ , $V_{VCOMP} = 3.75\text{V}$		-50	-20	$\mu\text{A}$
Output Voltage High		5.5	6		V
Output Voltage Low			0.6	0.9	V
<b>Current Loop Error Amplifier Section</b>					
Offset Voltage		0		6	mV
Voltage Gain	$V_{ICOMP} = 1\text{V} - 4\text{V}$		70		dB
Sink Current	$V_{IMO} = 100\text{mV}$ , $V_{ICOMP} = 3\text{V}$	1			mA
Source Current	$V_{IMO} = -0.1\text{V}$ , $V_{ICOMP} = 3\text{V}$		-150	-80	$\mu\text{A}$
Output High	$I_{ICOMP} = -50\text{mA}$	6	6.8		V
Output Low	$I_{ICOMP} = 50\mu\text{A}$		0.3	0.8	V
PWM Modulator Gain	$V_{ICOMP} = 2\text{V} - 3\text{V}$ (Note 1)		20		%/V

# **ELECTRICAL CHARACTERISTICS** **(continued)**

Unless otherwise stated, these parameters apply for T<sub>A</sub> = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; V<sub>CC</sub> = 16V, V<sub>FB</sub> = 3V, I<sub>AC</sub> = 100μA, V<sub>VCOMP</sub> = 3.75V, V<sub>ICOMP</sub> = 3V, T<sub>A</sub> = T<sub>J</sub>.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Multiplier Section</b>					
Output Current – IAC Limited	V <sub>CC</sub> = 11V, V <sub>VCOMP</sub> = 6V	–230	–200	–170	μA
Output Current – Zero	I <sub>AC</sub> = 0μA	–2	–0.2	2	μA
Output Current – Power Limited	V <sub>CC</sub> = 12V, V <sub>VCOMP</sub> = 5.5V	–236	–178	–168	μA
Output Current	V <sub>CC</sub> = 12V, V <sub>VCOMP</sub> = 2V		–22		μA
	V <sub>CC</sub> = 12V, V <sub>VCOMP</sub> = 5V		–156		μA
	V <sub>CC</sub> = 40V, V <sub>VCOMP</sub> = 2V		–2		μA
	V <sub>CC</sub> = 40V, V <sub>VCOMP</sub> = 5V		–14		μA
Multiplier Gain Constant	V <sub>CC</sub> = 12V, V <sub>VCOMP</sub> = 5.5V (Note 2)	–1.05	–0.9	–0.75	V <sup>–1</sup>
<b>Oscillator Section</b>					
Oscillator Initial Frequency	T <sub>A</sub> = 25°C	67.5	75	82.5	kHz
Oscillator Frequency	Line, Load, Temperature	56	75	94	kHz
Synchronization Frequency Range				100	kHz
Synchronization Pulse Amplitude	Pulse slew rate = 100V/μsec (Note 3)		2		V
<b>Output Driver Section</b>					
Maximum Output Voltage	0mA load, V <sub>CC</sub> = 20V	12	15	17.5	V
Output High	0mA load, V <sub>CC</sub> = 12V, ref. to V <sub>CC</sub>	–2.7	–1.7		V
	–50mA load, V <sub>CC</sub> = 12V, ref. to V <sub>CC</sub>	–3	–2.2		V
Output Low (Device Inactive)	V <sub>CC</sub> = 0V, 20mA load (Sinking)		0.9	2.0	V
Output Low (Device Active)	50mA load (Sinking)		0.5	1	V
OUT Rise Time	1nF from OUT to GND		55	100	ns
OUT Fall Time	1nF from OUT to GND		35	100	ns
OUT Maximum Duty Cycle	V <sub>ICOMP</sub> = 0V	88	93		%
<b>OVP Comparator Section</b>					
Threshold Voltage	Volts Above EA Input V	90	150		mV
Hysteresis			80		mV

Note 1:

$$PWM \text{ modulator gain} = \frac{\Delta DutyCycle}{\Delta V_{ICOMP}}$$

Note 2:

$$Gain \text{ constant } (K) = \frac{I_{AC} \bullet (V_{COMP} - 1.5V)}{I_{MO} \bullet V_{CC} \bullet \frac{V_{CC}}{64}}, V_{CC} = 12V.$$

Note 3.

Synchronization is accomplished with a falling edge of 2V magnitude and 100V/μsec slew rate.

## PIN DESCRIPTIONS

**FB:** Voltage Amplifier Inverting Input, Overvoltage Comparator Input, Sync Input. This pin serves three functions. FB accepts a fraction of the power factor corrected output voltage through a voltage divider, and is nominally regulated to 3V. FB voltages 5% greater than nominal will trip the overvoltage comparator, and shut down the output stage until the output voltage drops 5%. The internal oscillator can be synchronized through FB by injecting a 2V clock signal through a capacitor. To prevent false tripping of the overvoltage comparator, the clock signal must have a fast falling edge, but a slow rising edge. See Application Note U-159 for more information.

**GND:** Ground. All voltages are measured with respect to GND. The VCC bypass capacitor should be connected to ground as close to the GND pin as possible.

**IAC:** AC Waveform Input. This input provides voltage waveform information to the multiplier. The current loop will try to produce a current waveform with the same shape as the IAC signal. IAC is a low impedance input, nominally at 2V, which accepts a current proportional to the input voltage. Connect a resistor from the rectified input line to IAC which will conduct 500mA at maximum line voltage.

**IMO:** Multiplier Output and Current Sense Inverting Input. The output of the multiplier and the inverting input of the current amplifier are connected together at IMO. Avoid bringing this input below -0.5V to prevent the internal protection diode from conducting. The multiplier output is a current, making this a summing node and allowing a differential current error amplifier configuration to reject ground noise. The input resistance at this node should be 3.9k to minimize input bias current induced offset voltage. See the Applications section for the recommended circuit configuration.

**OUT:** Gate Driver Output. OUT provides high current gate drive for the external power MOSFET. A 15V clamp pre-

vents excessive MOSFET gate-to-source voltage so that the UC3853 can be operated with VCC and high as 40V. A series gate resistor of at least 5 ohms should be used to minimize clamp voltage overshoot. In addition, a Schottky diode such as a 1N5818 connected between OUT and GND may be necessary to prevent parasitic substrate diode conduction.

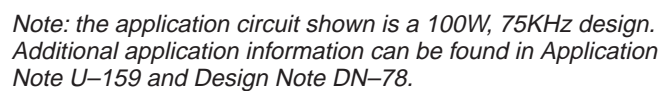
**ICOMP:** Current Loop Error Amplifier Output. The current loop error amplifier is a conventional operational amplifier with a 150μA current source class A output stage. Compensate the current loop by placing an impedance between ICOMP and IMO. This output can swing above the oscillator peak voltage, allowing zero duty cycle when necessary.

**VCC:** Input Supply Voltage. This pin serves two functions. It supplies power to the chip, and an input voltage level signal to the squarer circuit. When this input is connected to a DC voltage proportional to the AC input RMS voltage, the voltage loop gain is reduced by

$$\frac{64}{V_{CC}^2}.$$

This configuration maintains constant loop gain. The UC3853 input voltage range extends from 12V to 40V, allowing an AC supply voltage range in excess of 85VAC to 265VAC. Bypass VCC with at least a 0.1μF ceramic capacitor to ensure proper operation. See the Applications section for the recommended circuit configuration.

**VCOMP:** Voltage Loop Error Amplifier Output. The voltage loop error amplifier is a transconductance type operational amplifier. A feedback impedance between VCOMP and FB for loop compensation must be avoided to maintain proper operation of the overvoltage protection comparator. Instead, compensate the voltage loop with an impedance between VCOMP and GND. When VCOMP is below 1.5V, the multiplier output current is zero.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
UC2853D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2853DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2853DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2853DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2853N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2853NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3853D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3853DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3853DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3853DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3853N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3853NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2853DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3853DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2853DTR	SOIC	D	8	2500	346.0	346.0	29.0
UC3853DTR	SOIC	D	8	2500	346.0	346.0	29.0

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