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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

June 2014

FDMC8884

N-Channel PowerTrench® MOSFET

30 V, 15 A, 19 mΩ

Features

- Max $r_{DS(on)}$ = 19 mΩ at V_{GS} = 10 V, I_D = 9.0 A
- Max $r_{DS(on)}$ = 30 mΩ at V_{GS} = 4.5 V, I_D = 7.2 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

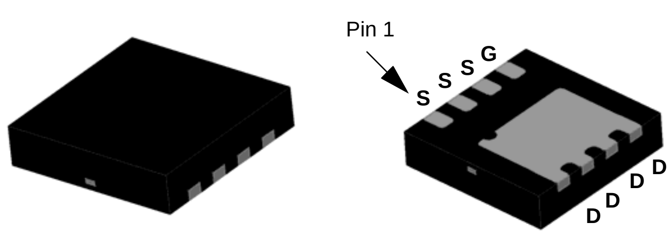
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

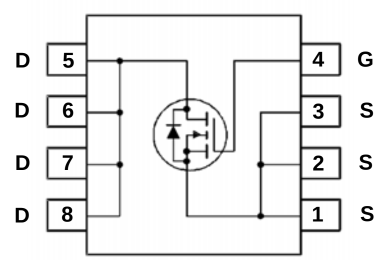
Application

- High side in DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook

Top **Bottom**



MLP 3.3x3.3



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		15	A
	-Continuous	T_A = 25 °C	(Note 1a)	9.0	
	-Pulsed			40	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	24	mJ
P_D	Power Dissipation	T_C = 25 °C		18	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		6.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8884	FDMC8884	MLP 3.3x3.3	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		T_J = 125 °C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.4	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 9.0 A		16	19	mΩ
		V_{GS} = 4.5 V, I_D = 7.2 A		22	30	
		V_{GS} = 10 V, I_D = 9.0 A, T_J = 125 °C		22	30	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 9.0 A		24		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		513	685	pF
C_{oss}	Output Capacitance			110	150	pF
C_{rss}	Reverse Transfer Capacitance			76	115	pF
R_g	Gate Resistance			1.4	2.1	Ω

Switching Characteristics

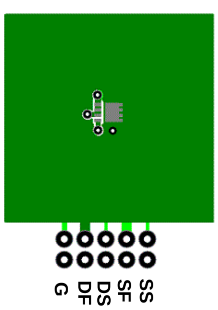
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 9.0 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 9.0 A		10	14	nC
	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D = 9.0 A		5.0	7.0	nC
Q_{gs}	Total Gate Charge	V_{DD} = 15 V, I_D = 9.0 A		1.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.2		nC

Drain-Source Diode Characteristics

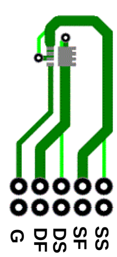
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.0 A (Note 2)		0.86	1.2	V
		V_{GS} = 0 V, I_S = 1.6 A (Note 2)		0.76	1.2	
t_{rr}	Reverse Recovery Time	I_F = 9.0 A, di/dt = 100 A/μs		13	18	ns
Q_{rr}	Reverse Recovery Charge			3	10	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. E_{AS} of 24 mJ is based on starting T_J = 25 °C, L = 1 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 4 A .

Typical Characteristics T_J = 25 °C unless otherwise noted

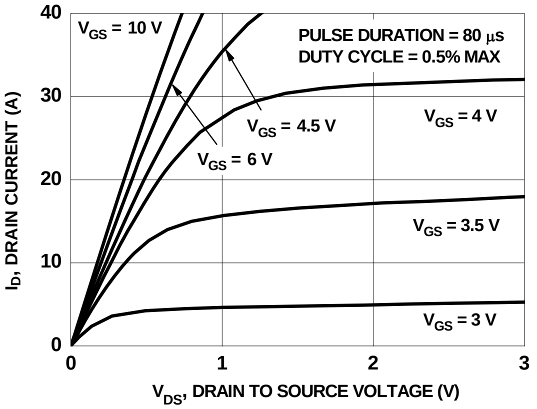


Figure 1. On-Region Characteristics

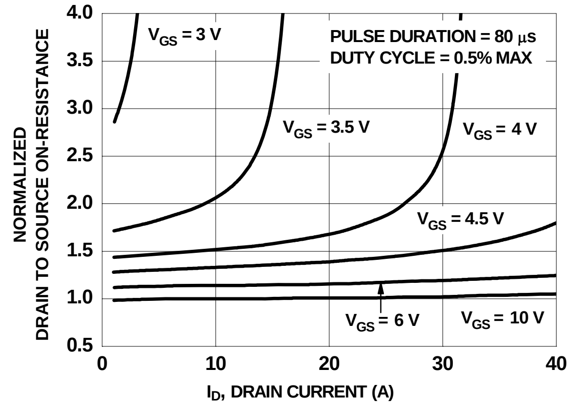


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

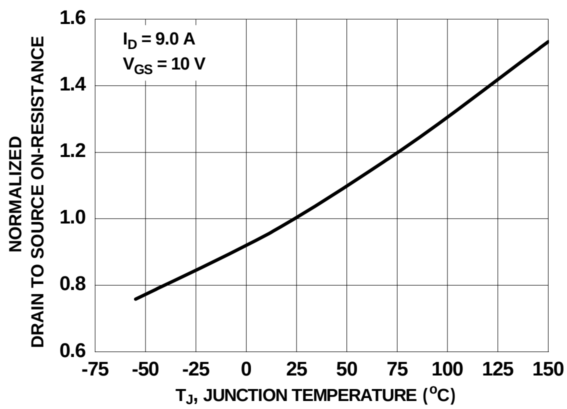


Figure 3. Normalized On-Resistance vs Junction Temperature

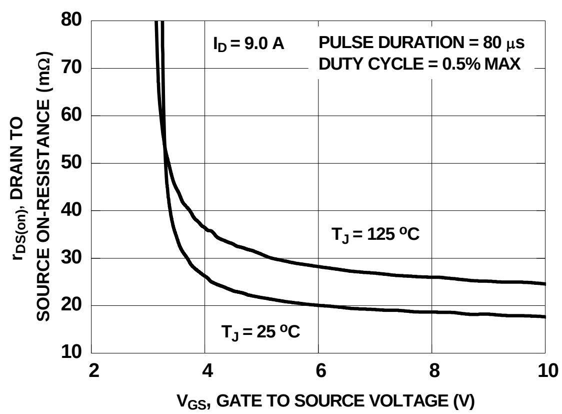


Figure 4. On-Resistance vs Gate to Source Voltage

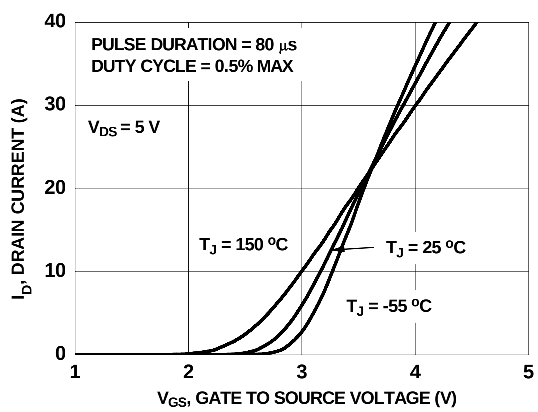


Figure 5. Transfer Characteristics

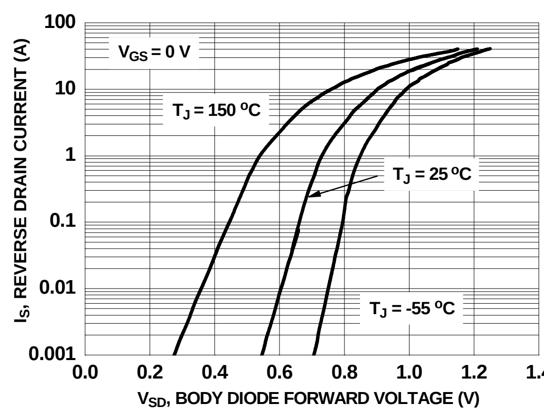


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

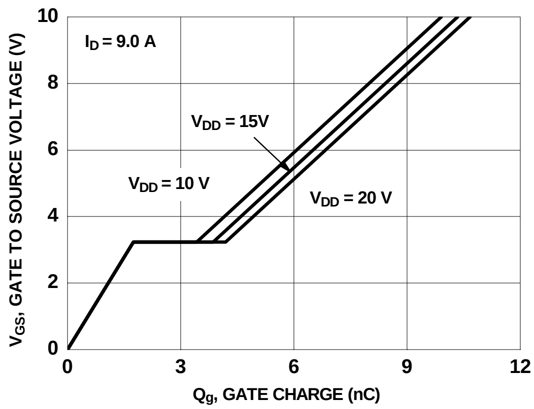


Figure 7. Gate Charge Characteristics

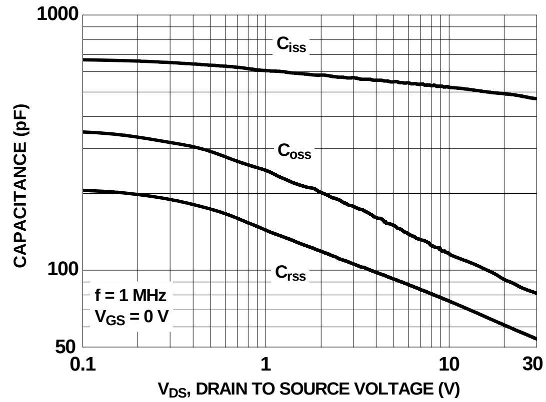


Figure 8. Capacitance vs Drain to Source Voltage

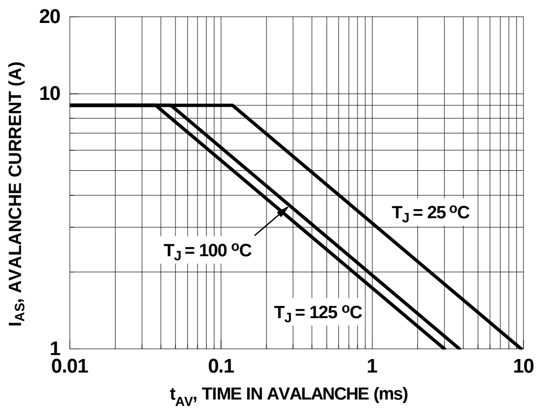


Figure 9. Unclamped Inductive Switching Capability

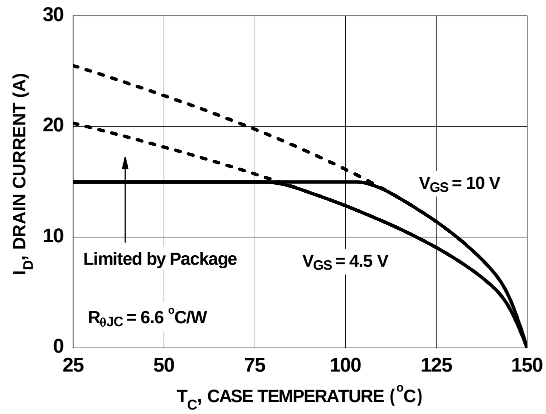


Figure 10. Maximum Continuous Drain Current vs Case Temperature

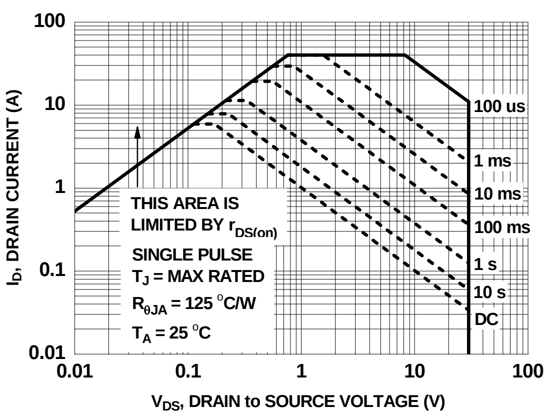


Figure 11. Forward Bias Safe Operating Area

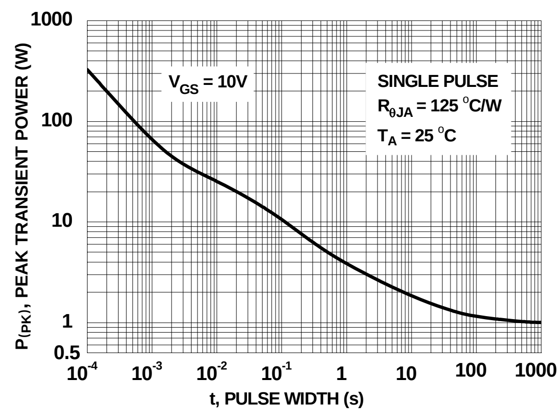


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

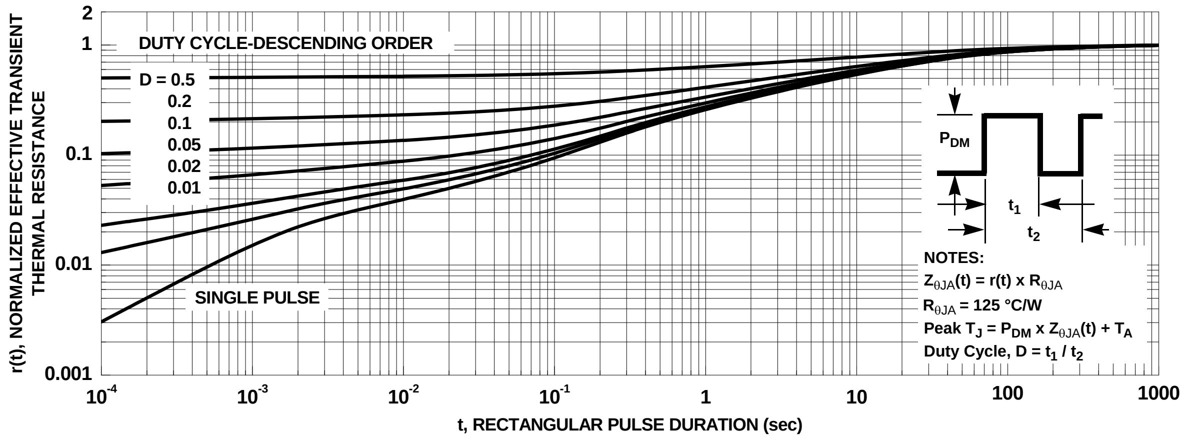
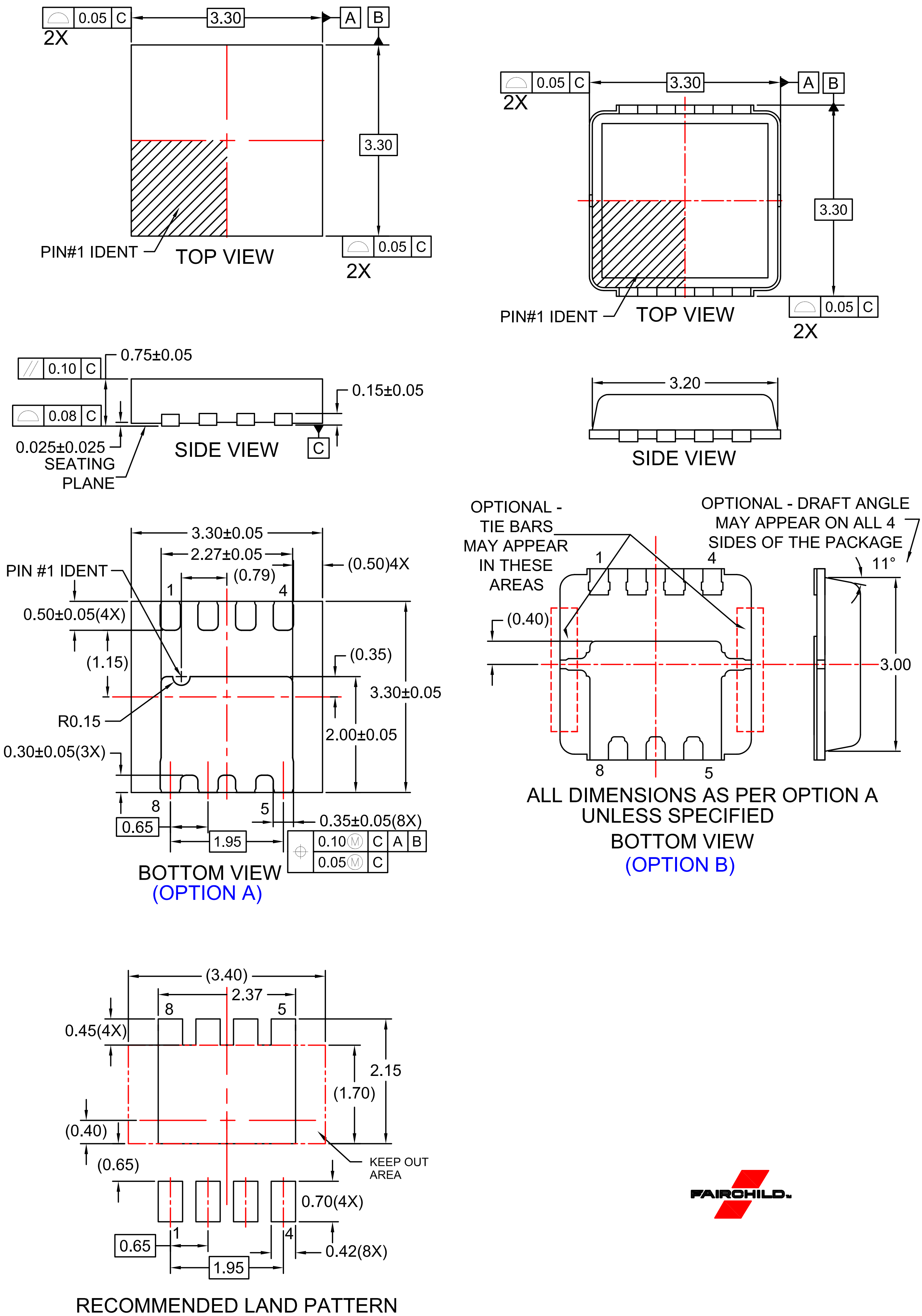
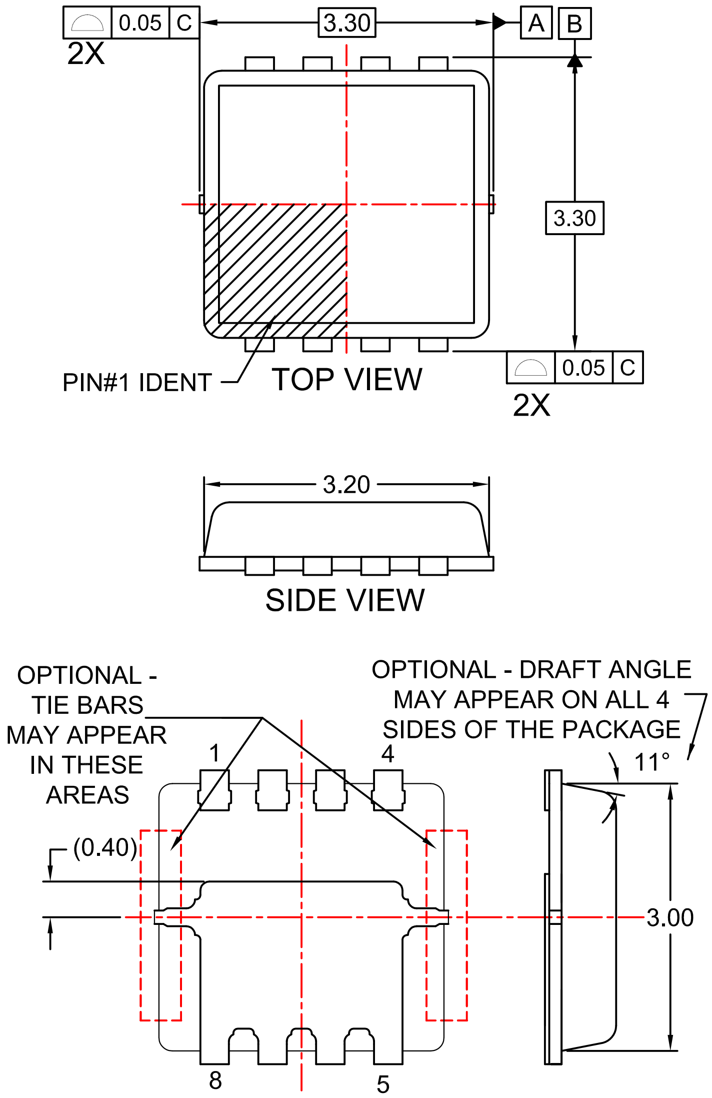


Figure 13. Transient Thermal Response Curve


0.05 C
2X
3.30
A B
3.30
PIN#1 IDENT
TOP VIEW
0.05 C
2X
0.10 C
0.75±0.05
0.08 C
0.15±0.05
0.025±0.025
SEATING PLANE
SIDE VIEW
C
3.20
SIDE VIEW
3.30±0.05
2.27±0.05
(0.79)
(0.50)4X
PIN #1 IDENT
1
4
0.50±0.05(4X)
(1.15)
(0.35)
3.30±0.05
R0.15
2.00±0.05
0.30±0.05(3X)
8
5
0.65
1.95
0.35±0.05(8X)
0.10 M C A B
0.05 M C
BOTTOM VIEW
(OPTION A)
OPTIONAL - TIE BARS MAY APPEAR IN THESE AREAS
OPTIONAL - DRAFT ANGLE MAY APPEAR ON ALL 4 SIDES OF THE PACKAGE
11°
(0.40)
3.00
ALL DIMENSIONS AS PER OPTION A UNLESS SPECIFIED
BOTTOM VIEW
(OPTION B)
(3.40)
2.37
0.45(4X)
2.15
(1.70)
(0.40)
(0.65)
KEEP OUT AREA
0.70(4X)
0.42(8X)
RECOMMENDED LAND PATTERN
FAIRCHILD



ALL DIMENSIONS AS PER OPTION A UNLESS SPECIFIED

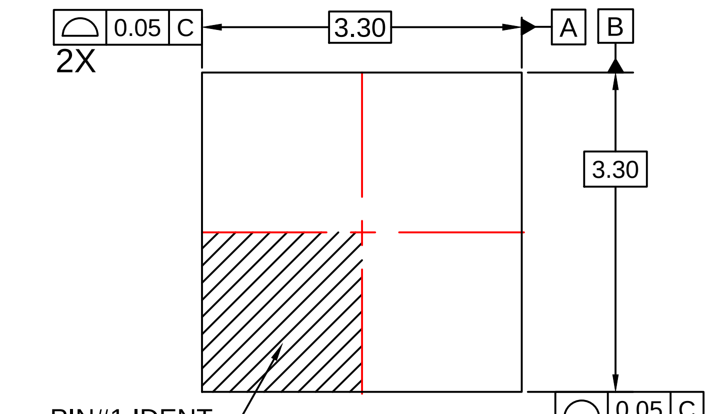
BOTTOM VIEW

(OPTION C)

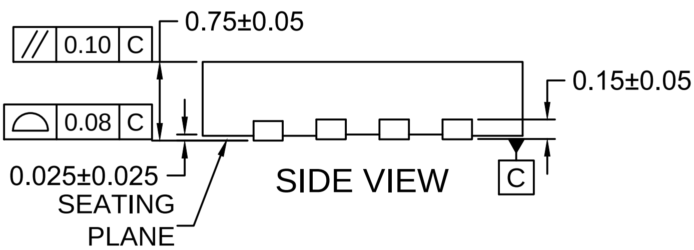
NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
F. DRAWING FILENAME: MKT-MLP08Wrev3.
G. OPTION A - SAWN MLP, OPTIONS B & C - PUNCH MLP.

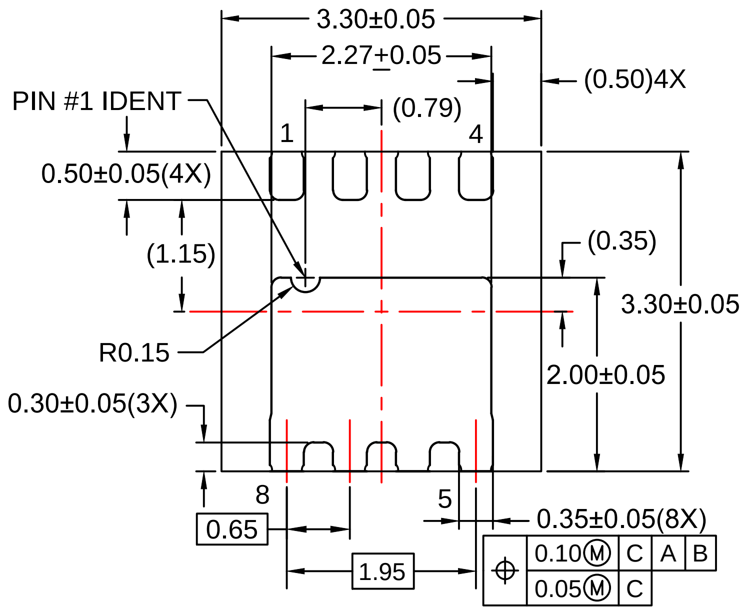
FAIRCHILD



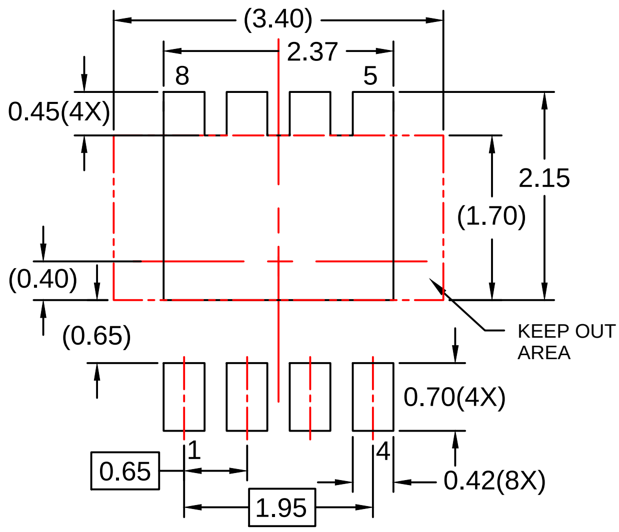
TOP VIEW



SIDE VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

FAIRCHILD.

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