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24 V Single-Phase BLDC Motor Driver

LV8324C

INTRODUCTION

Overview

The LV8324C is the driver for 24 V single phase BLDC motor. Its target output duty-cycle can be set by input PWM duty cycle. The output duty-cycle curve setting can be stored to the internal nonvolatile memory (NVM). In addition, lead-angle can also be adjusted by the configuration saved in the internal NVM. Thus, it can drive various kinds of motors at high efficiency and low noise.

Features

- Selectable Soft Start or Direct Output PWM Duty Control in Start-up
- Power On Delay Function
  (Programmable Ignore Time for PWM Input)
- Single-phase Full Wave Driver with Open-loop Output Duty−cycle Control
- Embedded Power FETs, $I_{omax[peak]}$ = 1.0 A
- PWM Duty Cycle Input (25 Hz to 80 kHz)
- PWM Soft Switching Phase Transition
- Soft PWM Duty Cycle Transitions
  (Changing the Target Output−Duty Gradually)
- Built-in Current Limit Function and Over Current Protection Function
- Built-in Thermal Protection Function
- Built-in Locked Rotor Protection and Automatic Recovery Function
- FG or RD or RDA Signal Output Selectable
- Dynamic Lead Angle Adjustment with Respect to Rotation Speed
- Parameter Setting by Serial Communication
- Embedded EEPROM as NVM
- Parameter Setting to the NVM
- The Device is Pb-Free and Halogen Free

Typical Applications

- Fan Motor in Factory Automation

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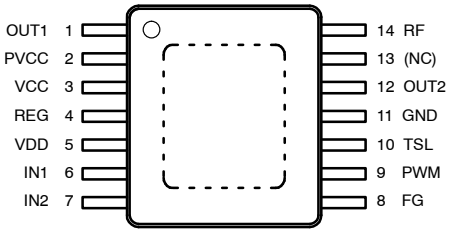
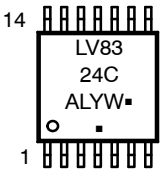
TSSOP−14
CASE 948AW

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM



LV8324C = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
LV8324CGR2G	TSSOP−14 (Pb-Free/ Halogen Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Application Diagram

Figure 1 shows the application diagram.

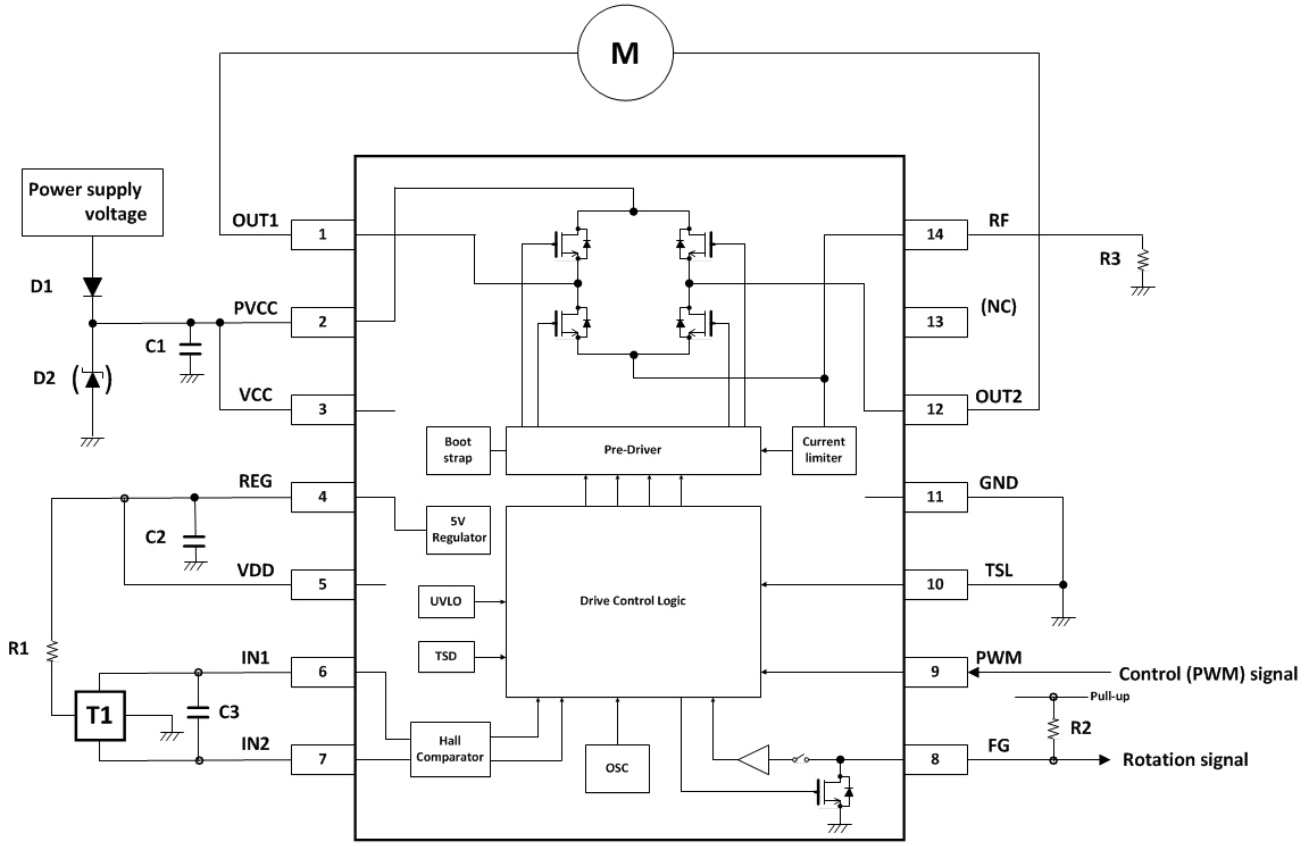


Figure 1. Application Diagram

The power supplies of the IC need to be decoupled properly. This means that at least one external capacitor C1 must be connected in between GND and VCC, and one external capacitor C2 between REG, VDD and GND.

External Components

Table 1 shows the external component list. Please refer to section “Pin Description” (Table 7) as well.

Table 1. EXAMPLE OF EXTERNAL COMPONENT VALUE FOR 24 V APPLICATION (Figure 1)

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
D1	1	Anti−reverse connection diode	–	–			
D2	1	Anti−abnormal boost Zener diode	–	–			
C1	1	VCC bypass capacitor	10 μF 50 V	10%			
C2	1	REG bypass capacitor	1 μF 25 V	10%			
C3	1	Filter of system noise	0.1 μF 50 V	10%			
R1	1	Current limiter resistor for Hall	2 kΩ 1/4 W	5%			
R2	1	FG pull−up resistor	10 kΩ 1/4 W	5%			
R3	1	Sense resistor for CLM/OCP	150 mΩ 1/8 W	1%			
T1	1	Hall element					

VCC and GND (VCC, GND)

The power supplies of the IC need to be decoupled properly. The following three capacitors must be connected.

- between VCC (pin 3) and ground as C1 in the application diagrams
- between REG (VDD) and ground as C2

The Zener diode (D2) in Figure 1 is mandatory to prevent the IC break down in case the supply voltage exceeds the absolute maximum ratings due to the flyback voltage.

Hall−Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are connected at IN1 and IN2. It is recommended that the capacitor (C3) is connected between both pins to filter system noise. The value of C3 should be selected properly depending on the system noise. When a Hall IC is used, the output of the Hall IC must be connected to the IN1 pin and the IN2 pin must be kept in the middle level of the Hall IC power supply voltage which should be corresponded to recommended operating range.

Command Input Pin (PWM)

This pin reads the duty cycle of the PWM pulse which controls rotational speed. The PWM input signal level is supported from 2.8 V to 5.5 V. Linear voltage control is not supported. The minimum pulse width is 100 ns.

Current Limiter Resistor for Hall (R1)

Hall output amplitude can be adjusted by R1.

The amplitude is proportional to Hall bias level VH for particular magnetic flux density. VH is determined by the following equation.

$$VH = VREG \times \left(\frac{Rh}{Rh + R1}\right) \quad \text{(eq. 1)}$$

Where
VREG: REG pin voltage (5 V)
Rh: Hall resistance

However, it should be considered with Hall sensor specification and Hall bias current. The bias current should be set under 20 mA which is REG pin max current.

Table 2. TRUTH TABLE

IN1	IN2	*Inner PWM state	OUT1	OUT2	FG	Operation state
L	H	On	L	H	Hi−Z	Drive mode
		Off	L	L		Regeneration mode
H	L	On	H	L	L	Drive mode
		Off	L	L		Regeneration mode

*Inner PWM state means the OUTPUT active period decided by inner control logic. Don't match with PWM−pin input signal.
*Condition: Register "DRVMODE [1:0]" = 01

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage	VCC_{MAX}	VCC pin	36	V
Maximum Output Voltage	V_{OUTMAX}	OUT1/OUT2 pin	36	V
Maximum Output Current (Note 1)	I_{OUTMAX}	OUT1/OUT2 pin	1.0	A
REG Pin Maximum Output Current	I_{REGMAX}	REG pin	20	mA
IN1/IN2 Pin Maximum Input Voltage	V_{INMAX}	IN1/IN2 pin	5.5	V
PWM Pin Maximum Input Voltage	V_{PWMMAX}	PWM pin	5.5	V
FG Pin Withstanding Voltage	V_{FGMAX}	FG pin	36	V
FG Pin Maximum Current	I_{FGMAX}	FG pin	7.5	mA
Allowable Power Dissipation (Note 2)	Pd_{MAX}	with exposed pad	0.93	W
		without exposed pad	0.80	
Operating Temperature	T_{OP}		−40 to +105	°C
Storage Temperature	T_{STG}		−55 to +150	°C
Maximum Junction Temperature	T_{jmax}		150	°C
Moisture Sensitivity Level (MSL) (Note 3)	MSL		1	–
Lead Temperature Soldering Pb-Free Versions (30 s or less) (Note 4)	T_{SLD}		255	°C
ESD Human Body Model: HBM (Note 5)	ESD_{HBM}		±3000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUTMAX} is the peak value of the motor supply current.
2. Specified circuit board: Toroidal shaped. The actual area is 369 mm^2, thickness is 0.8 mm and glass epoxy 2-layer board which has 1 oz internal power and ground plane and 1/2 oz copper traces on top and bottom of the board.
3. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J−STD−020A.
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
5. ESD Human Body Model is based on JEDEC standard: JESD22−A114.

Table 4. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient without Exposed Pad (Note 2)	$R_{\theta JA}$	156	°C/W
Thermal Resistance, Junction-to-Ambient with Exposed Pad (Note 2)	$R_{\theta JA}$	134	°C/W
Thermal Resistance, Junction-to-Case (Top) without Exposed Pad (Note 2)	$R_{\Psi JT}$	13.5	°C/W
Thermal Resistance, Junction-to-Case (Top) with Exposed Pad (Note 2)	$R_{\Psi JT}$	5.7	°C/W

Table 5. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Rating	Unit
VCC Supply Voltage	VCC_{TYP}	VCC pin	24	V
VCC Operating Supply Voltage Range1	VCC_{OP1}	VCC pin	6.0 to 34	V
VCC Operating Supply Voltage Range for NVM Program/ Erase Operation	VCC_{NVM}	VCC pin	14 to 34	V
PWM Input Frequency Range	F_{PWM}	PWM pin	25 to 80k	Hz
PWM Minimum Input Low/High Pulse Width	T_{WPWM}	PWM pin	100	ns
IN1 Input Voltage Range	V_{IN1}	IN1 pin	0 to VDD	V
IN2 Input Voltage Range	V_{IN2}	IN2 pin	0.3 to 0.55 × VDD	V
Minimum External Resister Value	R_RFmin		0.15	Ω

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS (T_A = 25°C, VCC_{OP} = 24 V unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	Under the Power On Delay state	–	7	10.5	mA
OUT1/OUT2 High-side On-resistance	R_{OH-ON}	I_O = 0.3 A	–	0.5	0.8	Ω
OUT1/OUT2 Low-side On-resistance	R_{OL-ON}	I_O = 0.3 A	–	0.5	0.8	Ω
OUT1/OUT2 PWM Output Frequency	f_{PWMO}		–	48	–	kHz
PWM Pin Low Level Input Voltage	V_{PWML}		0	–	0.7	V
PWM Pin High Level Input Voltage	V_{PWMH}		2.8	–	VDD	V
PWM Input Resolution	Δ_{PWM}		–	8	–	Bit
PWM Input Bias Current (VDD = 5.5 V, PWM = 0 V)	Ipwmin		25	50	75	μA
FG Pin On-resistance	V_{FGL}	I_{FG} = 5 mA			60	Ω
FG Pin Leak Current	I_{FGLK}	V_{CC} = 34 V, V_{FG} = 34 V	–	–	1	μA
REG Pin Output Voltage	V_{REG}		4.7	5.0	5.3	V
REG Pin Output Voltage Load Regulation	ΔV_{REGLD}	I_{REG} = −10 mA	–	–	50	mV
Lock-detection Time1 (Note 6)	T_{LD1}	Under rotation	–	0.3	–	S
Lock-detection Time2 (Note 7)	T_{LD2}	Start-up/Restart, LOCK_DET = 3	–	0.95	–	S
Lock-Stop Release Time1 from 1st to 4th Off Time (Note 7)	T_{LRoff1}	RESTART_INT = 3	–	9.0	–	S
Lock-Restart On Time (Note 7)	T_{LRon}	LOCK_DET = 3	–	0.95	–	S
Lock-Restart Time Ratio1	R_{LR1}	T_{LRoff1}/T_{LRon}, LOCK_DET = 3, RESTART_INT = 3	–	9	–	–
Lock-Stop Release Time2 as from 5th Off Time (Note 8)	T_{LRoff2}		–	14	–	S
Lock-Restart Time Ratio2 as from 5th Off Time (Note 8)	R_{LR2}	T_{LRoff2}/T_{LRon}, LOCK_DET = 3	–	15	–	–
Thermal Shutdown Protection Detection Temperature	T_{TSD}	(Guaranteed by design)	150	180	–	°C
Thermal Shutdown Protection Detection Hysteresis	ΔT_{TSD}	(Guaranteed by design)	–	40	–	°C
Over Current Detection Voltage	I_{OVC}		–	150	–	mV
Current Limiter	I_{CL}		90	100	110	mV
Hall Input Bias Current	I_{hin}	IN1, IN2 = 0 V	–	–	1	μA
Hall Input Sensitivity	ΔVhin		40	–	–	mV
UVLO Detection Voltage	Vuvdet		–	5.2	–	V
UVLO Release Voltage	Vuvrls		–	5.6	–	V
UVLO Hysteresis Voltage	ΔVuv		–	0.4	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. When a motor rotates with below 50 rpm (phase change period over 0.3 s), lock protection will works. See Figure 17 for the detail.
7. When a motor can't rotate for the time which is set by the register named LOCK_DET after start-up, lock protection will work. See Figure 18 for the detail.
8. When the locked rotor state continues for long time, lock stop period changes as from 5th off time. See Figure 18 for the detail.

BLOCK DIAGRAM

Figure 2 shows the functional block diagram of LV8324C.

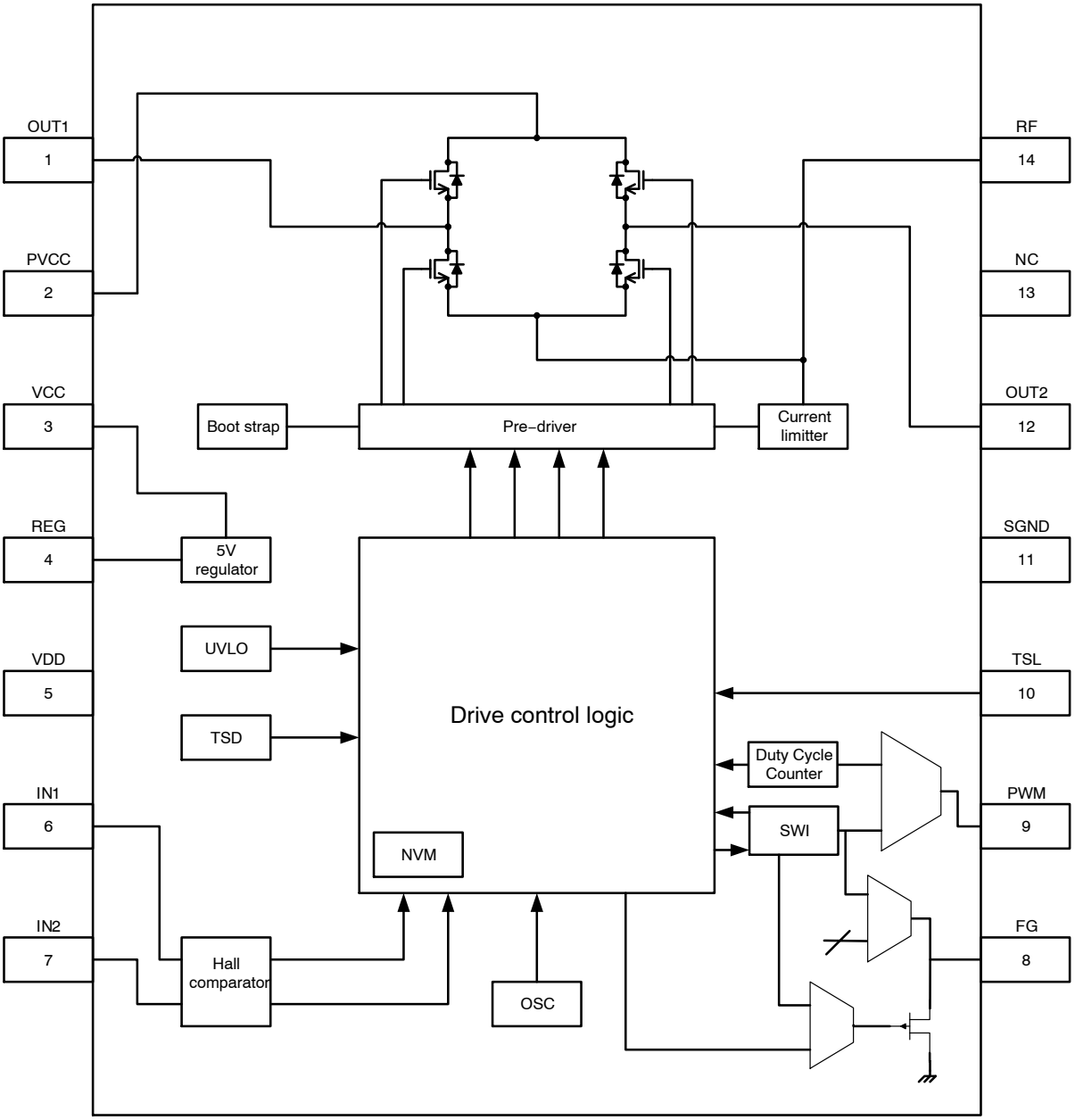


Figure 2. Block Diagram

PIN DESCRIPTION

Table 7 shows the pin list and their functions.

Table 7. PIN LIST AND FUNCTION

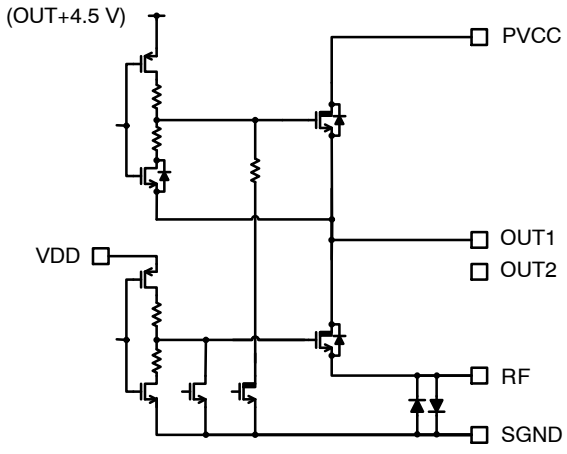
Pin No.	Pin Name	Description
1	OUT1	Motor drive output pin. This pin is connected to the built−in power MOSFET.
2	PVCC	Power supply pin for built−in power MOSFET.
3	VCC	Power supply for internal circuit, ex. pre−driver, charge−pump.
4	REG	5.0 V regulator output. This voltage acts as a power source for oscillator, protection circuits, and so on. The maximum load current of REG is 20 mA. Be sure not to exceed this maximum current
5	VDD	Power supply pin for both digital and analog circuits. This pin must be connected to REG pin
6	IN1	Hall sensor input pin. The differential outputs of the hall sensor need to be connected to IN1 and IN2 each.
7	IN2	
8	FG	The FG (frequency generator) output controls the motor electrical rotational speed (FG output synchronizes with the Hall sensor signal). This pin can function as RD (rotation detection) and RDA (Rotation Decline Alarm) by bit setting of Reg. 0x010C “TACHSEL”. The FG pin is an open drain output. Recommended pull up resistor is 1 kΩ to 100 kΩ. Leave the pin open when not in use. Parameter setting through the communication is performed by the pin use
9	PWM	Rotational control signal input pin. The rotational speed is controlled by duty−cycle of the pulse and is proportional to the duty−cycle ratio. Parameter setting through the communication is performed by this pin
10	TSL	Communication input selection and internal test mode pin. When short to GND, FG pin is serial in/out. When short to REG, PWM pin is serial in and FG pin is for serial out
11	SGND	Internal circuit ground pin
12	OUT2	Motor drive output pin. This pin is connected to the built−in power MOSFET.
13	NC	No connection
14	RF	Sense resistor voltage input for current limit / over current protection

SIMPLIFIED EQUIVALENT CIRCUITS

Table 8 shows the pin information. The pull-up/down resistor and diode path are included.

Table 8. PIN EQUIVALENT CIRCUIT

OUT1, OUT2



PVCC, VCC/SGND

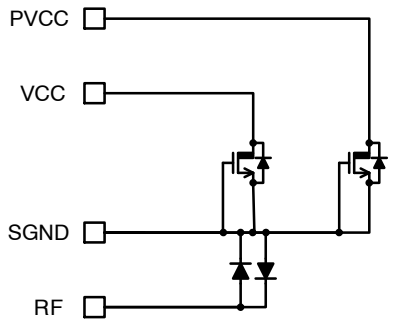
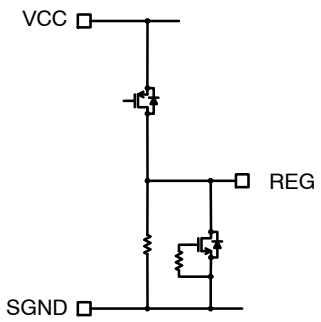
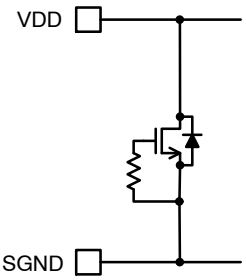
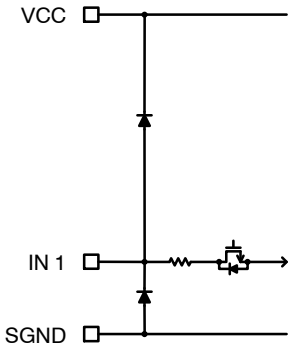
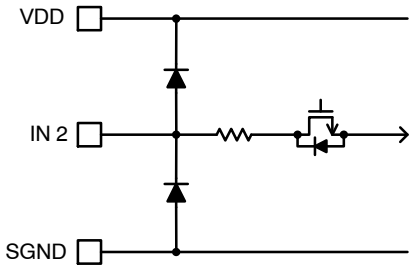
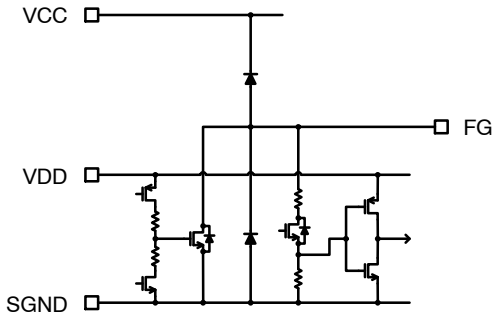
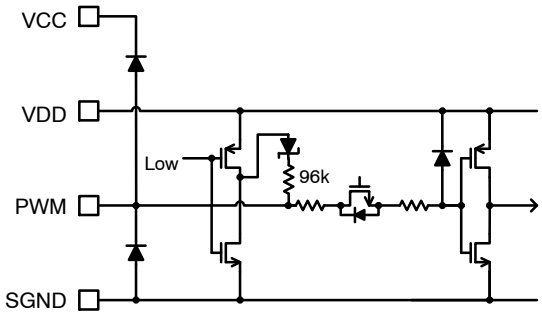
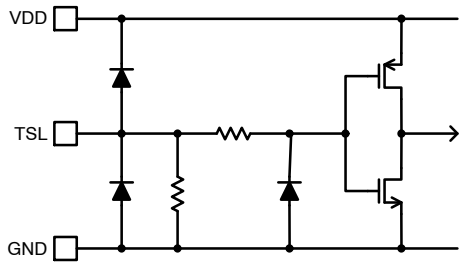
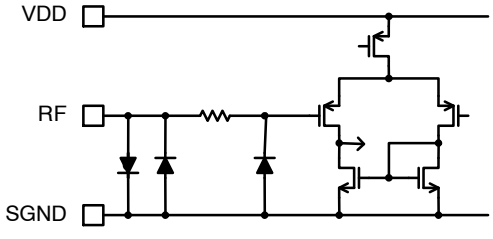


Table 8. PIN EQUIVALENT CIRCUIT (continued)

REG 	**VDD** 
IN1 	**IN2** 
FG 	**PWM** 
TSL 	**RF** 

OPERATION DESCRIPTION

The LV8324C has various functions and parameters which are defined by built-in registers. Refer to the Register map and description page for the detail.

Spin-up Sequence

To spin-up a motor, power is applied to VCC pin and the appropriate input PWM signal (see "DUTY_L" and"DUTY_S" setting description in section "Steady Rotation") is applied to PWM pin. The LV8324C starts driving the motor whose current direction is determined by the Hall sensor signal. In this sequence, the wait time for spin-up is adjustable by "ST_DLY_TIM" which set the time to ignore PWM signal as shown in Table 9. This setting is stored to NVM. In the wait time, both OUT1 and OUT2 are Hi-Z and other circuits are active. After the wait time, OUT1 and OUT2 are active.

Table 9. PWM INPUT IGNORE TIME

ST_DLY_TIM	PWM Input Ignore Time [s]
0	0
1	0.5
2	1.0
3	1.5

To avoid the unnecessary rush current, the "soft start" mode is provided, which gradually increases output duty-cycle. After the soft start mode, LV8324C goes to steady rotation mode. The detail of the soft start mode and steady rotation mode are described in the sections below.

In addition, soft switch function in start-up mode is available. In case of "SS_SW_SEL = 0", falling time of duty-cycle is 5 ms and rising time is 2.5 ms. In case of "SS_SW_SEL = 1", each time is half of the case of "SS_SW_SEL = 0".

If a motor already rotates at the power on in faster speed than 304 rpm, the soft start mode is skipped and goes to steady rotation mode immediately.

Soft Start

For soft start mode, the duty-cycle ramp up profile is defined by the initial duty-cycle, slope, and exit condition. The initial duty-cycle is fixed and it starts from 4%. The slope is programmable. It is determined by registers "SSTART_SEL" and "INCTIM". The duty-cycle is increased up to the end duty-cycle "SSTART_SEL" for duration time "INCTIM". The end duty-cycle is selectable at 0%, 24%, 54% or 80% (see Table 10). The duration time can be selected from 0.0002 sec to 15.2 s (see Table 11). The exit condition means it's in the state of either the duty-cycle reaches "SSTART_SEL". Soft start operation requires at least 8 electrical cycles (4 mechanical cycles in case of 4 poles single phase motor) independent on the exit condition.

Table 10. SOFT START END DUTY-CYCLE

SSTART_SEL	End Duty-cycle
0	0% output duty-cycle (Disable Soft Start)
1	24% output duty-cycle
2	54% output duty-cycle
3	80% output duty-cycle

Table 11. SOFT START DURATION TIME

INCTIM			Duration Time (s)			
[2]	[1]	[0]	SSTART_SEL = 0	SSTART_SEL = 1 (End Duty-cycle = 24%)	SSTART_SEL = 2 (End Duty-cycle = 54%)	SSTART_SEL = 3 (End Duty-cycle = 80%)
0	0	0	0	0.0002	0.10	0.15
0	0	1	0	0.48	0.50	0.76
0	1	0	0	0.96	1.00	1.52
0	1	1	0	1.50	1.50	2.28
1	0	0	0	2.00	2.00	3.04
1	0	1	0	3.00	3.00	4.56
1	1	0	0	5.00	5.00	7.60
1	1	1	0	10.0	10.0	15.2

Figure 3 shows the image of soft start mode.

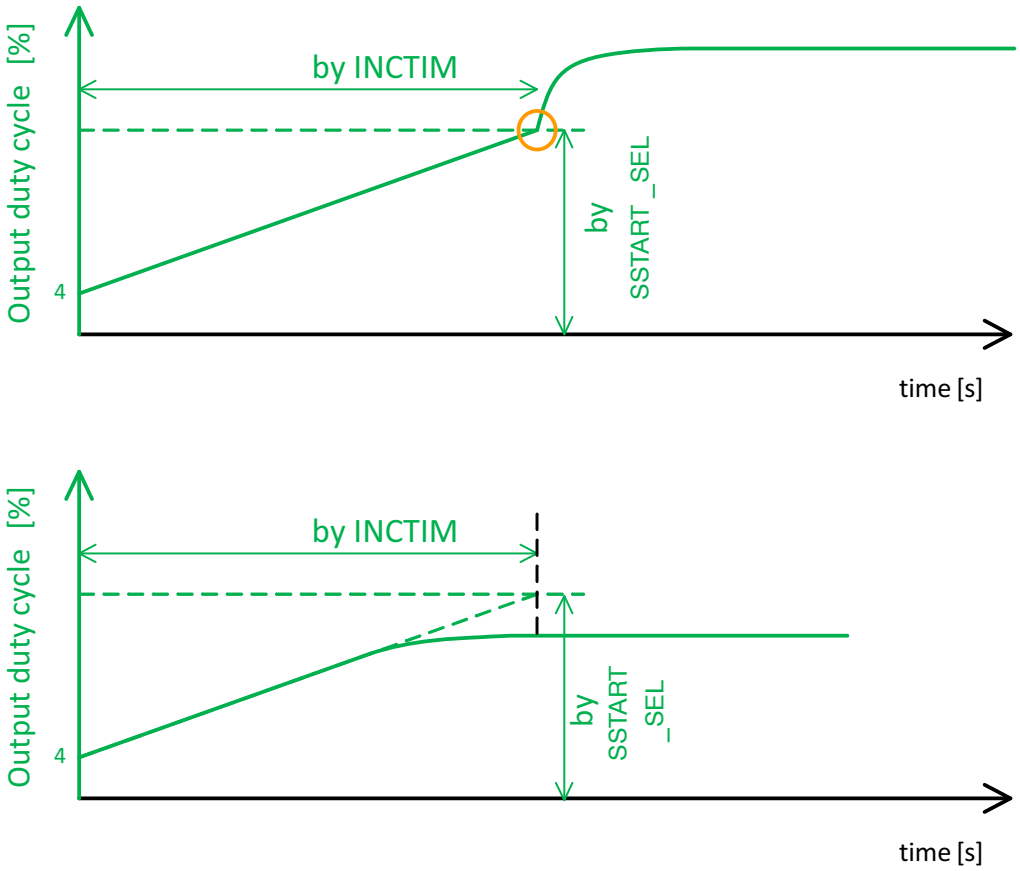


Figure 3. The Image of Soft Start Exit by End Duty-cycle

As the green curve shown in Figure 3, the output duty-cycle in the soft start mode starts from 4% of the output duty. Then the output duty-cycle is increased to the end duty-cycle linearly, which is shown by yellow circle. After that, LV8324C goes to the steady rotation mode.

Figure 4 is the example of the duration time in case of "SSTART_SEL = 3".

In case of "SSTART_SEL = 0", the output duty-cycle increases according to the input duty-cycle and the setting of registers which are "PWM_ROC" and "STEPSEL". About these registers, see the section "Output duty cycle transitions" and Table 13 for more detail.

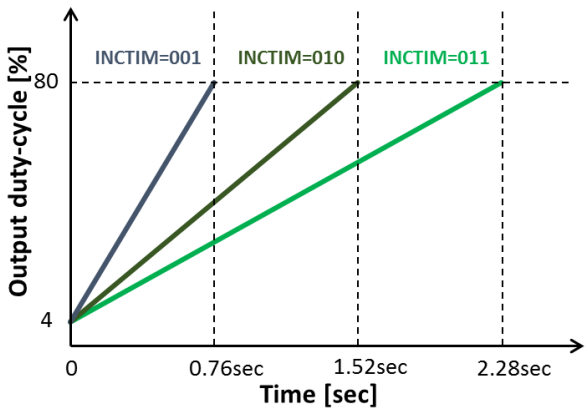


Figure 4. Example: The Image of Soft Start Duration Time in Case of SSTART_SEL = 3

Steady Rotation

The motor speed is defined by the output duty−cycle which is controlled by input PWM pin.

The input PWM frequency range is 25 Hz−80 kHz. The output frequency is fixed to 48 kHz and it is not related to input PWM frequency. Figure 5 shows the output duty-cycle control profile which is relationship between input PWM duty-cycle and the target output duty-cycle. Registers to determine this relationship are;

- TAG_L (Address 0x0100 D [7:0]):
  Minimum output duty-cycle
- TAG_H (Address 0x0101 D [7:0]):
  Maximum output duty-cycle
- DUTY_L (Address 0x0102 D [7:0]):
  Minimum input duty-cycle
- DUTY_H (Address 0x0103 D [7:0]):
  Maximum input duty-cycle
- FULL (Address 0x0108 D [6]):
  Output duty-cycle selection at input duty-cycle over DUTY_H
- DUTY_S (Address 0x0109 D [3:0]):
  Output duty-cycle selection at input duty-cycle under DUTY_L

The detail of each register will be explained later.

TAG_L/TAG_H: Minimum/Maximum Target Output Duty-cycle Setting

The minimum output duty-cycle is set by “TAG_L” and the maximum output duty-cycle is set by “TAG_H” within the range of DUTY_L and DUTY_H (See Figure 6).

Do not set the maximum output duty-cycle setting (TAG_H) less than the minimum output duty-cycle setting (TAG_L).

DUTY_L/DUTY_H: Minimum/Maximum Input Duty-cycle Setting

The range of PWM input duty-cycle can be set by the registers “DUTY_L” and “DUTY_H” whose range is 0 to 100%. The equation of resolution is

$$D_{mit} = \frac{DUTY\_L}{255} \times 100\ [\%] \qquad \text{(eq. 2)}$$

$$D_{max} = \frac{DUTY\_H}{255} \times 100\ [\%] \qquad \text{(eq. 3)}$$

Where:

D_{min} is minimum input duty-cycle.

D_{max} is maximum input duty-cycle.

Do not set “DUTY_H” less than “DUTY_L”.

Figure 7 shows the relationship between input duty-cycle and target output duty-cycle. TAG_L/TAG_H define the start and end points of the output duty-cycle curve and the value between (DUTY_L, TAG_L) and (DUTY_H, TAG_H) are interpolated linearly.

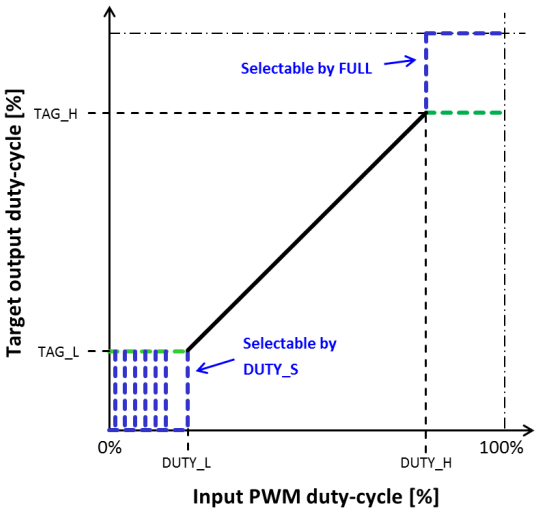


Figure 5. Target Output Duty-cycle Control Profile

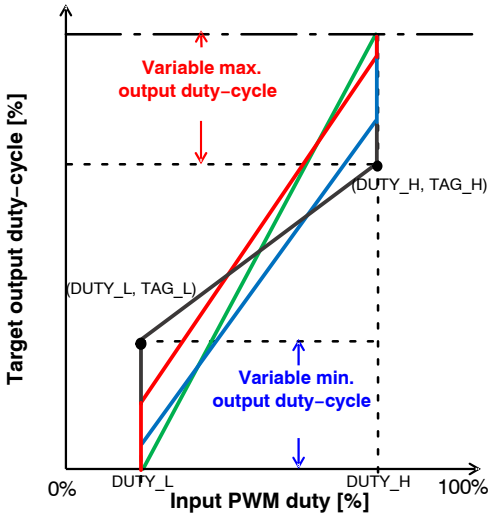


Figure 6. Max/Min Speed Setting

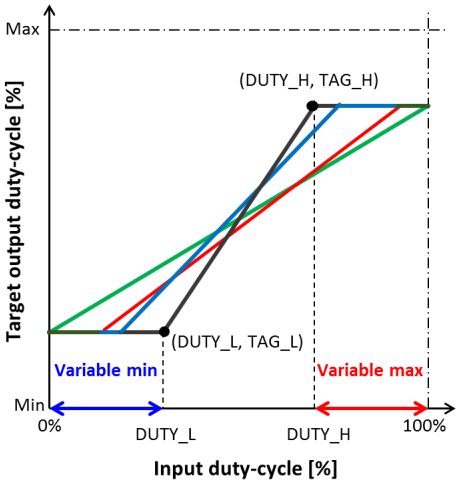


Figure 7. Input Duty-cycle Setting

FULL: Output Duty-cycle Selection at Input Duty-cycle over DUTY_H

For the behavior at input duty-cycle which is over DUTY_H, the register "FULL" provides two options. FULL = 0 is to keep the output duty-cycle specified by "TAG_H" and FULL = 1 is to go to 100% output duty-cycle as shown in Figure 8.

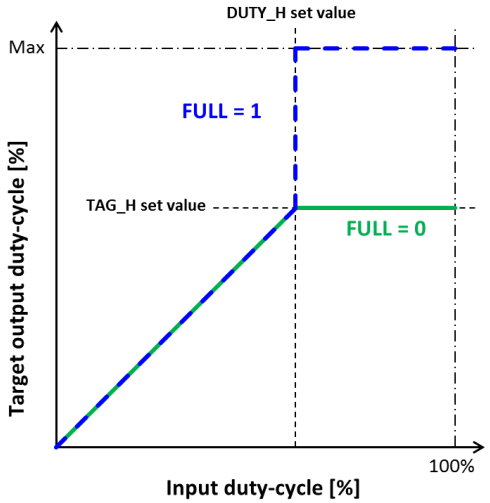


Figure 8. Max Speed Function Setting

DUTY_S: Output Duty-cycle Selection at Input Duty-cycle under DUTY_L

For the behavior at input duty-cycle less than DUTY_L, the register "DUTY_S" provides several options.

The "DUTY_S" sets the input duty cycle of the output duty-cycle to 0%. It is calculated by Equation 4, except for the case of "DUTY_S" = 15.

$$D_0 = \frac{5 \times DUTY\_S}{255} \times 100\ [\%] \qquad \text{(eq. 4)}$$

Where D_0 is input duty-cycle of the motor speed 0 rpm.

Table 12 shows the option of "DUTY_S".

Table 12. THE SETTING OF DUTY_S

DUTY_S	Motor Stop Duty Setting (%)
0	0
1	1.9
2	3.9
3	5.8
4	7.8
5	9.8
6	11.7
7	13.7
8	15.6
9	17.6
10	19.6
11	21.5
12	23.5
13	25.4
14	27.4
15	The value of DUTY_L

When DUTY_S = 15, the threshold duty-cycle is same as the "DUTY_L" setting.

When DUTY_S = 1 to 14, the output duty-cycle keeps "TAG_L" setting from "DUTY_L" to "DUTY_S" and goes to 0 % at defined by Equation 2.

When DUTY_S = 0, the output duty keeps "TAG_L" setting whenever input duty-cycle is less than "DUTY_L".

If "DUTY_L" setting is smaller than "DUTY_S" setting, the threshold is same as "DUTY_L" setting.

To restart the motor rotation, the input duty-cycle must be set higher than "DUTY_S" + 1.6% (i.e. the hysteresis is 1.6%).

Figure 9 shows the speed curves for various "DUTY_S".

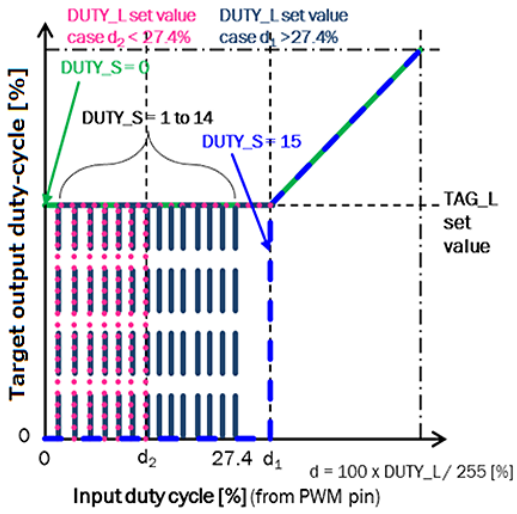


Figure 9. Min Speed Function Setting

Output Duty Cycle Transitions

When PWM input duty cycle changes, output PWM target duty changes along with input and output characteristics setting. The rate that actual output duty cycle changes is set by the register “STEPSEL” and “PWM_ROC”. In case of STEPSEL = 0, actual output duty cycle changes immediately to the target. In case of STEPSEL = 1, actual output duty cycle transfers gradually to the target according to the rate which is defined by PWM_ROC as shown in Table 13. In addition, this register setting is effective not only in changing the input duty cycle but also in changing the mode from Start-up to normal.

Table 13. RATE OF CHANGE FOR OUTPUT DUTY

STEPSEL	PWM_ROC	Rate of Change for Output Duty
0	x	Change immediately to the target
1	0	0.1% per 64 output PWM pulses
1	1	0.1% per 128 output PWM pulses
1	2	0.1% per 256 output PWM pulses
1	3	0.1% per 512 output PWM pulses

NOTE: x: Don’t care

Output Waveform

The output pulse signal is about 0 V–V_{CC}. The duty before commutation change decreases gradually to 0% and the duty after commutation change increases gradually to the duty level controlled by speed control function by built-in function called Soft Switch. This state is shown in Figure 10 as a schematic view.

Soft Switch Setting

The LV8324C can adjust soft switch period as the ratio of L and S shown in Figure 11. It is defined by Equation 5 and Register “SSWHIGH” and “SSWLOW” can adjust it.

$$\text{Soft Switch Period [\%]} = \frac{S}{L} \times 100 \qquad \text{(eq. 5)}$$

Where:

S is Soft Switch period.

L is one commutation period.

Figure 11 shows the soft switch image.

Due to the Soft switch, the averaged output voltage is shown in the blue in Figure 11.

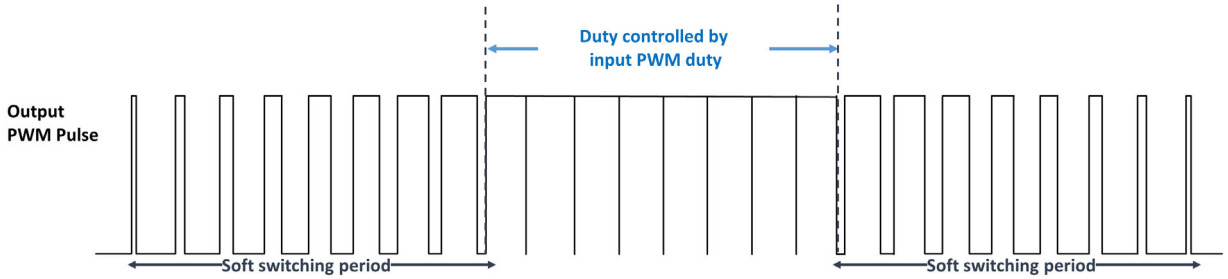


Figure 10. Output Waveform

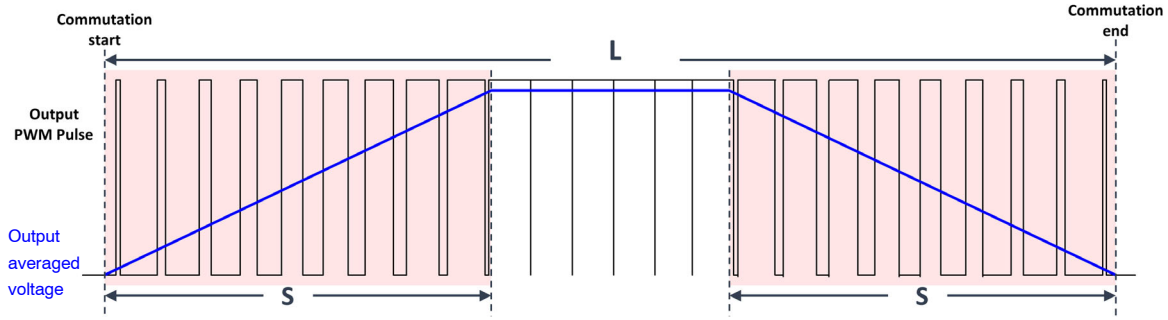


Figure 11. L (Length) and S (Soft Switch)

SSWHIGH is for the maximum output duty-cycle defined by TAG_H and SSWLOW is for the minimum output duty-cycle defined by TAG_L. Each register has 4 bits and Table 14 shows the adjustable value.

Table 14. SOFT SWITCH PERIOD ADJUSTMENT

SSWHIGH SSWLOW	S/L Ratio	SSWHIGH SSWLOW	S/L Ratio
0	2.9%	8	26.4%
1	5.9%	9	29.3%
2	8.8%	10	32.2%
3	11.7%	11	35.2%
4	14.6%	12	38.1%
5	17.6%	13	41.0%
6	20.5%	14	43.9%
7	23.4%	15	46.9%

Once “SSWHIGH” and “SSWLOW” are set, the ratio of Soft Switch in other speed settings is as shown in Figure 12.

FG Output

FG signal output is decided by the Hall signal cross point. The relationship between motor speed and FG frequency represents the following equation.

$$f_{FG}\,[Hz] = \frac{N}{60} \times \frac{p}{2} \qquad \text{(eq. 6)}$$

Where:

N is motor speed [rpm].

p is number of Pole.

Figure 13 shows the timing chart of the hall sensor output and the FG output.

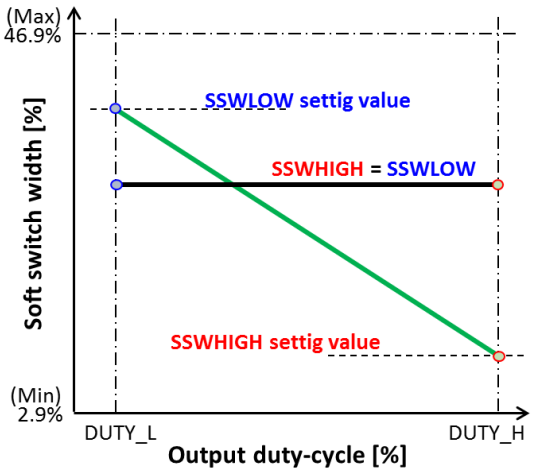


Figure 12. The Relationship between Soft Switch and Speed

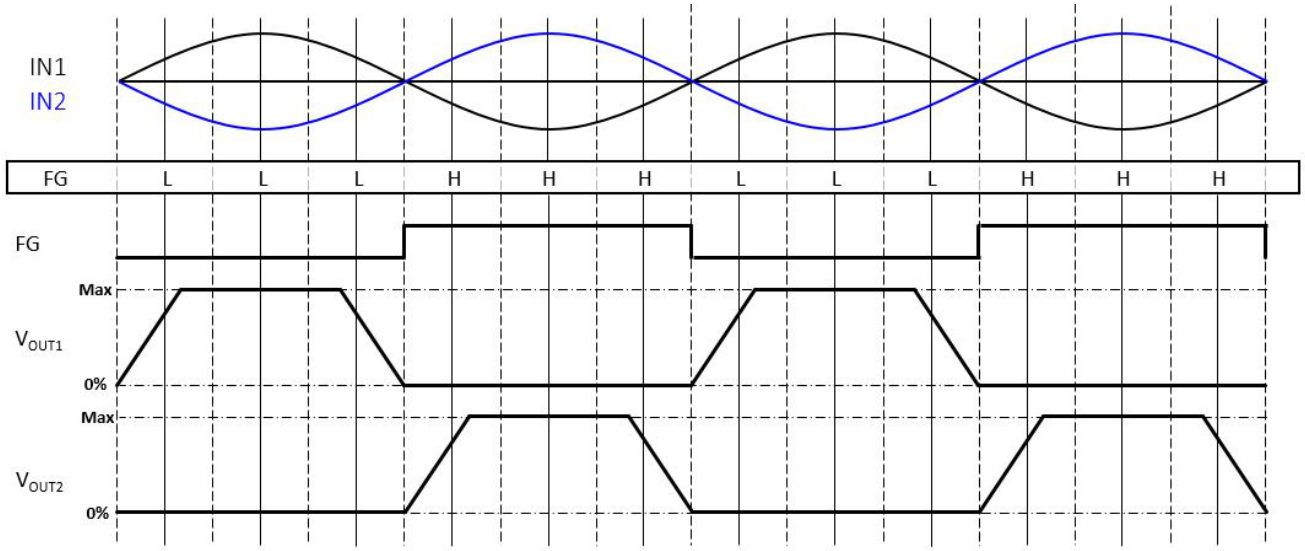


Figure 13. Timing Chart of Output

Lead Angle Setting

In the output, the output current delays from the output voltage because of the inductance of motor coil. The output current which flows in a motor coil generates torque for the motor and the torque is maximized by the synchronization of output current with the BEMF phase. Therefore, this delay decreases an efficiency of motor rotation. It is generally increased in proportion to the rotational speed.

The LV8324C can cancel the delay by earlier commutation than the Hall sensor signal as shown in Figure 14. This phase adjustment is called the “Lead-angle”.

In Figure 14, when the output voltage VOUT1 and the output current IOUT1 in black are changed to the waveform in red after the Lead-angle adjustment and it is the most optimum commutation timing.

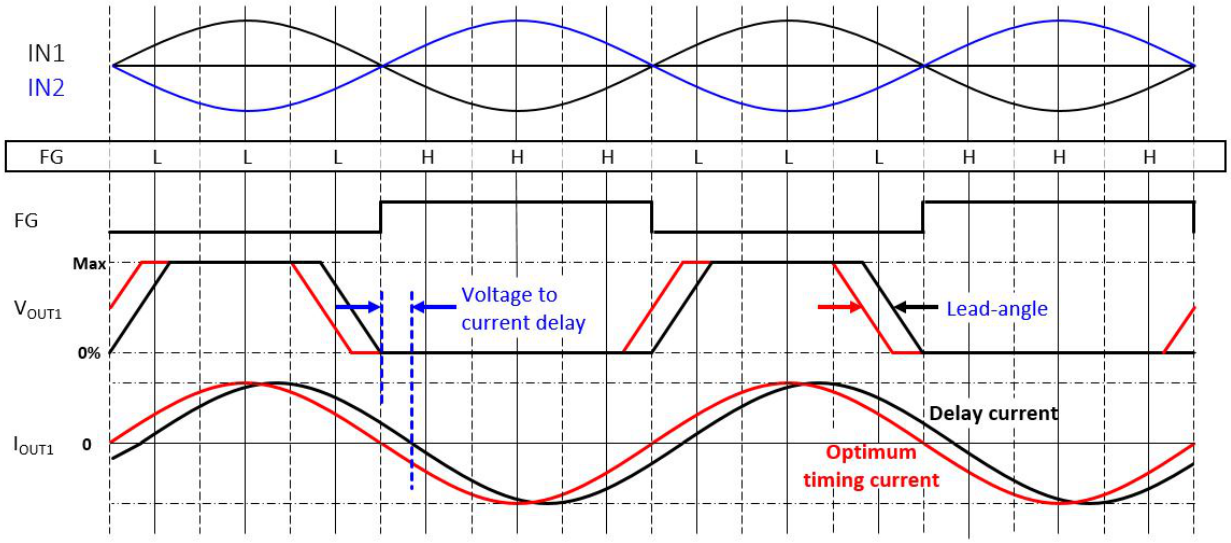


Figure 14. The Relationship between the Lead-angle and the Delay of Output Current

The relationship between output duty-cycle and Lead-angle is shown in Figure 15. The optimum Lead-angle will vary by the motor characteristics so it is necessary to adjust the Lead-angle based on the motor in use.

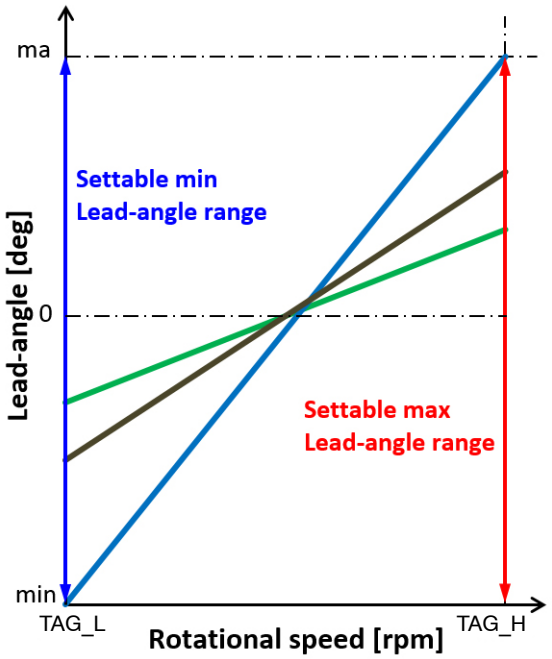


Figure 15. Lead-angle Curve Image

The LV8324C can set the Lead-angle at maximum target output duty-cycle (TAG_H) and at minimum target output duty-cycle (TAG_L) by “DLDEG_H” and “DLDEG_L” individually. These register have 8 bits D[7:0] in each and both MSBs define the direction of phase delay. When MSB sets to “0”, the Lead-angle is set to minus value which means phase delay, that is, the output voltage commutation is delay than the Hall sensor signal. When MSB sets to 1, the Lead-angle is set to plus value which means phase advance, that is, the output voltage commutation is earlier than the Hall sensor signal. The resolution is approximately 0.175°. Hence, the adjustable range of both is from −22.225° to 22.225° expressed in the following equation.

$$L_{max} = \frac{22.225}{127} \times DLDEG_H\ [deg] \qquad \text{(eq. 7)}$$

$$L_{min} = \frac{22.225}{127} \times DLDEG_L\ [deg] \qquad \text{(eq. 8)}$$

Where:

L_{max} is Lead-angle at maximum target output duty-cycle (TAG_H)

L_{min} is Lead-angle at minimum target output duty-cycle (TAG_L)

Once DLDEG_H and DLDEG_L are set, the Lead-angle in other output duty-cycle is set to interpolated and extrapolated value according to the output duty-cycle, even though the output duty-cycle is defined by FULL = 1.

Protections

The LV8324C has the following protection functions:

- TSD (Thermal Shut Down)
- UVLO (Under Voltage Lock Out)
- RDA Detection
- Lock Protection
- CLM (Current Limiter)
- OCP (Over Current Protection)

When the TSD or Lock protection works, all of the internal FETs are turned off. When UVLO or CLM works, the output PWM is off and the motor goes to re-circulation mode.

Thermal Shutdown Protection (TSD)

When LV8324C junction temperature rises to 180°C, TSD will activate and turns off high-side and low-side Power FET. Therefore, OUT1 and OUT2 will become high impedance and the coil current will shut off. When it falls under 140°C, TSD will deactivate and motor will start to rotate.

Under Voltage Lock Out (UVLO)

When VCC voltage goes to low level (5.2 V), UVLO will active and stop the motor. VCC voltage is recovered to above 5.6 V.

The TRUTH TABLE of Operating State with UVLO is as shown in Table 15.

Table 15. UVLO TRUTH TABLE

Input		Register	Output	
IN1	IN2	DRVMODE	OUT1	OUT2
L	H	00 / 01	L	Hi-Z
H	L	00 / 01	Hi-Z	L

RDA (Rotation Decline Alarm) Detection

When motor rotational speed is lower than the threshold, the detect signal is output from FG pin. This function is called “RDA detection”. When the LV8324C detects it, FG pin goes to high and “RDA” register (Address 0x020A, D[3]) posts 1. This detection is enable by “TACHSEL”=1. Motor rotational speed is calculated with hall signal cycle and the threshold is defined by “RDA_DET” as shown in Table 16.

Table 16. RDA THRESHOLD SPEED SETTING

RDA_DET	RDA Threshold Speed Setting
0 to 15	100 rpm step from 500 rpm to 2000 rpm
16 to 63	200 rpm step from 2200 rpm to 11600 rpm

When motor rotational speed is higher than the threshold, RDA is cleared. The threshold of rotational speed to release RDA is defined by “RDA_HYS”.

Table 17. RDA CLEAR SPEED

RDA_HYS	RDA Clear Speed
0	Detection speed + (Detection speed) × 1/16
1	Detection speed + (Detection speed) × 1/8
2	Detection speed + (Detection speed) × 1/4
3	Detection speed + (Detection speed) × 1/2

This detection is masked in Spin-up sequence and in the input duty lower than the “Available duty” which is defined by RDA_MASK. The “available duty” is calculated by following equation.

$$\text{Available Duty [\%]} = N \times 4 \qquad \text{(eq. 9)}$$

Where:

N is value of RDA_MASK

Hence, the “Available duty” is set from 0% to 60% by 4% step. Figure 16 shows the image of RDA detection.

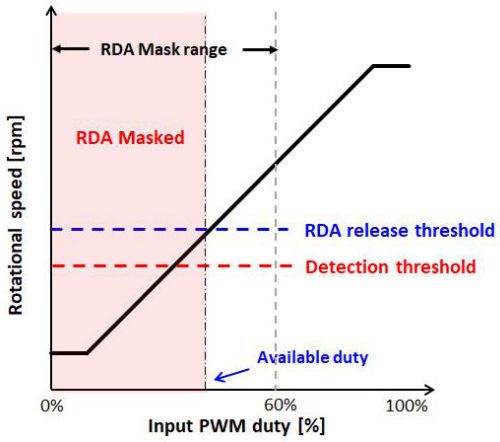


Figure 16. The Image of RDA Detection

Lock Detection and Lock Protection

When the motor is locked, the heat is continuously generated because the LV8324C keeps trying to rotate the motor.

The lock protection works to prevent such a heat generation by turning OUT1 and OUT2 into high impedance and shutting off the motor current. When a motor is locked in the steady rotation mode and the LV8324C doesn’t detect the FG edge for more than 0.3 s which is equivalent to 50 rpm, the lock protection works (Figure 17).

The lock protection signal can be output from FG pin by setting the register “TACHSEL”. In this mode, the RD signal goes to “High”, though it is “Low” at motor starts.

When the motor restarts and IC detects 4 phase changes at least (depends on rotation speed), the RD signal goes to “Low”.

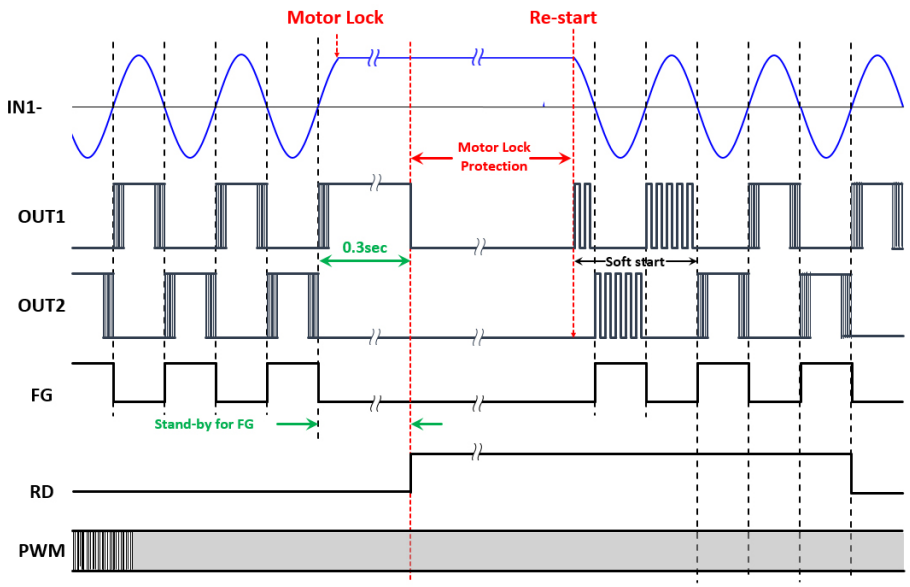


Figure 17. Timing Chart of the Lock Protection

The period of motor lock protection is adjustable and is defined by “RESTART_INT” as shown in Table 18.

Table 18. MOTOR LOCK PROTECTION PERIOD

RESTART_INT	Motor Lock Protection Period [s]
0	3.5
1	5.5
2	7.7
3	9.0

After the period of motor lock protection, the LV8324C tries to rotate the motor and stand-by for FG edge for a certain period defined by “LOCK_DET” as shown in Table 19.

Table 19. STAND-BY PERIOD FOR FG

LOCK_DET	Stand-by Period for FG [s]
0	0.4
1	0.7
2	0.85
3	0.95

Figure 18 shows the relationship between protection period and the number of protection times. The 1st to 4th protection period take a time set by “RESTART_INT” and 5th protection period takes 14 s. To reset the lock protection mode, Stop duty cycle must be applied to the PWM input signal. To retry the motor rotation, Proper duty cycle must be applied to the PWM input signal.

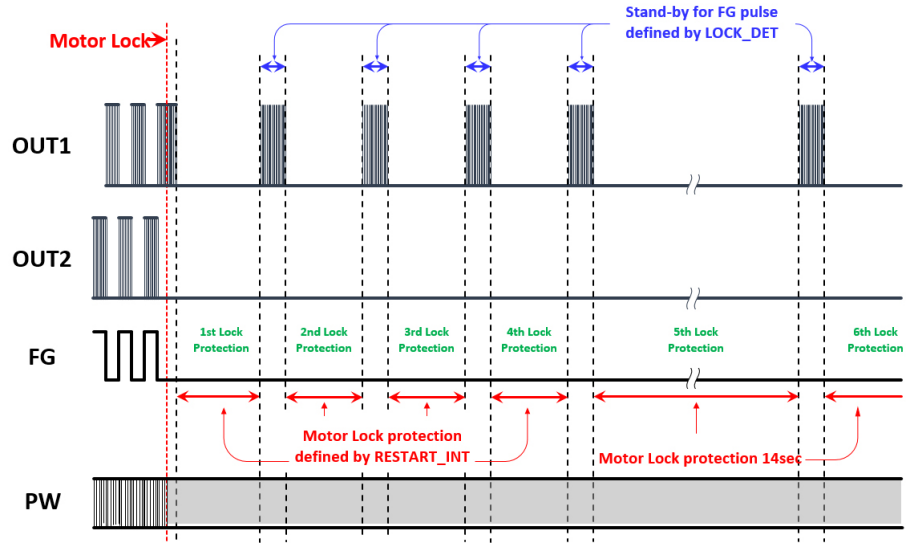


Figure 18. The Relationship between Protection Time and the Number of Protection Times

These protection periods and the number of protection times are applied in accordance with the internal counter. It will reset the counter if the duty−cycle which sets the motor speed to 0 rpm determined by “DUTY_L” and “DUTY_S” is entered during lock protection period. In this case, the lock protection counter will activate from the initial state starting from PWM Pos−Edge and protection period will start from 1st time as shown in Figure 19 and Figure 20.

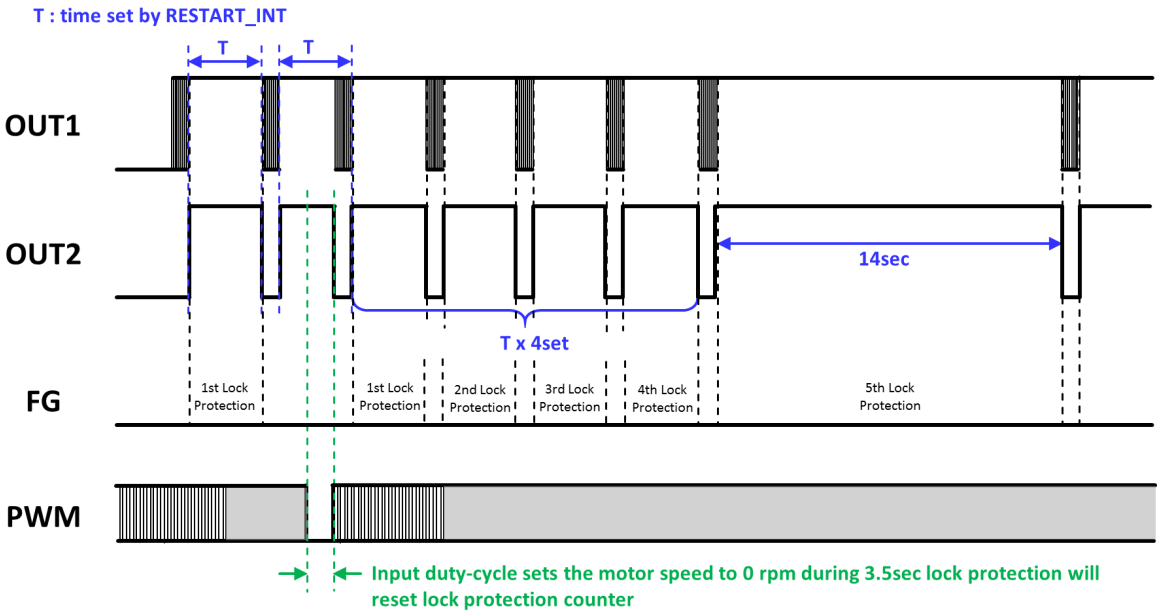


Figure 19. Lock Protection Counter Reset during 3.5 Sec Lock Protection Period

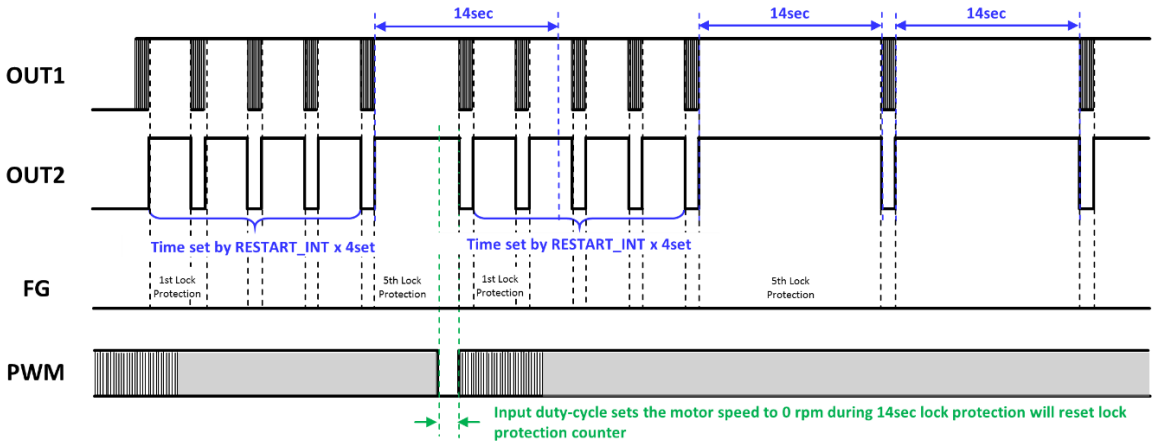


Figure 20. Lock Protection Counter Reset during 14 Sec Lock Protection Period

The lock protection period is changed by the condition of output signal. If the duty−cycle which sets motor speed to 0 rpm is input and the output signals are disappeared during the restart period in lock protection period as shown in light blue in Figure 21, the counter is not reset and the remaining restart period is applied immediately when PWM Pos−Edge will be input as shown in pink in Figure 21. In this case, the protection period is not related to the internal lock protection timer and protection period is not fixed to 3.5 sec or 14 sec.

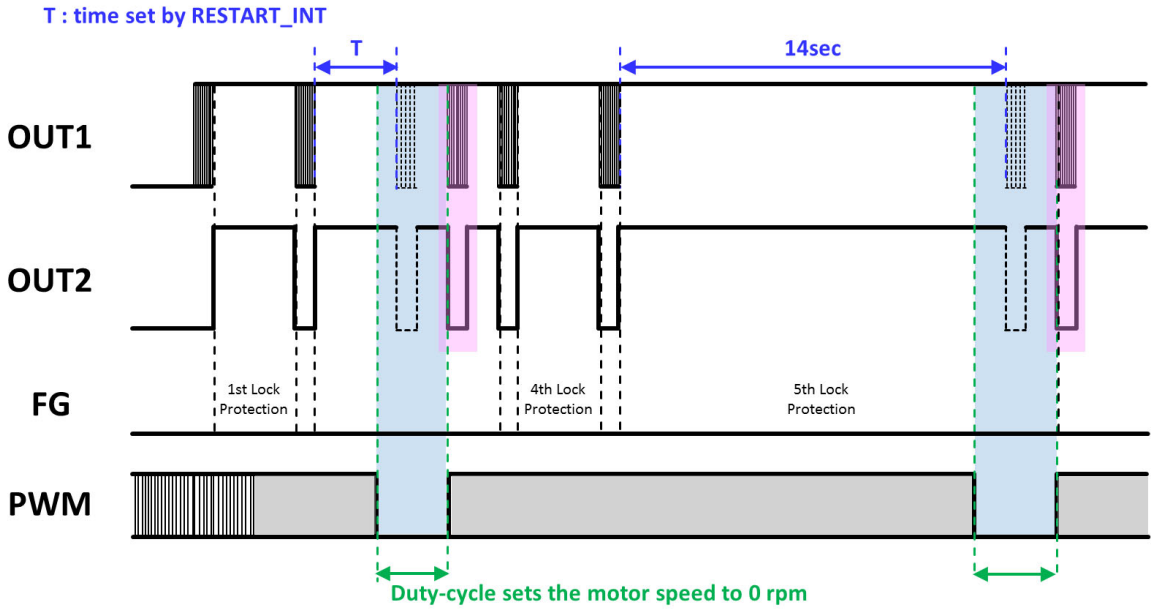


Figure 21. In Case of having Changes in Protection Period

Current Limiter (CLM)

When the coil current becomes large, CLM will activate and then output will be in the re-circulation state. The current is monitored by RF pin and the threshold is 100 mV.

There are three registers related to the current limiter function. The first one is CL_SKIP which can set the period of protection operation when CLM is detected. The second one is CL_ASYNC. When “1” is set to this register while CLM is active, synchronous rectification of the output becomes disabled. The third one is OCP_MASK which sets the masking time to ignore upper and lower FET’s reverse recovery. Table 20 shows the mask time.

Table 20. CLM MASK TIME

OCP_MASK	CLM Mask Time [µs]
0	0.5
1	1.0
2	2.0
3	4.0

Overcurrent Protection (OCP)

OCP monitors the coil current by RF pin and if it becomes larger than 150 mV even if CLM is activated, OCP works to prevent the device or motor from breakdown. OCP operation is to turn OUT1 and OUT2 into high impedance and to shut off the motor current.

This function has also the mask time same as CLM function shown in Table 20.

Register called OCP_LAT_CLR allows to select behavior when OCP is activated. One is to keep the motor stopped until the next power on sequence, and the other one is to activate Lock protection mode.

Nonvolatile Memory

The LV8324C has internal nonvolatile memory which can store register values which define various parameters and settings. The stored register values will be reloaded at POR shown as Figure 22. LV8324C has also the communication mode. It allows user to modify register values, and to store them to the nonvolatile memory (Figure 22). It doesn’t need the resistors as like the conventional models to set the various review. In addition, PCB design becomes simpler.

Here is a list of the main configurable items:

- Max/Min Output duty-cycle
- Max/Min input duty-cycle
- Lead-angle
- Soft start

Program/Erase to the memory is performed through a built-in register. Please note that Program/Erase is allowed for 10 times only. For the detail, please see the application note “NVM Programming Procedure”.

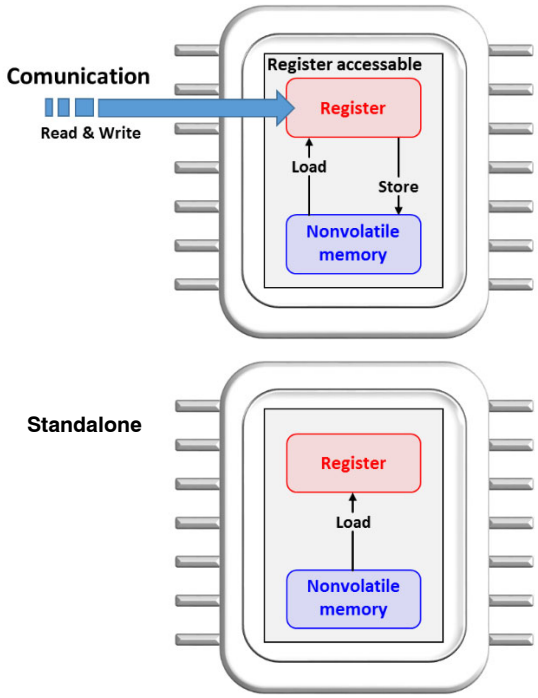


Figure 22. Image of the Internal Register and Nonvolatile Memory

Serial Interface

The LV8324C allows communication via UART (Universal Asynchronous Receiver Transmitter). Various parameter registers can be accessed through UART communication.

UART is one to one communication and the LV8324C doesn’t support parallel access to the multiple devices, so be sure to turn on only the target devices.

The LV8324C provides two UART modes, a one-wire mode and a two-wire mode. In one-wire mode, the FG pin is used for both input and output. In two-wire mode, the FG pin is used as output and the PWM pin is used as input. The state of the TSL pin defines the UART mode as shown in Table 21.

Table 21. I/O PIN CONDITION IN UART MODE

	One-wire Mode	Two-wire Mode
TSL pin	Pull down (GND)	Pull-up (VDD)
Communi-cation Pin	FG pin (for Read and Write)	PWM pin (for Write) FG pin (for Read)

Figure 23 shows the connection image of one-wire mode. The communication line FG should be open-drain type because it supports duplex mode. Therefore the communication pin of the MPU or CPU must be an open-drain output. Figure 24 shows the connection image of two-wire mode. Please refer to the Application note AND9761/D for the detail.

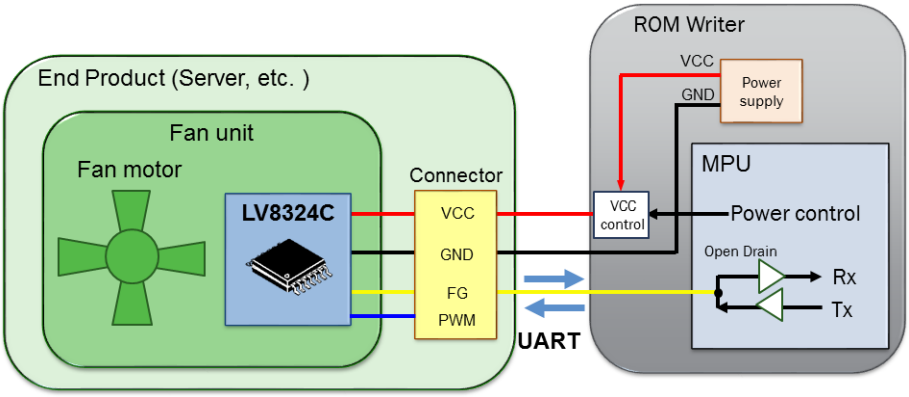


Figure 23. Connection Image of One-wire Mode UART

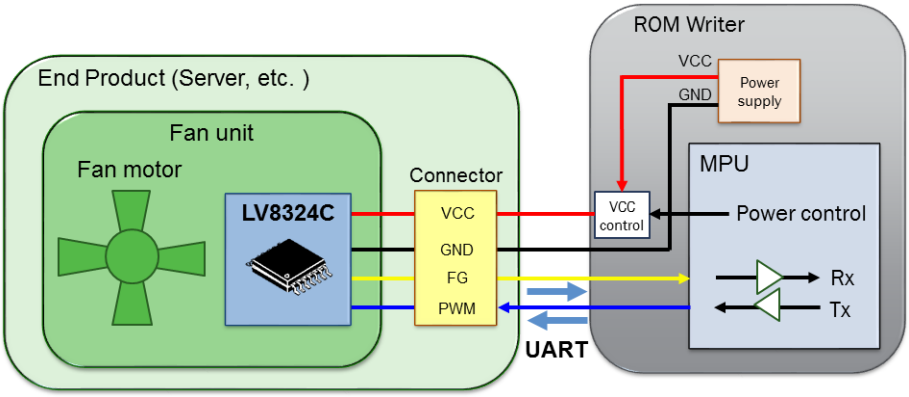


Figure 24. Connection Image of Two-wire Mode UART

About the detail of communication protocol, please see the Application note, AND9761/D.

REGISTER MAP

Register MAP

Internal register map can be classified into four types as shown in Table 22 and 23.

- Read Only
- Read/Write, User defined registers to be written to nonvolatile memory.
- Read/Write
- Write Only (Auto Clear)

Table 22. REGISTER MAP 1 (ADDRESS 0x0000−0x0116)

Address	Initial	Register							
		D7	D6	D5	D4	D3	D2	D1	D0
0x0000	0xAA	1	0	1	0	1	0	1	0
0x0001	0x55	0	1	0	1	0	1	0	1
0x0002	0x00					0	0	RECALC_EN	RELOAD_EN
0x0003	0x00								RELOAD
0x0004	0x00								RECALC
0x0005	0x10	Identification Number							
0x0100	0x00	TAG_L[7:0]							
0x0101	0xFF	TAG_H[7:0]							
0x0102	0x00	DUTY_L[7]	DUTY_L[6:0]						
0x0103	0xFF	DUTY_H[7]	DUTY_H[6:0]						
0x0104	0x00	DLDEG_L[7:0]							
0x0105	0x00	DLDEG_H[7:0]							
0x0106	0x66	SSWHIGH[3:0]				SSWLOW[3:0]			
0x0107	0x01					0	PWMIN_INV	0	DRVMODE[0]
0x0108	0xA4	Reserved	FULL	SS_SW_SEL	SSTART_SEL[1:0]		INCTIM[2:0]		
0x0109	0x00					DUTY_S[3:0]			
0x010A	0x02							DTIME[1:0]	
0x010B	0x02					CL_SKIP	CL_ASYNC	OCP_LAT_CLR	STEPSEL
0x010C	0x00							TACHSEL[1:0]	
0x010D	0x00							PWMAV[1:0]	
0x010E	0x02							OCP_MASK[1:0]	
0x010F	NA			0	0	0	0	ON_INTERNAL	0
0x0110	0x00					LOCK_FAULT	0	0	0
0x0111	0x00	MSKDEG_TP[3:0]				0	0	0	0
0x0112	0x0A					1	0	PWM_ROC[1:0]	
0x0113	0xF0	LOCK_DET[1:0]		RESTART_INT[1:0]		RDA_MASK[3:0]			
0x0114	0x40	RDA_HYS[1:0]		RDA_DET[5:0]					
0x0115	NA	ON_INTERNAL							
0x0116	0x08					ST_DLY_TIM[1:0]		0	0

Table 23. REGISTER MAP 3 (ADDRESS 0x0219)

Address	Key	Initial	Register							
			D7	D6	D5	D4	D3	D2	D1	D0
0x0219	Free	0x00		SWI_ERR[6:0]						

Registers in the black cells do not exist. Therefore, these registers cannot be written and the read values are always zero. The bits with numeric values (0 or 1) must remain as-is.

There are some register addresses which contain both the bits stored in NVM and the bits not stored in NVM. Confirm the bit types to save the data to NVM.

Register Description

Table 24. REGISTER ADDRESS 0x0000−0x0005 − REGISTER DESCRIPTION 1

Function	Address	Bits	Register Name	Description
Fixed Register 1	0x0000	[7:0]	−	Data of 0xAA are stored. (Read only)
Fixed Register 2	0x0001	[7:0]	−	Data of 0x55 are stored. (Read only)
Enable Re-calculation	0x0002	[1]	RECALC_EN	This register enable re-calculation of Speed/Lead Angle/Soft SW setting. 0: Disable 1: Enable
Register Re-loading (Memory to Register)	0x0002	[0]	RELOAD_EN	This register enables data reloading from NVM. 0: Disable 1: Enable
Register Re-loading (Memory to Register)	0x0003	[0]	RELOAD	When this bit is set to 1, data reloading from NVM is executed while RELOAD_EN is set to 1. This register is auto clear type.
Trigger of Re-calculation	0x0004	[0]	RECALC	When this bit is set to 1, re-calculation of Speed/Lead Angle/Soft SW setting is executed while RECALC_EN is set to 1. This register is auto clear type.
Device ID	0x0005	[7:0]	ID_NUMBER	Data of device ID are stored. (Read only)

Table 25. REGISTER ADDRESS 0x0100−0x0116 − REGISTER DESCRIPTION 2

Function	Address	Bits	Register Name	Description
Minimum Speed Setting	0x0100	[7:0]	TAG_L	These registers set minimum/maximum output duty−cycle. TAG_L\TAG_H = 0 to 250 Output duty_cycle (%) = TAG_L\TAG_H x 0.4 TAG_L\TAG_H = 251 to 255 Output duty_cycle (%) = 100 * Refer to the section “Steady Rotation” for details.
Maximum Speed Setting	0x0101	[7:0]	TAG_H	
Minimum Input Duty Cycle Setting	0x0102	[7:0]	DUTY_L	These registers set minimum input duty−cycle. 0000 0000: Duty 0% 0111 1111: Duty 49.8%
Maximum Input Duty Cycle Setting	0x0103	[7:0]	DUTY_H	These registers set maximum input duty−cycle. 1000 0000: Duty 50.2% 1111 1111: Duty 100%
Lead−angle Setting at Minimum Speed	0x0104	[7:0]	DLDEG_L	This register adjusts lead-angle at rotational speed set by TAG_L. 000 0000: 0 degree, 111 1111: −22.225 deg (DLDEG_L[7] = 0) 000 0000: 0 degree, 111 1111: +22.225 deg (DLDEG_L[7] = 1)
Lead−angle Setting at Maximum Speed	0x0105	[7:0]	DLDEG_H	This register adjusts lead−angle at rotational speed by TAG_H. 000 0000: 0 degree, 111 1111: −22.225 deg (DLDEG_H[7] = 0) 000 0000: 0 degree, 111 1111: +22.225 deg (DLDEG_H[7] = 1)
Soft Switch Width Setting at Maximum Output Duty-cycle	0x0106	[7:4]	SSWHIGH	Soft switch width is set at output duty-cycle set by TAG_H. 0000: 2.9% equivalency of one commutation period. 1111: 46.9% equivalency of one commutation period.
Soft Switch Width Setting at Minimum Output Duty-cycle	0x0106	[3:0]	SSWLOW	Soft switch width is set at output duty-cycle set by TAG_L. 0000: 2.9% equivalency of one commutation period. 1111: 46.9% equivalency of one commutation period.

Table 25. REGISTER ADDRESS 0x0100−0x0116 − REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
Speed Control Slope Invert	0x0107	[2]	PWMIN_INV	Control slope polarity for input duty−cycle is changed. 0: Normal mode (Low duty−cycle is low speed rotation) 1: Invert mode (Low duty−cycle is high speed rotation)
Sync/Async Drive Select	0x0107	[0]	DRVMODE	This register selects synchronous/asynchronous drive. 00: High-side switching is PWM. Low-side switching is asynchronous 01: High-side switching is PWM. Low-side switching is synchronous
Reserved	0x0108	[7]	Reserved	Must be kept as 1
Maximum Speed Setting 2	0x0108	[6]	FULL	This register defines the output behavior when input PWM is greater than the duty cycle set by DUTY_H. 0: Fixed speed set by TAG_H 1: Fixed duty cycle of 100% with soft switch
Soft Switch Mask Time Select	0x0108	[5]	SS_SW_SEL	This register sets soft switch period in soft start mode. 0: Rise 2.5 ms, Fall 5 ms 1: Rise 1.25 ms, Fall 2.5 ms
Soft Start End Duty-cycle	0x0108	[4:3]	SSTART_SEL[1:0]	This register sets Soft start end duty-cycle. 0: 0% output duty-cycle (Disable Soft Start) 1: 24% output duty-cycle 2: 54% output duty-cycle 3: 80% output duty-cycle
Soft Start Release Time	0x0108	[2:0]	INCTIM	This register sets the soft start duration time.
Minimum Speed Setting 2	0x0109	[3:0]	DUTY_S	This register sets the various speed when input duty-cycle is less than DUTY_L.
Dead Time setting	0x010A	[1:0]	DTIME	This register sets dead time in synchronous rectification drive. 00: 125 ns 01: 250 ns 10: 500 ns 11: 0 ns
Disable Period of Motor Current in CL	0x010B	[3]	CL_SKIP	This register sets disable period of motor current when CLM is active. 0: only for corresponding PWM pulse 1: for corresponding and next PWM pulse
Disable Motor Synchronous Rectification in CL	0x010B	[2]	CL_ASYNC	This register disables motor synchronous rectification when CLM is active. 0: Synchronous rectification is not disable when CLM is active. 1: Synchronous rectification is disable until detecting Hall signal or motor stop signal when CLM is active. After detecting Hall signal or motor stop, synchronous rectification is enabled.
Condition to Enter Lock Protection Mode in OCP Active	0x010B	[1]	OCP_LAT_CLR	This register selects the status when OCP is activated. 0: The motor stops until next power on sequence. 1: The IC goes to “Lock Protection mode”.
Speed Control Slope Setting	0x010B	[0]	STEPSEL	To prevent drastic changes of a target speed in the closed loop control, this register selects slopes of the target speed change against the input duty cycle change. (The amount is prescribed in the time per 1FG pulse) 0: 1/4 of the existing speed, or ±2047 rpm (smaller one is chosen) 1: 1/8 of the existing speed, or ±1023 rpm (smaller one is chosen)
FG/RD Select	0x010C	[1:0]	TACHSEL	This register sets FG pin function. 00: FG output 01: RDA output 10: RD output (Rotation is Low, Locked motor is High) 11: RD output (Rotation is High Locked motor is Low)

Table 25. REGISTER ADDRESS 0x0100–0x0116 – REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
Input PWM Average Setting	0x010D	[1:0]	PWMAV	The number of times to perform averaging for input PWM duty cycle. 00: Not averaged 01: Averaged 4 times 10: Averaged 8 times 11: Averaged 16 times
Mask Time for Reverse Recovery Time Setting	0x010E	[1:0]	OCP_MASK	This register sets the masking time to ignore the reverse recovery for both high-side and low-side Power FET. 00: 0.5 μs 01: 1.0 μs 10: 2.0 μs 11: 4.0 μs
Lock Protection Enable	0x0110	[3]	LOCK_FAULT	This register selects enable or disable of the lock protection function. 0: Lock protection enable 1: Lock protection disable
OFF Time Setting (TOP)	0x0111	[7:4]	MSKDEG_TP	This register sets off period at commutation initiation. It is selected as follows: [7] 0: In angle 1: In time [6:4] 000: 0 deg or 0 s 001: 0.35 deg or 2.0 μs 010: 0.70 deg or 4.0 μs 011: 1.05 deg or 10.0 μs 100: 2.10 deg or 14.0 μs 101: 3.50 deg or 20.0 μs 110: 4.90 deg or 28.0 μs 111: 7.00 deg or 40.0 μs
Increment Ratio of the Output-duty	0x0112	[1:0]	PWM_ROC	This register sets the increment ratio of the output-duty in case of “STEPSEL=1”. 00: 0.1% per 64 pulses 01: 0.1% per 128 pulses 10: 0.1% per 256 pulses 11: 0.1% per 512 pulses
Standby Period for FG Pulse in Lock Protection	0x0113	[7:6]	LOCK_DET	This register sets standby period for FG pulse in Lock protection. 00: 0.4s 01: 0.7s 10: 0.85s 11: 0.95s
Lock Protection Period	0x0113	[5:4]	RESTART_INT	This register sets Lock protection period. 00: 3.5 s 01: 5.5 s 10: 7.7 s 11: 9.0 s
Threshold of RDA MASK	0x0113	[3:0]	RDA_MASK[3:0]	This register sets the input duty-cycle to mask RDA. See (eq. 9) to calculate the output duty-cycle of RDA MASK.
RDA Release Threshold	0x0114	[7:6]	RDA_HYS	This register sets the threshold of RDA release. 00: Detection speed + (Detection speed) × 1/16 01: Detection speed + (Detection speed) × 1/8 10: Detection speed + (Detection speed) × 1/4 11: Detection speed + (Detection speed) × 1/2
RDA Detection Threshold	0x0114	[5:0]	RDA_DET	This register sets the threshold of RDA detection. 0–15: 100 rpm step from 500 rpm to 2000 rpm 16–63: 200 rpm step from 2200 rpm to 11600 rpm

Table 25. REGISTER ADDRESS 0x0100–0x0116 – REGISTER DESCRIPTION 2 (continued)

Function	Address	Bits	Register Name	Description
Ignore Time of PWM Input Duty Cycle	0x0116	[3:2]	ST_DLY_TIM	This register sets the ignore time of PWM input duty-cycle. 00: 0 s 01: 0.5 s 10: 1.0 s 11: 1.5 s

Table 26. REGISTER ADDRESS 0x0219 REGISTER DESCRIPTION

Function	Address	Bits	Register Name	Description
Communication Error Status	0x0219	[6:0]	SWI_ERR	Communication error status store to these registers. (Read only) Refers to the section “COMMUNICATION ERROR” for details.

Communication Error

The Communication error is reported in the Register (Address 0x0219). Table 27 shows the error report functions.

Table 27. ERROR REPORT DESCRIPTION

Address	Bit	DRV MODE	Error Description	State after Error		
				Mode	Communication	Transferred Data
0x0219	D[6]	R/W Field Data Error	Non-zero value is written in the D[5:1] in R/W Field	Wait for the data from the master	Enable	In write mode; Nullified In read mode; No action
	D[5]	Time Out Error	The delay between the fields in “Communication mode” is longer than 3 fields	“Standby”	Terminated	–
	D[4]	Checksum Error	Checksum value is wrong in write mode	“Error”	Terminated	Nullified
	D[3]	Data Length Field Parity Error	The parity in “Data Length Field” is wrong	“Error”	Terminated	Nullified
	D[2]	R/W Field Parity Error	The parity in “R/W Field” is wrong	“Error”	Terminated	Nullified
	D[1]	Header Error	Header input is not correct	“Error”	Terminated	Nullified
	D[0]	Framing Error	The signal pin is “Low” state in Stop bits	“Error”	Terminated	Nullified

When “Time out error” posts “1” in D[5] of register 0x0219, the LV8324C goes into standby mode.

If the data length is long and the “Time out Error” is happened during the Register write, the data with the correct “Checksum” transferred before the “Time out Error” is stored in register, then the LV8324C goes to “Standby mode”.

When “Checksum error” posts “1” in D[4] of Register 0x0219 while in the Write mode, the LV8324C goes into Error mode and the communication is terminated. In this case, the transferred data is discarded but the data with correct “Checksum” transferred before the “Checksum error” is stored in the register.

Other errors, except for “R/W Field Data Error” also write “1” in the specified register and the LV8324C goes to “Error mode” as well. To recover from “Error mode”, the communication pin should be kept “High” for longer than the time corresponding to 4 “Fields”, then the LV8324C goes to “Standby mode” automatically despite of the status of error register.

Each error register keeps the error bit until the master reads the error register.

Reading Reg. 0x0219 as 1 byte will clear the error bits. Multiple read will not clear the error bits.

It is recommended to read the error register after every transaction to confirm that the communication is completed successfully.

Figure 25 shows the state diagram. Refer to the application note AND9761/D as well for more information regarding the communication.

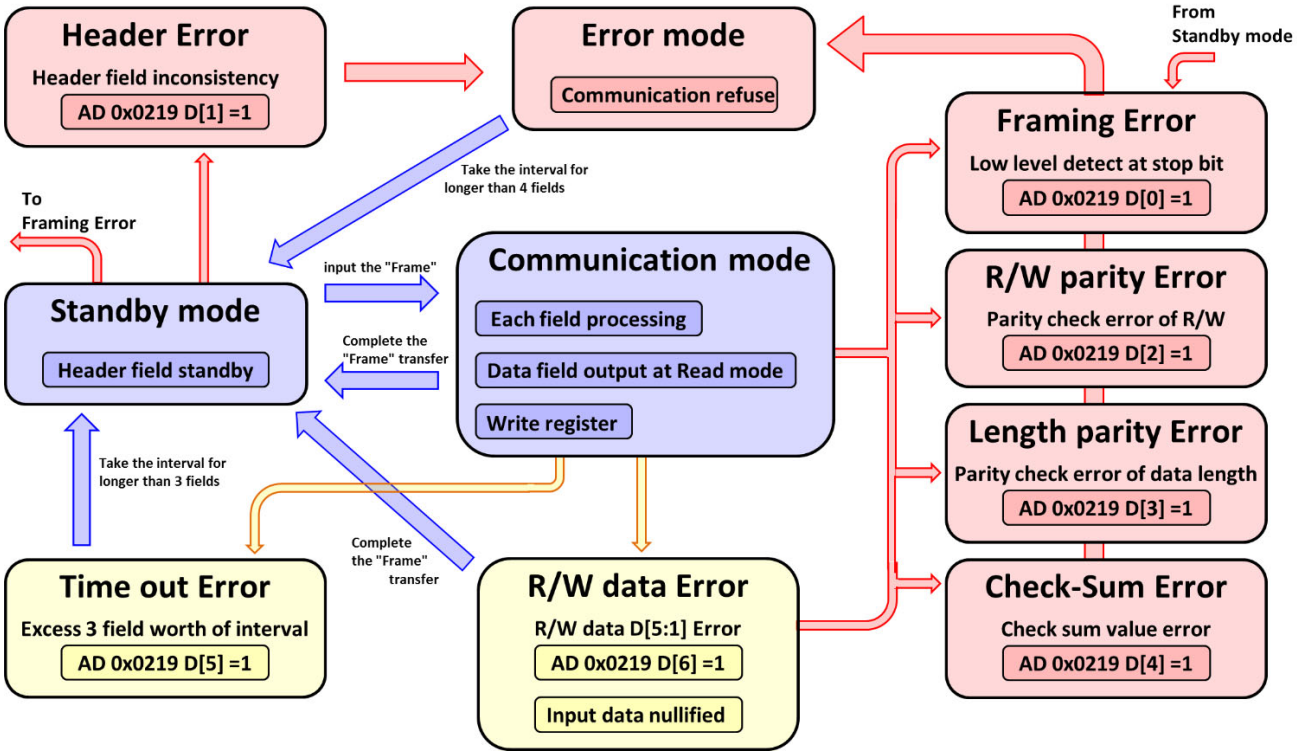
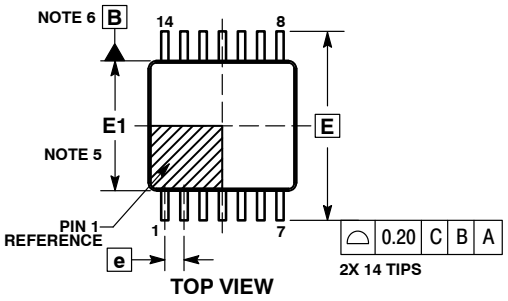
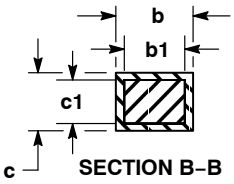


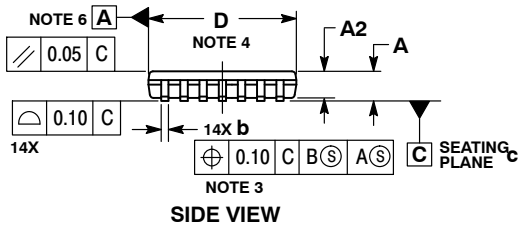
Figure 25. State Transition Diagram of Each Error

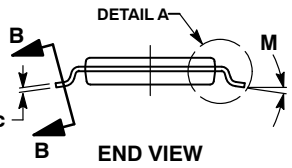
PACKAGE DIMENSIONS

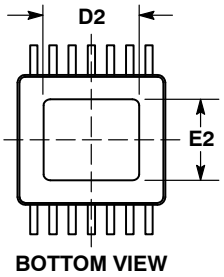
TSSOP−14 EP
CASE 948AW
ISSUE C

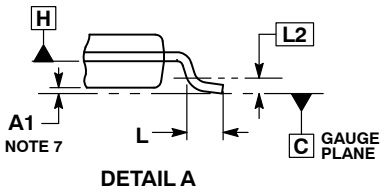








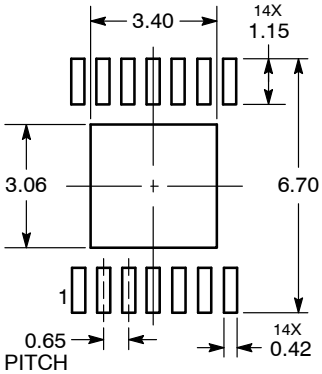




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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