

# PACVGA105

## VGA Port Companion Circuit

### Product Description

The PACVGA105 incorporates 7 channels of ESD protection for signal lines commonly found in a VGA port for PCs. ESD protection is implemented with current steering diodes designed to safely handle the high peak surge currents associated with the IEC-1000-4-2 Level-4 ESD Protection Standard ( $\pm 8$  kV contact discharge). When the channels are subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into the positive supply rails or ground where they may be safely dissipated.

The upper ESD diodes for the R, G and B channels are connected to a separate supply rail ( $V_{RGB}$ ) to facilitate interfacing to graphics controller ICs with low voltage supplies. The remaining channels are connected to the main 5 V rail ( $V_{CC}$ ). The lower diodes for the R, G and B channels are also connected to a dedicated ground pin (GNDA) to minimize crosstalk due to common ground impedance.

Two non-inverting buffers are also included in this IC for buffering the HSYNC and VSYNC signals from the graphics controller IC. These buffers will accept TTL input levels and convert them to CMOS output levels that swing between GND and  $V_{CC}$ . These drivers have a nominal  $60\ \Omega$  output impedance to match the characteristic impedance of the HSYNC and VSYNC lines of the video cables typically used. The inputs of these drivers also have high impedance pull-ups ( $50\ \text{k}\Omega$  nom.) pulling up to the  $V_{AUX}$  rail. In addition, the DDC\_CLOCK and DDC\_DATA channels have  $1.8\ \text{k}\Omega$  resistors pulling these inputs up to the main 5 V ( $V_{CC}$ ) rail.

### Features

- Seven Channels of ESD Protection Designed to Meet IEC-1000-4-2 Level-4 ESD Requirements ( $\pm 8$  kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes at Less than 5 pF Typical
- TTL to CMOS Level-Translating Buffers for the HSYNC and VSYNC Lines
- Three Independent Supply Pins ( $V_{CC}$ ,  $V_{RGB}$  and  $V_{AUX}$ ) to Facilitate Operation with Sub-Micron Graphics Controller ICs
- High impedance Pull-Ups ( $50\ \text{k}\Omega$  Nominal to  $V_{AUX}$ ) for HSYNC and VSYNC Inputs
- Pull-Up Resistors ( $1.8\ \text{k}\Omega$  Nominal to  $V_{CC}$ ) for DDC\_CLK and DDC\_DATA Lines
- Compact 16-Pin QSOP Package
- These Devices are Pb-Free and are RoHS Compliant

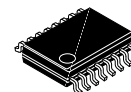
### Applications

- ESD Protection and Termination Resistors for VGA (Video) Port Interfaces
- Desktop PCs
- Notebook Computers
- LCD Monitors



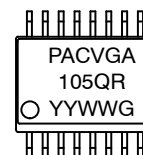
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**QSOP16  
QR SUFFIX  
CASE 492**

### MARKING DIAGRAM



PACVGA105QR = Specific Device Code  
YY = Year  
WW = Work Week  
G = Pb-Free Package

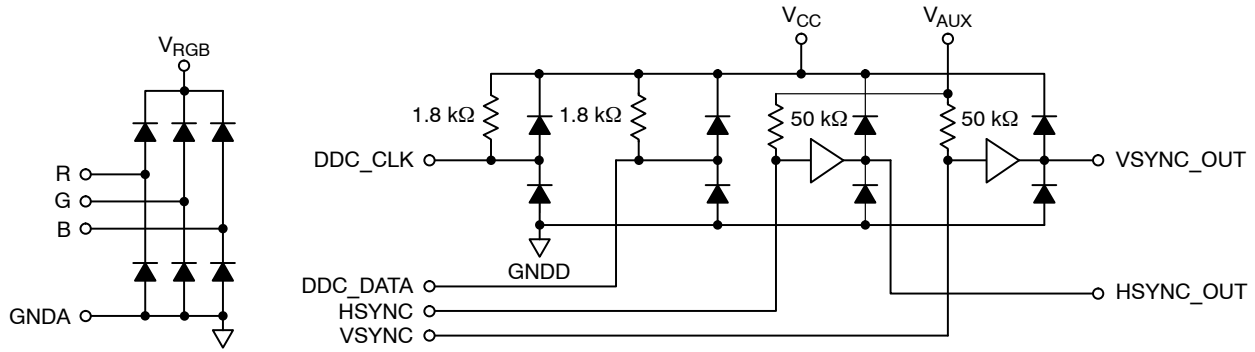
### ORDERING INFORMATION

| Device      | Package             | Shipping†        |
|-------------|---------------------|------------------|
| PACVGA105QR | QSOP16<br>(Pb-Free) | 2500/Tape & Reel |

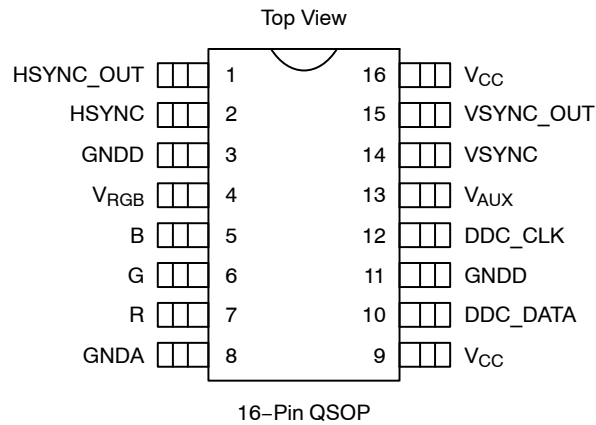
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# PACVGA105

## SIMPLIFIED ELECTRICAL SCHEMATIC



## PACKAGE / PINOUT DIAGRAMS



**Table 1. PIN DESCRIPTIONS**

| Lead(s) | Name      | Description   |
|---------|-----------|---|
| 1       | HSYNC_OUT | Horizontal sync signal buffer output. Connects to the video connector side of the horizontal sync line.   |
| 2       | HSYNC     | Horizontal sync signal buffer input. Connects to the VGA Controller side of the horizontal sync line.   |
| 3, 11   | G_NDD     | Digital ground reference supply pin.  |
| 4       | V_RGB     | V_RGB supply pin. This is an isolated supply pin for the R, G and B ESD protection circuits.  |
| 5       | B         | Blue signal video protection channel. This pin is typically tied to the B video line between the VGA controller device and the video connector.   |
| 6       | G         | Green signal video protection channel. This pin is typically tied to the G video line between the VGA controller device and the video connector.  |
| 7       | R         | Red signal video protection channel. This pin is typically tied to the R video line between the VGA controller device and the video connector.  |
| 8       | G_NDA     | Analog ground reference supply pin.   |
| 9, 16   | V_CC      | V_CC supply pin. This is the main supply input for the DDC_CLK and DDC_DATA pullup resistors and ESD protection circuits. It is also connected to the sync buffers and to the ESD protection diodes present on the HSYNC_OUT and VSYNC_OUT lines. |
| 10      | DDC_DATA  | DDC data pin.   |
| 12      | DDC_CLK   | DDC clock pin.  |
| 13      | V_AUX     | V_AUX supply pin. This is the supply input for the 50 kΩ pullups connected to the HSYNC and VSYNC buffer inputs.  |
| 14      | VSYNC     | Vertical sync signal buffer input. Connects to the VGA Controller side of the vertical sync line.   |
| 15      | VSYNC_OUT | Vertical sync signal buffer output. Connects to the video connector side of the vertical sync line.   |

# PACVGA105

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Parameter  | Rating   | Units |
|--|--|-------|
| $V_{CC}$ , $V_{RGB}$ , $V_{AUX}$ Supply Voltage Inputs               | [GND – 0.5] to +6.0  | V     |
| Diode Forward Current (One Diode Conducting at a Time)               | 20   | mA    |
| DC Voltage at Inputs<br>R, G, B<br>HSYNC, VSYNC<br>DDC_CLK, DDC_DATA | [GND – 0.5] to [ $V_{RGB}$ + 0.5]<br>[GND – 0.5] to [ $V_{AUX}$ + 0.5]<br>[GND – 0.5] to [ $V_{CC}$ + 0.5] | V     |
| Operating Temperature Range  | 0 to +70   | °C    |
| Storage Temperature Range  | –40 to +150  | °C    |
| Package Power Rating   | 750  | mW    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

| Symbol    | Parameter   | Min         | Max                                | Units |
|-----------|---|-------------|------------------------------------|-------|
| $V_{CC}$  | Main Supply Voltage                                       | 4.5         | 5.5                                | V     |
| $V_{RGB}$ | RGB Supply Voltage  | 1.7         | 3.7                                | V     |
| $V_{AUX}$ | Auxiliary Supply Voltage                                  | 2.9         | 3.7                                | V     |
| $V_{IH}$  | Logic High Input Voltage (Note 1)                         | 2.0         |                                    | V     |
| $V_{IL}$  | Logic Low Input Voltage (Note 1)                          |             | 0.8                                | V     |
| $V_I$     | Input Voltage<br>RGB<br>HSYNC, VSYNC<br>DDC_CLK, DDC_DATA | 0<br>0<br>0 | $V_{RGB}$<br>$V_{AUX}$<br>$V_{CC}$ | V     |
| $I_{OH}$  | High Level Output Current (Note 1)                        |             | –8                                 | mA    |
| $I_{OL}$  | Low Level Output Current (Note 1)                         |             | 8                                  | mA    |
| $T_A$     | Free–Air Operating Temperature                            | 0           | +70                                | °C    |

1. These parameters apply only to the HSYNC and VSYNC signals.

# PACVGA105

## SPECIFICATIONS (Cont'd)

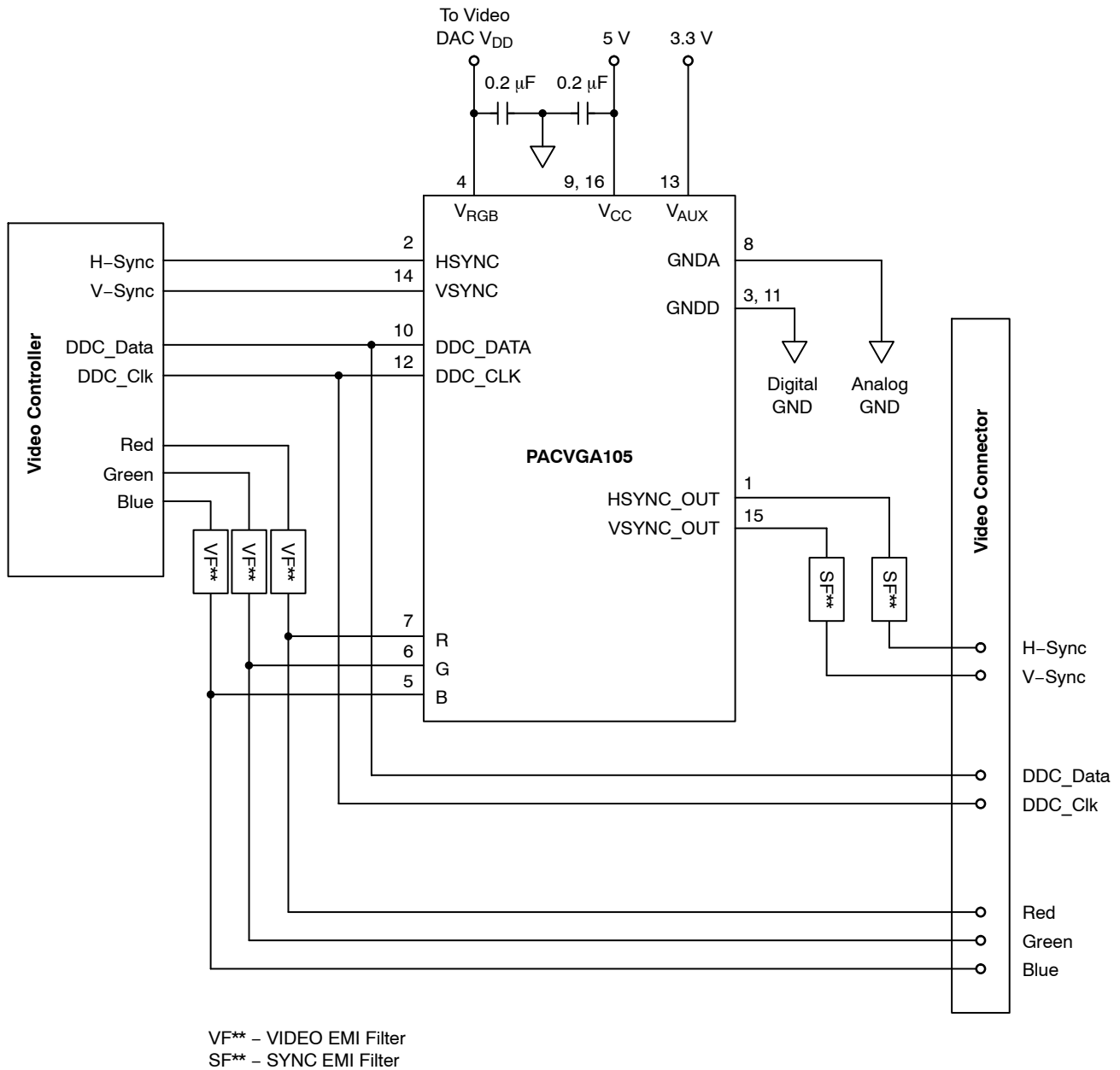
**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

| Symbol     | Parameter   | Conditions  | Min     | Typ          | Max                         | Units         |
|------------|---|---|---------|--------------|-----------------------------|---------------|
| $V_F$      | Diode Forward Voltage   | $I_F = 10 \text{ mA}$   |         |              | 1.0                         | V             |
| $V_{OH}$   | Logic High Output Voltage   | $I_{OH} = -4 \text{ mA}$ , $V_{CC} = 4.5 \text{ V}$   | 4.0     |              |                             | V             |
| $V_{OL}$   | Logic Low Output Voltage  | $I_{OL} = 4 \text{ mA}$ , $V_{CC} = 4.5 \text{ V}$  |         |              | 0.4                         | V             |
| $I_{IN}$   | Input Current<br>R, G and B Pins<br>HSYNC, VSYNC Pins<br>HSYNC, VSYNC Pins          | $V_{RGB} = 3.63 \text{ V}$ , $V_{IN} = V_{RGB}$ or GND<br>$V_{AUX} = 3.63 \text{ V}$ , $V_{IN} = V_{AUX}$<br>$V_{AUX} = 3.63 \text{ V}$ , $V_{IN} = \text{GND}$ | -30.0   | -72.5        | $\pm 1$<br>$\pm 1$<br>-95.0 | $\mu\text{A}$ |
| $I_{CC}$   | $V_{CC}$ Supply Current   | $V_{CC} = 5.5 \text{ V}$ , $V_{AUX} = V_{RGB} = 2.97 \text{ V}$ ,<br>All Inputs and Outputs Floating  |         | 35           | 100                         | $\mu\text{A}$ |
| $I_{RGB}$  | $V_{RGB}$ Supply Current  | R, G and B Pins at $V_{CC}$ or GND,<br>All Inputs and Outputs Floating  |         |              | 10                          | $\mu\text{A}$ |
| $C_{IN}$   | Input Capacitance<br>R, G and B pins<br>HSYNC, VSYNC pins<br>DDC_DATA, DDC_CLK pins | Note 2 Applies for All Cases  |         | 5<br>10<br>5 |                             | pF            |
| $R_{PU}$   | Pull-up Resistance<br>DDC_DATA, DDC_CLK pins  |   | 1.62    | 1.80         | 1.98                        | k $\Omega$    |
| $V_{ESD}$  | ESD Withstand Voltage   | $V_{CC} = 5 \text{ V}$ , $V_{RGB} = 3.3 \text{ V}$ , $V_{AUX} = 3.3 \text{ V}$<br>(Note 3)  | $\pm 8$ |              |                             | kV            |
| $t_{PLH}$  | SYNC Buffer L $\geq$ H<br>Propagation Delay   | $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ , $R_L = 500 \Omega$<br>(Note 4)   |         | 7.0          | 15.0                        | ns            |
| $t_{PHL}$  | SYNC Buffer H $\geq$ L<br>Propagation Delay   | $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ , $R_L = 500 \Omega$<br>(Note 4)   |         | 7.0          | 15.0                        | ns            |
| $t_R, t_F$ | SYNC Buffer Output Rise & Fall Times  | $C_L = 50 \text{ pF}$ , $V_{CC} = 5.0 \text{ V}$ , $R_L = 500 \Omega$<br>(Note 4)   |         | 7.0          |                             | ns            |

1. All parameters specified over standard operating conditions unless otherwise noted.
2. Measured at 1 MHz. R/G/B inputs biased at 1.65 V with  $V_{RGB} = 3.3 \text{ V}$ . DDC\_CLK and DDC\_DATA biased at 2.5 V with  $V_{CC} = 5 \text{ V}$ . HSYNC and VSYNC inputs biased at  $V_{AUX}$  or GND with  $V_{AUX} = 3.3 \text{ V}$  and  $V_{CC} = 5 \text{ V}$ .
3. Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method.  $V_{RGB}$  and  $V_{CC}$  must be bypassed to GND via a low impedance ground plane with a 0.2  $\mu\text{F}$ , low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: R, G, B, HSYNC\_OUT, VSYNC\_OUT, DDC\_CLK and DDC\_DATA. The HSYNC and VSYNC inputs are ESD protected to the industry standard 2 kV per the Human Body Model (MIL-STD-883, Method 3015).
4. Applicable to the SYNC buffers only. Input signals swing between 0 V and 3.0 V, with rise and fall times  $\leq 5 \text{ ns}$ . Guaranteed by correlation to buffer output drive currents.

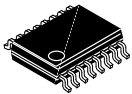
# PACVGA105

## APPLICATION INFORMATION



**Figure 1. Typical Connection Diagram**

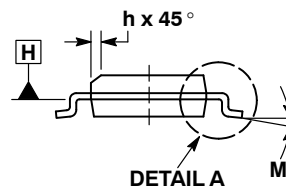
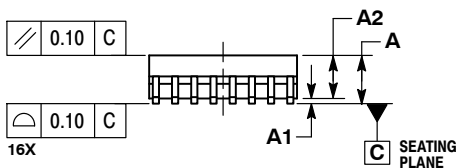
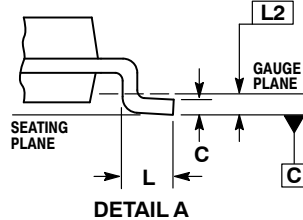
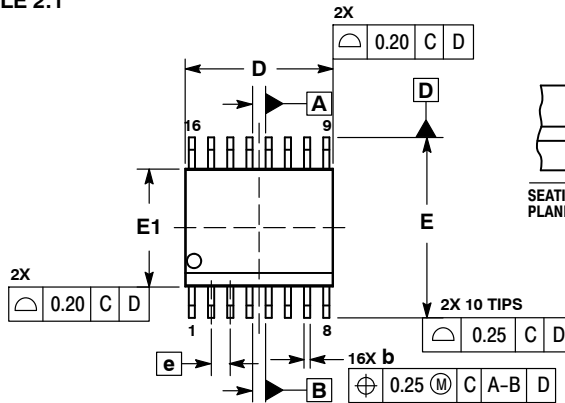
GNDA, the negative voltage rail for the R, G and B diodes is not connected internally to GNDD. GNDA should ideally be connected to the ground of the video DAC IC. This will prevent any ground bounce caused by digital signals from injecting noise onto the R, G and B signals. Analog GND and digital GND are typically connected on the printed circuit board.



SCALE 2:1

**QSOP16**  
CASE 492-01  
ISSUE A

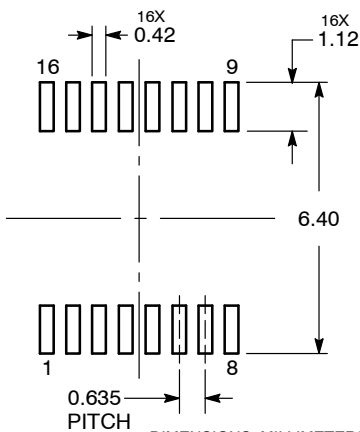
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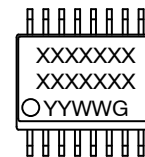
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.053     | 0.069 | 1.35        | 1.75 |
| A1  | 0.004     | 0.010 | 0.10        | 0.25 |
| A2  | 0.049     | ----  | 1.24        | ---- |
| b   | 0.008     | 0.012 | 0.20        | 0.30 |
| c   | 0.007     | 0.010 | 0.19        | 0.25 |
| D   | 0.193 BSC |       | 4.89 BSC    |      |
| E   | 0.237 BSC |       | 6.00 BSC    |      |
| E1  | 0.154 BSC |       | 3.90 BSC    |      |
| e   | 0.025 BSC |       | 0.635 BSC   |      |
| h   | 0.009     | 0.020 | 0.22        | 0.50 |
| L   | 0.016     | 0.050 | 0.40        | 1.27 |
| L2  | 0.010 BSC |       | 0.25 BSC    |      |
| M   | 0°        | 8°    | 0°          | 8°   |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


DIMENSIONS: MILLIMETERS

**GENERIC  
MARKING DIAGRAM\***


XXXXX = Specific Device Code  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                    |  |
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