HIP2210, HIP2211

100V, 3A Source, 4A Sink, High Frequency Half-Bridge Drivers with HI/LI or Tri-Level PWM Input and Adjustable Dead Time

The HIP2210 and HIP2211 are 100V, 3A source, 4A sink high-frequency half-bridge NMOS FET drivers. The HIP2211 features standard HI/LI inputs and is pin-compatible with popular Renesas bridge drivers such as the HIP2101 and ISL2111. The HIP2210 features a tri-level PWM input with programmable dead time. Its wide operating supply range of 6V to 18V and integrated high-side bootstrap diode supports driving the high-side and low-side NMOS in 100V half-bridge applications.

These drivers feature strong 3A source, 4A sink drivers with very fast 15ns typical propagation delay and 2ns typical delay matching, making it optimal for high-frequency switching applications. VDD and boot UVLO protects against an undervoltage operation.

The tri-level input of the HIP2210 PWM pin controls the high-side and low-side drivers with a single pin. When the PWM input is at logic high, the high-side bridge FET is turned on and the low-side FET is off. When the input is at logic low, the low-side bridge FET is turned on and the high-side FET is turned off. When the input voltage is in the mid-level state, both the high-side and low-side bridge FETs are turned off. The PWM threshold levels are proportional to an external input reference voltage on the VREF pin, allowing PWM operation across a 2.7V to 5.5V logic range.

The HIP2210 is offered in a 10 Ld 4x4mm TDFN package. The HIP2211 is offered in 8 Ld SOIC, 8 Ld 4x4mm DFN, and 10 Ld 4x4mm TDFN packages.

Related Literature

For a full list of related documents, visit our website:

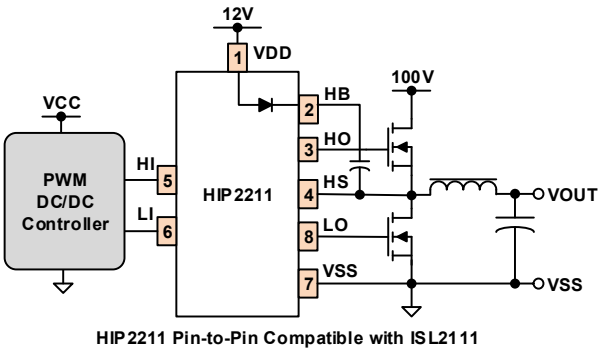
- HIP2210, HIP2211 device pages

Features

- HIP2211 drop-in replacement for the ISL2111 and HIP2101 8 Ld SOIC, 8 Ld DFN, and 10 Ld TDFN packages
- 115V_{DC} bootstrap supply maximum voltage supports 100V on the half-bridge
- 3A source and 4A sink gate drivers for NMOS FETs
- Fast propagation delay and matching: 15ns typical delay; 2ns typical matching (HIP2211)
- Integrated 0.5Ω typical bootstrap diode
- Wide 6V to 18V operating voltage range
- VDD and boot Undervoltage Lockout (UVLO)
- Robust noise tolerance: wide hysteresis at inputs; HS pin tolerates up to -10V continuous
- HIP2211: HI/LI inputs 3.3V logic compatible with VDD voltage tolerance
- HIP2210: Tri-Level PWM input with logic threshold levels set by external VREF pin from 2.7V to 5.5V
- HIP2210: Programmable dead time prevents shoot-through; adjustable from 35ns to 350ns with a single resistor

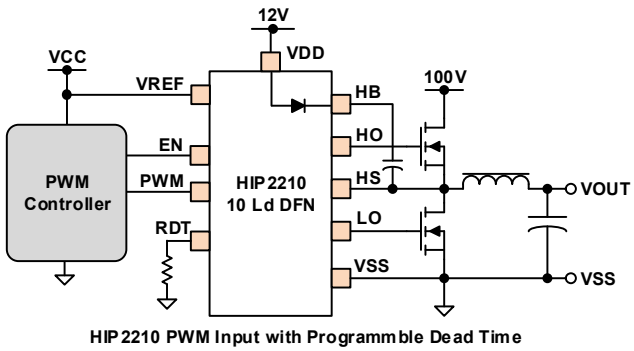
Applications

- Telecom half-bridge and full-bridge DC/DC converters
- 3-phase BLDC motor driver; H-Bridge motor driver
- Two-switch forward and active clamp converters
- Multiphase PWM DC/DC controllers
- Class-D amplifiers



HIP2211 Pin-to-Pin Compatible with ISL2111

Figure 1. HIP2211 HI/LI Input Bridge Driver Typical Application



HIP2210 PWM Input with Programmble Dead Time

Figure 2. HIP2210 PWM Input Bridge Driver Typical Application

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1. Overview

1.1 Block Diagrams

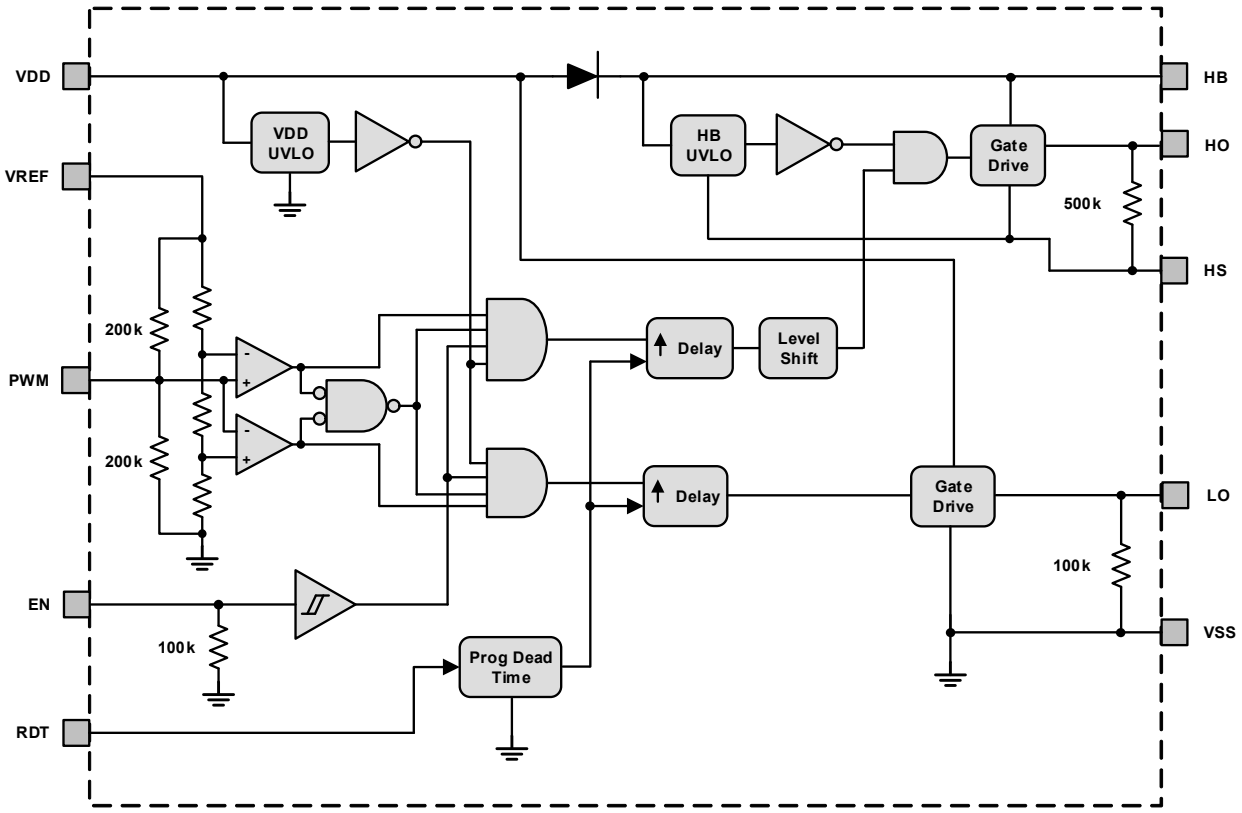


Figure 3. HIP2210 Block Diagram

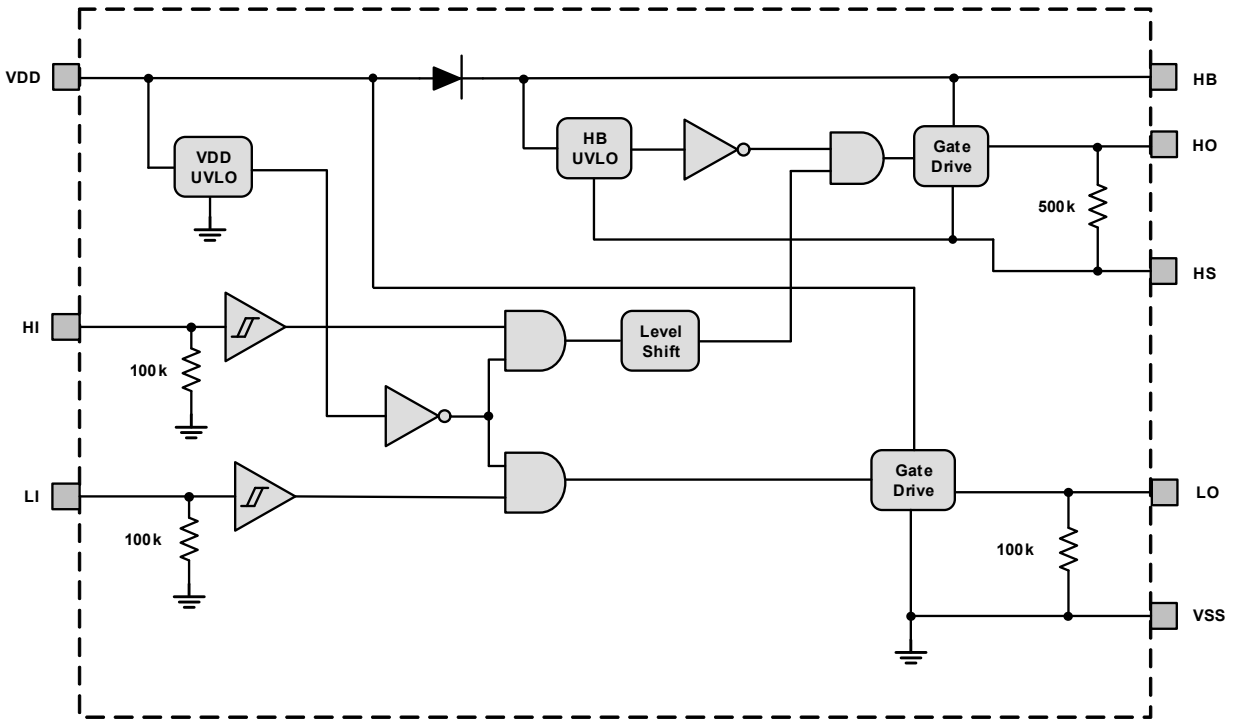


Figure 4. HIP2211 Block Diagram

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1.2 Ordering Information

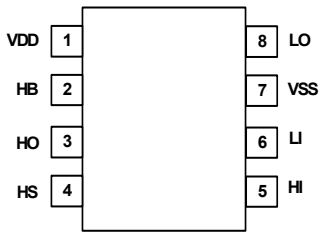
Part Number (Note 4)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
HIP2210FRTZ (Note 2)	HIP221 0FRTZ	-40°C to +125°C	-	10 Ld 4x4 DFN	L10.4x4
HIP2210FRTZ-T (Note 2)			6k		
HIP2210FRTZ-T7A (Note 2)			250		
HIP2211FRTZ (Note 2)	HIP221 1FRTZ		-	10 Ld 4x4 DFN	L10.4x4
HIP2211FRTZ-T (Note 2)			6k		
HIP2211FRTZ-T7A (Note 2)			250		
HIP2211FBZ (Note 3)	2211 FBZ		-	8 Ld SOIC	M8.15
HIP2211FBZ-T (Note 3)			2.5k		
HIP2211FBZ-T7A (Note 3)			250		
HIP2211FR8Z (Note 2)	HIP221 1FR8Z		-	8 Ld 4x4 DFN	L8.4x4
HIP2211FR8Z-T (Note 2)			6k		
HIP2211FR8Z-T7A (Note 2)			250		
HIP2210EVAL1Z	HIP2210 Evaluation Board				
HIP2211EVAL2Z	HIP2211 (SOIC Package) Evaluation Board				
HIP2211EVAL3Z	HIP2211 (10Ld TDFN Package) Evaluation Board				

Notes:

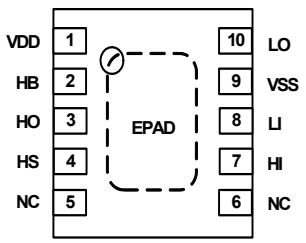
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the HIP2210 and HIP2211 device pages. For more information about MSL, see TB363.

1.3 Pin Configurations

HIP2211FBZ
(8 Ld SOIC)
Top View

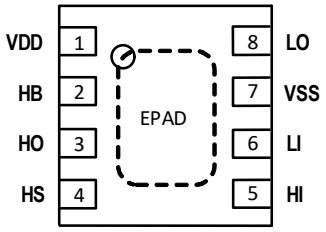


HIP2211FRTZ
(10 Ld 4x4 TDFN)
Top View

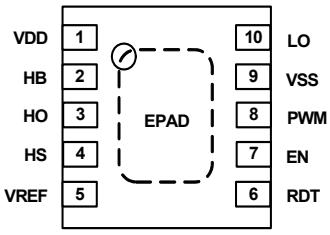


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HIP2211FR8Z
(8 Ld 4x4 DFN)
Top View



HIP2210FRTZ
(10 Ld 4x4 TDFN)
Top View



1.4 Pin Descriptions

Pin Name	Pin Number				Description
	HIP2210	HIP2211			
	10 Ld DFN	10 Ld DFN	8 Ld SOIC	8 Ld DFN	
VDD	1	1	1	1	Analog input supply voltage and positive supply for the lower gate driver. Decouple this pin to ground with a 4.7µF or larger high-frequency ceramic capacitor to VSS. An additional 0.1µF ceramic decoupling capacitor placed close to VDD and VSS pin is recommended.
HB	2	2	2	2	High-side bootstrap supply voltage for the upper gate driver referenced to HS. Connect the bootstrap capacitor to this pin and HS.
HO	3	3	3	3	High-side output driver. Connect to the gate of the high-side NMOS FET.
HS	4	4	4	4	High-side gate driver reference node. Connect to the source of the high-side NMOS FET. Connect the bootstrap capacitor to this pin and HB.
HI	-	7	5	5	High-side driver logic input. 3.3V logic compatible and VDD tolerant.
LI	-	8	6	6	Low-side driver logic input. 3.3V logic compatible and VDD tolerant.
VREF	5	-	-	-	Reference voltage that sets the PWM logic level thresholds. Analog supply range of 2.7V to 5.5V. Decouple VREF to VSS with a 0.1µF ceramic capacitor. If VREF is below 2.7V, the PWM inputs are ignored and HO = LO = 0. An internal 100kΩ pull-down resistor places VREF in the low state when the pin is left floating.
RDT	6	-	-	-	Programmable dead time control pin. Place a resistor from the RDT pin to VSS to set the dead time from 35ns to 350ns. The resistor range is 10kΩ to 100kΩ. Short the RDT pin to VSS to set the dead time to 15ns. See "PCB Layout Guidelines" on page 22 and "RDT and Dead Time Delay (HIP2210 Only)" on page 20 for more information.
EN	7	-	-	-	Output enable pin. When EN is low, HO = LO = 0. An internal 100kΩ pull-down resistor places EN in the low state when the pin is left floating. Output is enabled when EN is high (VDD tolerant).
PWM	8	-	-	-	Tri-level PWM input. Logic high drives HO high and LO low. Logic low drives HO low and LO high. In the mid-level state, both outputs are driven low. An internal resistor network biases the PWM pin to 50% of VREF when the pin is left floating to set the mid-level state.
VSS	9	9	7	7	Ground reference for the VDD supply. When EPAD is available, connect VSS to EPAD.
LO	10	10	8	8	Low-side output driver. Connect to the gate of the low-side NMOS FET.
NC	-	5, 6	-	-	No Connect. No electrical connection from this pin to the IC.
-	EPAD	EPAD	-	EPAD	The EPAD is electrically isolated. Connect the EPAD to the PCB ground plane with thermal vias for heat removal. See "PCB Layout Guidelines" on page 22 for more information.

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2. Specifications

2.1 Absolute Maximum Ratings

Parameter (Note 5)	Minimum	Maximum	Unit
Supply Voltage, VDD	-0.3	+20	V
Boot Voltage, HB Referenced to HS	-0.3	+20	V
Bootstrap Voltage, HB Referenced to VSS	-0.3	+120	V
Bootstrap Voltage, HB Referenced to VDD	-0.3	+110	V
Continuous Voltage on HS	The greater of [-10 or -(20 - V_{DD})]	+120	V
EN, HI, and LI Voltage	-0.3	V_{DD} + 0.3	V
PWM, VREF, RDT Voltage	-0.3	+6	V
Voltage on LO	-0.3	V_{DD} + 0.3	V
Transient Voltage on LO (Repetitive Transient for 100ns)	-2	-	V
Voltage on HO	V_{HS} - 0.3	V_{HB} + 0.3	V
Transient Voltage on HO (Repetitive Transient for 100ns)	V_{HS} - 2	-	V
ESD Ratings	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2.5		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

5. All voltages referenced to VSS unless otherwise specified.

2.2 Thermal Information

Package Type	Thermal Resistance (Typical)		Max Power Dissipation at +25°C in Free Air (W) (Note 10)
	θ_{JA} (°C/W)	θ_{JC} (°C/W)	
8 Ld SOIC (Notes 8, 9)	102	50	1.22
10 Ld TDFN, 8 Ld DFN (Notes 6, 7)	40	2.5	3.12

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
7. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.
8. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
9. For θ_{JC}, the case temperature location is taken at the package top center.
10. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See Note 6 for test condition to establish junction to ambient thermal resistance.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-65	+150	°C
Maximum Storage Temperature Range	-55	+140	°C
Pb-Free Reflow Profile	see TB493		

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2.3 Recommended Operating Conditions

Parameter (Note 5)	Minimum	Maximum	Units
Supply Voltage, VDD	+6	+18	V
HI, LI, EN Inputs	0	V_{DD}	V
PWM, VREF Inputs	0	+5.5	V
Resistor on RDT pin to VSS for Programmable Dead Time	+10	+100	kΩ
Boot Voltage, HB Referenced to HS	V_{DD} - 1	+18	V
Bootstrap Voltage, HB	-	+115	V
Continuous Voltage on HS	The greater of [-10 or -(20 - V_{DD})]	+100	V
HS Slew Rate		<50	V/ns
Temperature	-40°C	+125	°C

2.4 Electrical Specifications

VDD = HB = EN = 12V; VSS = HS = 0V; HI = LI = 0; VREF = 5V; PWM = 2.5V. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
Supply Currents (HIP2211)						
V_{DD} Quiescent Current	I_{DDQ}	HI = LI = 0	-	390	**628**	µA
V_{DD} Operating Current	I_{DDO}	f_{SW} = 500kHz; HI = LI = 50% square wave to VDD	-	1.5	**1.69**	mA
HB to HS Quiescent Current	I_{HBQ}	HI = 1; LI = 0	-	370	**475**	µA
HB to HS Operating Current	I_{HBO}	f_{SW} = 500kHz; HI = LI = 50% square wave to VDD	-	1.4	**1.6**	mA
HB to V_{SS} Current, Operating	I_{HBSO}	f_{SW} = 500kHz; HI = LI =50% square wave to VDD; V_{HB} = 115V; V_{HS} = 100V	-	88	**110**	µA
HB to V_{SS} Leakage Current	I_{HBS}	HI = LI = 0; V_{HB} = V_{HS} = 100V	-	29	**47**	µA
Supply Currents (HIP2210)						
V_{DD} Quiescent Current	I_{DDQ}	PWM = 0.5 x VREF; EN = 1; RDT = 1kΩ; 100kΩ	-	455	**700**	µA
V_{DD} Quiescent Current	I_{DDQ}	PWM = 0.5 x VREF; EN = 1; RDT = 10kΩ	-	800	**1000**	µA
V_{DD} Operating Current	I_{DDO}	f_{SW} = 500kHz; PWM = 50% square wave to VREF; RDT = 10kΩ	-	2	**2.32**	mA
V_{DD} Disabled Current	I_{DDSD}	EN = 0; RDT = 1kΩ; 100kΩ	-	440	**580**	µA
V_{DD} Disabled Current	I_{DDSD}	EN = 0; RDT = 10kΩ	-	780	**900**	µA
HB to HS Quiescent Current	I_{HBQ}	PWM = VREF; EN = 1	-	370	**475**	µA
HB to HS Operating Current	I_{HBO}	f_{SW} = 500kHz; PWM = 50% square wave to V_{REF}; RDT = 100kΩ	-	1.7	**2**	mA
HB to V_{SS} Current, Operating	I_{HBSO}	f_{SW} = 500kHz; PWM = 50% square wave to VREF; V_{HB} = 115V; V_{HS} = 100V; RDT = 100kΩ	-	95	**126**	µA
HB to V_{SS} Leakage Current	I_{HBS}	PWM = 0.5 x VREF; V_{HB} = V_{HS} = 100V	-	28	**52**	µA

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VDD = HB = EN = 12V; VSS = HS = 0V; HI = LI = 0; VREF = 5V; PWM = 2.5V. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
HI and LI Inputs (HIP2211)						
Low Level Threshold	V_{IL}		**1.29**	1.4	**1.47**	V
High Level Threshold	V_{IH}		**1.84**	2.1	**2.35**	V
Input Threshold Hysteresis	V_{HYS}		-	0.7	-	V
Input Pull-Down Resistance	R_{IN}	HI = LI = VDD; Resistance to VSS	-	95	-	kΩ
Minimum Input Pulse Width for Response at Output	T_{MIN}	No load on HO and LO; Output drives to rail	-	10	-	ns
Tri-Level PWM Input (HIP2210)						
Middle to High Level Threshold	V_{PWMHR}	VREF = 2.7V and 5.5V	**63.6**	66	**69.7**	% VREF
High to Middle Level Threshold	V_{PWMHF}	VREF = 2.7V and 5.5V	**53.7**	56	**59.6**	% VREF
High/Middle Level Hysteresis		VREF = 2.7V and 5.5V	-	10	-	% VREF
Low to Middle Level Threshold	V_{PWMLR}	VREF = 2.7V and 5.5V	**30.3**	33	**36.3**	% VREF
Middle to Low Level Threshold	V_{PWMLF}	VREF = 2.7V and 5.5V	**19.5**	23	**26.3**	% VREF
Low/Middle Level Hysteresis		VREF = 2.7V and 5.5V	-	10	-	% VREF
PWM Open Circuit Voltage	V_{FLOAT}	PWM pin floating; VREF = 2.7V and 5.5V	**48**	50	**52**	% VREF
Logic High Input Current	I_{PWMH}	PWM = 3V; VREF = 3V; Sourcing	-	16	-	µA
Logic Low Input Current	I_{PWML}	PWM = 0V; VREF = 3V; Sinking	-	16	-	µA
PWM Pull-Up Resistance	R_{UP}	To V_{REF}	-	180	-	kΩ
PWM Pull-Down Resistance	R_{DOWN}	To VSS	-	180	-	kΩ
Minimum Input Pulse Width for Response at Output	T_{MIN}	No load on HO and LO; Output drives to rail	-	20	-	ns
VREF Input (HIP2210)						
VREF Enabled Rising Threshold	V_{VREF_R}	PWM = 0; EN = 1; RDT = 1kΩ	-	2.55	**2.7**	V
VREF Disabled Hysteresis	V_{VREF_H}	PWM = 0; EN = 1; RDT = 1kΩ	-	0.18	-	V
VREF Enable Delay	t_{VREF_R}	PWM = 0; EN = 1; RDT = 1kΩ	-	175	-	ns
VREF Disabled Delay	t_{VREF_F}	PWM = 0; EN = 1; RDT = 1kΩ	-	110	-	ns
VREF Pull-Down Resistance to VSS	R_{VREF}	VREF = 3V; PWM = Float	-	90	-	kΩ
EN Input (HIP2210)						
Low-Level Threshold	V_{ENL}		**1.26**	1.38	**1.47**	V
High-Level Threshold	V_{ENH}		**1.84**	2.1	**2.31**	V
Input Threshold Hysteresis	V_{HYS}		-	0.72	-	V
Input Pull-Down Resistance	R_{EN}	V_{EN} = VDD; To VSS	-	90	-	kΩ
EN High Propagation Delay	t_{ENH}	RDT = 1kΩ; PWM = 0	**450**	800	**1100**	ns
EN Low Propagation Delay	t_{ENL}	RDT = 1kΩ; PWM = 0	-	115	**150**	ns
Undervoltage Protection						
V_{DD} Rising UVLO Threshold	VDDR		**5.3**	5.6	**5.9**	V
V_{DD} Falling UVLO Threshold	VDDF		**4.75**	5.1	**5.35**	V
V_{DD} Threshold Hysteresis	VDDH		-	0.5	-	V

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VDD = HB = EN = 12V; VSS = HS = 0V; HI = LI = 0; VREF = 5V; PWM = 2.5V. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
V_{DD} Rising UVLO Delay		Characterization only. No limits.	-	1	-	µs
V_{DD} Falling UVLO Delay		Characterization only. No limits.	-	2	-	µs
V_{HB} Rising Threshold	VHBR		**4.8**	5.1	**5.4**	V
V_{HB} Falling Threshold	VHBF		**4.25**	4.6	**4.85**	V
V_{HB} Threshold Hysteresis	VHBH		-	0.5	-	V
V_{HB} Rising UVLO Delay		Characterization only. No limits.	-	10	-	µs
V_{HB} Falling UVLO Delay		Characterization only. No limits.	-	12	-	µs
Bootstrap Diode						
Low Current Forward Voltage	V_{FL}	$I_{VDD - HB}$ = 100µA	-	0.65	**0.85**	V
High Current Forward Voltage	V_{FH}	$I_{VDD - HB}$ = 100mA	-	0.85	**1**	V
Dynamic Resistance	R_D	$R_D = \Delta V_D/\Delta I_{VDD-HB}$ I_{VDD-HB} = 80mA and 100mA	-	0.5	**0.9**	Ω
Reverse Bias Leakage	I_R	$V_{HB} = V_{HS}$ = 100V; VDD = 0V	-	0.11	-	µA
Reverse Recovery Time	t_{RR}	100mA forward to 100V reverse	-	50	-	ns
LO Gate Driver						
Low-Level Output Voltage	V_{OL_LO}	I_{LO} = 100mA sink	-	0.1	**0.17**	V
High-Level Output Voltage	V_{OH_LO}	I_{LO} = 100mA source $V_{OH_LO} = VDD - V_{LO}$	-	0.16	**0.27**	V
Peak Pull-Up Source Current	I_{OH_LO}	V_{LO} = 0V; Limits are internal specifications only	-	3	-	A
Peak Pull-Down Sink Current	I_{OL_LO}	V_{LO} = 12V; Limits are internal specifications only	-	4	-	A
LO Pin Pull-Down Resistance	R_{LO}	VDD = 0V; LO = 100mV; To VSS	-	140	-	kΩ
HO Gate Driver						
Low-Level Output Voltage	V_{OL_HO}	I_{HO} = 100mA sink	-	0.1	**0.17**	V
High-Level Output Voltage	V_{OH_HO}	I_{HO} = 100mA source $V_{OH_HO} = V_{HB} - V_{HO}$	-	0.16	**0.27**	V
Peak Pull-Up Current	I_{OH_HO}	V_{HO} = 0V; Limits are internal specifications only.	-	3	-	A
Peak Pull-Down Current	I_{OL_HO}	$V_{HO} = V_{HB}$; Limits are internal specifications only.	-	4	-	A
HO Pin Pull-Down Resistance	R_{HO}	HB - HS = 0V; HO = 100mV; To HS	-	450	-	kΩ

2.5 Switching Specifications

VDD = HB = 12V; VSS = HS = 0V; HI = LI = 0V to 5V; PWM = 0V to V_{REF}; RDT = 1kΩ, 10kΩ, or 100kΩ. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, - 40°C to +125°C.**

Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
Propagation Delays (HIP2211)						
LO Turn-Off Propagation Delay	t_{PDLI_F}	LI = 1 to 0; VDD = 12V	-	15	**30**	ns
		LI = 1 to 0; VDD = 6V	-	15	**30**	ns
LO Turn-On Propagation Delay	t_{PDLI_R}	LI = 0 to 1; VDD = 12V	-	15	**30**	ns
		LI = 0 to 1; VDD = 6V	-	15	**30**	ns

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VDD = HB = 12V; VSS = HS = 0V; HI = LI = 0V to 5V; PWM = 0V to V_{REF}; RDT = 1kΩ, 10kΩ, or 100kΩ. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, - 40°C to +125°C. (Continued)**

Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
HO Turn-Off Propagation Delay	t_{PDHI_F}	HI = 1 to 0; HB - HS = 12V	-	15	**30**	ns
		HI = 1 to 0; HB - HS = 6V	-	15	**30**	ns
HO Turn-On Propagation Delay	t_{PDHI_R}	HI = 0 to 1; HB - HS = 12V	-	15	**30**	ns
		HI = 0 to 1; HB - HS = 6V	-	15	**30**	ns
Propagation Delay Matching	t_{MATCH_LH}	LI = 1 to 0; HI = 0 to 1 LO falling to HO rising	**-6**	1.5	**6**	ns
	t_{MATCH_HL}	HI = 1 to 0; LI = 0 to 1 HO falling to LO rising	**-6**	1.5	**6**	ns
Propagation Delays (HIP2210)						
HO Turn-Off Propagation Delay	t_{PDHO}	PWM falling to HO falling; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 12V	-	30	**40**	ns
		PWM falling to HO falling; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 6V	-	30	**40**	ns
LO Turn-Off Propagation Delay	t_{PDLO}	PWM rising to LO falling; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 12V	-	30	**43**	ns
		PWM rising to LO falling; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 6V	-	30	**43**	ns
Turn-Off Propagation Delay Matching	$t_{PDMATCH}$	t_{PDHO} - t_{PDLO}; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 12V	-10	2	**10**	ns
		t_{PDHO} - t_{PDLO}; VREF = 5V; RDT = 1kΩ; VDD = HB - HS = 6V	-10	2	**10**	ns
PWM High to Mid State to HO Off Propagation Delay	$t_{PD_PWM_HM}$	VREF = 5V; RDT = 1kΩ; PWM 5V to 2.5V	-	70	**90**	ns
PWM Mid to High State to HO On Propagation Delay	$t_{PD_PWM_MH}$	VREF = 5V; RDT = 1kΩ; PWM 2.5V to 5V	-	60	**82**	ns
PWM Low to Mid state to LO Off Propagation Delay	$t_{PD_PWM_LM}$	VREF = 5V; RDT = 1kΩ; PWM 0V to 2.5V	-	70	**87**	ns
PWM Mid to Low State to LO On Propagation Delay	$t_{PD_PWM_ML}$	VREF = 5V; RDT = 1kΩ; PWM 2.5V to 0V	-	60	**79**	ns
RDT Programmable Dead Time Delays (HIP2210)						
Minimum Dead Time Delay (Note 12) HO Falling to LO Rising	t_{DTHL_MIN}	RDT = 1kΩ, PWM high to low	**5**	11	**18**	ns
Minimum Dead Time Delay (Note 12) LO Falling to HO Rising	t_{DTLH_MIN}	RDT = 1kΩ, PWM low to high	**5**	11	**18**	ns
Low Range Delay (Note 12) HO Falling to LO Rising	t_{DTHL_LOW}	RDT = 10kΩ, PWM high to low	**30**	36	**45**	ns
Low Range Delay (Note 12) LO Falling to HO Rising	t_{DTLH_LOW}	RDT = 10kΩ, PWM low to high	**30**	36	**45**	ns
High Range Delay (Note 12) HO Falling to LO Rising	t_{DTHL_HIGH}	RDT = 100kΩ, PWM high to low	**300**	360	**425**	ns
High Range Delay (Note 12) LO Falling to HO Rising	t_{DTLH_HIGH}	RDT = 100kΩ, PWM low to high	**300**	360	**425**	ns
Maximum Dead Time Delay (Note 12) HO Falling to LO Rising	t_{DTHL_MAX}	RDT = 200kΩ, PWM high to low	-	715	-	ns

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VDD = HB = 12V; VSS = HS = 0V; HI = LI = 0V to 5V; PWM = 0V to V_{REF}; RDT = 1kΩ, 10kΩ, or 100kΩ. No load on LO or HO, unless otherwise specified. **Boldface limits apply across the operating temperature range, - 40°C to +125°C. (Continued)**

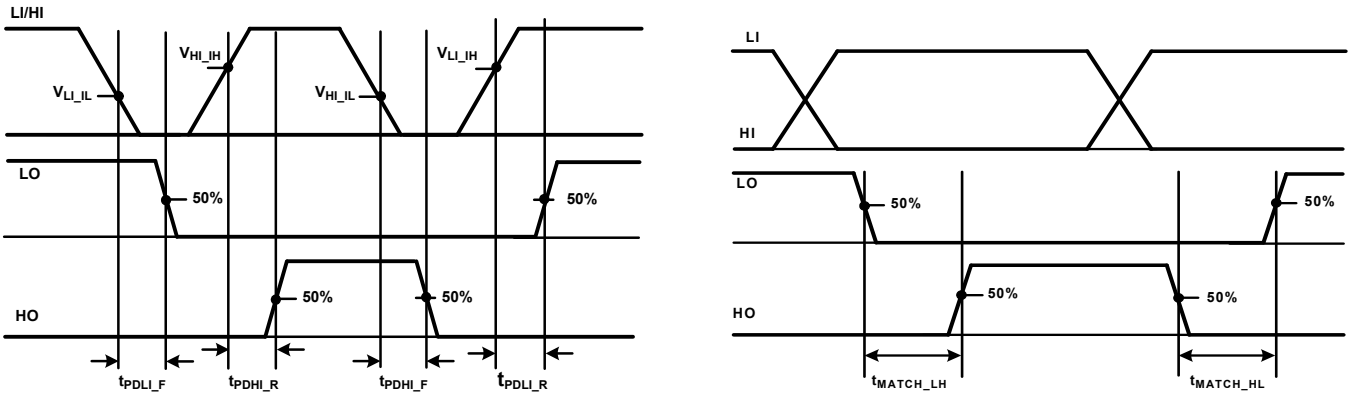
Parameters	Symbol	Test Conditions	Min (Note 11)	Typ	Max (Note 11)	Units
Maximum Dead Time Delay (Note 12) LO Falling to HO Rising	t_{DTLH_MAX}	RDT = 200kΩ, PWM low to high	-	745	-	ns
Dead Time Delay Matching (Note 12)	t_{MATCH_MIN}	RDT = 1kΩ	-	2.5	-	ns
	t_{MATCH_LOW}	RDT = 10kΩ	-	2.5	-	ns
	t_{MATCH_HIGH}	RDT = 100kΩ	**-30**	-	**30**	ns
	t_{MATCH_HIGH}	RDT = 200kΩ	-	30	-	ns
Rise and Fall Times						
LO/HO Output Rise Time	t_{RISE1}	C_{LOAD} = 1nF; VDD = HB - HS = 12V 10% to 90%	-	20	-	ns
		C_{LOAD} = 1nF; VDD = HB - HS = 6V 10% to 90%	-	20	-	ns
	t_{RISE2}	C_{LOAD} = 100nF; VDD = HB - HS = 12V 10% to 90%	-	435	**1010**	ns
		C_{LOAD} = 100nF; VDD = HB - HS = 6V 10% to 90%	-	355	**1010**	ns
LO/HO Output Fall Time	t_{FALL1}	C_{LOAD} = 1nF; VDD = HB - HS = 12V 90% to 10%	-	20	-	ns
		C_{LOAD} = 1nF; VDD = HB - HS = 6V 90% to 10%	-	20	-	ns
	t_{FALL2}	C_{LOAD} = 100nF; VDD = HB - HS = 12V 90% to 10%	-	365	**790**	ns
		C_{LOAD} = 100nF; VDD = HB - HS = 6V 90% to 10%	-	290	**790**	ns

Notes:

11. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
12. Dead Time is defined as the time between LO falling to HO rising or between HO falling to LO rising. See Timing Diagrams for measurement specification.

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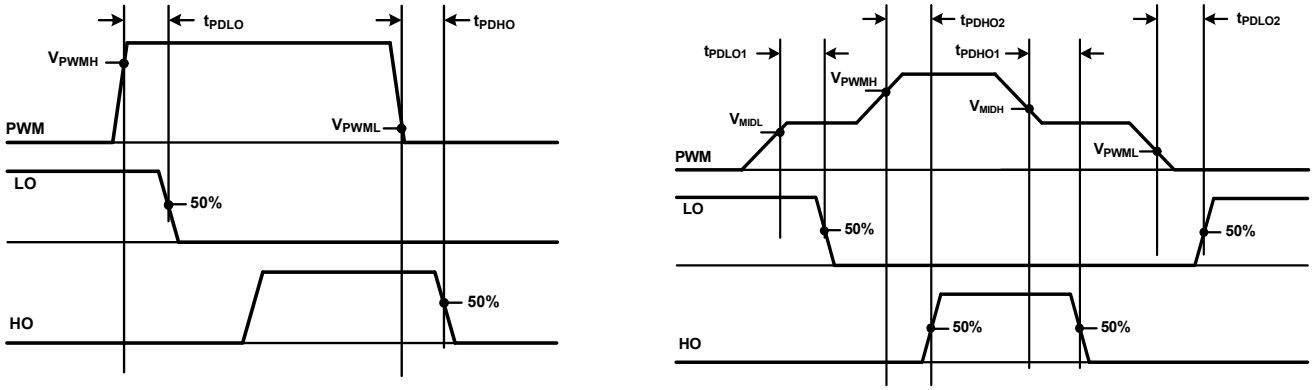
2.6 Timing Diagrams



t_{PDLI_F}: Propagation Delay from LI falling to LO falling to 50% of VDD.
t_{PDLI_R}: Propagation Delay from LI rising to LO rising to 50% of VDD.
t_{PDHI_F}: Propagation Delay from HI falling to HO falling to 50% of HB.
t_{PDHI_R}: Propagation Delay from HI rising to HO rising to 50% of HB.

Delay matching: t_{MATCH_LH} - t_{MATCH_HL}

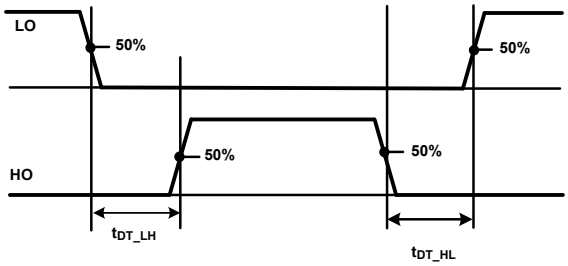
Figure 5. HIP2211 Propagation Delay Timing Diagram



t_{PDLO}: Propagation Delay from PWM rising to LO falling to 50% of LO.
t_{PDHO}: Propagation Delay from PWM falling to HO falling to 50% of HO.
Delay matching: t_{PDLO} - t_{PDHO}

t_{PDLO1}: Propagation Delay from PWM entering mid state to LO falling.
t_{PDHO1}: Propagation Delay from PWM entering mid state to HO falling.
t_{PDLO2}: Propagation Delay from PWM exiting mid state to LO rising.
t_{PDHO2}: Propagation Delay from PWM exiting mid state to HO rising.

Figure 6. HIP2210 Propagation Delay Timing Diagram



t_{DTLH}: Dead time from LO falling to 50% to HO rising to 50%.
t_{DTHL}: Dead time from HO falling to 50% to LO rising to 50%.
Programmable Dead Time Delay Matching: t_{DTLH} - t_{DTHL}

Figure 7. HIP2210 Programmable Dead Time Delay Timing Diagram

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3. Typical Performance Curves

Unless otherwise specified, operating conditions at: T = +25°C; VDD = EN = 12V; VSS = HS = 0V; Capacitor from HB to HS pin C_{BOOT} = 0.22µF; 100kΩ load on LO to VSS and HO to HS.

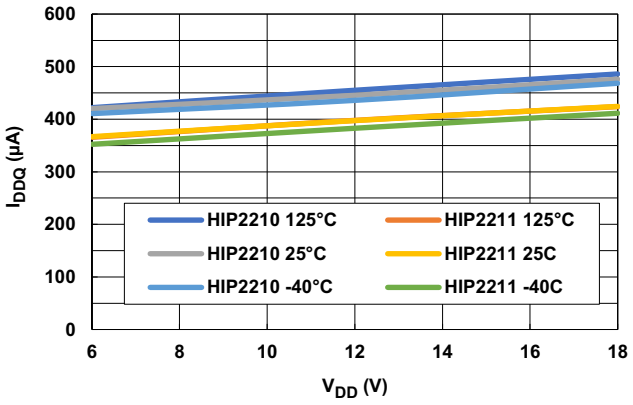


Figure 8. I_{DD} Quiescent Current (RDT = 1k) vs Temperature vs V_{DD}

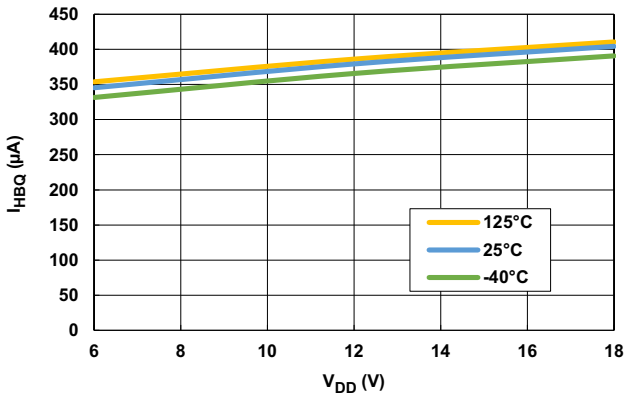


Figure 9. I_{HB} Quiescent Current vs Temperature vs V_{DD}

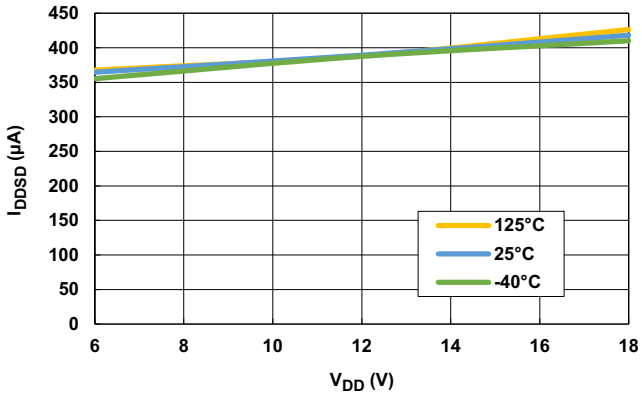


Figure 10. I_{DD} Disabled Current (RDT = 1k) vs Temperature vs V_{DD}

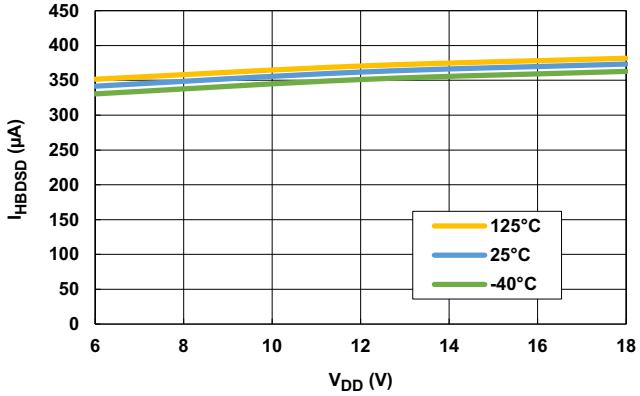


Figure 11. I_{HB} Disabled Current (RDT = 1k) vs Temperature vs V_{DD}

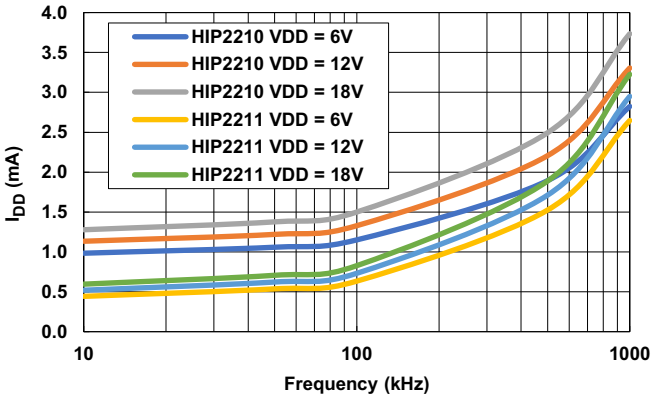


Figure 12. I_{DD} Operating Current (RDT = 10k) vs Frequency vs V_{DD}

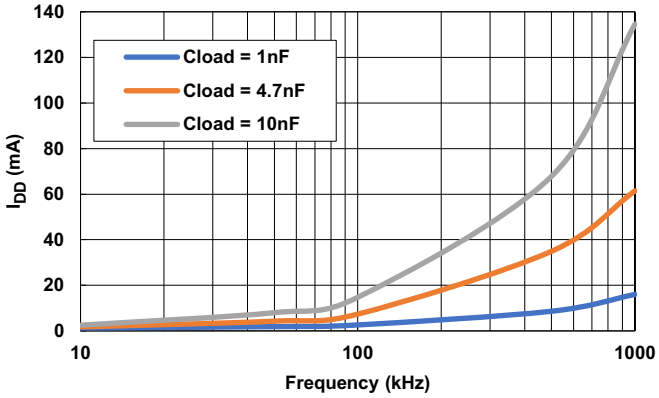


Figure 13. I_{DD} Operating Current (RDT = 10k) vs Frequency vs Capacitance Load

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Unless otherwise specified, operating conditions at: T = +25°C; VDD = EN = 12V; VSS = HS = 0V; Capacitor from HB to HS pin C_{BOOT} = 0.22µF; 100kΩ load on LO to VSS and HO to HS. **(Continued)**

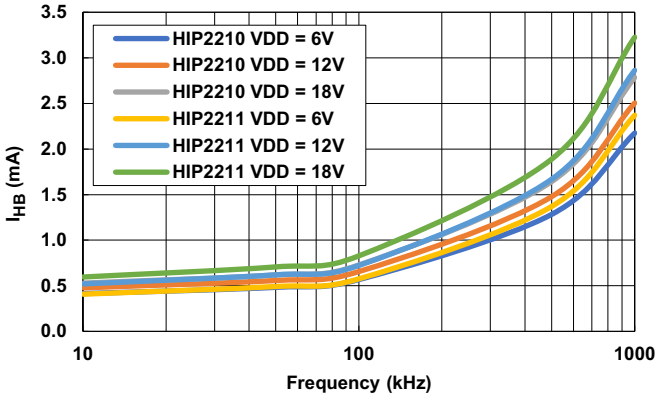


Figure 14. I_{HB} Operating Current (RDT = 10k) vs Frequency vs V_{DD}

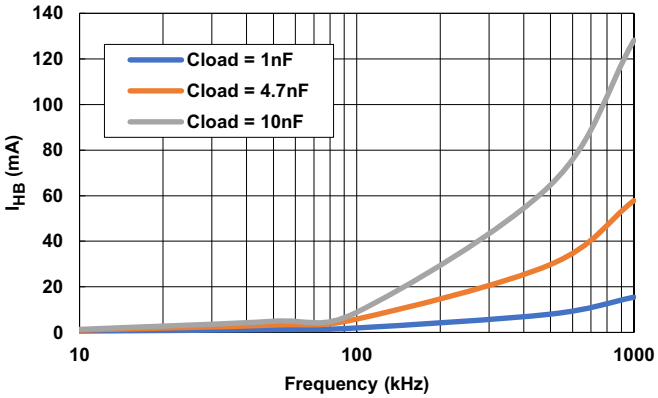


Figure 15. I_{HB} Operating Current (RDT = 10k) vs Frequency vs Capacitance Load

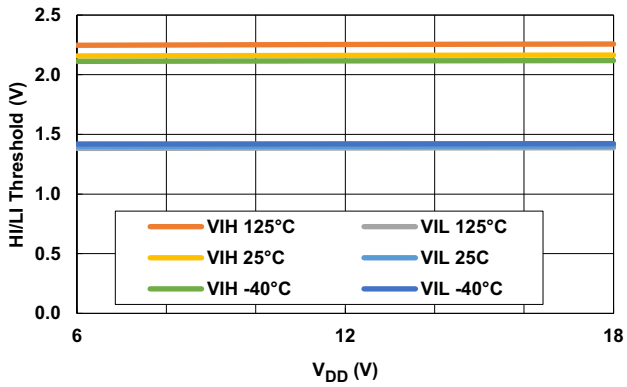


Figure 16. HI/LI Threshold Levels vs Temperature vs V_{DD}

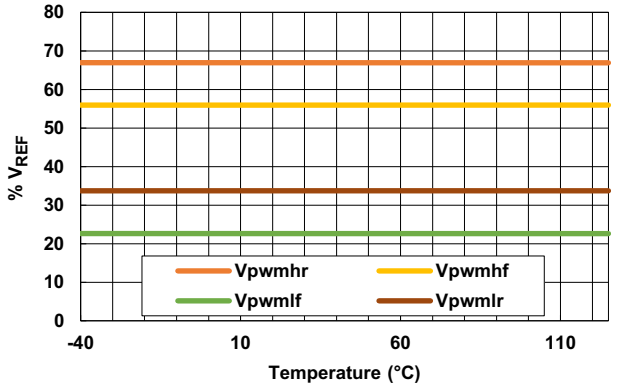


Figure 17. PWM Threshold Levels vs Temperature

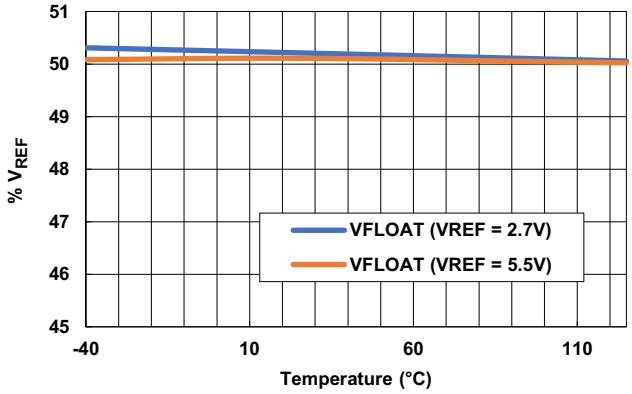


Figure 18. PWM Floating Pin Voltage vs Temperature vs V_{DD}

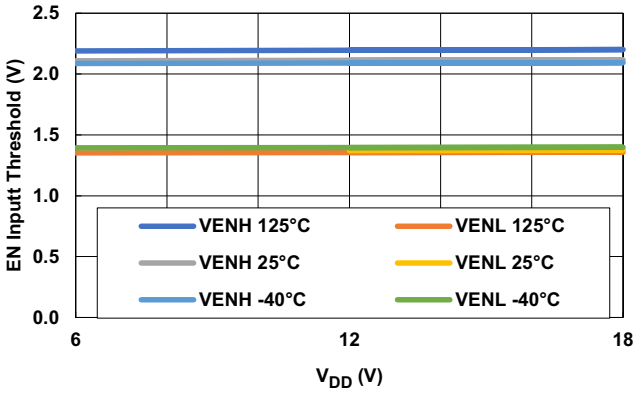


Figure 19. EN Input Threshold vs Temperature vs V_{DD}

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Unless otherwise specified, operating conditions at: T = +25°C; VDD = EN = 12V; VSS = HS = 0V; Capacitor from HB to HS pin C_{BOOT} = 0.22µF; 100kΩ load on LO to VSS and HO to HS. **(Continued)**

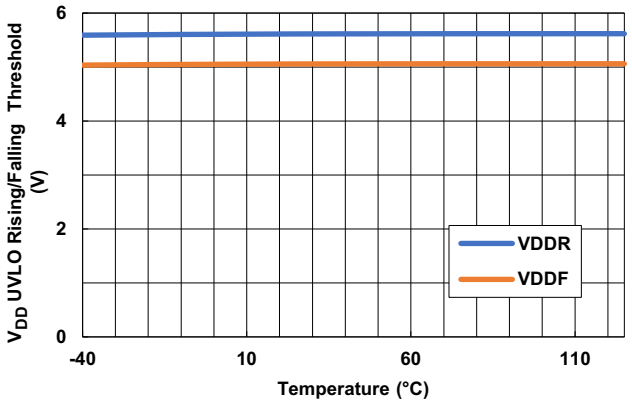


Figure 20. VDD UVLO Rising and Falling Threshold vs Temperature

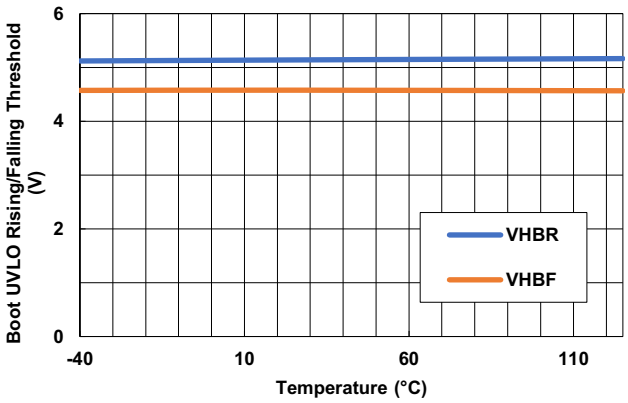


Figure 21. HB UVLO Rising and Falling Threshold vs Temperature

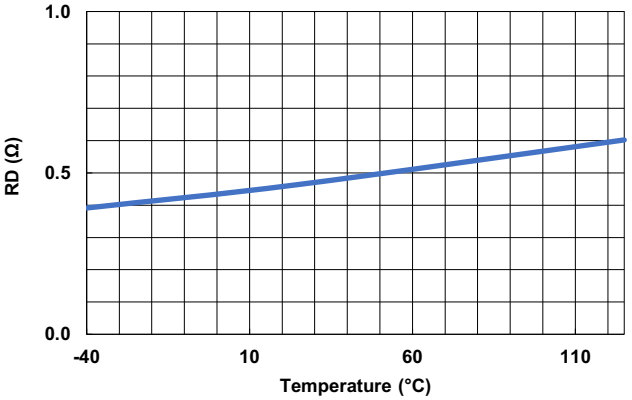


Figure 22. Boot Diode Impedance vs Temperature

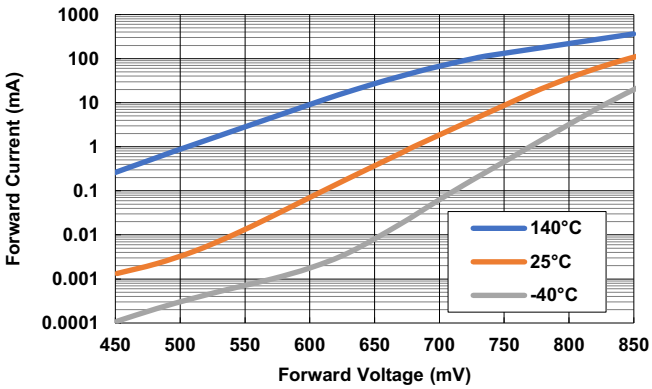


Figure 23. Boot Diode I-V Curve vs Temperature

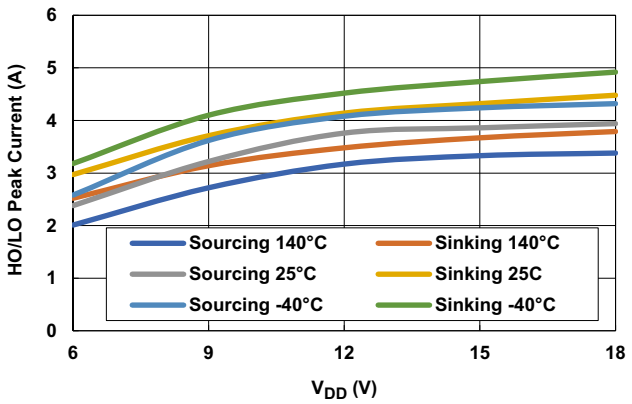


Figure 24. HO/LO Output Current (100nF load) vs Temperature vs Supply Voltage

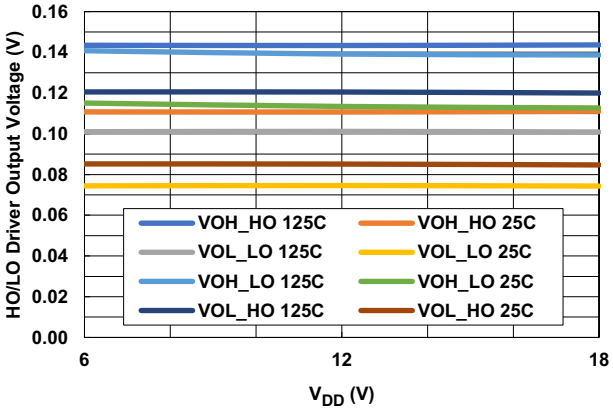


Figure 25. HO/LO Output Voltage vs Temperature vs Supply Voltage (For Loading See EC Table)

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Unless otherwise specified, operating conditions at: T = +25°C; VDD = EN = 12V; VSS = HS = 0V; Capacitor from HB to HS pin C_{BOOT} = 0.22µF; 100kΩ load on LO to VSS and HO to HS. **(Continued)**

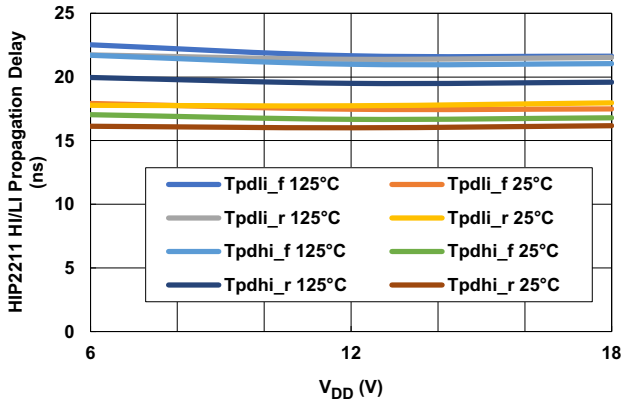


Figure 26. HI/LI Propagation Delay vs Temperature vs V_{DD}

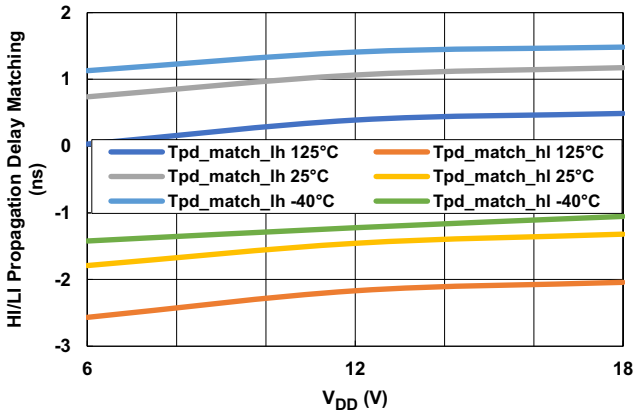


Figure 27. HI/LI Propagation Delay Matching vs Temperature vs V_{DD}

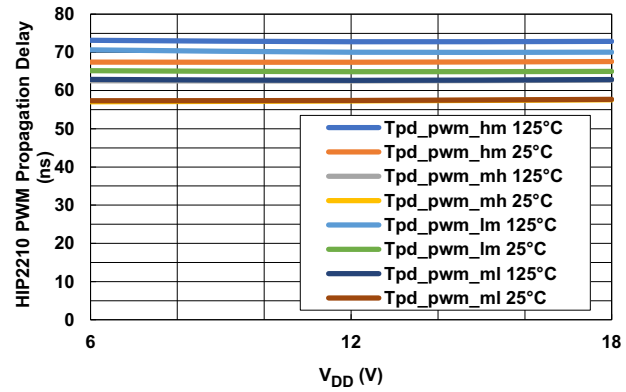


Figure 28. PWM Propagation Delay vs Temperature vs V_{DD}

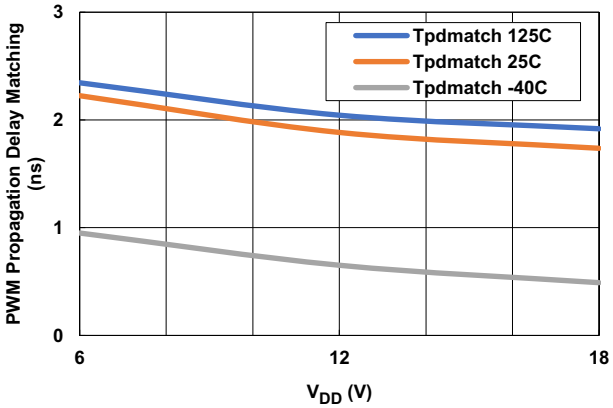


Figure 29. PWM Propagation Delay Matching vs Temperature vs V_{DD}

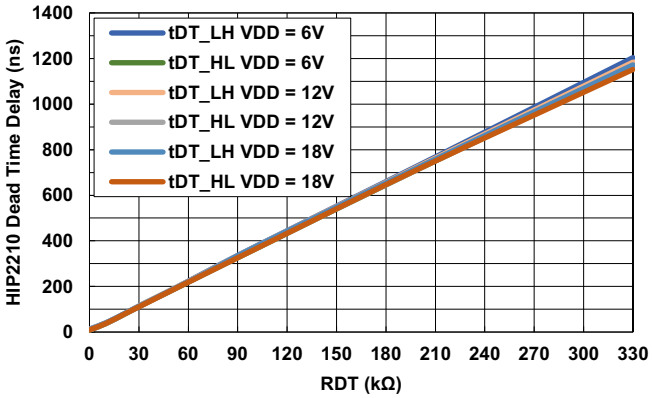


Figure 30. Dead Time Delay (25°C) vs RDT Resistor vs V_{DD}

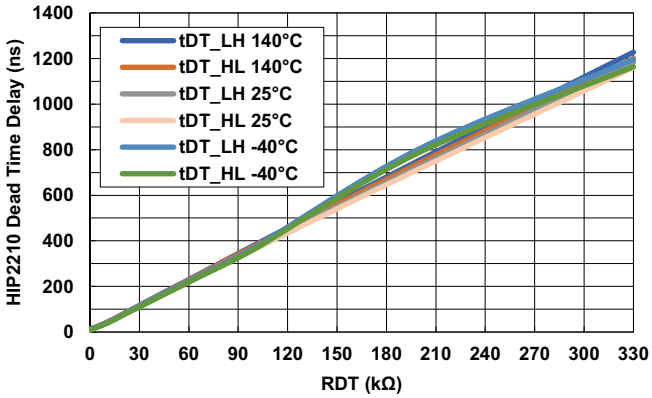


Figure 31. Dead Time Delay (VDD = 12V) vs RDT Resistor vs Temperature

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4. Functional Description

4.1 Gate Drive for NMOS Half-Bridge

The HIP2210 and HIP2211 are NMOS FET drivers for half-bridge, full-bridge, two-switch forward, active clamp, or synchronous buck configurations. In half-bridge configurations, the gate of the low-side FET requires a ground referenced signal above the gate threshold voltage to switch on and off. The high-side FET source terminal is connected to the drain of the low-side FET and is called the Phase or Switch node. When the high-side FET is on, its source terminal is at the high voltage supply. The gate drive of the high-side FET requires a floating bootstrap supply to properly drive the high-side FET gate voltage relative to its source terminal. A bootstrap circuit is implemented on these drivers to properly switch the high-side and low-side NMOS FETs.

4.2 Functional Overview

The HIP2210 and HIP2211 drivers are designed to switch NMOS FETs in up to 100V half-bridge configurations. The drivers feature strong 3A sourcing and 4A sinking output drive capability and fast 15ns propagation delay times to switch low $r_{DS(ON)}$ NFETs for up to 1MHz applications. With an integrated bootstrap diode, the floating high-side bias requires only an external bootstrap capacitor to properly drive the high-side FET.

The drivers have integrated UVLO on both the VDD and Boot supply to prevent low gate voltage drive to the NFETs. The HIP2210 and HIP2211 can operate across a wide VDD voltage range of 6V to 18V.

The HIP2211 has 3.3V CMOS compatible HI and LI inputs to control the high-side and low-side driver outputs, respectively.

The HIP2210 features a single tri-level PWM input to control the high-side and low-side drivers. The tri-level thresholds are set by an external VREF pin, which allows PWM control from 2.7V to 5.5V logic supply voltages. When PWM is high, the high-side driver is sourcing and the low-side driver is sinking. When PWM is low, the low-side driver is sourcing and the high-side driver is sinking. When PWM is at mid-level, both driver outputs are sinking to put the half-bridge in a high impedance state. The HIP2210 also has an EN pin to enable the input logic control, or disable it and place the half-bridge in high impedance state. This EN pin feature is useful to prevent false switching of the NFETs during controller start-up. See “Applications Information” on page 18 for more information about the PWM input control.

The HIP2210 controls dead time with an adjustable dead time delay pin (RDT). A resistor to ground sets a dead time delay of the rising edge of the driver output. See Applications Information for more information about setting the adjustable dead time delay.

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5. Applications Information

5.1 HI/LI Input Control (HIP2211 Only)

The HIP2211 HI and LI logic inputs control the high-side driver and low-side driver, respectively. The inputs are 3.3V logic level compatible and VDD voltage tolerant. Typical 100kΩ pull-down resistors internally bias the HI and LI inputs logic low when they are left floating. The HIP2211 HI and LI inputs do not have any logic input lockout protection. If HI and LI are logic high, both output drivers are turned on sourcing and can cause a shoot-through condition on the half-bridge MOSFETs. It is critical to provide adequate dead time on the controller side when operating the HI and LI inputs in half-bridge applications.

5.2 PWM Input Control (HIP2210 Only)

The HIP2210 PWM input is a tri-level logic pin. The following are the three levels:

- Low-level: Turns on the lower gate drive
- High-level: Turns on the upper gate drive
- Mid-level: Turns both gate drivers off for high impedance of the half-bridge

By design, the PWM input prevents a controller from turning both drivers on, providing shoot-through protection against faulted input logic that can occur from a two input driver inadvertently turning both drivers on. PWM logic thresholds are referenced to the VREF pin and function from 2.7V to 5.5V. Typical 180kΩ internal resistors on the PWM pin bias to the mid-level of 50% VREF when there is no external PWM signal, turning both sink drivers on and setting the half-bridge to high impedance. The PWM input is tolerant up to 5.5V regardless of the VREF voltage.

5.3 VREF Input (HIP2210 Only)

The VREF input sets the PWM input threshold levels. The valid VREF voltage range is 2.7V to 5.5V. If VREF is below its UVLO threshold, driver outputs do not respond to PWM inputs and both output sink drivers turn on, setting the half-bridge to high impedance. An internal pull-down impedance of 100kΩ pulls VREF below the UVLO threshold when the pin is floating.

5.4 EN Pin (HIP2210 Only)

When EN pin is logic high, driver outputs respond to PWM inputs. When logic low, driver outputs do not respond to PWM inputs and both output sink drivers turn on, setting the half-bridge to high impedance. An internal pull-down impedance of 100kΩ pulls EN low when it is floating. The EN input is 3.3V logic level compatible and VDD voltage tolerant.

5.5 Power Sequencing HIP2210

Renesas recommends using the HIP2210 by tying the EN pin to an external MCU logic I/O for proper power sequencing control.

The proper power turn-on sequence is:

1. VDD
2. VREF
3. EN pin high to enable the driver

The proper power turn-off sequence is:

1. EN pin low to disable the driver
2. VREF
3. VDD

In applications where you prefer to tie the EN pin to VDD, you should understand there can be unintended turn-on transitions on LO and HO when VREF is rising or falling with EN logic high, depending on the PWM pin voltage to VREF. With the driver enabled and when VREF is rising or falling, the PWM tri-level logic input thresholds are

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dependent on the transitioning VREF voltage. The PWM open-circuit voltage is referenced to 50% of the VREF voltage. The high impedance voltage divider resistors on the PWM pin coupled with the internal pin capacitance form an RC circuit. During the transient turn-on and turn-off of VREF, the PWM pin open-circuit floating voltage rises to (and falls from) 50% of VREF with an RC time constant delay relative to VREF voltage. Depending on the dv/dt of VREF, the PWM open-circuit floating voltage can lag VREF. When PWM lags behind VREF, the PWM comparators can see logic low on VREF turn-on (and therefore LO turns on) and see logic high on VREF turn-off (and therefore HO turns on) until the PWM voltage falls into the mid-level logic window or VREF hits its UVLO threshold. Although the HO/LO transitions in response to VREF ON and OFF do not violate driver operation or produce bridge shoot through, it is not a desired transient response.

Therefore, the recommended operation of HIP2210 is to externally control the EN pin logic input such that VDD and VREF voltages are stabilized before enabling the driver or the driver is disabled first before turning off VDD and VREF. The VREF pin can also be tied to the bias voltage for the PWM output of the controlling MCU.

For EN = VDD applications, several options can be considered to mitigate the potential issue:

- External pull-up and pull-down resistors (such as 22kΩ) on the PWM pin to reduce the overall resistance and the lag of the PWM voltage behind VREF
- Slower rise/fall time (1-2µs) on VREF to allow the PWM floating pin to track VREF

5.6 Selecting the Boot Capacitor Value

To provide the proper gate drive to the high-side FET, the high-side driver bias on the HIP2210 and HIP2211 is handled with a bootstrap capacitor across the HB and HS pins. The boot capacitor is recharged whenever the HS pin voltage goes low and forward biases the boot diode across VDD to HB. Select the boot capacitor based on the total Q_{gs} of the high-side NMOS FETs, switching frequency, VDD supply, and the total boot impedance, including the dynamic resistance of the boot diode. Connect the boot capacitor close to the HIP2210/HIP2211 HB and HS pins. A low ESL, high-frequency X7R or better ceramic capacitor is recommended.

The boot capacitor value is chosen not only to supply the internal bias current of the high-side driver but also more significantly, to provide the gate charge of the high-side driven NMOS FET without causing the boot voltage to sag excessively. To ensure the proper value of the bootstrap capacitor is selected, the following guideline provides equations for calculating the boot capacitance needed.

- V_{DD} = Driver bias charging supply
- ΔV_{BOOT} = Maximum allowable voltage dip to ensure proper function; generally 500mV
- $V_{HB} = V_{DD} - 0.7V = V_{HO}$ = Boot voltage and high-side driver bias voltage, referenced to HS
- t_{ON} = Longest on-time of the high-side; for simplicity assume the entire switching period $t_{ON} = 1/f_{SW}$
- Q_{GS_MAX} = Maximum gate charge, from NMOS FET datasheet
- I_{GS_LKG} = Maximum NMOS FET gate-source leakage current, from NMOS FET datasheet
- R_{GS} = Minimum gate-source discharge resistance; usually not less than 10kΩ
- I_{HBQ} = Boot quiescent current with HI = 1 or PWM = 1

The minimum C_{BOOT} capacitance required to ensure proper functionality becomes dependent on the total charge required during the on state of the high side when the C_{BOOT} is not charging, along with the allowable change in voltage of the boot.

Equation 1 calculates the total charge required for one switching cycle of the high-side NMOS FET.

(EQ. 1) $$Q_{TOTAL} = Q_{GS_MAX} + \left(I_{GS_LKG} + I_{HBQ} + \frac{V_{HO}}{R_{GS}}\right) \times t_{ON}$$

Equation 2 calculates the boot capacitor needed to support the total charge and allowable boot voltage dip requirements:

(EQ. 2) $$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{BOOT}}$$

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5.7 VDD Decoupling Capacitor

For VDD decoupling, Renesas recommends selecting a capacitor that is at least 10x the value of the boot capacitor. In addition, place a low ESL, high-frequency, X7R or better ceramic capacitor of 1nF to 10nF close to the HIP2210/HIP2211 VDD and VSS pins for high-frequency decoupling.

5.8 RDT and Dead Time Delay (HIP2210 Only)

The PWM function of the HIP2210 inherently prevents driver input shoot-through conditions by allowing only one driver that is sourcing output to be active at one time. However, because NMOS FET gate-source capacitance causes FET turn-on/off times to be delayed, it is necessary to have some extra dead time at the driver outputs to prevent shoot-through conditions. The HIP2210 implements programmable dead time through the RDT pin function.

A resistor on the RDT pin to VSS sets the HIP2210 adjustable dead time delay. The delay is between the following:

- The falling edge of the LO output to the rising edge of the HO output
- The falling edge of the HO output to the rising edge of the LO output

The propagation delay from the PWM input to the falling edge on LO or HO is not affected by the adjustable dead time delay circuit. For example, when PWM goes high, LO goes low from the PWM with the LO propagation delay and HO goes high after the dead time delay set by the RDT resistor. Similarly, when PWM goes low, HO goes low from the PWM with the HO propagation delay and LO goes high after the dead time delay set by the RDT resistor.

The recommended resistance range on RDT pin to VSS is 10kΩ to 100kΩ, which sets a dead time delay range typically of 35ns to 350ns. If resistance is less than 1kΩ, the adjustable dead time delay is disabled and the nominal dead time delay on the rising edge is 15ns. Renesas recommends shorting the RDT pin to VSS to disable the adjustable delay function. The dead time delay set by the RDT resistor is adjustable on the fly in operation except for the disabled condition, where the disabled state is detected and latched in on POR and resets after going through UVLO. Resistance values outside of 10kΩ to 100kΩ produce a faster or slower dead time delay beyond the 35ns to 350ns range but the accuracy and matching performance is not guaranteed.

A 1.2V reference on the RDT pin drives a current through the RDT resistor. The current is mirrored and drives an internal oscillator to set the dead time delay.

Note: Because the RDT pin signal is analog, as the RDT resistance is increased, the sensitivity to parasitic capacitive and inductive pickup increases. When laying out the PCB, keep high dv/dt nodes away from the RDT pin and resistor. Guard ringing and/or shielding can also be used to shunt away dv/dt injected currents.

5.9 HO and LO Outputs

The HO and LO driver outputs can source 3A peak and sink 4A peak currents for driving capacitive loads such as the NMOS gate-source terminals. The strong gate drive allows low $r_{DS(ON)}$, high Q_{gs} FETs to be switched on and off quickly with minimal switching loss during the voltage and current cross-over region at the NMOS FET drain and source.

The fast propagation delay (15ns typical) and excellent delay matching (2ns typical) supports wide duty cycle and high-frequency applications robustly up to 1MHz.

Additionally, the LO pin has a pull-down impedance to VSS of 140kΩ and the HO pin has a pull-down impedance to HS of 450kΩ. These internal pull-down resistors prevent charge accumulation at the external NMOS FET gate-source capacitance that would turn on the FETs when there is no VDD bias on the HIP2210/HIP2211 driver, preventing a possible shoot-through condition at initial power-up.

5.10 Power Dissipation

The power dissipation of the HIP2210/HIP2211 is typically dominated by the gate charge required by the driven bridge MOSFETs and the switching frequency. The internal bias, boot diode, and MOSFET gate leakage also contribute to the total dissipation, but these losses are usually less significant compared to the switching gate

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charge losses. The calculation of the power dissipation of the HIP2210/HIP2211 is approximated by Equation 3 through Equation 9:

5.10.1 Gate Power (for the HO and LO Outputs)

(EQ. 3) $$P_{gate} = (Q_{gateH} + Q_{gateL}) \times Freq \times VDD$$

where Q_{gateH} and Q_{gateL} are the total gate charge of the high-side and low-side bridge FET, respectively.

This information is commonly found in the MOSFET datasheet typical performance curves for Q_{gs} vs Gate Voltage. VDD is the bias to the HIP2210/HIP2211 and Freq is the PWM switching frequency operation.

5.10.2 Boot Diode Dissipation

Equation 4 and Equation 5 represent the boot diode conduction loss from recharging the boot capacitor during the boot refresh cycle (phase node is low). The average current is proportional to the total charge delivered to the high-side NMOS FET and the switching frequency.

(EQ. 4) $$I_{diode_avg} = Q_{gate} \times Freq$$

(EQ. 5) $$P_{diode} = I_{diode_avg} \times (0.7V + I_{diode_avg} \times R_{diode})$$

where 0.7V is the typical internal boot diode forward voltage of the HIP2210/HIP2211, and R_{diode} is the dynamic resistance of the boot diode. See Figure 22 and Figure 23.

5.10.3 Dynamic Operating Current

(EQ. 6) $$P_{dynamic} = I_{dynamic} \times V_{HB}$$

where $I_{dynamic}$ is the dynamic operating current of the HIP2210 or HIP2211 into the HB pin at the switching frequency.

V_{HB} is the average boot to phase voltage and is approximately V_{HB} - V_{HS} = V_{DD} - 0.7V.

5.10.4 Total Power Dissipation

(EQ. 7) $$P_{total} = P_{gate} + P_{diode} + P_{dynamic}$$

5.10.5 Junction Operating Temperature

(EQ. 8) $$T_J = P_{total} \times \theta_{JA} + T_A$$

where T_J is the junction temperature at the operating ambient temperature in the vicinity of the part, T_A.

(EQ. 9) $$T_J = P_{total} \times \theta_{JC} + T_{PCB}$$

where T_J is the junction temperature with the operating temperature of the PCB, T_{PCB}, as measured where the EPAD is soldered.

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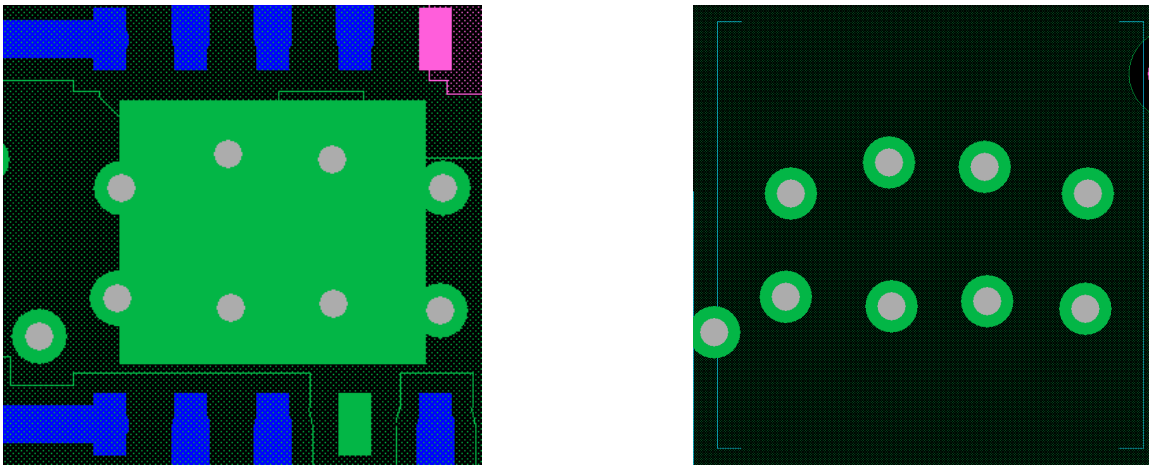
6. PCB Layout Guidelines

The AC performance of the HIP2210/HIP2211 depends significantly on the design of the PCB. The following layout design guidelines are recommended to achieve optimum switching performance:

- It may be necessary to add resistance to dampen resonating parasitic circuits. PCB designs with long trace lengths on the LO and HO outputs may require series gate resistors on the bridge FETs to dampen the oscillations. It is good practice to place 0Ω chip resistors in series with the HO and LO driver outputs to the MOSFET gates.
- The routing of the half-bridge switching phase node to the HIP2210/HIP2211 HS pin should implement optimum layout practices. The PCB trace should be short and wide to minimize lead inductance. Also, route the HO trace directly above or below the HS trace to minimize ground loops.
- Understand how power currents flow. The high amplitude di/dt currents of the half-bridge FETs induce significant voltage transients on the associated traces and ground planes. Keep these high current paths away from sensitive low voltage signal traces.
- Avoid paralleling high di/dt traces with low-level signal lines. High di/dt induces currents in the low-level signal lines.
- Keep power loops as short as possible by routing the source and return traces on adjacent layers, directly above and beneath each other.
- When practical, minimize impedances in low-level signal circuits. The noise magnetically induced on a 10k resistor is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Core gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines.
- Use low inductance components such as SMD chip resistors and chip capacitors with low Equivalent Series Inductance (ESL).
- Use decoupling capacitors to reduce the influence of parasitic inductance. To be effective, these capacitors must also have the shortest possible lead lengths to the component pins. If vias are used, connect several paralleled vias to reduce their inductance.
- Keep high dv/dt nodes away from low-level circuits. Guard ringing and/or shielding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for the RDT pin and resistor, and also the PWM and HI/LI signals.
- Avoid having a signal ground plane under a high dv/dt circuit. This injects high di/dt currents into the signal ground paths.
- Calculate power dissipation and voltage drop calculations for the power traces. Most PCB/CAD programs have built-in tools for calculation of trace resistance.
- Large power components (power FETs, electrolytic capacitors, power resistors, etc.) have internal parasitic inductance, which cannot be eliminated. Accounted for this in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components.
- If available, connect the EPAD on the bottom side of the package to the PCB ground plane with thermal vias for heat removal.

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6.1 PCB Layout and EPAD Recommendation



Top Layer Ground Plane

Figure 32. Recommended PCB Heatsink

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7. Revision History

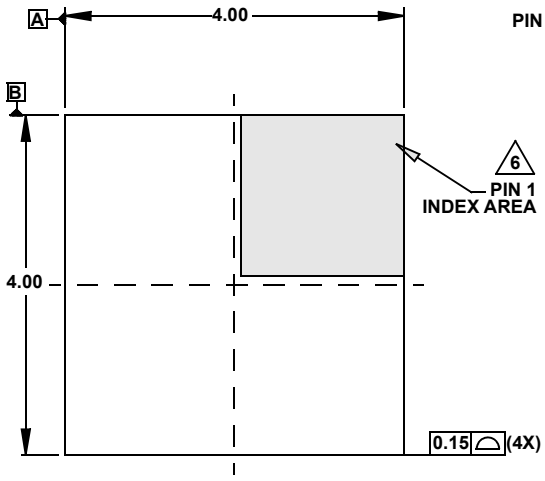
Rev.	Date	Description
1.02	Jun.23.20	Updated Robust noise tolerance Features bullet. Added Evaluation Boards to the Ordering Information table. Updated the Voltage on HS minimum specification from -1V to The greater of [-10 or -(20 - VDD)] in the Absolute Maximum Ratings and Recommended Operating Conditions sections. Removed the Transient Voltage on HS (Repetitive Transient for 100ns) specification from Absolute Maximum Ratings section. Removed the Transient Voltage on HS (Repetitive Transient for 10ns specification from Recommended Operating Conditions section.
1.01	Mar.16.20	Added 8 Ld DFN information throughout.
1.00	Feb.19.20	Initial release

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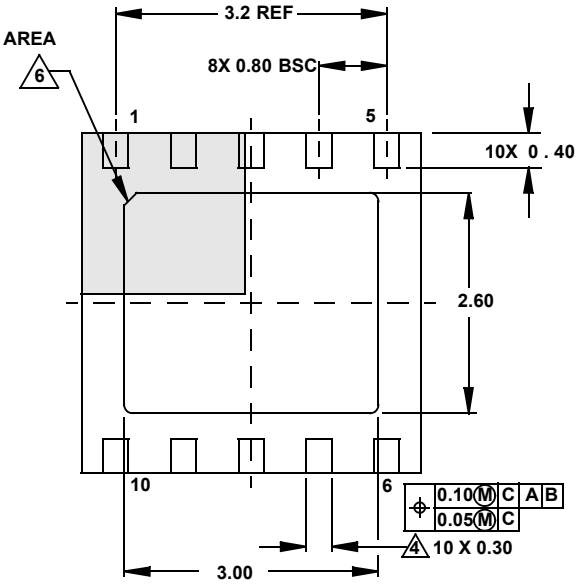
8. Package Outline Drawings

For the most recent package outline drawing, see L10.4x4.

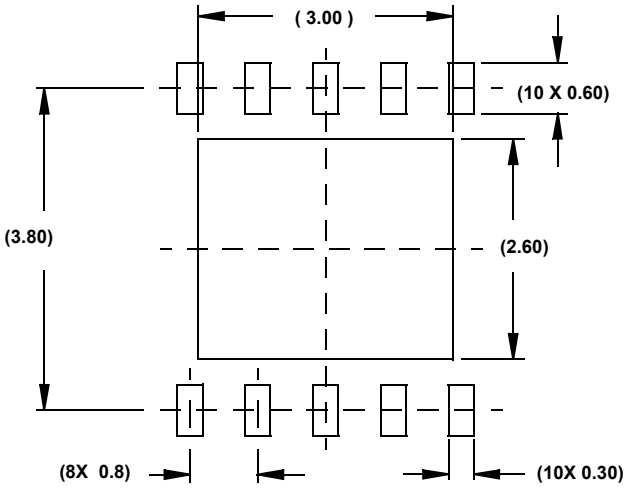
L10.4x4
10 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 2, 4/15



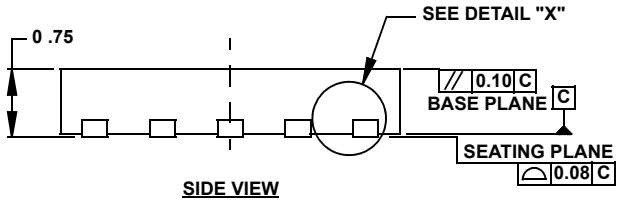
TOP VIEW



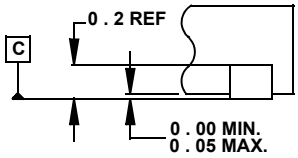
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

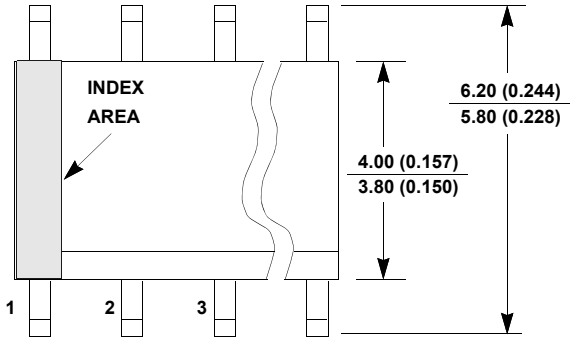
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

either a mold or mark feature.

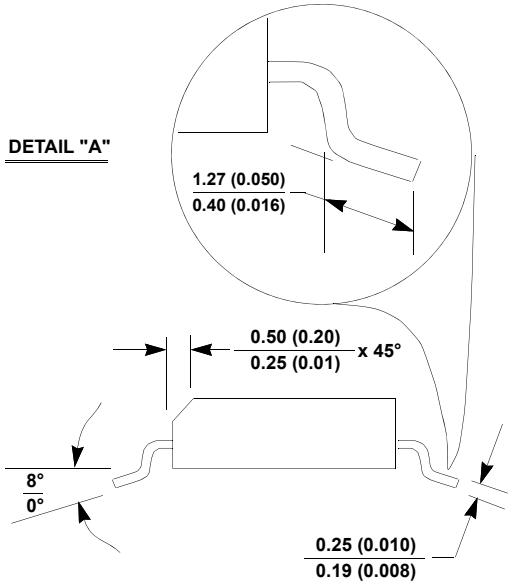
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M8.15
8 Lead Narrow Body Small Outline Plastic Package (SOIC)
Rev 4, 1/12

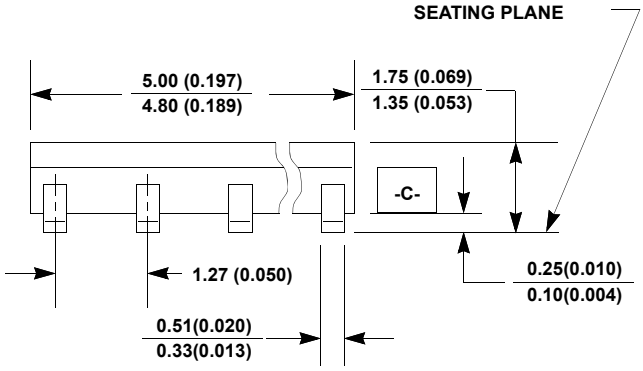
For the most recent package outline drawing, see M8.15.



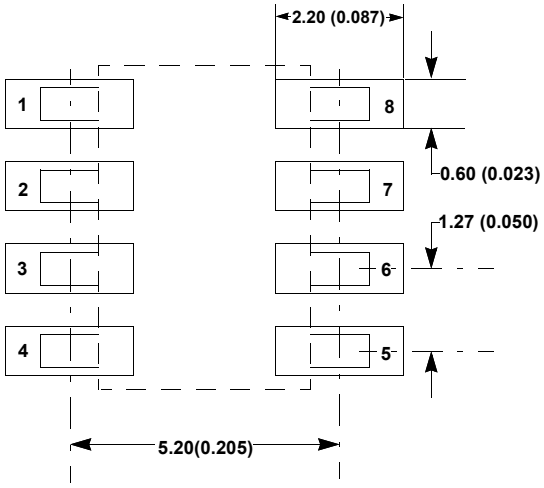
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

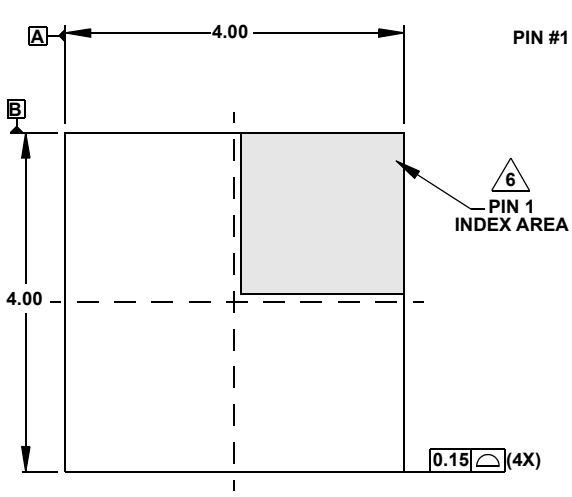
Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

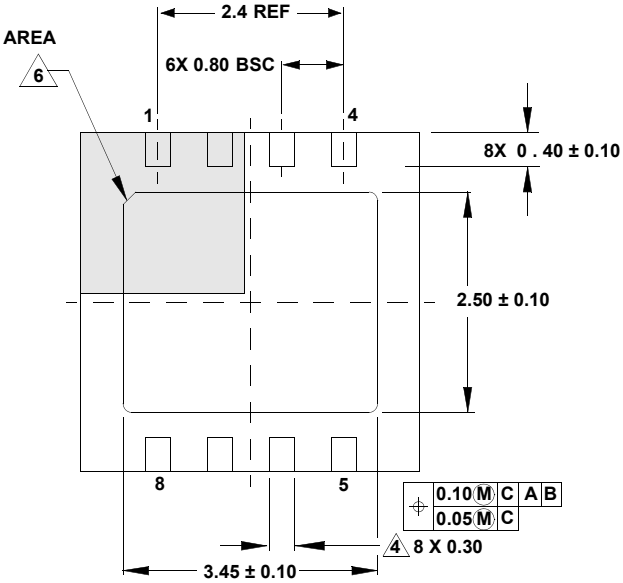
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L8.4x4
8 Lead Dual Flat No-Lead Plastic Package (DFN)
Rev 1, 03/15

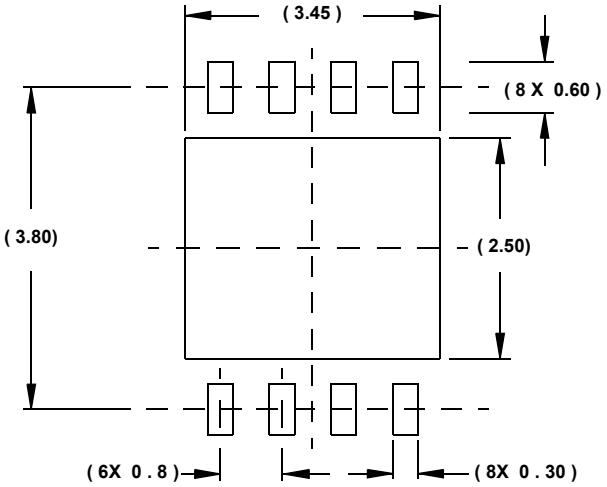
For the most recent package outline drawing, see L8.4x4.



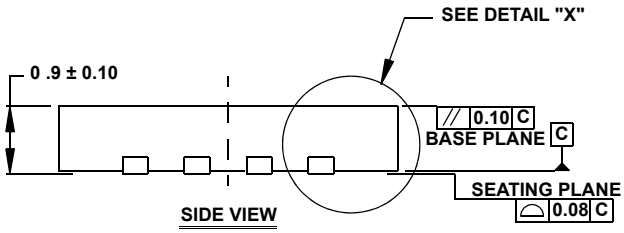
TOP VIEW



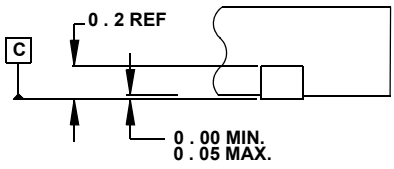
BOTTOM VIEW



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SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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