

# 2.5" PATA-SSD Datasheet

## CONTENTS

|                                                  |           |
|--------------------------------------------------|-----------|
| <b>1. Overview .....</b>                         | <b>4</b>  |
| <b>2. Features .....</b>                         | <b>5</b>  |
| <b>3. General Description .....</b>              | <b>7</b>  |
| <b>4. Pin Assignment and Description .....</b>   | <b>9</b>  |
| 4.1 2.5" PATA-SSD Interface Pin Assignments..... | 9         |
| 4.2 2.5" PATA-SSD Pin Descriptions .....         | 10        |
| <b>5. Identify Drive Information.....</b>        | <b>11</b> |
| <b>6. Power Management .....</b>                 | <b>13</b> |
| 6.1 Power Saving Flow .....                      | 14        |
| <b>7. ATA Command Set .....</b>                  | <b>15</b> |
| <b>8. System Power Consumption .....</b>         | <b>19</b> |
| <b>9. Electrical Specifications .....</b>        | <b>19</b> |
| <b>10. DC Characters.....</b>                    | <b>19</b> |
| <b>11. AC Characters.....</b>                    | <b>20</b> |
| 11.1 PIO Data Transfer .....                     | 20        |
| 11.2 Multi Word DMA .....                        | 22        |
| 11.3 Ultra DMA.....                              | 24        |
| <b>12. Physical Dimension.....</b>               | <b>31</b> |
| <b>Appendix: Part Number Table .....</b>         | <b>32</b> |

## Revision History

| Rev. | Date       | History                                       |
|------|------------|-----------------------------------------------|
| 0.1  | 2009/3/25  | 1. 1 <sup>st</sup> draft                      |
| 0.2  | 2009/3/30  | 1. Modify description                         |
| 0.3  | 2009/4/16  | 1. Increase testing information               |
| 0.4  | 2009/6/25  | 1. Increase extended temperature product line |
| 0.5  | 2009/7/14  | 1. Fixed the data transfer mode information.  |
| 0.6  | 2009/7/29  | 1. Define form template                       |
| 1.0  | 2010/11/25 | 1. Update Emb'Core Logo & PN List             |
|      |            |                                               |

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## **1. Overview**

Advantech SQFlash 2.5" PATA-SSD (Solid State Drive) is a non-volatile, solid state data storage system. Due to rapid reduction of flash media, Solid State Drive becomes more and more popular storage media to replace conventional Hard Disk Drive. Free of any mechanical components, 2.5" PATA-SSD provides more robust and cost effective storage solution for embedded application. Offering standard ATA interface, which is fully compatible with traditional HDD, 2.5" PATA-SSD offers the designer an easy solution to implement in PC-based systems.

Advantech SQFlash 2.5" PATA-SSD is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

## 2. Features

### ■ Standard 2.5" PATA Form Factor

### ■ Operating Voltage : 3.3V 、 5.0V

### ■ Standard ATA/IDE Bus Interface

- 512 Bytes/Sector
- ATA command set compatible
- Selectable Master/Slave Setting

### ■ Capacities

- SLC type : 4GB , 8GB , 16GB , 32GB , 64GB
- MLC type : 8GB , 16GB , 32GB , 64GB , 128GB

### ■ Data Transfer mode

- Support Data Transfer up to PIO mode 4
- Support Data Transfer up to Multiword DMA mode 2
- Support Data Transfer up to Ultra DMA mode 4

### ■ Performance

- SLC type
  - Sustain Read Speed up to 65 MB/s
  - Sustain Write Speed up to 55 MB/s
- MLC type
  - Sustain Read Speed up to 63 MB/s
  - Sustain Write Speed up to 28 MB/s

### ■ Temperature Ranges

- Commercial Temperature
  - 0°C to 70°C for operating
  - -25°C to 85°C for storage
- Extended Temperature
  - -40°C to 85°C for operating
  - -55°C to 125°C for storage

### ■ Mechanical Specification

- Shock : 2,500G / 0.5ms
- Vibration : 20G / 80~2,000Hz

### ■ Humidity

- Operating Humidity : 5% ~ 95%
- Non-Operating Humidity : 5% ~ 95%

### ■ Flash Endurance

- SLC type : 100,000 Program/Erase Cycle
- MLC type : 5,000 Program/Erase Cycle

### ■ MTBF

- 2,000,000 hours

### ■ Data Retention

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- 10 years

■ **Intelligent ATA/IDE Module**

- Built-in Embedded Flash File System
- Implements dynamic wear-leveling algorithms and static wear-leveling algorithms to increase endurance of flash media
- This algorithm can correct up to 12 random bits per 512bytes area.

■ **Acquired RoHS 、 CE 、 FCC Certificate**

■ **Dimension : 100mm x 69.85mm x 7.2 mm**

### 3. General Description

#### ■ **Advanced NAND Flash Controller**

Advantech SQFlash 2.5" PATA-SSD includes Bad Block Management Algorithm, Wear Leveling Algorithm and Error Detection / Correction Code (EDC/ECC) Algorithm.

#### ■ **Bad Block Management**

Bad blocks are blocks that contain one or more invalid bits of which the reliability is not guaranteed. Bad blocks may be representing when flash is shipped and may developed during life time of the device.

Advantech SQFlash 2.5" PATA-SSD implement an efficient bad block management algorithm to detect the factory produced bad blocks and manages any bad blocks that may develop over the life time of the device. This process is completely transparent to the user, user will not aware of the existence of the bad blocks during operation.

#### ■ **Wear Leveling**

NAND Type flash have individually erasable blocks, each of which can be put through a finite number of erase cycles before becoming unreliable. It means after certain cycles for any given block, errors can be occurred in a much higher rate compared with typical situation. Unfortunately, in the most of cases, the flash media will not been used evenly. For certain area, like file system, the data gets updated much frequently than other area. Flash media will rapidly wear out in place without any rotation.

Wear leveling attempts to work around these limitations by arranging data so that erasures and re-writes are distributed evenly across the full medium. In this way, no single sector prematurely fails due to a high concentration of program/erase cycles.

Advantech SQFlash 2.5" PATA-SSD provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. By implement both dynamic and static wear leveling algorithms, the life expectancy of the flash media can be improved significantly.

#### ■ **Error Detection / Correction**

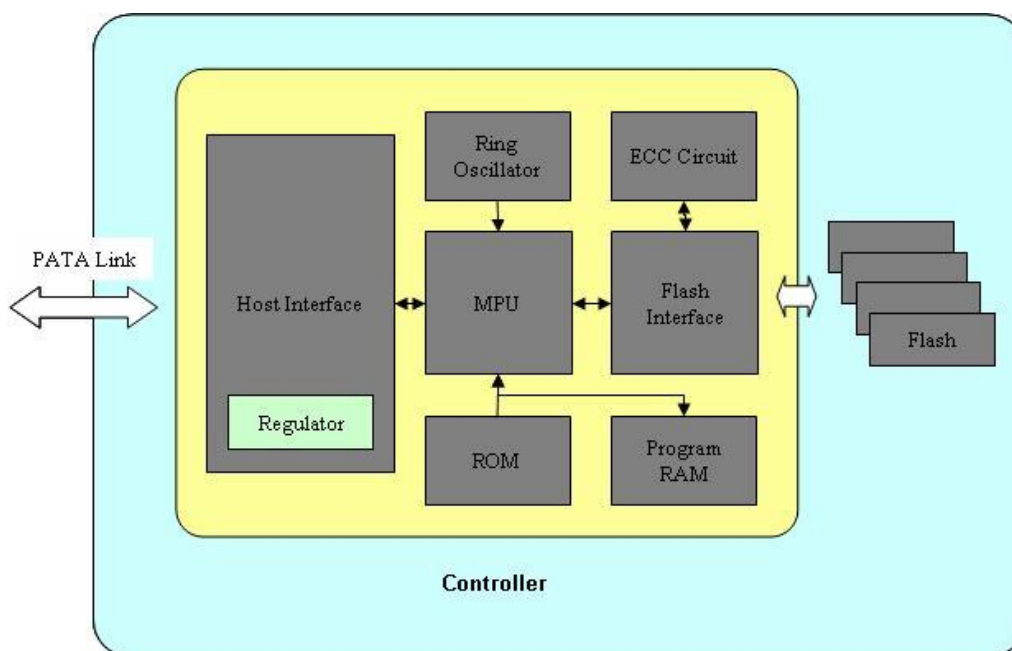
Advantech SQFlash 2.5" PATA-SSD utilizes BCH ECC Algorithm which offers one of the most powerful ECC algorithms in the industry. This algorithm can correct up to 12 random bits per 512bytes area.

#### ■ **Sophisticate Product Management Systems**

Since industrial application require much more reliable devices compare with consumer product, a more sophisticated product management system become necessary for industrial customer requirement. The key to providing reliable devices is product traceability and failure analysis system. By implement such systems end customer can expect much more reliable product.

#### ■ **Block Diagram**

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■ LBA 、Cylinders 、Heads 、Sectors value

| Density | LBA (K bytes) | Cylinders | Heads | Sectors |
|---------|---------------|-----------|-------|---------|
| 4 GB    | 7,880,544     | 7,818     | 16    | 63      |
| 8 GB    | 15,072,624    | 14,953    | 16    | 63      |
| 16 GB   | 30,146,256    | 16,383    | 16    | 63      |
| 32 GB   | 61,078,752    | 16,383    | 16    | 63      |
| 64 GB   | 122,158,512   | 16,383    | 16    | 63      |
| 128 GB  | 249,822,720   | 16,383    | 16    | 63      |

## 4. Pin Assignment and Description

### 4.1 2.5" PATA-SSD Interface Pin Assignments

| Pin # | Signal Name           | Pin Type | Pin # | Signal Name   | Pin Type |
|-------|-----------------------|----------|-------|---------------|----------|
| 1     | -RESET                | I        | 2     | GND           | -        |
| 3     | DD7                   | I/O      | 4     | DD8           | I/O      |
| 5     | DD6                   | I/O      | 6     | DD9           | I/O      |
| 7     | DD5                   | I/O      | 8     | DD10          | I/O      |
| 9     | DD4                   | I/O      | 10    | DD11          | I/O      |
| 11    | DD3                   | I/O      | 12    | DD12          | I/O      |
| 13    | DD2                   | I/O      | 14    | DD13          | I/O      |
| 15    | DD1                   | I/O      | 16    | DD14          | I/O      |
| 17    | DD0                   | I/O      | 18    | DD15          | I/O      |
| 19    | GND                   | -        | 20    | KEY PIN(OPEN) |          |
| 21    | DMARQ                 | O        | 22    | GND           | -        |
| 23    | -DIOW:STOP            | I        | 24    | GND           | -        |
| 25    | -DIOR:-HDMARDY:HSTOBE | O        | 26    | GND           | -        |
| 27    | IORDY:DDMARDY:DSTROBE |          | 28    | CSEL          | I        |
| 29    | -DMACK                | I        | 30    | GND           | -        |
| 31    | INTRQ                 | O        | 32    | IOIS16        | O        |
| 33    | DA1                   | I        | 34    | -PDIAG:-CBLID | I/O      |
| 35    | DA0                   | I        | 36    | DA2           | I        |
| 37    | -CS0                  | I        | 38    | -CS1          | I        |
| 39    | -DASP                 | I/O      | 40    | GND           | -        |
| 41    | VCC                   | P        | 42    | VCC           | P        |
| 43    | GND                   | -        | 44    | NC            |          |

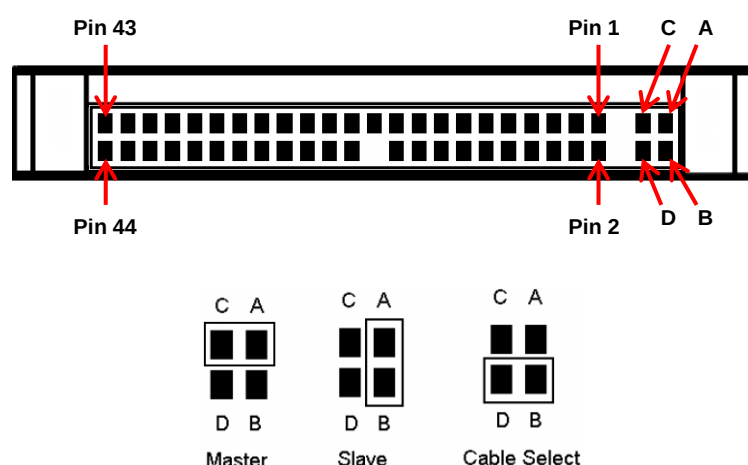
**\*Note :**

"I" : An input from the host system to the device.

"O" : An output from the device to the host system.

"I/O" : An input/output (bi-direction) common.

"P" : Power supply.



## 4.2 2.5" PATA-SSD Pin Descriptions

| Pin #                                                         | Signal Name                                       | Pin Type | Description                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------------|---------------------------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                             | <b>-RESET</b>                                     | I        | Hardware reset signal from the host                                                                                                                                                                                                                                                     |
| 17, 15, 13, 11, 9,<br>7, 5, 3, 4, 6, 8,<br>10, 12, 14, 16, 18 | <b>DD0~DD15</b><br>(Device Data)                  | I/O      | 16-bit bi-direction Data Bus. DD (7:0) are used for 8-bit register transfers.                                                                                                                                                                                                           |
| 21                                                            | <b>DMARQ</b><br>(DMA Request)                     | O        | For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.                                                                                                                                                                         |
| 23                                                            | <b>-DIOW</b><br>(I/O Write)                       | I        | This is the strobe signal used by the host to write to the device register or Data port                                                                                                                                                                                                 |
|                                                               | <b>STOP</b><br>(Stop UDMA Burst)                  |          | The host assert this signal during an UDMA burst to stop the DMA burst                                                                                                                                                                                                                  |
| 25                                                            | <b>IORDY</b><br>(I/O channel ready)               | O        | This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.                                                                                                                                    |
|                                                               | <b>DDMARDY</b><br>(UDMA ready)                    |          | The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.                                                                                                                                                                                 |
|                                                               | <b>DSTROBE</b><br>(UDMA data strobe)              |          | When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.                                                                                                                                                                                           |
| 28                                                            | <b>CSEL</b><br>(Cable select)                     | I        | This pin is used to configure this device as Device 0 or Device 1.                                                                                                                                                                                                                      |
| 29                                                            | <b>-DMACK</b><br>(DMA acknowledge)                | I        | This signal is used by the host in respond to DMARQ to initiate DMA transfer.                                                                                                                                                                                                           |
| 31                                                            | <b>INTRQ</b><br>(Interrupt)                       | O        | When this device is selected, this signal is the active high Interrupt Request to the host                                                                                                                                                                                              |
| 32                                                            | <b>IOIS16</b>                                     | O        | During PIO transfer mode0, 1 or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word. When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted. |
| 35, 33, 36                                                    | <b>DA0~DA2</b><br>(Device Address)                | I        | This is 3-bit binary coded Address Bus.                                                                                                                                                                                                                                                 |
| 34                                                            | <b>-PDIAG</b><br>(Passed diagnostics)             | I/O      | This signal will be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics,                                                                                                                                                                               |
|                                                               | <b>-CBLID</b><br>(Cable assembly type identify)   |          |                                                                                                                                                                                                                                                                                         |
| 37, 38                                                        | <b>-CS0, -CS1</b><br>(Chip select)                | I        | These signals are used to select the Command Block and Control Block registers. When -DMACK is asserted, -Cs0 and -Cs1 shall be negated and transfers shall be 16-bit wide.                                                                                                             |
| 39                                                            | <b>-DASP</b><br>(Device active, Device 1 present) | I/O      | During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.                                                                                                                                                                                  |
| 41, 42                                                        | <b>VCC</b>                                        | P        | Power supply                                                                                                                                                                                                                                                                            |
| 2, 19, 22, 24, 26,<br>30, 40, 43                              | <b>GND</b>                                        | --       | Ground.                                                                                                                                                                                                                                                                                 |

## 5. Identify Drive Information

The Identify Drive Command enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

| Word Address | Default Value | Total Bytes | Data Field Type Information                                                        |
|--------------|---------------|-------------|------------------------------------------------------------------------------------|
| 0            | 044Ah         | 2           | General configuration – bit significant for Non-removable device                   |
| 1            | xxxxh         | 2           | Default number of cylinders                                                        |
| 2            | 0000h         | 2           | Reserved                                                                           |
| 3            | xxxxh         | 2           | Default number of heads                                                            |
| 4            | 7E00h         | 2           | Retired                                                                            |
| 5            | 0200h         | 2           | Retired                                                                            |
| 6            | xxxxh         | 2           | Default number of sectors per track                                                |
| 7 - 8        | xxxxh         | 4           | Number of sectors per device                                                       |
| 9            | 0000h         | 2           | Retired                                                                            |
| 10 - 19      | xxxxh         | 20          | Serial Number in ASCII                                                             |
| 20           | 0002h         | 2           | Retired                                                                            |
| 21           | 0002h         | 2           | Retired                                                                            |
| 22           | 0004h         | 2           | Number of ECC Bytes passed on Read/Write Long Commands                             |
| 23 - 26      | aaaah         | 8           | Firmware revision in ASCII                                                         |
| 27 - 46      | xxxxh         | 40          | Model number in ASCII                                                              |
| 47           | 8001h         | 2           | Maximum number of sector that shall be transferred on Read/Write Multiple commands |
| 48           | 0000h         | 2           | Reserved                                                                           |
| 49           | 2B00h         | 2           | Capabilities-LBA/DMA Supported                                                     |
| 50           | 4000h         | 2           | Reserved                                                                           |
| 51           | 0200h         | 2           | PIO data transfer cycle timing mode 2                                              |
| 52           | 0000h         | 2           | Retired                                                                            |
| 53           | 0007h         | 2           | Word 54 - 58, 64 - 70 and 88 are valid                                             |
| 54           | xxxxh         | 2           | Current numbers of cylinders                                                       |
| 55           | xxxxh         | 2           | Current numbers of heads                                                           |
| 56           | xxxxh         | 2           | Current sectors per track                                                          |
| 57 - 58      | xxxxh         | 4           | Current capacity in sectors (LBAs)(Word 57= LSW, Word 58= MSW)                     |
| 59           | 0101h         | 2           | Multiple sector setting is valid                                                   |
| 60 - 61      | xxxxh         | 4           | Total number of sectors addressable in LBA Mode                                    |
| 62           | 0000h         | 2           | Retired                                                                            |
| 63           | 0007h         | 2           | Multiword DMA mode 2 and below are supported                                       |
| 64           | 0003h         | 2           | Advance PIO transfer modes supported                                               |
| 65           | 0078h         | 2           | Minimum Multiword DMA transfer cycle time 120nsec                                  |
| 66           | 0078h         | 2           | Manufacturer's recommended Multiword DMA transfer cycle time 120nsec               |
| 67           | 0078h         | 2           | Minimum PIO transfer cycle time without flow control 120nsec                       |
| 68           | 0078h         | 2           | Minimum PIO transfer cycle time with IORDY flow control 120 nsec                   |
| 69 - 79      | 0000h         | 26          | Reserved                                                                           |
| 80           | 0030h         |             | Major version number                                                               |
| 81           | 0000h         |             | Reserved                                                                           |
| 82           | 7009h         | 2           | Supports Security Mode feature set                                                 |
| 83           | 5004h         | 2           | Reserved                                                                           |

| Word Address | Default Value | Total Bytes | Data Field Type Information                                 |
|--------------|---------------|-------------|-------------------------------------------------------------|
| 84           | 4000h         |             |                                                             |
| 85           | 7009h         |             | Feature Setting                                             |
| 86           | 1004h         |             | Feature Setting                                             |
| 87           | 4000h         |             | Feature Setting                                             |
| 88           | 203Fh         | 2           | Ultra DMA mode 5 and below are supported, UDMA mode5 select |
| 89 - 92      | 0000h         | 8           | Reserved                                                    |
| 93           | xxxxh         |             |                                                             |
| 94 - 128     | 0000h         | 2           | Enhanced security erase supported                           |
| 129 - 159    | 0000h         | 62          | Reserved vendor unique bytes                                |
| 160 - 255    | 0000h         | 192         | Reserved                                                    |

**\*Note :**

“a” : Vender Specific Configuration

“n” : Host Selectable Configuration

## 6. Power Management

2.5" PATA-SSD provides automatic power saving mode. There are four modes on this system.

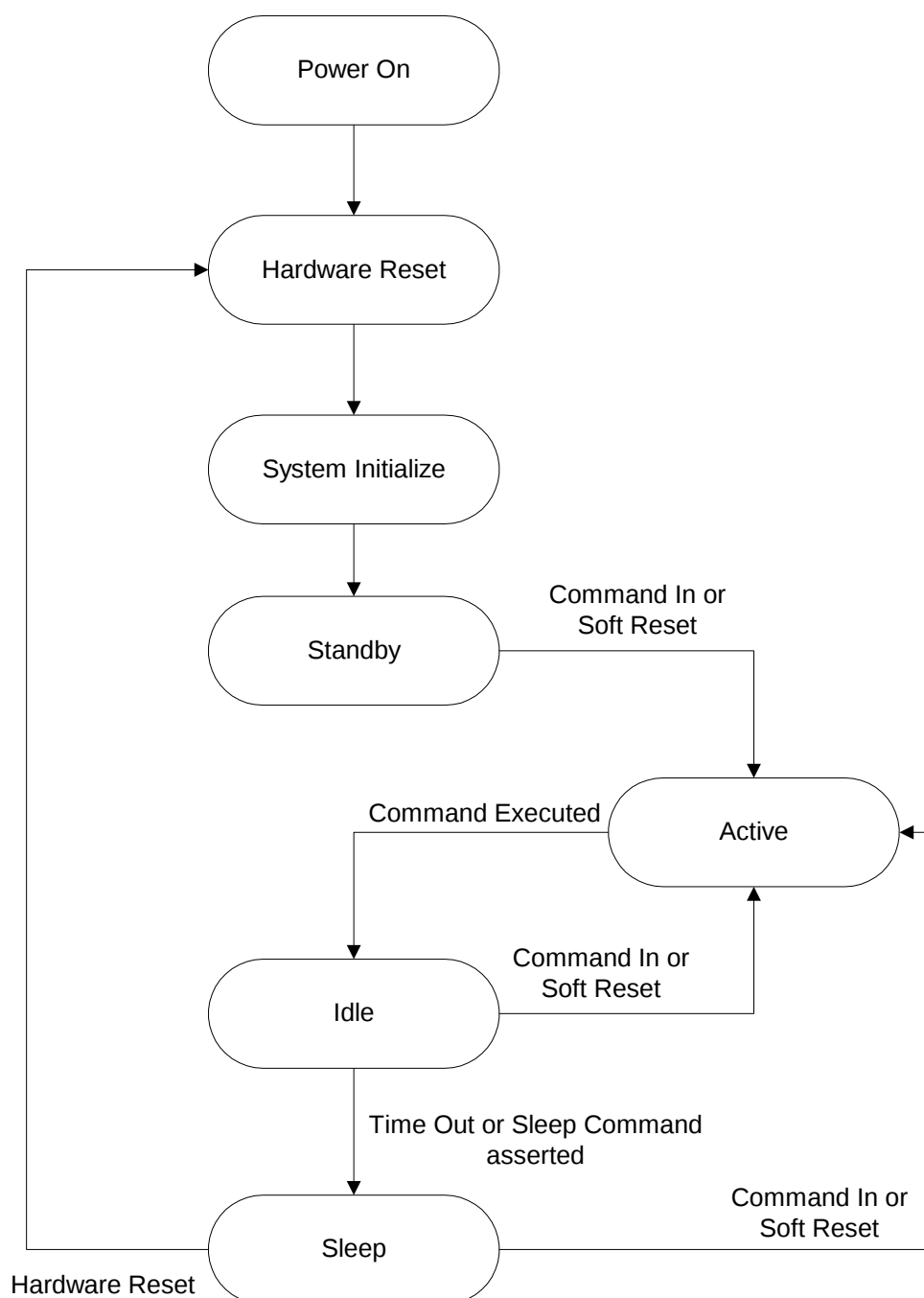
**Standby Mode:** When 2.5" PATA-SSD finishes the initialization routine after power reset, it goes into Standby Mode and wait for Command In or Soft Reset.

**Active Mode:** If 2.5" PATA-SSD received any Command In or Soft Reset, it goes into Active Mode. In Active Mode, it is capable to execute any ATA commands. The power consumption is the greatest in this mode.

**Idle Mode:** After 2.5" PATA-SSD executed any ATA Commands or Soft Reset, it goes into Idle Mode. Power consumption is reduced from Active Mode.

**Sleep Mode:** The 2.5" PATA-SSD will enter Sleep Mode if there is no Command In or Soft Reset from the host. Sleep Mode provides the lowest power consumption. During Sleep Mode, the system main clock is stopped. This mode can be waked up from hardware reset, software reset or any ATA command asserted.

## 6.1 Power Saving Flow



## 7. ATA Command Set

[Command Set List]

| No. | Command set                    | Code    | FR  | SC | SN | CY | DR | HD | LBA |
|-----|--------------------------------|---------|-----|----|----|----|----|----|-----|
| 1   | CHECK POWER MODE               | 98h,E5h | N   | N  | N  | N  | Y  | N  | N   |
| 2   | EXECUTE DEVICE DIAGNOSTIC      | 90h     | N   | N  | N  | N  | N  | N  | N   |
| 3   | IDENTIFY DEVICE                | Ech     | N   | N  | N  | N  | Y  | N  | N   |
| 4   | IDLE                           | 97h,E3h | N   | Y  | N  | N  | Y  | N  | N   |
| 5   | IDLE IMMEDIATE                 | 95h,E1h | N   | N  | N  | N  | Y  | N  | N   |
| 6   | INITIALIZE DEVICE PARAMETERS   | 91h     | N   | Y  | N  | N  | Y  | Y  | N   |
| 7   | NOP                            | 00h     | N   | N  | N  | N  | Y  | N  | N   |
| 8   | READ BUFFER                    | E4h     | N   | N  | N  | N  | Y  | N  | N   |
| 9   | READ DMA                       | C8h,C9h | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 10  | READ MULTIPLE                  | C4h     | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 11  | READ NATIVE MAX ADDRESS        | F8h     | N   | N  | N  | N  | Y  | N  | Y   |
| 12  | READ LONG SECTOR               | 22h,23h | N   | N  | Y  | Y  | Y  | Y  | Y   |
| 13  | READ SECTOR(S)                 | 20h,21h | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 14  | READ VERIFY SECTOR(S)          | 40h,41h | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 15  | RECALIBRATE                    | 1Xh     | N   | N  | N  | N  | Y  | N  | N   |
| 16  | SECURITY DISABLE PASSWORD      | F6h     | N   | N  | N  | N  | Y  | N  | N   |
| 17  | SECURITY ERASE PREPARE         | F3h     | N   | N  | N  | N  | Y  | N  | N   |
| 18  | SECURITY ERASE UNIT            | F4h     | N   | N  | N  | N  | Y  | N  | N   |
| 19  | SECURITY FREEZE LOCK           | F5h     | N   | N  | N  | N  | Y  | N  | N   |
| 20  | SECURITY SET PASSWORD          | F1h     | N   | N  | N  | N  | Y  | N  | N   |
| 21  | SECURITY UNLOCK                | F2h     | N   | N  | N  | N  | Y  | N  | N   |
| 22  | SEEK                           | 7Xh     | N   | N  | Y  | Y  | Y  | Y  | Y   |
| 23  | SET FEATURE                    | EFh     | Y   | Y  | Y  | Y  | Y  | Y  | N   |
| 24  | SET MULTIPLE                   | C6h     | N   | Y  | N  | N  | Y  | N  | N   |
| 25  | SLEEP                          | 99h,E6h | N   | N  | N  | N  | Y  | N  | N   |
| 26  | SMART ENABLE/DISABLE AUTO SAVE | B0h     | D2h | Y  | N  | Y  | Y  | N  | N   |
| 27  | SMART ENABLE OPERATION         | B0h     | D8h | N  | N  | Y  | Y  | N  | N   |
| 28  | SMART DISABLE OPERATION        | B0h     | D9h | N  | N  | Y  | Y  | N  | N   |
| 29  | SMART RETURN STATUS            | B0h     | DAh | N  | N  | Y  | Y  | N  | N   |
| 30  | STANDBY                        | 96h,E2h | N   | N  | N  | N  | Y  | N  | N   |
| 31  | STANDBY IMMEDIATE              | 94h,E0h | N   | N  | N  | N  | Y  | N  | N   |
| 32  | WRITE BUFFER                   | E8h     | N   | N  | N  | N  | Y  | N  | N   |
| 33  | Write DMA                      | CAh,CBh | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 34  | Write Multiple                 | C5h     | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 35  | Write Long Sector              | 32h,33h | N   | N  | Y  | Y  | Y  | Y  | Y   |
| 36  | Write Sector(s)                | 30h,31h | N   | Y  | Y  | Y  | Y  | Y  | Y   |
| 37  | Write Verify                   | 3Ch     | N   | Y  | Y  | Y  | Y  | Y  | Y   |

Note : FR: Feature Register

SN: Sector Number register

DR: Device bit of Device/Head register

NH: No. of Heads

Y: Setup

SC: Sector Count registers

CY: Cylinder Low/High register

HD: Head No. (3 to 0) of Device/Head register

LBA: Logical Block Address

N: Not setup

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## [Command Set Descriptions]

**1. CHECK POWER MODE (code: E5h);**

This command checks the power mode.

**2. EXECUTE DEVICE DIAGNOSTIC (code: 90h);**

This command performs the internal diagnostic tests implemented by the module.

**3. IDENTIFY DEVICE (code: ECh);**

The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

**4. IDLE (code: 97h or E3h);**

This command allows the host to place the module in the Idle mode and also set the Standby timer. H\_INTRQ\_P may be asserted even though the module may not have fully transitioned to Idle mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

**5. IDLE IMMEDIATE (code: 95h or E1h);**

This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

**6. INITIALIZE DEVICE PARAMETERS (code: 91h);**

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

**7. NOP (code: 00h);**

If this command is issued, the module respond with command aborted.

**8. READ BUFFER (code: E4h);**

This command enables the host to read the current contents of the module's sector buffer.

**9. READ DMA (code: C8h,C9h);**

This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**10. READ MULTIPLE (code: C4h);**

This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple commands.

**11. READ NATIVE MAX ADDRESS (code: F8h);**

This command returns the native maximum address.

**12. READ LONG SECTOR (code: 22h, 23h);**

This command is provided for compatibility purposes and nearly performs "1" sector READ SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are all 0 data.

**13. READ SECTOR(S) (code: 20h or 21h);**

This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**14. READ VERIFY SECTOR(S) (code: 40h or 41h);**

Specifications subject to change without notice, contact your sales representatives for the most update information.

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

**15. RECALIBRATE (code: 1Xh);**

This command return value is select address mode by the host request.

**16. SECURITY DISABLE PASSWORD (code: F6h);**

This command transfers 512Bytes of data from the host. Table Security Password defines the content of this information.

**17. SECURITY ERASE PREPARE (code: F3h);**

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlock. This command prevents accidental erase of the device.

**18. SECURITY ERASE UNIT (code: F4h);**

This command requests transfer of a single sector of data as form of table SECURITY ERASE UNIT password from the host.

If the password is not match, this command will be reject, the Security Erase Prepare command should be completed immediately prior the Security Erase Unit command.

If Normal Erase mode, the all user data area will be written binary 0, if Enhanced Erase mode, the predetermined data pattern will written to the user data area.

**19. SECURITY FREEZE LOCK (code: F5h);**

This command sets the device to Frozen mode. After command completion, all other commands that update device lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset.

**20. SECURITY SET PASSWORD (code: F1h);**

This command requests a transfer of a single sector of data from the host.

**21. SECURITY UNLOCK (code: F2h);**

This command requests transfer of a single sector of data from the host.

**22. SEEK (code: 7Xh);**

This command performs a range check.

**23. SET FEATURE (code: EFh);**

This command is used by the host to establish parameters that affect the execution of certain device features.

**24. SET MULTIPLE MODE (code: C6h);**

This command enables the module to perform READ and Write Multiple operations and establishes the block count for these commands.

**25. SLEEP (code: 99h or E6h );**

This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

**26. SMART ENABLE/DISABLE AUTO SAVE (code: B0h);**

This command enables and disables the optional attribute auto save feature of the module.

**27. SMART ENABLE OPEARIONS (code: B0h);**

This command enables access to all SMART capabilities within the module.

**28. SMART DISABLE OPEMTIONS (code: B0h);**

This command disables all SMART capabilities within the module.

**29. SMART RETURN STATUS (code: B0h);**

This command causes the module return the reliability status of the module to the host.

**30. STANDBY (code: 96h or E2h);**

This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

**31. STANDBY IMMEDIATE (code: 94h or E0h);**

This command causes the module to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.

**32. WRITE BUFFER (code: E8h);**

This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.

**33. WRITR DMA (code: CAh or CBh);**

This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**34. WRITE MULTIPLE (code: C5h);**

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

**35. WRITE LONG SECTOR (code: 32h or 33h);**

This command is provided for compatibility purposes and nearly performs "1" sector WRITE SECTOR command except that it transfers the data and 4 bytes appended to the sector. These appended 4 bytes are not written on the flash memories.

**36. WRITE SECTOR(S) (code: 30h or 31h);**

This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**37. WRITE VERIFY (code: 3Ch);**

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

## 8. System Power Consumption

(Ta = 0 to 70°C)

| Symbol           | Parameter          | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------|------------|-----|-----|-----|------|
| I <sub>ccr</sub> | Read current       | 5V         | -   | 130 | -   | mA   |
| I <sub>ccw</sub> | Write current      | 5V         | -   | 140 | -   | mA   |
| I <sub>pd</sub>  | Power down current | 5V         | -   | 0.2 | 0.4 | mA   |
| I <sub>ccr</sub> | Read current       | 3.3V       | -   | 200 | -   | mA   |
| I <sub>ccw</sub> | Write current      | 3.3V       | -   | 210 | -   | mA   |
| I <sub>pd</sub>  | Power down current | 3.3V       | -   | 0.3 | -   | mA   |

## 9. Electrical Specifications

### Absolute Maximum Rating

| Symbol                           | Parameter             | Min                  | Max                  | Unit | Remark             |
|----------------------------------|-----------------------|----------------------|----------------------|------|--------------------|
| V <sub>DD</sub> -V <sub>SS</sub> | DC Power Supply       | -0.3                 | +5.5                 | V    |                    |
| V <sub>IN</sub>                  | Input Voltage         | V <sub>SS</sub> -0.3 | V <sub>DD</sub> +0.3 | V    |                    |
| Ta                               | Operating Temperature | 0                    | +70                  | °C   | Commercial version |
| Tst                              | Storage Temperature   | -25                  | +85                  | °C   | Commercial version |
| Ta                               | Operating Temperature | -40                  | +85                  | °C   | Extended version   |
| Tst                              | Storage Temperature   | -55                  | +125                 | °C   | Extended version   |

| Symbol          | Parameter               | Min | Typ | Max | Unit | Remark |
|-----------------|-------------------------|-----|-----|-----|------|--------|
| V <sub>DD</sub> | V <sub>DD</sub> Voltage | 3.0 | 3.3 | 3.6 | V    |        |
|                 |                         | 4.5 | 5.0 | 5.5 | V    |        |

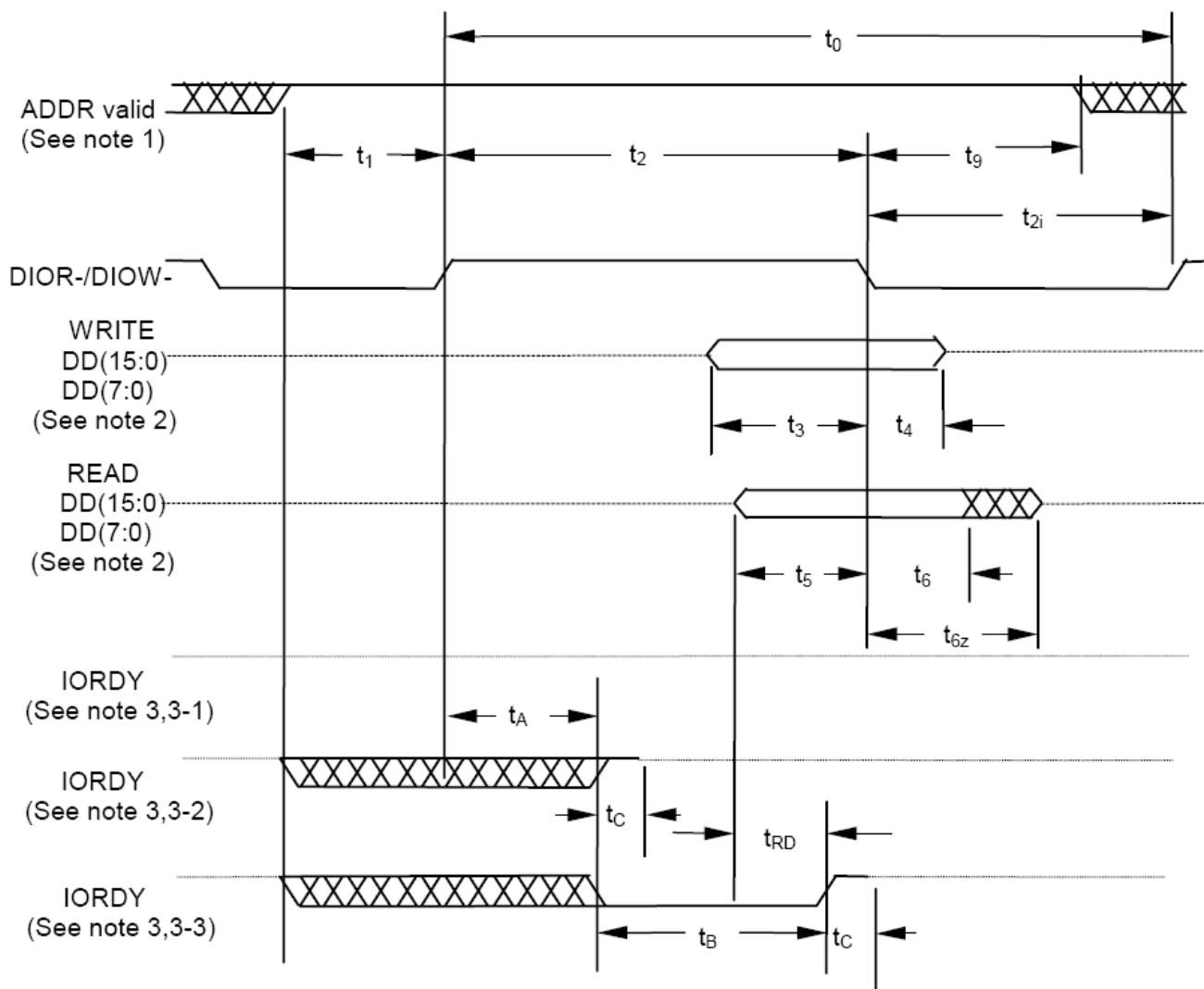
## 10. DC Characters

### DC characteristics of 5.0V I/O Cells (Host Interface)

| Symbol          | Parameter                        | Conditions                    | Min  | Typ | Max  | Unit |
|-----------------|----------------------------------|-------------------------------|------|-----|------|------|
| V <sub>OL</sub> | Output Low Voltage               | I <sub>OL</sub>   = 4 ~ 32 mA | -    | -   | 0.4  | V    |
| V <sub>OH</sub> | Output High Voltage              | I <sub>OH</sub>   = 4 ~ 32 mA | 2.8  | -   | -    | V    |
| V <sub>IL</sub> | Input Low Voltage                | TTL (5V)                      | -    | -   | 0.85 | V    |
| V <sub>IH</sub> | Input High Voltage               |                               | 1.25 | -   | -    | V    |
| V <sub>IL</sub> | Input Low Voltage                | TTL (3.3V)                    | -    | -   | 1.05 | V    |
| V <sub>IH</sub> | Input High Voltage               |                               | 1.75 | -   | -    | V    |
| I <sub>IN</sub> | Input Leakage Current            | No pull-up or pull-down       | -10  | ±1  | 10   | μA   |
| I <sub>OZ</sub> | Tri-state Output Leakage Current |                               | -10  | ±1  | 10   | μA   |

## 11. AC Characters

### 11.1 PIO Data Transfer



#### NOTES –

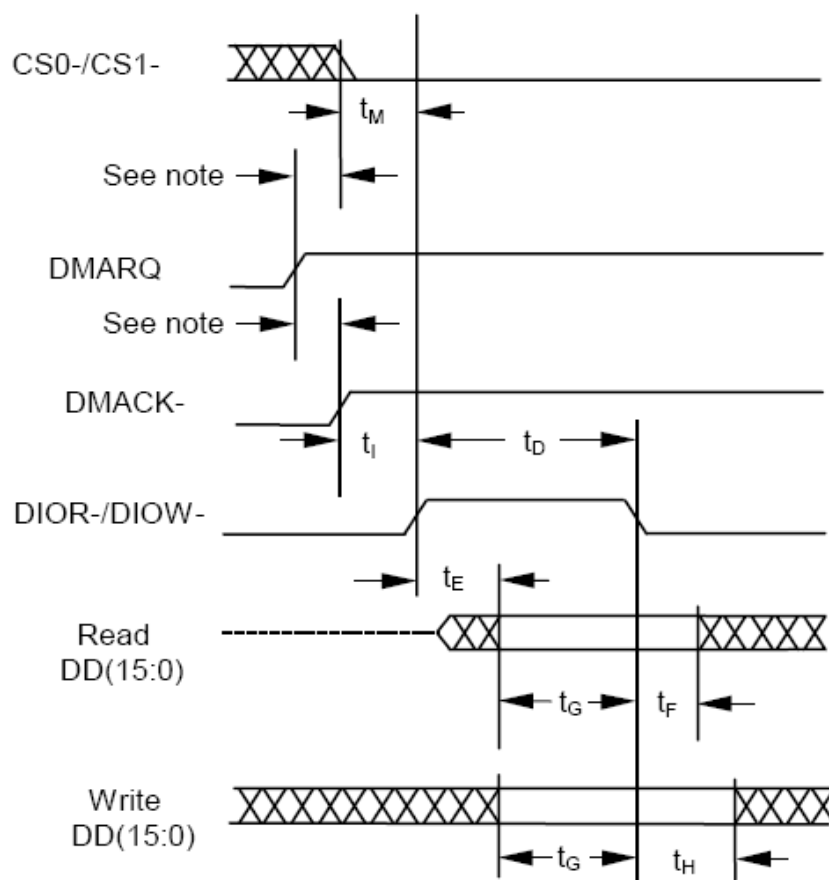
- 1 Device address consists of signals CS0-, CS1- and DA(2:0)
- 2 Data consists of DD(15:0) for all devices except devices implementing the CFA feature set when 8-bit transfers is enabled. In that case, data consists of DD(7:0).
- 3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after  $t_A$  from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
  - 3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
  - 3-2 Device negates IORDY before  $t_A$ , but causes IORDY to be asserted before  $t_A$ . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
  - 3-3 Device negates IORDY before  $t_A$ . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for  $t_{RD}$  before asserting IORDY.
- 4 DMACK- shall be negated during a PIO data transfer.

| PIO timing parameters |                                                                             | Mode<br>0<br>ns | Mode<br>1<br>ns | Mode<br>2<br>ns | Mode<br>3<br>ns | Mode<br>4<br>ns | Note |
|-----------------------|-----------------------------------------------------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|
| $t_0$                 | Cycle time (min)                                                            | 600             | 383             | 240             | 180             | 120             | 1,4  |
| $t_1$                 | Address valid to DIOR-/DIOW- setup (min)                                    | 70              | 50              | 30              | 30              | 25              |      |
| $t_2$                 | DIOR-/DIOW- (min)                                                           | 165             | 125             | 100             | 80              | 70              | 1    |
| $t_{2i}$              | DIOR-/DIOW- recovery time (min)                                             | -               | -               | -               | 70              | 25              | 1    |
| $t_3$                 | DIOW- data setup (min)                                                      | 60              | 45              | 30              | 30              | 20              |      |
| $t_4$                 | DIOW- data hold (min)                                                       | 30              | 20              | 15              | 10              | 10              |      |
| $t_5$                 | DIOR- data setup (min)                                                      | 50              | 35              | 20              | 20              | 20              |      |
| $t_6$                 | DIOR- data hold (min)                                                       | 5               | 5               | 5               | 5               | 5               |      |
| $t_{6Z}$              | DIOR- data tristate (max)                                                   | 30              | 30              | 30              | 30              | 30              | 2    |
| $t_9$                 | DIOR-/DIOW- to address valid hold (min)                                     | 20              | 15              | 10              | 10              | 10              |      |
| $t_{RD}$              | Read Data Valid to IORDY active (if IORDY initially low after $t_A$ ) (min) | 0               | 0               | 0               | 0               | 0               |      |
| $t_A$                 | IORDY Setup time                                                            | 35              | 35              | 35              | 35              | 35              | 3    |
| $t_B$                 | IORDY Pulse Width (max)                                                     | 1250            | 1250            | 1250            | 1250            | 1250            |      |
| $t_C$                 | IORDY assertion to release (max)                                            | 5               | 5               | 5               | 5               | 5               |      |

**NOTES –**

- $t_0$  is the minimum total cycle time,  $t_2$  is the minimum DIOR-/DIOW- assertion time, and  $t_{2i}$  is the minimum DIOR-/DIOW- negation time. A host implementation shall lengthen  $t_2$  and/or  $t_{2i}$  to ensure that  $t_0$  is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
- This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.
- The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the  $t_A$  after the activation of DIOR- or DIOW-, then  $t_5$  shall be met and  $t_{RD}$  is not applicable. If the device is driving IORDY negated at the time  $t_A$  after the activation of DIOR- or DIOW-, then  $t_{RD}$  shall be met and  $t_5$  is not applicable.
- Mode may be selected at the highest mode for the device if CS(1:0) and AD(2:0) do not change between read or write cycles or selected at the highest mode supported by the slowest device if CS(1:0) or AD(2:0) do change between read or write cycles.

## 11.2 Multi Word DMA

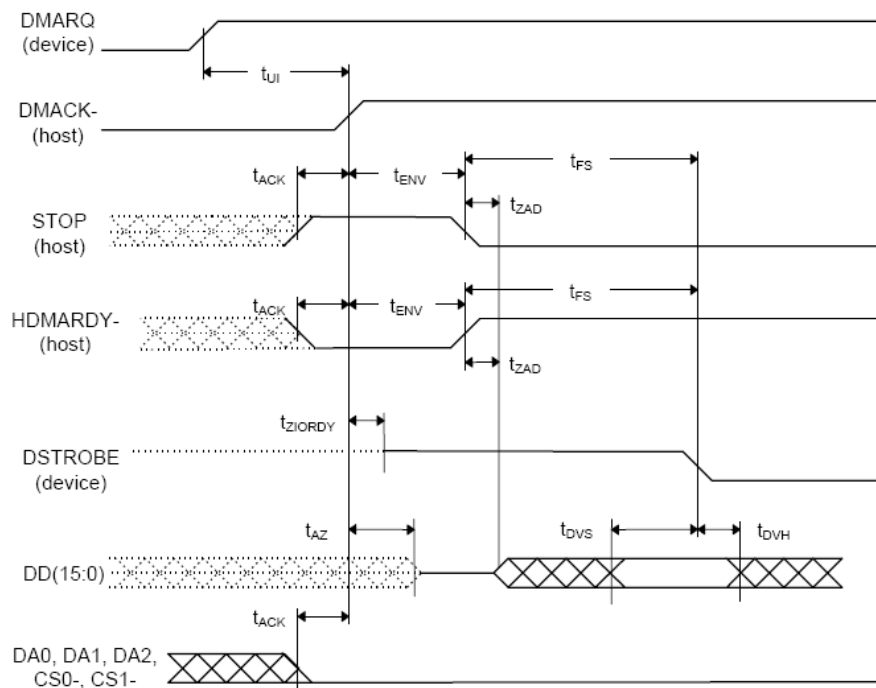


NOTE – The host shall not assert DMACK- or negate both CS0 and CS1 until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK- or the negation of both CS0 and CS1 is not defined.

| Multiword DMA timing parameters                                                                                                                                                                                                                                                                                          |                                           | Mode 0<br>(ns) | Mode 1<br>(ns) | Mode2<br>(ns) | Note     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|----------------|----------------|---------------|----------|
| $t_0$                                                                                                                                                                                                                                                                                                                    | Cycle time<br>(min)                       | 480            | 150            | 120           | See note |
| $t_D$                                                                                                                                                                                                                                                                                                                    | DIOR-/DIOW- asserted pulse width<br>(min) | 215            | 80             | 70            | See note |
| $t_E$                                                                                                                                                                                                                                                                                                                    | DIOR- data access<br>(max)                | 150            | 60             | 50            |          |
| $t_F$                                                                                                                                                                                                                                                                                                                    | DIOR- data hold<br>(min)                  | 5              | 5              | 5             |          |
| $t_G$                                                                                                                                                                                                                                                                                                                    | DIOR-/DIOW- data setup<br>(min)           | 100            | 30             | 20            |          |
| $t_H$                                                                                                                                                                                                                                                                                                                    | DIOW- data hold<br>(min)                  | 20             | 15             | 10            |          |
| $t_I$                                                                                                                                                                                                                                                                                                                    | DMACK to DIOR-/DIOW- setup<br>(min)       | 0              | 0              | 0             |          |
| $t_J$                                                                                                                                                                                                                                                                                                                    | DIOR-/DIOW- to DMACK hold<br>(min)        | 20             | 5              | 5             |          |
| $t_{KR}$                                                                                                                                                                                                                                                                                                                 | DIOR- negated pulse width<br>(min)        | 50             | 50             | 25            | See note |
| $t_{KW}$                                                                                                                                                                                                                                                                                                                 | DIOW- negated pulse width<br>(min)        | 215            | 50             | 25            | See note |
| $t_{LR}$                                                                                                                                                                                                                                                                                                                 | DIOR- to DMACK delay<br>(max)             | 120            | 40             | 35            |          |
| $t_{LW}$                                                                                                                                                                                                                                                                                                                 | DIOW- to DMACK delay<br>(max)             | 40             | 40             | 35            |          |
| $t_M$                                                                                                                                                                                                                                                                                                                    | CS(1:0) valid to DIOR-/DIOW-<br>(min)     | 50             | 30             | 25            |          |
| $t_N$                                                                                                                                                                                                                                                                                                                    | CS(1:0) hold<br>(min)                     | 15             | 10             | 10            |          |
| $t_Z$                                                                                                                                                                                                                                                                                                                    | DMACK- to read data released<br>(max)     | 20             | 25             | 25            |          |
| Notes- $t_0$ is the minimum total cycle. $t_D$ is the minimum DIOR-/DIOW- assertion time, and $t_K$ ( $t_{KR}$ or $t_{KW}$ , as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen $t_D$ and/or $t_K$ to ensure that $t_0$ is equal to the value reported in the devices IDENTIFY DEVICE data. |                                           |                |                |               |          |

## 11.3 Ultra DMA

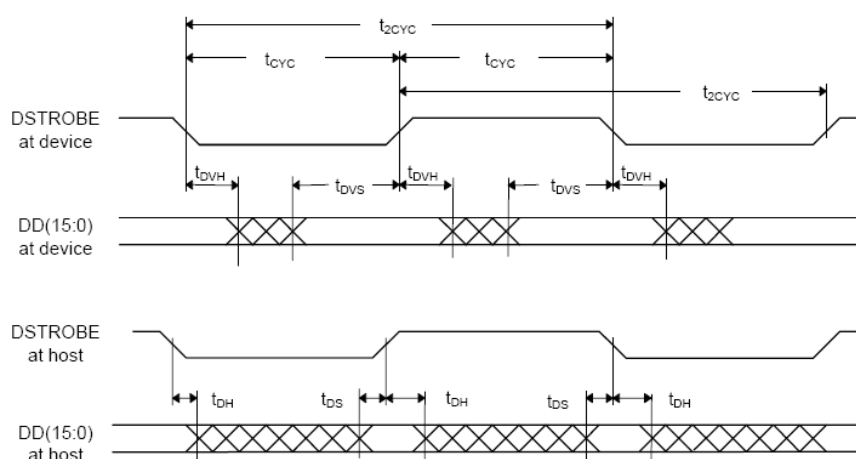
### [Initiating an Ultra DMA data-in burst]



#### NOTES –

- 1 See 9.13.1 Initiating an Ultra DMA data-in burst.
- 2 The definitions for the DIOW::STOP, DIOR::HDMARDY::HSTROBE and IORDY::DDMARDY::DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

### [Sustained Ultra DMA data-in burst]



#### NOTES –

- 1 See 9.13.2 The data-in transfer.
- 2 DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

DMARQ (device)

DMACK- (host)

STOP (host)

HDMARDY- (host)

DSTROBE (device)

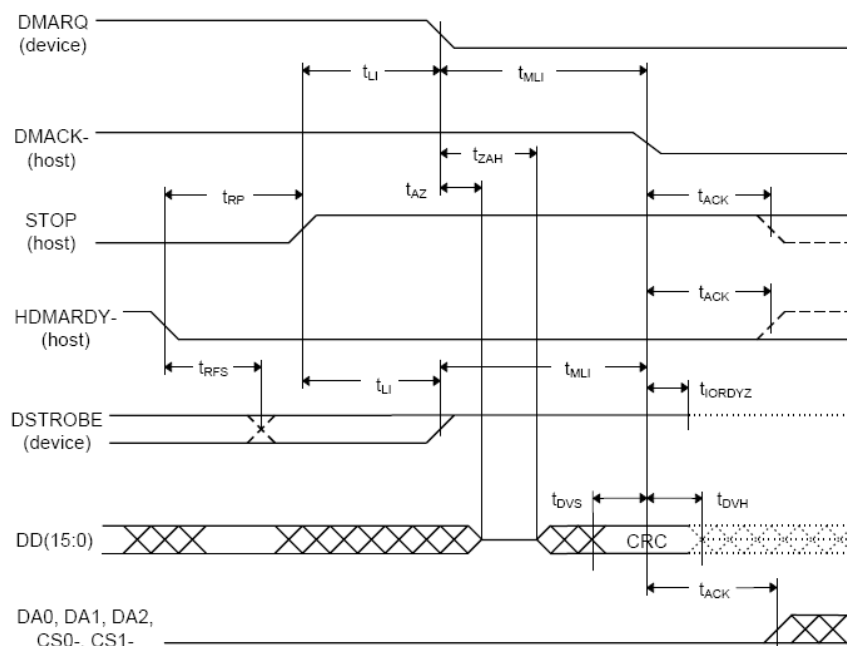
DD(15:0) (device)

$t_{RP}$

$t_{RFS}$

2 The definitions for the DIOW-STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

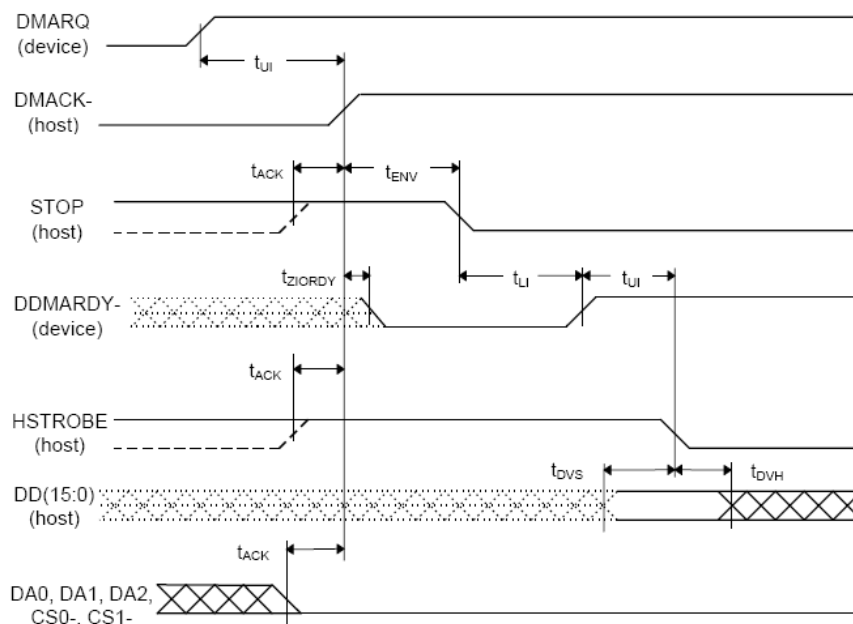
[Host terminating an Ultra DMA data-in burst]



NOTES –

- 1 See 9.13.4.2 Host pausing an Ultra DMA data-in burst.
- 2 The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

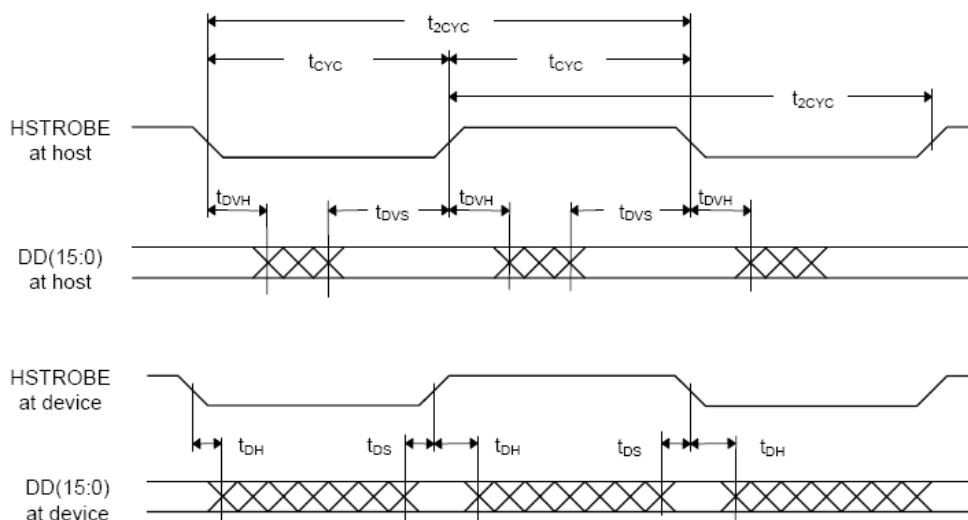
[Initiating an Ultra DMA data-out burst]



NOTES –

- 1 See 9.14.1 Initiating an Ultra DMA data-out burst.
- 2 The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE and DIOR-:HDMARDY-:HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

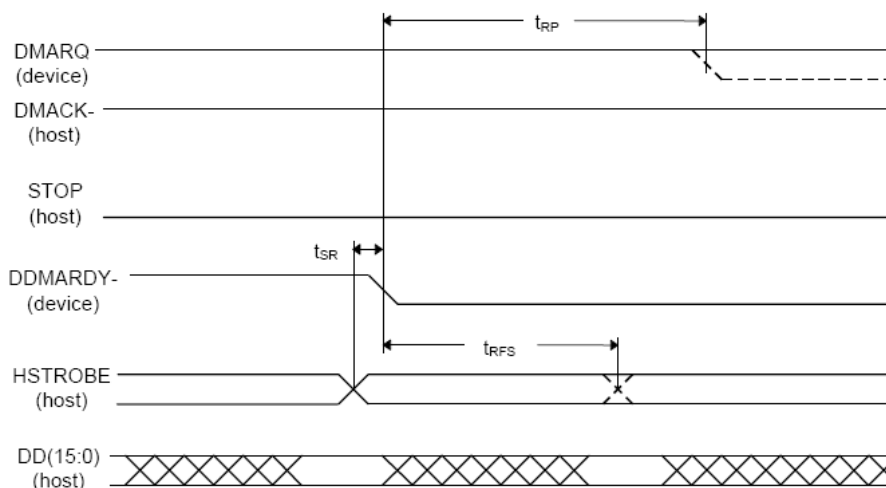
[Sustained Ultra DMA data-out burst]



NOTES –

- 1 See 9.14.2 The data out-transfer.
- 2 DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

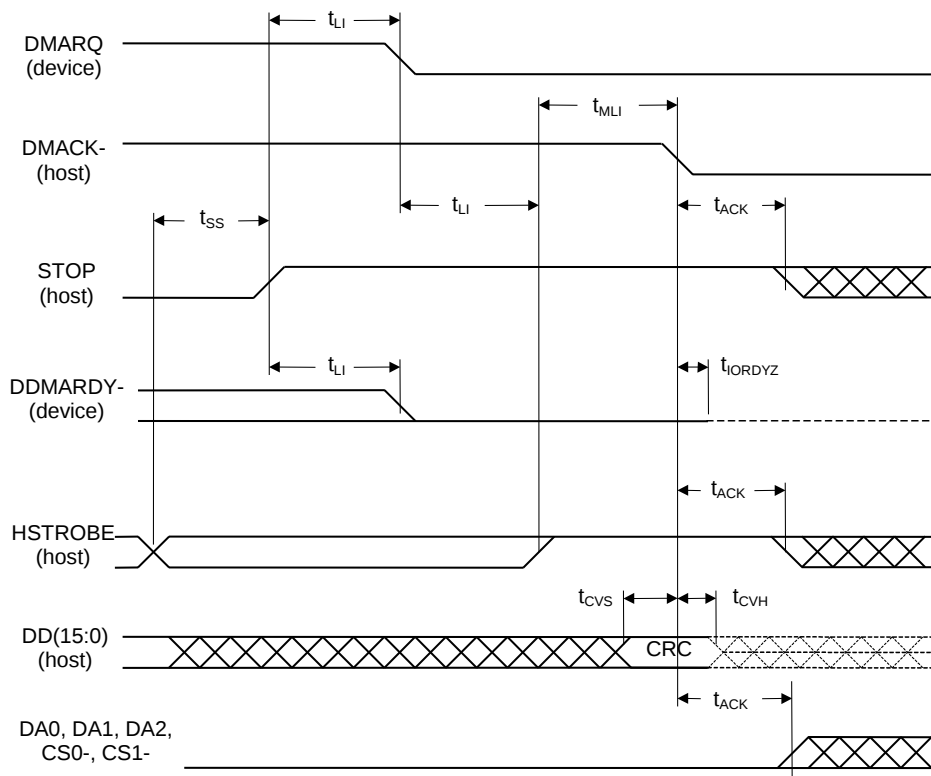
[Device pausing an Ultra DMA data-out burst]



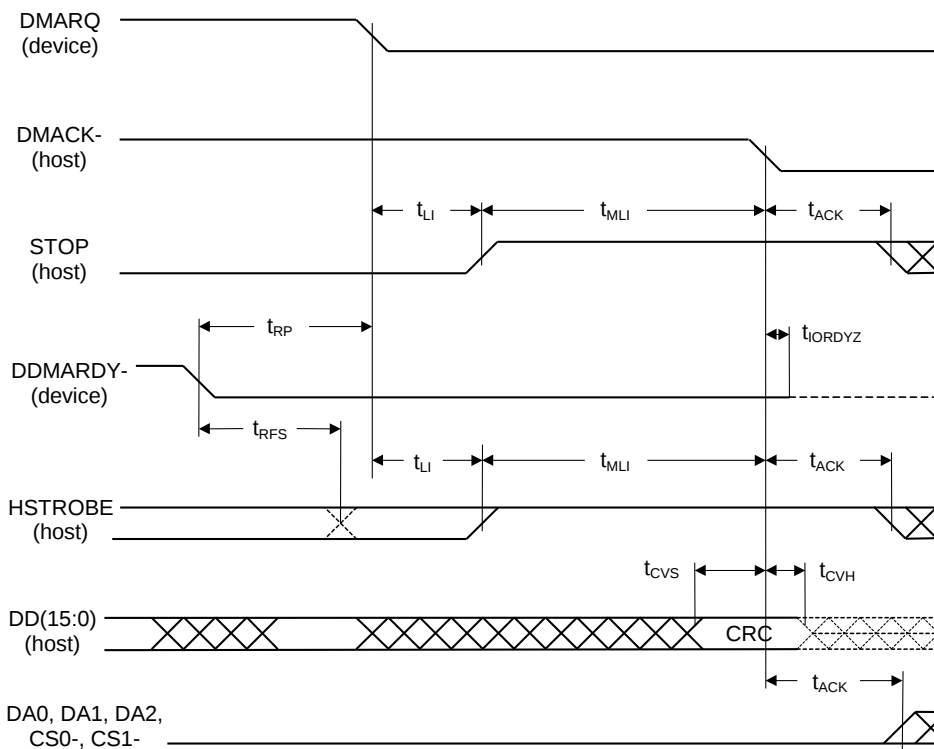
NOTES –

- 1 See 9.14.3.2 Device pausing an Ultra DMA data-out burst.
- 2 The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than  $t_{RP}$  after DDMARDY- is negated.
- 3 If the  $t_{SR}$  timing is not satisfied, the device may receive zero, one, or two more data words from the host.

[Host terminating an Ultra DMA data-out burst]



[Device terminating an Ultra DMA data-out burst]



**[Ultra DMA data burst timing requirements]**

| Name                 | Mode 0 (ns) |     | Mode 1 (ns) |     | Mode 2 (ns) |     | Mode 3 (ns) |     | Mode 4 (ns) |     | Mode 5 (ns) |     | Measurement location |
|----------------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|----------------------|
|                      | Min         | Max | Min         | Max | Min         | Max | Min         | Max | Min         | Max | Min         | Max |                      |
| t <sub>2CYCTYP</sub> | 240         |     | 160         |     | 120         |     | 90          |     | 60          |     | 40          |     | Sender               |
| t <sub>CYC</sub>     | 112         |     | 73          |     | 54          |     | 39          |     | 25          |     | 16.8        |     | Note 3               |
| t <sub>2CYC</sub>    | 230         |     | 153         |     | 115         |     | 86          |     | 57          |     | 38          |     | Sender               |
| t <sub>DS</sub>      | 15.0        |     | 10.0        |     | 7.0         |     | 7.0         |     | 5.0         |     | 4.0         |     | Recipient            |
| t <sub>DH</sub>      | 5.0         |     | 5.0         |     | 5.0         |     | 5.0         |     | 5.0         |     | 4.6         |     | Recipient            |
| t <sub>DVS</sub>     | 70.0        |     | 48.0        |     | 31.0        |     | 20.0        |     | 6.7         |     | 4.8         |     | Sender               |
| t <sub>DVH</sub>     | 6.2         |     | 6.2         |     | 6.2         |     | 6.2         |     | 6.2         |     | 4.8         |     | Sender               |
| t <sub>CS</sub>      | 15.0        |     | 10.0        |     | 7.0         |     | 7.0         |     | 5.0         |     | 5.0         |     | Device               |
| t <sub>CH</sub>      | 5.0         |     | 5.0         |     | 5.0         |     | 5.0         |     | 5.0         |     | 5.0         |     | Device               |
| t <sub>CVS</sub>     | 70.0        |     | 48.0        |     | 31.0        |     | 20.0        |     | 6.7         |     | 10.0        |     | Host                 |
| t <sub>CVH</sub>     | 6.2         |     | 6.2         |     | 6.2         |     | 6.2         |     | 6.2         |     | 10.0        |     | Host                 |
| t <sub>ZFS</sub>     | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | 35          |     | Device               |
| t <sub>DZFS</sub>    | 70.0        |     | 48.0        |     | 31.0        |     | 20.0        |     | 6.7         |     | 25          |     | Sender               |
| t <sub>FS</sub>      |             | 230 |             | 200 |             | 170 |             | 130 |             | 120 |             | 90  | Device               |
| t <sub>LI</sub>      | 0           | 150 | 0           | 150 | 0           | 150 | 0           | 100 | 0           | 100 | 0           | 75  | Note 4               |
| t <sub>MLI</sub>     | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | Host                 |
| t <sub>UI</sub>      | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | Host                 |
| t <sub>AZ</sub>      |             | 10  |             | 10  |             | 10  |             | 10  |             | 10  |             | 10  | Note 5               |
| t <sub>ZA</sub>      | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | Host                 |
| t <sub>ZAD</sub>     | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | Device               |
| t <sub>ENV</sub>     | 20          | 70  | 20          | 70  | 20          | 70  | 20          | 55  | 20          | 55  | 20          | 50  | Host                 |
| t <sub>RFS</sub>     |             | 75  |             | 70  |             | 60  |             | 60  |             | 60  |             | 50  | Sender               |
| t <sub>RP</sub>      | 160         |     | 125         |     | 100         |     | 100         |     | 100         |     | 85          |     | Recipient            |
| t <sub>IORDYZ</sub>  |             | 20  |             | 20  |             | 20  |             | 20  |             | 20  |             | 20  | Device               |
| t <sub>ZIORDY</sub>  | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | 0           |     | Device               |
| t <sub>ACK</sub>     | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | 20          |     | Host                 |
| t <sub>SS</sub>      | 50          |     | 50          |     | 50          |     | 50          |     | 50          |     | 50          |     | Sender               |

**NOTES –**

- 1 All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
- 2 All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t<sub>RFS</sub>, both STROBE and DMARDY-transitions are measured at the sender connector.
- 3 The parameter t<sub>CYC</sub> shall be measured at the recipient's connector farthest from the sender.
- 4 The parameter t<sub>LI</sub> shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
- 5 The parameter t<sub>AZ</sub> shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

**[Ultra DMA data burst timing descriptions]**

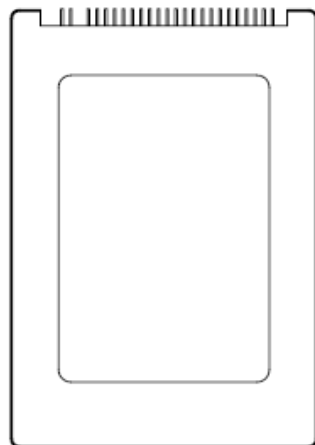
| Name          | Comment                                                                                                                                  |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{2CYCTYP}$ | Typical sustained average two cycle time                                                                                                 |
| $t_{CYC}$     | Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)                                                 |
| $t_{2CYC}$    | Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)  |
| $t_{DS}$      | Data setup time at recipient (from data valid until STROBE edge) (See note 2,5)                                                          |
| $t_{DH}$      | Data hold time at recipient (from STROBE edge until data may become invalid) (See note 2,5)                                              |
| $t_{DVS}$     | Data valid setup time at sender (from data valid until STROBE edge) (See note 3)                                                         |
| $t_{DVH}$     | Data valid hold time at sender (from STROBE edge until data may become invalid) (See note 3)                                             |
| $t_{CS}$      | CRC word setup time at device (See note 2)                                                                                               |
| $t_{CH}$      | CRC word hold time device (See note 2)                                                                                                   |
| $t_{CVS}$     | CRC word valid setup time at host (from CRC valid until DMACK- negation) (See note 3)                                                    |
| $t_{CVH}$     | CRC word valid hold time at sender (from DMACK- negation until CRC may become invalid) (See note 3)                                      |
| $t_{ZFS}$     | Time from STROBE output released-to-driving until the first transition of critical timing.                                               |
| $t_{DZFS}$    | Time from data output released-to-driving until the first transition of critical timing.                                                 |
| $t_{FS}$      | First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)                                                  |
| $t_{LI}$      | Limited interlock time (See note 1)                                                                                                      |
| $t_{MLI}$     | Interlock time with minimum (See note 1)                                                                                                 |
| $t_{UI}$      | Unlimited interlock time (See note 1)                                                                                                    |
| $t_{AZ}$      | Maximum time allowed for output drivers to release (from asserted or negated)                                                            |
| $t_{ZAH}$     | Minimum delay time required for output                                                                                                   |
| $t_{ZAD}$     | drivers to assert or negate (from released)                                                                                              |
| $t_{ENV}$     | Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from DMACK to STOP during data out burst initiation) |
| $t_{RFS}$     | Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)                                           |
| $t_{RP}$      | Ready-to-pause time (that recipient shall wait to pause after negating DMARDY-)                                                          |
| $t_{IORDYZ}$  | Maximum time before releasing IORDY                                                                                                      |
| $t_{ZIORDY}$  | Minimum time before driving IORDY (See note 4)                                                                                           |
| $t_{ACK}$     | Setup and hold times for DMACK- (before assertion or negation)                                                                           |
| $t_{SS}$      | Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)                                         |

**NOTES –**

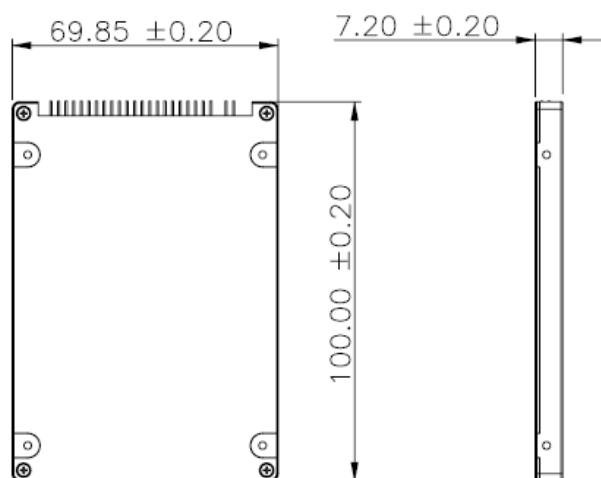
- 1 The parameters  $t_{UI}$ ,  $t_{MLI}$ , and  $t_{LI}$  indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding.  $t_{UI}$  is an unlimited interlock that has no maximum time value.  $t_{MLI}$  is a limited time-out that has a defined minimum.  $t_{LI}$  is a limited time-out that has a defined maximum.
- 2 80-conductor cabling shall be required in order to meet setup ( $t_{DS}$ ,  $t_{CS}$ ) and hold ( $t_{DH}$ ,  $t_{CH}$ ) times in modes greater than 2.
- 3 Timing for  $t_{DVS}$ ,  $t_{DVH}$ ,  $t_{CVS}$  and  $t_{CVH}$  shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
- 4 For all modes the parameter  $t_{ZIORDY}$  may be greater than  $t_{ENV}$  due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
- 5 The parameters  $t_{DS}$ ,  $t_{DH}$  for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for  $t_{DS}$  and  $t_{DH}$  for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

## 12. Physical Dimension

2.5" PATA SSD (Unit: mm)



(Top View)



(Bottom View)

## Appendix: Part Number Table

| Product                                                  | Advantech PN       |
|----------------------------------------------------------|--------------------|
| Advantech SQFlash 2.5" PATA SSD 4G SLC, DMA (0~70°C)     | SQF-P25S4-4G-CTE   |
| Advantech SQFlash 2.5" PATA SSD 8G SLC, DMA (0~70°C)     | SQF-P25S4-8G-CTE   |
| Advantech SQFlash 2.5" PATA SSD 16G SLC, DMA (0~70°C)    | SQF-P25S4-16G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 32G SLC, DMA (0~70°C)    | SQF-P25S4-32G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 64G SLC, DMA (0~70°C)    | SQF-P25S4-64G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 4G SLC, DMA (-40~85°C)   | SQF-P25S4-4G-ETE   |
| Advantech SQFlash 2.5" PATA SSD 8G SLC, DMA (-40~85°C)   | SQF-P25S4-8G-ETE   |
| Advantech SQFlash 2.5" PATA SSD 16G SLC, DMA (-40~85°C)  | SQF-P25S4-16G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 32G SLC, DMA (-40~85°C)  | SQF-P25S4-32G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 64G SLC, DMA (-40~85°C)  | SQF-P25S4-64G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 8G MLC, DMA (0~70°C)     | SQF-P25M4-8G-CTE   |
| Advantech SQFlash 2.5" PATA SSD 16G MLC, DMA (0~70°C)    | SQF-P25M4-16G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 32G MLC, DMA (0~70°C)    | SQF-P25M4-32G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 64G MLC, DMA (0~70°C)    | SQF-P25M4-64G-CTE  |
| Advantech SQFlash 2.5" PATA SSD 128G MLC, DMA (0~70°C)   | SQF-P25M4-128G-CTE |
| Advantech SQFlash 2.5" PATA SSD 8G MLC, DMA (-40~85°C)   | SQF-P25M4-8G-ETE   |
| Advantech SQFlash 2.5" PATA SSD 16G MLC, DMA (-40~85°C)  | SQF-P25M4-16G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 32G MLC, DMA (-40~85°C)  | SQF-P25M4-32G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 64G MLC, DMA (-40~85°C)  | SQF-P25M4-64G-ETE  |
| Advantech SQFlash 2.5" PATA SSD 128G MLC, DMA (-40~85°C) | SQF-P25M4-128G-ETE |