PI3V724

1 to 2 VGA Demux

Features

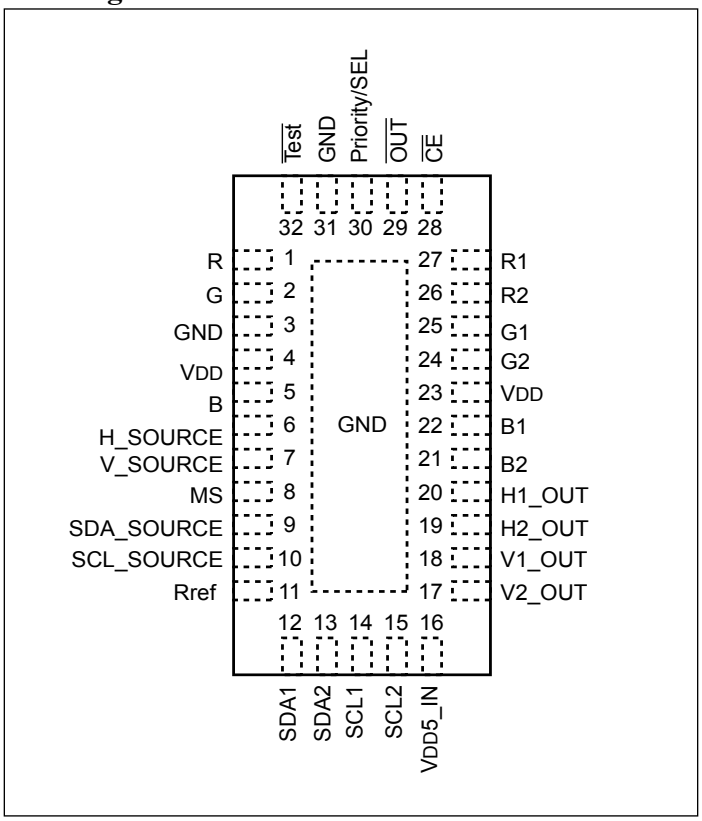
- Full VGA 1:2 demux with VSIS compliance
  - R, G, B, Hsync, Vsync, DDC data, and DDC clk channels are switched
- Integrated monitor detection circuit allows Automatic or manual control
- Generates hot plug output signal to inform system when monitor is present or not
- Dual Power Supply, 3.3V and 5V
- Integrated DDC level shifter from 5V to 3.3V(bi-directional)
- Integrated 5V H/V output buffer with +/-24mA drive
- ESD tolerance on video I/O pins up to +/-4kV contact per IEC61000-4-2 specification
- -3dB BW of 1.7GHz (typ)
- Low Xtalk, (-38dB typ)
- Low and Flat ON-STATE resistance (Ron = 4-Ohm, Ron(Flat) = 0.5ohm, typ)
- Low input/output capacitance (Con = 5.6pF, typ)
- Packaging (Pb-free and Green):
  - 32-contact TQFN (ZL)

Description

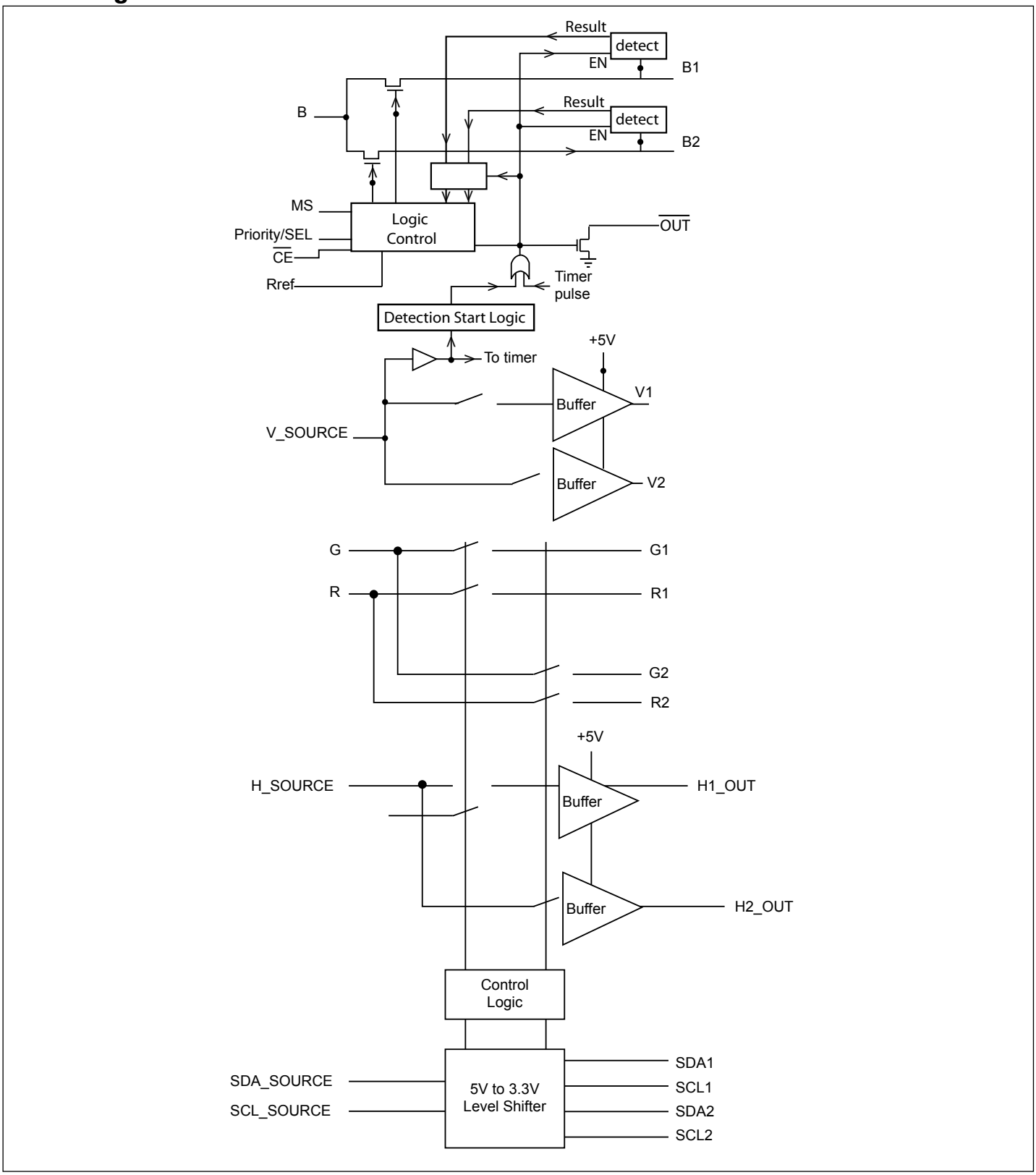
Pericom's PI3V724 is a 7-channel video mux/demux used to switch between multiple VGA sources or end points. In a notebook application where analog video signals are found in both the notebook and the dock, a switch solution is required to switch between the two video port locations. With the high bandwidth of ~1.7GHz, the signal integrity will remain strong even through the long FR4 trace between the notebook and the docking station. In addition to high signal performance, the video signals are also protected against high ESD with integrated diodes to VDD and GND that will support up to +/-4kV contact ESD protection.

In addition to switching, the product also integrates a monitor detection feature. The monitor detection feature works independently on each of the two outputs and allows automatic switching as well as a self generated HPD signal that lets the system know when a monitor is connected or disconnected.

Pin Diagram



Block Diagram



Pinout Table

Pin #	Name	Type	Description
1	R	I/O	Red signal from source
2	G	I/O	Green signal from source
3	GND	Ground	Ground
4	Vdd	Power	3.3V Power Supply
5	B	I/O	Blue signal from source
6	H_Source	I	Horizontal Synchronous signal from source. Internal 300Kohm pull-down
7	V_Source	I	Vertical Synchronous signal from source. Internal 300Kohm pull-down
8	MS	I	Mode Select (switch between auto switch vs. manual switch). OUTx pins work regardless of MS pin status. Internal pull down.
9	SDA_Source	I/O	DDC data signal from source
10	SCL_Source	I/O	DDC clock signal from source
11	Rref	I	Connect external resistor to ground to determine which application scheme best matches your design. For actual R values, please see page 6
12	SDA1	I/O	DDC data signal from VGA connector 1
13	SDA2	I/O	DDC data signal from VGA connector 2
14	SCL1	I/O	DDC clock signal from VGA connector 1
15	SCL2	I/O	DDC clock signal from VGA connector 2
16	Vdd5_IN	I (Power)	5V input power supply
17	V2_out	O	Buffered, vertical synch signal output for VGA connector #2
18	V1_out	O	Buffered vertical synchronous signal driving VGA connector #1
19	H2_out	O	Buffered, horizontal synch signal output for VGA connector #2
20	H1_out	O	Buffered horizontal synchronous signal driving VGA connector #1
21	B2	I/O	Un-buffered, Blue signal driving VGA connector 2
22	B1	I/O	Un-buffered, Blue signal driving VGA connector 1
23	Vdd	Power	3.3V Power Supply
24	G2	I/O	Un-buffered, Green signal driving VGA connector 2
25	G1	I/O	Un-buffered, Green signal driving VGA connector 1
26	R2	I/O	Un-buffered, Red signal driving VGA connector 2
27	R1	I/O	Un-buffered, Red signal driving VGA connector 1
28	$\overline{CE}$	I	Chip enable input. If signal is LOW, then chip is fully functional. If signal is HIGH, then IC is powered down and all I/O's are hi-z
29	$\overline{OUT}$	O	open drain output describing external monitor status. If connected, OUT is LOW, if not connected, OUT is hi-z. OUT will only provide the status of the CHOSEN port. Chosen port can be determined based on manual switching or automatic switching (please see truth table for more information on how to configure into auto mode or manual mode)
30	Priority/SEL	I	Output Port selection or output port priority depending on MS pin status
31	GND	Ground	Ground
32	$\overline{Test}$	I	please tie high or leave floating for normal operation. internal pull-up

Truth Table

CE/	MS (Internal pull-down)	Switching Mode	Pin 30 Role	SEL	Priority	Result
0	0	Automatic Switching	Priority Pin	N/A	0	Port1 has priority
0	0	Automatic Switching	Priority Pin	N/A	1	Port 2 has priority
0	1	Manual Switching	SELpin	0	N/A	Port 1 is active
0	1	Manual Switching	SELpin	1	N/A	Port 2 is active
1	x	N/A	N/A	x	x	all I/O's hi-z

Automatic switching scheme

As external monitors are properly detected, the PI3V724 can support automatic switching.

If only one monitor is connected, then the port is easily chosen regardless of what pin 30 (priority) pin status is.

Port selection (only one monitor is present)

At power on, MS pin (pin 31) is checked to determine if auto switching is enabled or not (to enable, MS needs to be LOW). Next the part will look to see if external monitors are connected or not. If only one monitor is connected, the PI3V724 will automatically enable the signal path to drive the connected the monitor. OUT pin will then be pulled LOW.

Port selection (both monitors are present)

At power on, MS pin (pin 31) is checked to determine if auto switching is enabled or not (to enable, MS needs to be LOW). Next the part will look to see if external monitors are connected or not. If only both monitors are connected, the PI3V724 will then check the priority pin (pin 30). If pin 30 is LOW, then port 1 will have priority and therefore will be activated. However, if pin 30 is HIGH, then port 2 will have priority and therefore port 2 will be enabled.

State Machine Reset Procedure

- If the monitor from chosen port is disconnected, the state machine is reset (to determine chosen port, see above).
- If MS pin status changes, state machine is reset
- If CE/ pin goes high then low again, state machine is reset
- If Vdd goes low and then high again, state machine resets

Application Note

Introduction

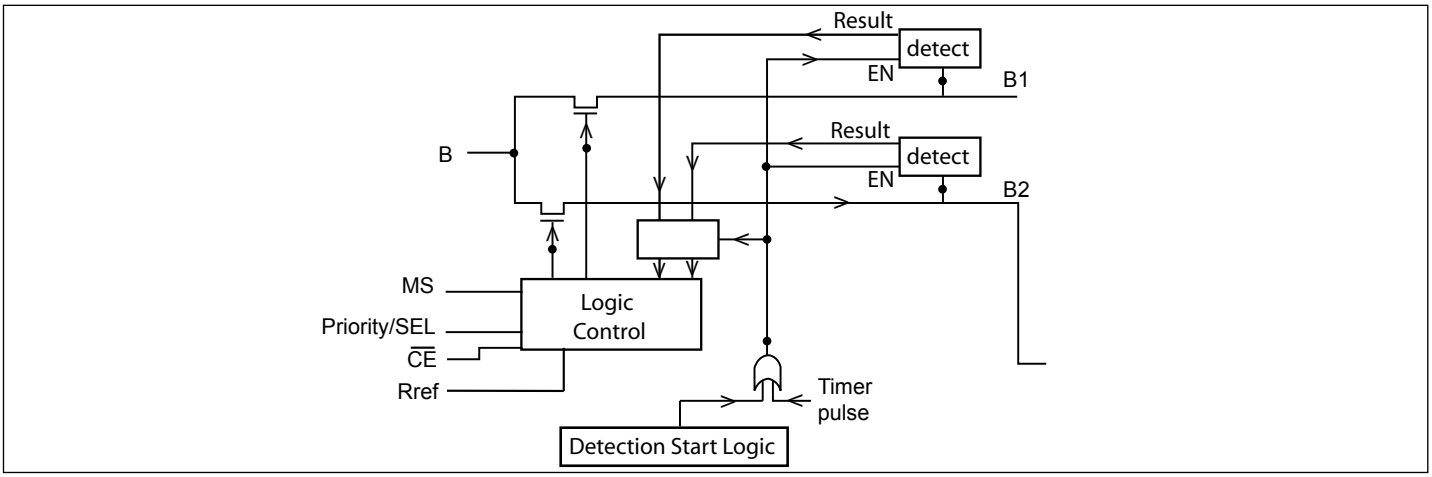
PI3V724 is a full VGA de-mux switch with integrated monitor detection circuit. Port switching can be selected manually or automatically to offer more flexibility to users.

Automatic Monitor Detection

If MS pin (pin 8) is set to low or float, PI3V724 enters auto switch mode. When external monitor(s) is/are properly detected, PI3V724 can support automatic switching.

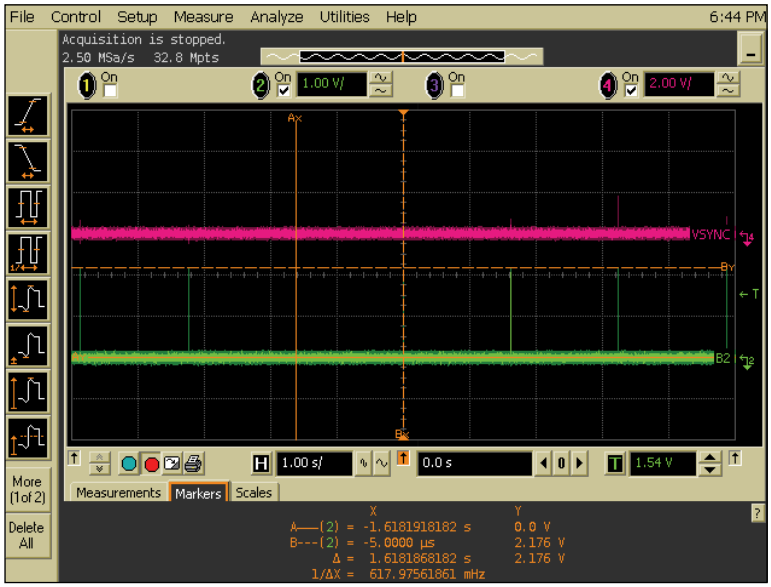
Detection Pulse

When auto switch mode is selected via MS pin, PI3V724 sends a detection pulse through BLUE signal to check if any termination is present. Once a monitor is attached, its termination is determined. PI3V724 will switch to the port with such termination accordingly.

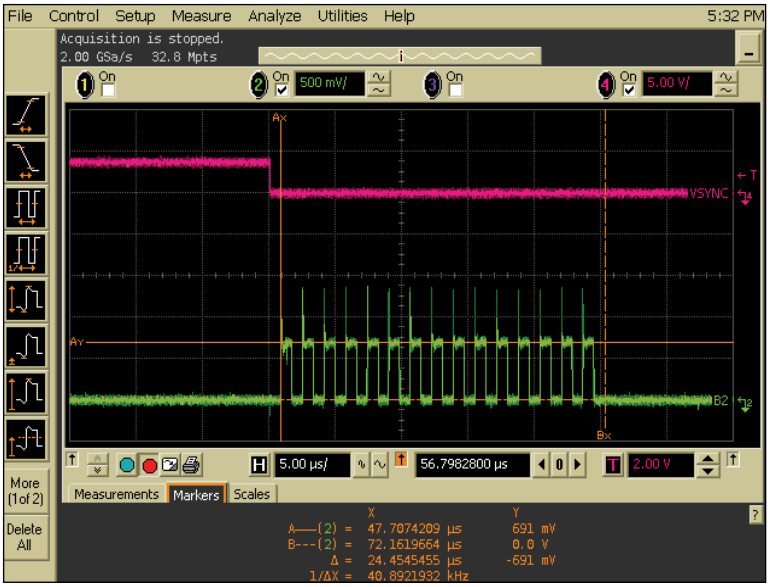


PI3V724 Detection Block Diagram

A detection pulse is sent by PI3V724 every 1.6 seconds when source or sink is not attached. Furthermore, the detection pulse is sent immediately after sensing Vsync pulse. The detection pulse is of the width within 30us and the voltage level around 0.7V.

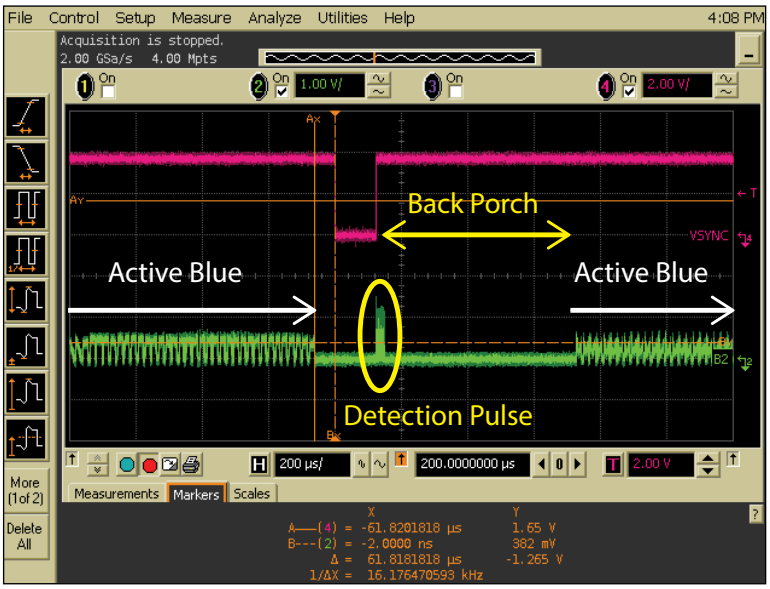


PI3V724 Detection Pulse on Blue B2 without Source or Sink Device

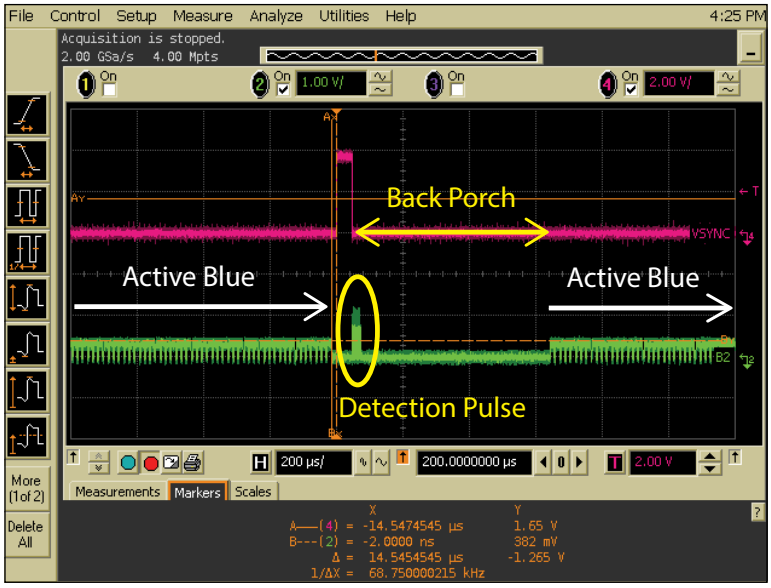


PI3V724 Detection Pulse on Blue B2 Immediately after Vsync Pulse

The detection pulse is generated by PI3V724 within the back porch period, which is before active BLUE video is delivered.



PI3V724 Vsync Pulse (with Negative Polarity) vs. Blue B2 at 1024x768@60Hz



PI3V724 Vsync Pulse (with Positive Polarity) vs. Blue B2 at 1280x1024@60Hz

Port Selection

When PI3V724 is powered up, MS pin (pin 8) is checked to determine if auto switching is enabled or not. If MS pin is set to low, PI3V724 will determine if any monitor is attached. If only one monitor is connected, PI3V724 will automatically en¬able the signal path to the attached monitor. /OUT pin (pin 29) will then be pulled low to indicate the presence of a monitor at the chosen port. If two monitors are attached to both output ports, PI3V724 will check the Priority pin (pin 30). If Priority pin is set to low, output port 1 will be prioritized and thus active. On the other hand, if Priority pin is high, output port 2 will be prioritized and thus enabled. / OUT pin will then be pulled low.

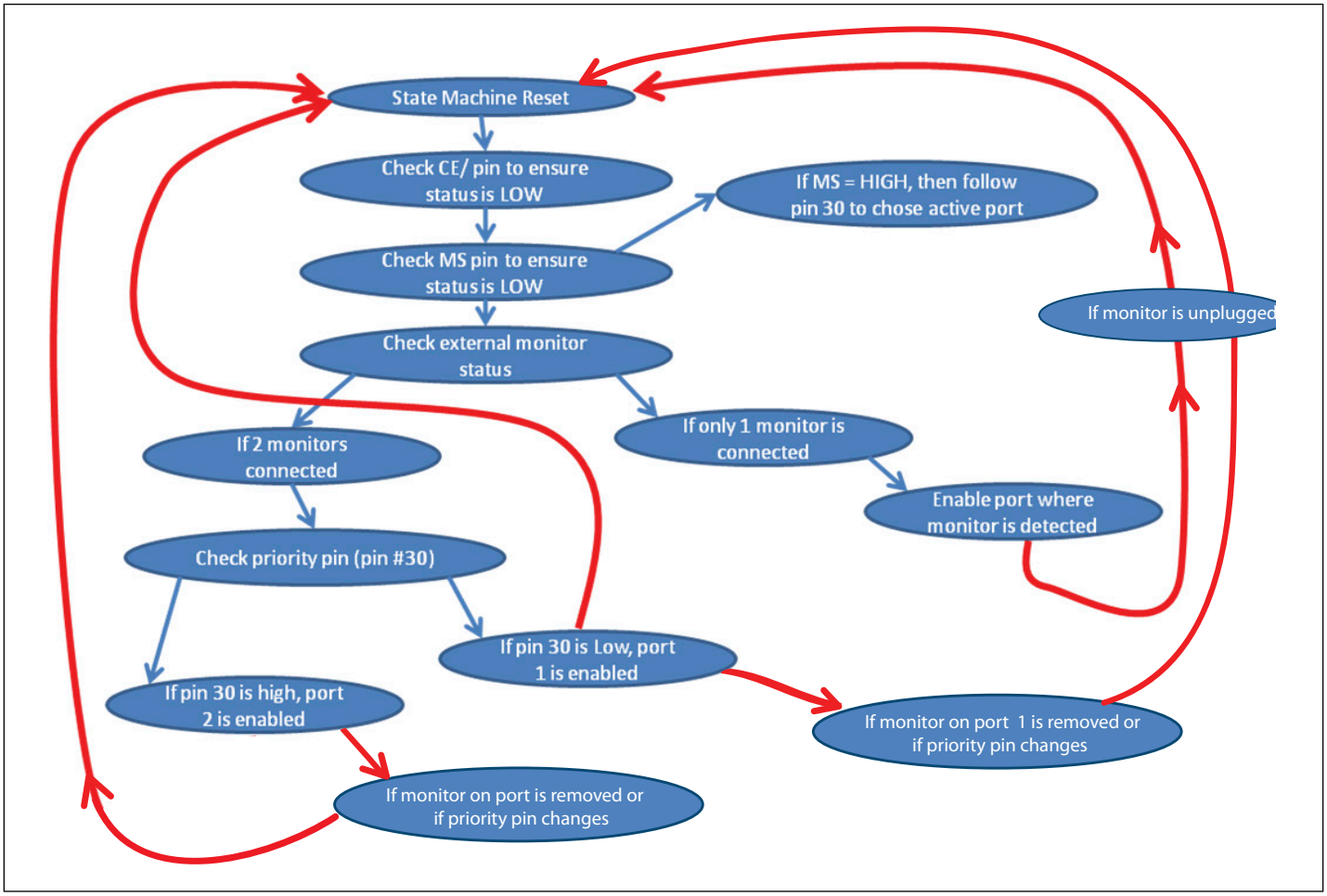
Application Scheme

With proper reference resistor assembled to Rref pin (pin 11), monitors with various application schemes can be determined automatically.

Rref External Value Truth Table

Rref	Application Case supported (see page 8 for drawings)
330Kohm	Case_150//75
250Kohm	Case_75//75
500K	Case_75

State Machine



Output Pin Behavior (Pin 29) with Auto Switch Enabled

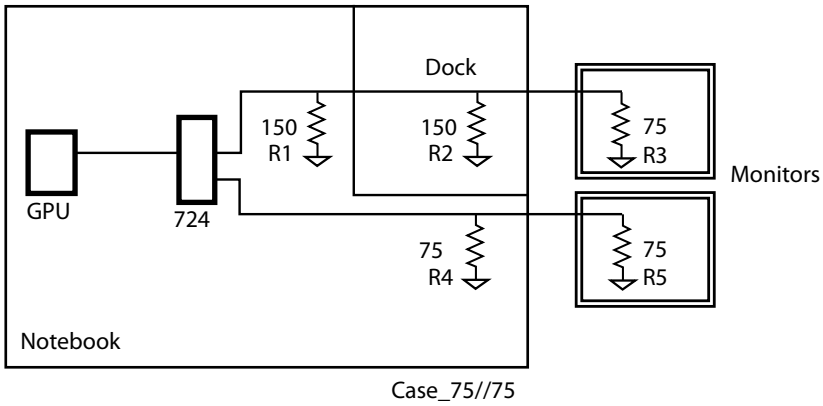
MS	Priority (0 = port 1) (1 = port 2)	Port 1 monitor Status 0 = Unplug, 1 = plug	Port 2 monitor Status 0 = Unplug, 1 = plug	Port 1 Path	Port 2 Path	Out Status
0	0	0	0	ON	OFF	Hi Z
0	0	0	1	OFF	ON	Low
0	0	1	0	ON	OFF	Low
0	0	1	1	ON	OFF	Low
0	1	0	0	OFF	ON	Hi Z
0	1	0	1	OFF	ON	Low
0	1	1	0	ON	OFF	Low
0	1	1	1	OFF	ON	Low

Output Pin Behavior (Pin 29) with Manual Switching Mode Enabled

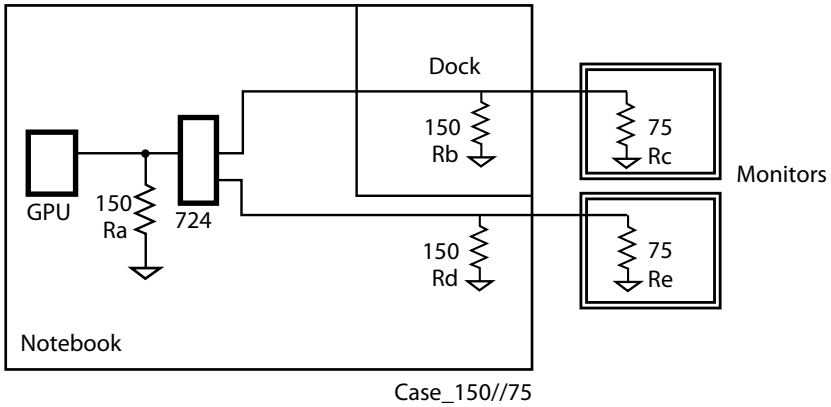
MS	Priority (0 = port 1) (1 = port 2)	Port 1 monitor Status 0 = Unplug, 1 = plug	Port 2 monitor Status 0 = Unplug, 1 = plug	Port 1 Path	Port 2 Path	Out Status
1	0	0	x	ON	OFF	Hi Z
1	0	1	x	ON	OFF	Low
1	1	x	0	OFF	ON	Hi Z
1	1	x	1	OFF	ON	Low

Rref (Pin 11) external value Truth Table

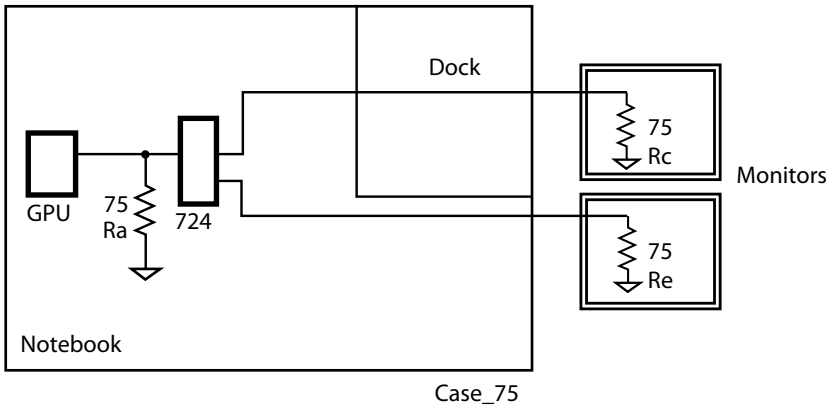
Rref	Application Case supported (see page 8 for drawings)
330Kohm	Case_150//75
250Kohm	Case_75//75
500K	Case_75



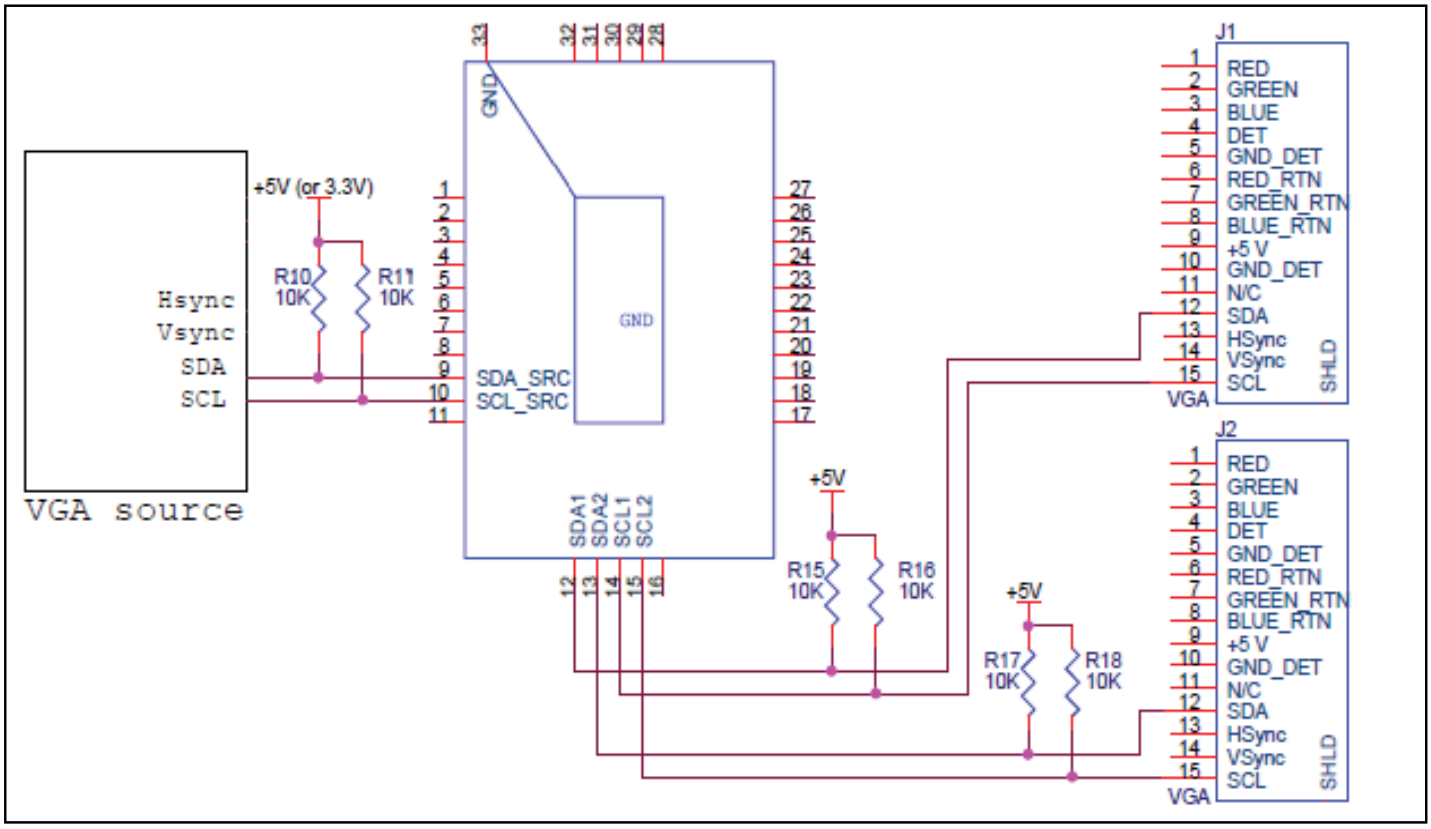
PI3V724 Application Drawing for case 75//75



PI3V724 Application Drawing for case 150//75



PI3V724 Application Drawing for case 75



Application Diagram for DDC path

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

V_{DD} (Power Supply)……..……3.0V to 3.6V
V_{DD}5_IN(Power Supply)…….4.5V to 5.5V
Operating Ambient Temperature…….40°C to +85°C
Storage Temperature…….-55°C to +150°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ElectricalCharacteristics for Video Switching over Operating Range

(T_A= –40°C to +85°C,V_{DD} = 3.3V±10% ,V_{DD}5_IN = 5V)

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
V_{IH}	Input HIGH Voltage (SEL/Priority and MS pins)	Guaranteed HIGH level	2	-	-	V
V_{IL}	Input LOW Voltage (SEL/Priority, and MS pins)	Guaranteed LOW level	–0.5	-	0.8	V
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., ISELx = –18mA	-	–0.8	–1.2	V
I_{IH}	Input HIGH Current (SEL/Priority)	V_{DD} = Max., VSELx = V_{DD}	-	-	±5	µA
I_{IL}	Input LOW Current (SEL/Priority)	V_{DD} = Max., VSELx = GND	-	-	±5	µA
$I_{OFF\_H/V}$	Power Down Leakage Current for H/V channels only	VDD = 0V, VB = 0V, VA ≤ 3.6	-	-	22	mA
I_{OFF_DDC}	Power Down Leakage Current for DDC channels only	VDD = 0V, VB = 0V, VA ≤ 3.6	-	-	±5	mA
IOZ (DDC and RGB path)	switch leakage when switch is off	V_{DD} = 3.6V, CE/ = High, Vinput = 0V to Vdd			±5	µA
R_{ON_RGB}	Switch On-Resistance for RGB path (3)	V_{DD} = Min., 0V ≤ Vinput ≤ 1.2V, Iinput = –40mA	-	4.8	5.6	Ω
$R_{FLAT(ON)}$	On-Resistance Flatness for RGB path (4)	V_{DD} = Min., Vinput @ 0V and 1.2V, Iinput = –40mA	-	0.5	+1	Ω
Δ_{RON}	On-Resistance match from center ports to any other port (RGB path only)(4)	V_{DD} = Min., 0V ≤ Vinput ≤ 1.2V, Iinput = –40mA	-	0.1	1	Ω
$V_{OH\ (H/V)}$	Output high for H1_out/V1_out signals	V_{DD}5 = 5V, I_{OH} = -24mA	3.0		VDD5	V
$V_{OL(H/V)}$	Output low for H1_out/V1_out signals	V_{DD}5 = 5V, I_{OL} = 24mA	0		0.8	V
Vout_DDC	DDC switch path ouput voltage	Vdd = min, Vinput = >2V (either side, since DDC path is bi-directional).		2		V

Capacitance (TA = -40° to+85°C, f = 1MHz)

Parameters[4]	Description	Test Conditions(1)	Typ.(2)	Units
C_{IN}	Input Capacitance		2.0	pF
C_{OFF_COM}	RGB Capacitance, Switch OFF		3.4	pF
C_{OFF_P1P2}	R1, G1, B1 or R2, G2, B2 switch off capacitance		2.4	pF
C_{ON_RGB}	RGB Switch Capacitance, Switch ON B path		5.8	pF
C_{ON_DDC}	DDC Switch Capacitance, Switch ON		5.8	pF

Power Supply Characteristics

Parameters	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
I_{CC} _ 3.3V rail	Quiescent Power Supply Current for 3.3V power rail	V_{DD} = 3.6V, 5V_V_{DD} = 5.5V V_{SEL} = GND or VDD	-	250	500	µA
I_{CC}_Vdd5_IN	Quiescent Power supply current for 5VV_{DD}	5V_V_{DD} = 5.5V, V_{DD} = 3.6V, V_{SEL}= GND or V_{DD}		100	500	nA
Iccq_3.3V	Chip disabled	CE/ = HIGH		10		µA
Iccq_Vdd5_IN	Chip disabled	CE/ = HIGH		100	500	nA

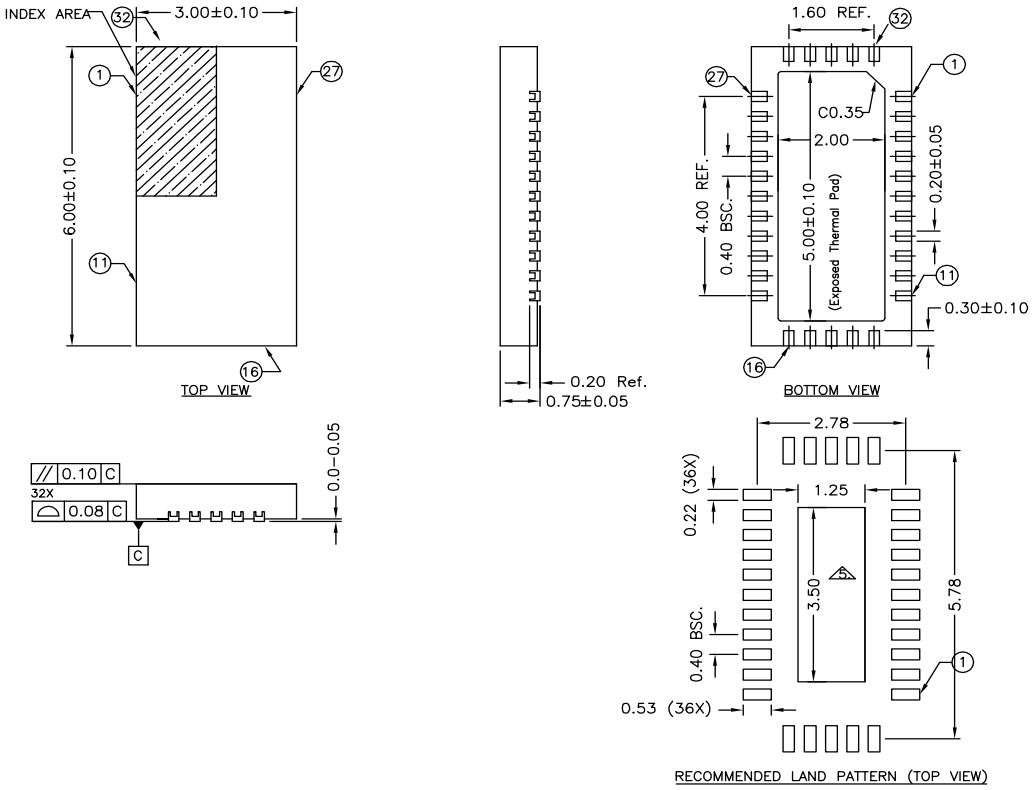
Dynamic Electrical Characteristics Over the Operating Range

(T_A=-40° to+85°C,V_{DD}=3.3V±10%, GND=0V)

Parameters	Description	Test Conditions	Min.	Typ.(2)	Max.	Units
XTALK	Crosstalk	f = 250MHz, See Fig. 2	-	-38	-	dB
OIRR	OFF Isolation	f = 250MHz, See Fig. 3	-	-46	-	dB
BW	Bandwidth –3dB	See Fig. 1	-	1.7	-	GHz
			Freq = 10MHz (VGA)		-1.77	dB
ILOSS	Insertion Loss for RGB path	with 75-Ohm load	Freq = 100MHz (XGA)		-1.88	dB
			Freq = 300MHz (UXGA)		-2.09	dB

Parameters	Description	Min.	Typ.[2]	Max.	Units
t_{PD}	Propagation Delay(2,3)	-	0.25		ns
t_{PZH}, t_{PZL}	Line Enable Time -SELto Input, Output	0.5	-	15	ns
t_{PHZ}, t_{PLZ}	Line Disable Time -SELto Input, Output	0.5	-	10	ns
$t_{SK(p)}$	Skew between opposite transitions of the same output (tPHL-tPLH) (2)	-	0.1	0.2	ns
$T_{rise\ (H/V)}$	Horizontal/Vertical synchronous output rise time (H1_out, V1_out)		1.5		ns
$T_{fall\ (H/V)}$	Horizontal/Vertical synchronous output fall time (H1_out, V1_out)		1.6		ns

Packaging Mechanical: 32-Pin TQFN (ZL)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM® Enabling Serial Connectivity — DATE: 10/09/09

DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZL (ZL32)

DOCUMENT CONTROL #: PD-2044 — REVISION: A

09-0125

Ordering Information

Ordering Code	Package Code	Package Description
PI3V724ZLE	ZL	32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **E = Pb-free and Green**
- **X suffix = Tape/Reel**