

INCH-POUND
MIL-M-38510/209H
21 April 2014
SUPERSEDING
MIL-M-38510/209G
13 September 2013

MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 8192-BIT, SCHOTTKY, BIPOLAR,  
PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

Inactive for new design after 24 July 1995
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This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome (NiCr) resistors, zapped vertical emitter, tungsten (W), titanium tungsten (TiW), or platinum silicide as the fusible link or programming element. Two product assurance class and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>	<u>Access time (ns)</u>
01	2048 word / 4 bits per word PROM with uncommitted collector	125
02, 08, 10	2048 word / 4 bits per word PROM with active pullup and a third high-impedance state output	125, 90, 55
03	1024 word / 8 bits per word PROM with uncommitted collector	90
04, 09	1024 word / 8 bits per word PROM with active pullup and a third high-impedance state output	90, 55
05	1024 word / 8 bits per word PROM with active pullup and a third high-impedance state output	90
06	1024 word / 8 bits per word PROM with uncommitted collector	90

NOTE: Device type 07 was deleted from this document under revision D.

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DLA Land and Maritime-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to <a href="mailto:memory@dla.mil">memory@dla.mil</a> . Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <a href="https://assist.dla.mil">https://assist.dla.mil</a>
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AMSC N/A

FSC 5962

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
X	See figure 1	18	Flat pack
Y	GDFP2-F18	18	Flat pack

1.3 Absolute maximum ratings.

Supply voltage range .....	-0.5 V to +7.0 V
Input voltage range .....	-1.5 V at -10 mA to +5.5 V
Storage temperature range .....	-65°C to +150°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction to case ( $\theta_{JC}$ ) :	
Cases J, K, V, and Y .....	See MIL-STD-1835 <u>1/</u>
Case X .....	35°C/W maximum <u>1/</u>
Output voltage .....	-0.5 V to +V <sub>CC</sub>
Output sink current .....	100 mA
Maximum power dissipation (P <sub>D</sub> ) :	
Device types 01, 02, 08, and 10 .....	950 mW <u>2/</u>
Device types 03, 04, 05, 06, and 09 .....	1.1 W <u>2/</u>
Maximum junction temperature (T <sub>J</sub> ) .....	+175°C

1.4 Recommended operating conditions.

Supply voltage range .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage (V <sub>IH</sub> ) .....	2.0 V
Maximum low-level input voltage (V <sub>IL</sub> ) .....	0.8 V
Normalized fanout (each output) :	
Device types 01, 02, 08, and 10 .....	12 mA <u>3/</u>
Device types 03, 04, 05, 06, and 09 .....	8 mA <u>3/</u>
Case operating temperature range (T <sub>C</sub> ) .....	-55 °C to +125 °C

1/ Heat sinking is recommended to reduce the junction temperature.

2/ Must withstand the added P<sub>D</sub> due to short circuit test (e.g. I<sub>OS</sub>).

3/ 16 mA for circuits B, D, and F devices.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.  
MIL-STD-1835 - Interface Standard Electronic Component Case Outline

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3.2 Truth table.

3.3.2.1 Unprogrammed devices. The truth tables for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3. When required in groups A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table II, and where applicable, the altered item drawing. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity.

3.8 Processing options. Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see Appendix A, MIL-PRF-38535.)

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C unless other wise specified	Device type	Limits		Units
				Min	Max	
High-level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2 mA, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.0 V	02, 04, 05, 08, 09, 10	2.4		V
Low-level output voltage <sup>2/</sup>	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.0 V	01, 02, 08, 10		0.5	V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8 mA	03, 04, 05, 06, 09		0.5	
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -10 mA, T <sub>C</sub> = +25°C	All		-1.5	V
Maximum collector cut-off current	I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.2 V	01, 03, 06		100	μA
High impedance (off-state) output high current	I <sub>OHZ</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.2 V	02, 04, 05, 08, 09, 10		100	μA
High impedance (off-state) output low current	I <sub>OLZ</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V	02, 04, 05, 08, 09, 10		-100	μA
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V	All		50	μA
	I <sub>IH2</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, special programming pin	03, 04, 06, 09		100	
Low level input current	I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V	All	-1.0	-250	μA
Short circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.0 V, <sup>3/</sup> V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V	02, 04, 05, 08, 09, 10	-15	-100	mA
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V, outputs = open	01, 02		170	mA
			03, 04, 05, 06, 08, 09, 10		185	
Propagation delay time, high to low level logic, address to output	t <sub>PHL1</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, C <sub>L</sub> = 30 pF, see figure 6	08		90	ns
			01, 02		125	
			03, 04, 05, 06		90	
			09, 10		55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <sup>1/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C unless other wise specified	Device type	Limits		Units
				Min	Max	
Propagation delay time, low to high level logic, address to output	t <sub>PLH1</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, C <sub>L</sub> = 30 pF, see figure 6	08		90	ns
			01, 02		125	
			03, 04, 05, 06		90	
			09, 10		55	
Propagation delay time, high to low level logic, enable to output	t <sub>PHL2</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, C <sub>L</sub> = 30 pF, see figure 6	08		50	ns
			01, 02		60	
			03, 04, 05, 06		50	
			09, 10		30	
Propagation delay time, low to high level logic, enable to output	t <sub>PLH2</sub>	V <sub>CC</sub> = 4.5 V and 5.5 V, C <sub>L</sub> = 30 pF, see figure 6	08		50	ns
			01, 02		60	
			03, 04, 05, 06		50	
			09, 10		30	

<sup>1/</sup> Complete terminal conditions shall be specified in table III.

<sup>2/</sup> I<sub>OL</sub> = 16 mA for circuits B, D, and F devices.

<sup>3/</sup> Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

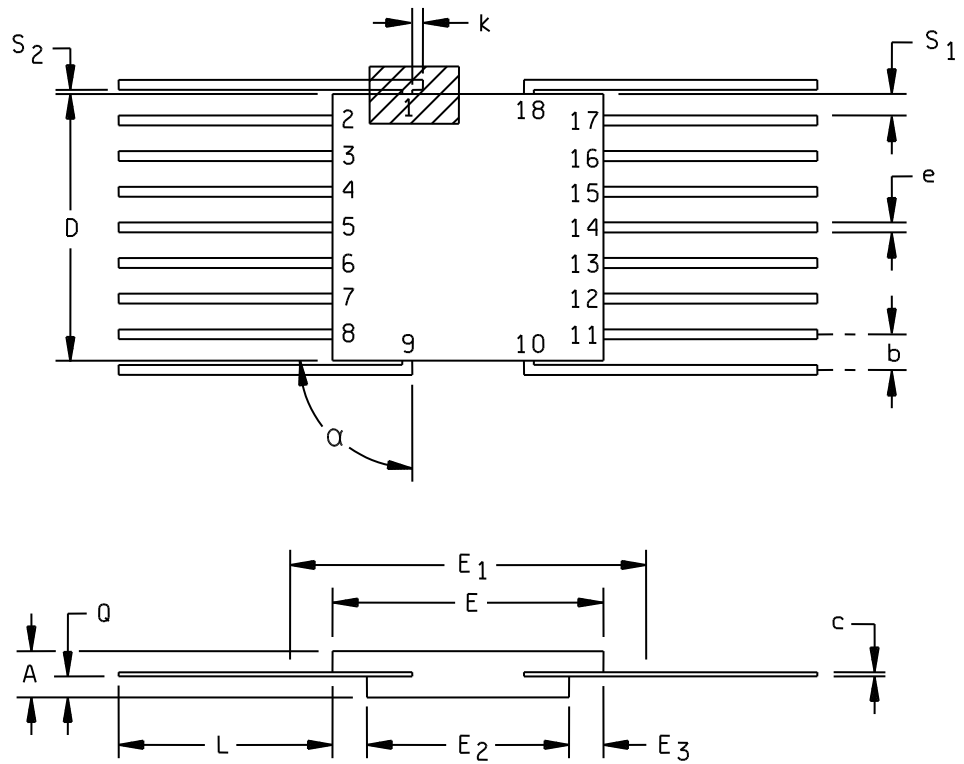


FIGURE 1. Case outline X.

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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.085	1.14	2.16	
b	.015	.020	.38	.51	5
C	.003	.006	.08	.15	5
D	.340	.380	8.64	9.65	
E	.340	.380	8.64	9.65	
E <sub>1</sub>		.400		10.16	3
E <sub>2</sub>	.260	.290	6.60	7.37	
E <sub>3</sub>	.025		.63		
e	.050	BSC	1.27	BSC	4, 6
K	.008	.015	.20	.38	9
L	.250	.330	6.35	8.38	
Q	.010	.040	.25	1.02	2
S <sub>1</sub>	.005		.13		7, 8
S <sub>2</sub>	.004		.10		10
$\alpha$	30°	90°	30°	90°	

## NOTES:

1. Index area; a tab (dim K) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.27 mm) between centerlines. Each pin centerline shall be located within  $\pm 0.005$  (0.13 mm) of its exact longitudinal position relative to pins relative to pins 1 and 18.
5. All leads – increase limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads number 2, 8, 11, and 17).
8. Dimension S<sub>1</sub> may be .000 (0.00 mm) if leads are brazed to the metallized ceramic body (see MIL-STD-1835).
9. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension K does not apply.
10. Applies to leads number 1, 9, 10, and 18.

FIGURE 1. Case outline X – Continued.

Device types	01, 02, 08, and 10	03, 04, and 09
Case outlines	V	J and K
Terminal number	Terminal symbol	
1	A <sub>6</sub>	A <sub>7</sub>
2	A <sub>5</sub>	A <sub>6</sub>
3	A <sub>4</sub>	A <sub>5</sub>
4	A <sub>3</sub>	A <sub>4</sub>
5	A <sub>0</sub>	A <sub>3</sub>
6	A <sub>1</sub>	A <sub>2</sub>
7	A <sub>2</sub>	A <sub>1</sub>
8	A <sub>10</sub>	A <sub>0</sub>
9	GND	O <sub>1</sub>
10	$\overline{CE}_1$	O <sub>2</sub>
11	O <sub>4</sub>	O <sub>3</sub>
12	O <sub>3</sub>	GND
13	O <sub>2</sub>	O <sub>4</sub>
14	O <sub>1</sub>	O <sub>5</sub>
15	A <sub>9</sub>	O <sub>6</sub>
16	A <sub>8</sub>	O <sub>7</sub>
17	A <sub>7</sub>	O <sub>8</sub>
18	V <sub>CC</sub>	CE <sub>4</sub>
19	---	CE <sub>3</sub>
20	---	$\overline{CE}_2$
21	---	$\overline{CE}_1$
22	---	A <sub>9</sub>
23	---	A <sub>8</sub>
24	---	V <sub>CC</sub>

FIGURE 2. Terminal connections.

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Device types	05 and 06	01, 02, and 08	02 and 10
Case outlines	J and K	X	Y
Terminal number	Terminal symbol		
1	A <sub>7</sub>	A <sub>6</sub>	A <sub>6</sub>
2	A <sub>6</sub>	A <sub>5</sub>	A <sub>5</sub>
3	A <sub>5</sub>	A <sub>4</sub>	A <sub>4</sub>
4	A <sub>4</sub>	A <sub>3</sub>	A <sub>3</sub>
5	A <sub>3</sub>	A <sub>0</sub>	A <sub>0</sub>
6	A <sub>2</sub>	A <sub>1</sub>	A <sub>1</sub>
7	A <sub>1</sub>	A <sub>2</sub>	A <sub>2</sub>
8	A <sub>0</sub>	A <sub>10</sub>	A <sub>10</sub>
9	O <sub>1</sub>	GND	GND
10	O <sub>2</sub>	$\overline{CE}_1$	$\overline{CE}_1$
11	O <sub>3</sub>	O <sub>4</sub>	O <sub>4</sub>
12	GND	O <sub>3</sub>	O <sub>3</sub>
13	O <sub>4</sub>	O <sub>2</sub>	O <sub>2</sub>
14	O <sub>5</sub>	O <sub>1</sub>	O <sub>1</sub>
15	O <sub>6</sub>	A <sub>9</sub>	A <sub>9</sub>
16	O <sub>7</sub>	A <sub>8</sub>	A <sub>8</sub>
17	O <sub>8</sub>	A <sub>7</sub>	A <sub>7</sub>
18	NC	V <sub>CC</sub>	V <sub>CC</sub>
19	NC	---	---
20	$\overline{CE}$	---	---
21	NC	---	---
22	A <sub>9</sub>	---	---
23	A <sub>8</sub>	---	---
24	V <sub>CC</sub>	---	---

FIGURE 2. Terminal connections – Continued.

Device types 01, 02, 08, and 10 ( see notes 1, 2, and 3 )

Word number	Enable	Address										
	$\overline{CE}_1$	A <sub>10</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
NA	L	X	X	X	X	X	X	X	X	X	X	X
NA	H	X	X	X	X	X	X	X	X	X	X	X

Word number	Data			
	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>
NA	See note 5			
NA	OC	OC	OC	OC

Device types 05 and 06 ( see notes 1, 2, and 3 )

Word number	Enable	Address									
	$\overline{CE}_1$	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
NA	L	X	X	X	X	X	X	X	X	X	X
NA	H	X	X	X	X	X	X	X	X	X	X

Word number	Data							
	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>
NA	See note 5							
NA	OC	OC	OC	OC	OC	OC	OC	OC

FIGURE 3. Truth tables (unprogrammed).

Device types 03, 04, and 09 ( see notes 1, 2, 3, and 4 )

Word number	Enable				Address									
	$\overline{CE}_1$	$\overline{CE}_2$	CE <sub>3</sub>	CE <sub>4</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
NA	L	L	H	H	X	X	X	X	X	X	X	X	X	X
NA	L	H	H	H	X	X	X	X	X	X	X	X	X	X
NA	H	L	H	H	X	X	X	X	X	X	X	X	X	X
NA	H	H	L	H	X	X	X	X	X	X	X	X	X	X
NA	H	H	L	L	X	X	X	X	X	X	X	X	X	X

Word number	Data							
	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>
NA	See note 5							
NA	OC	OC	OC	OC	OC	OC	OC	OC
NA	OC	OC	OC	OC	OC	OC	OC	OC
NA	OC	OC	OC	OC	OC	OC	OC	OC
NA	OC	OC	OC	OC	OC	OC	OC	OC

## NOTES:

1. NA = Not applicable.
2. X = Input may be high level, low level or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with both enable inputs at low level.
5. The outputs for an unprogrammed device shall be high for circuits A, B (device types 03 and 04), and F; and shall be low for circuits B (device types 01, 02, and 08), C, D, E, G and H.

FIGURE 3. Truth tables (unprogrammed) – Continued.

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Device types 01, 02, and 08 (Circuit B)  
Device types 01 and 02 (Circuit A)  
Device type 02 (Circuit F)  
Device types 03 and 04 (Circuit E)

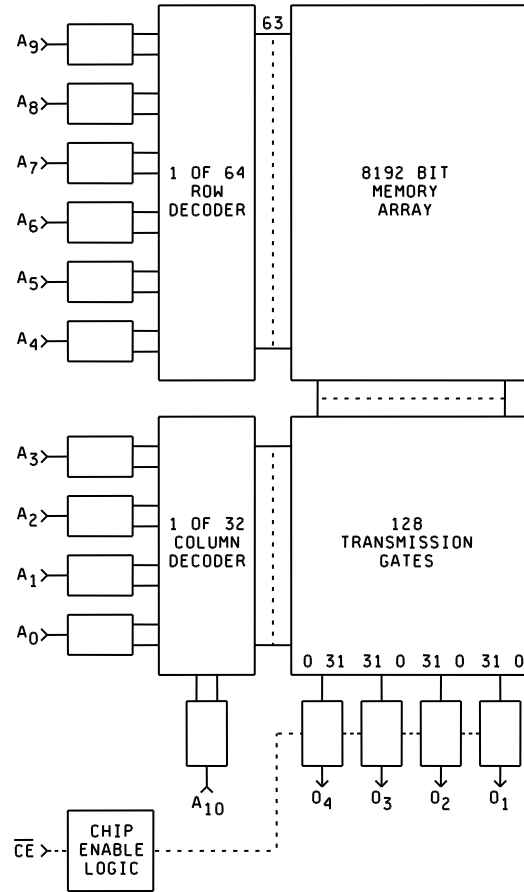


FIGURE 4. Functional block diagrams.

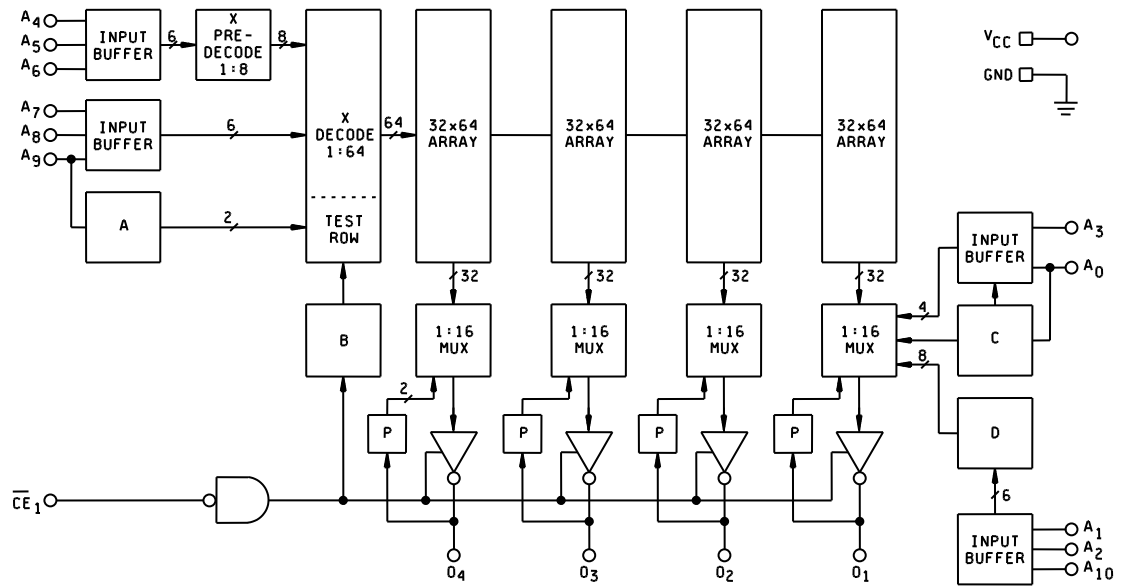


FIGURE 4. Functional block diagrams – Continued.

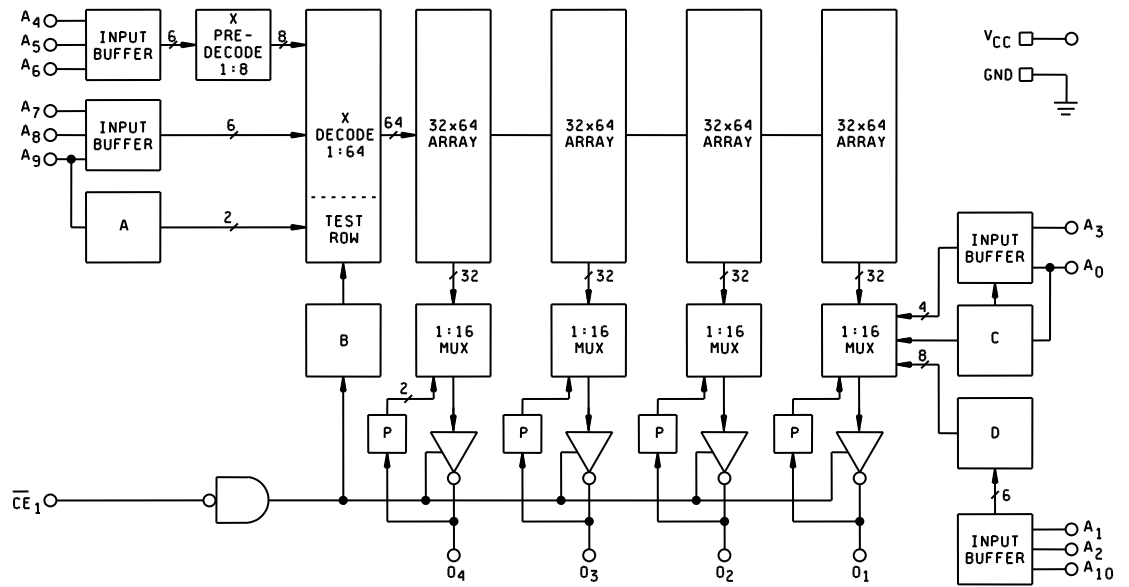


FIGURE 4. Functional block diagrams – Continued.

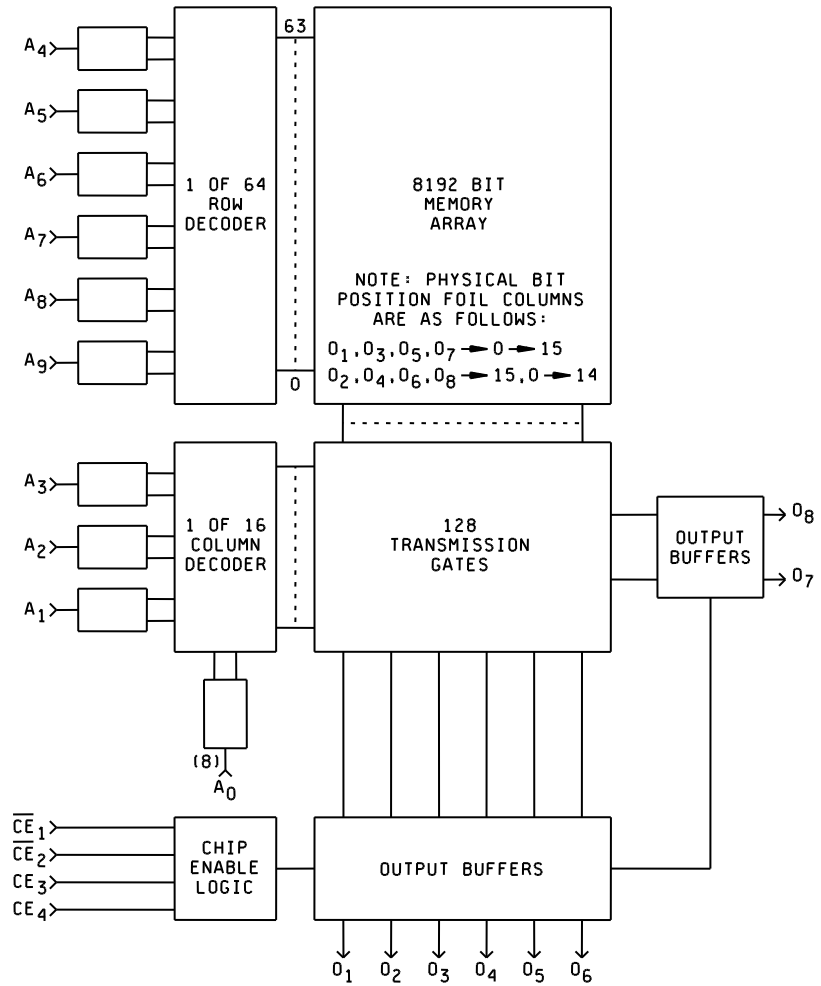
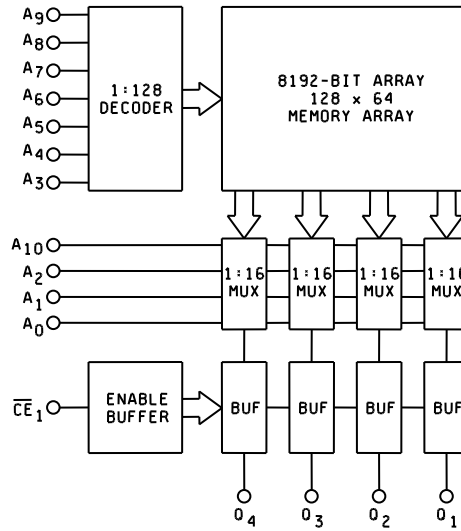


FIGURE 4. Functional block diagrams – Continued.

DEVICE TYPES 01 AND 02  
CIRCUIT G



DEVICE TYPES 03 AND 04  
CIRCUIT G

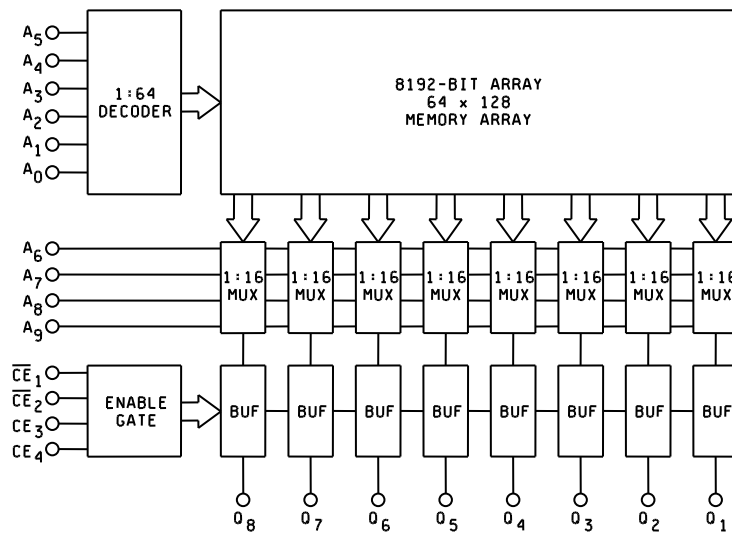


FIGURE 4. Functional block diagrams – Continued.

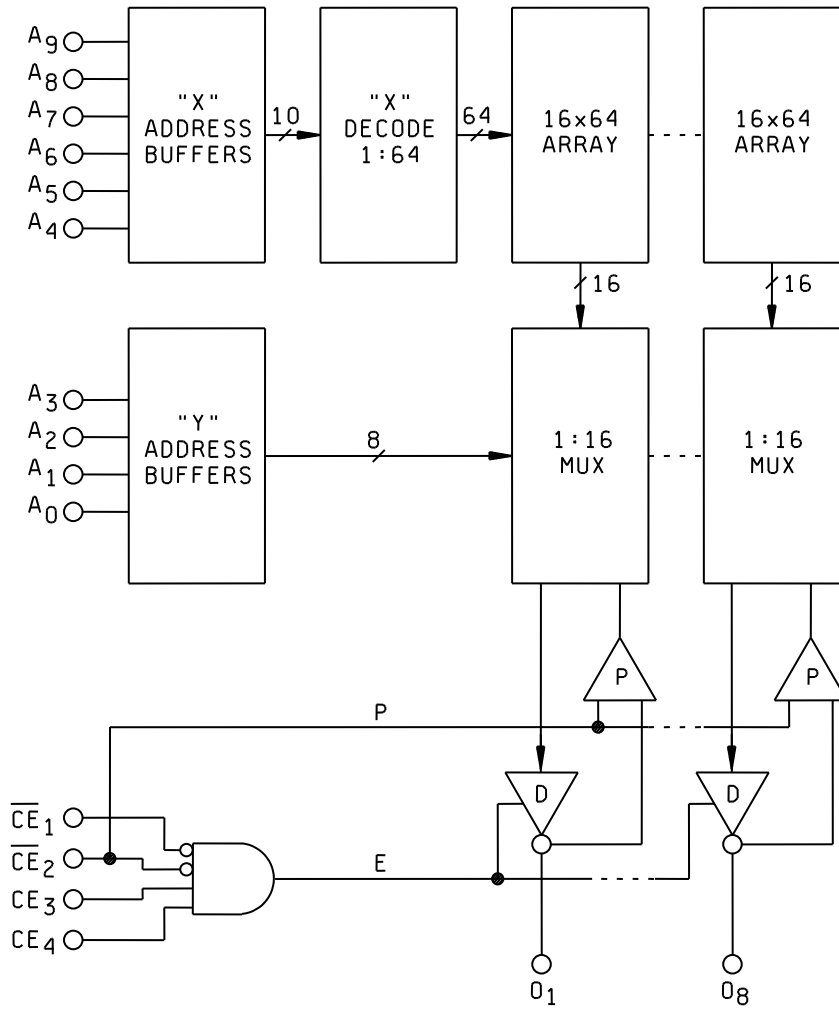


FIGURE 4. Functional block diagrams – Continued.

Device types 03, 04, 05, and 09  
Circuit C

Device types 04  
Circuit H

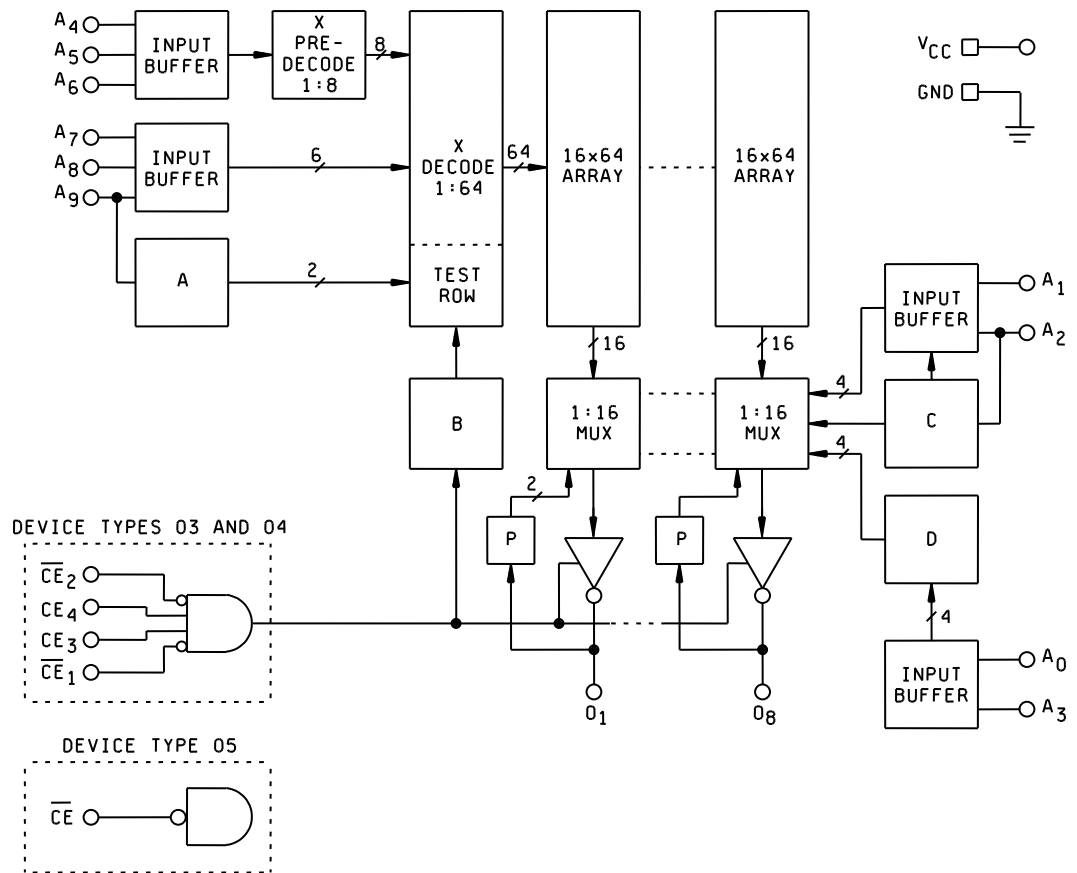


FIGURE 4. Functional block diagrams – Continued.

Device types 03, 04, 05, 06, and 09  
Circuits B and D

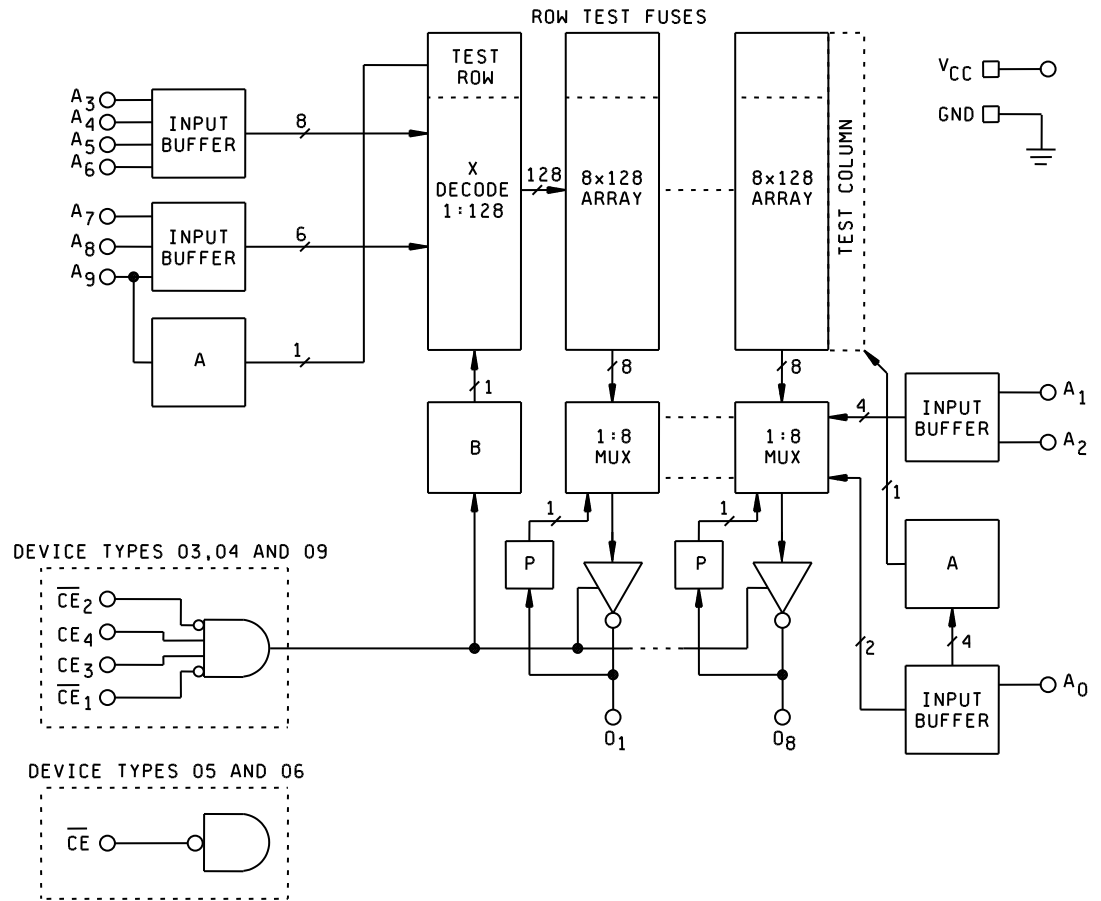
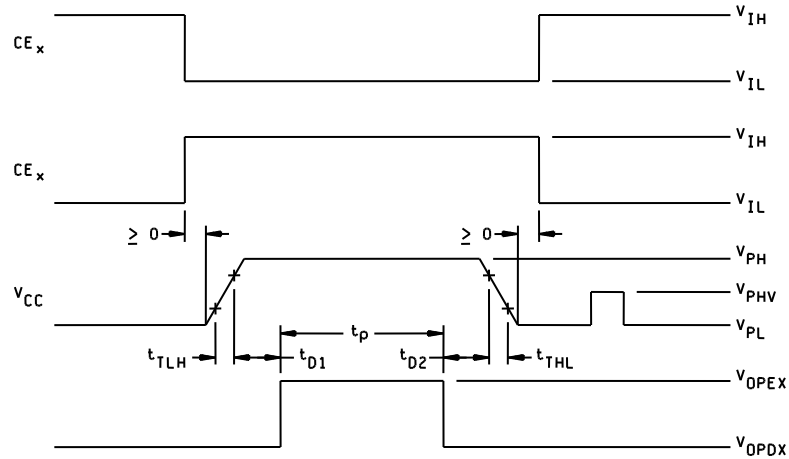
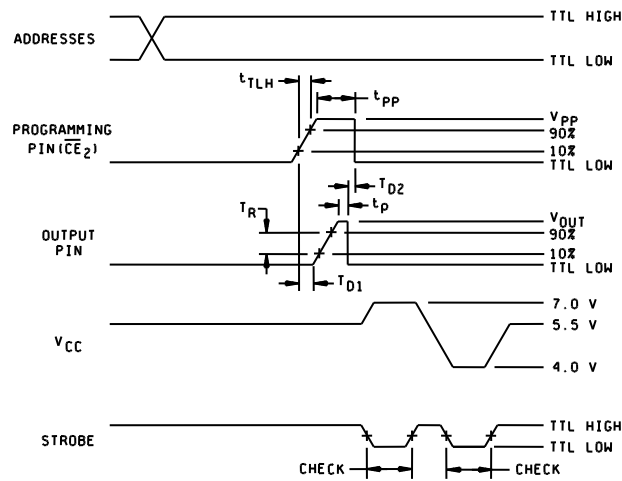


FIGURE 4. Functional block diagrams – Continued.



NOTE: All other waveform characteristics shall be as specified in table IVA.

FIGURE 5A. Programming voltage waveforms during programming for circuit A.

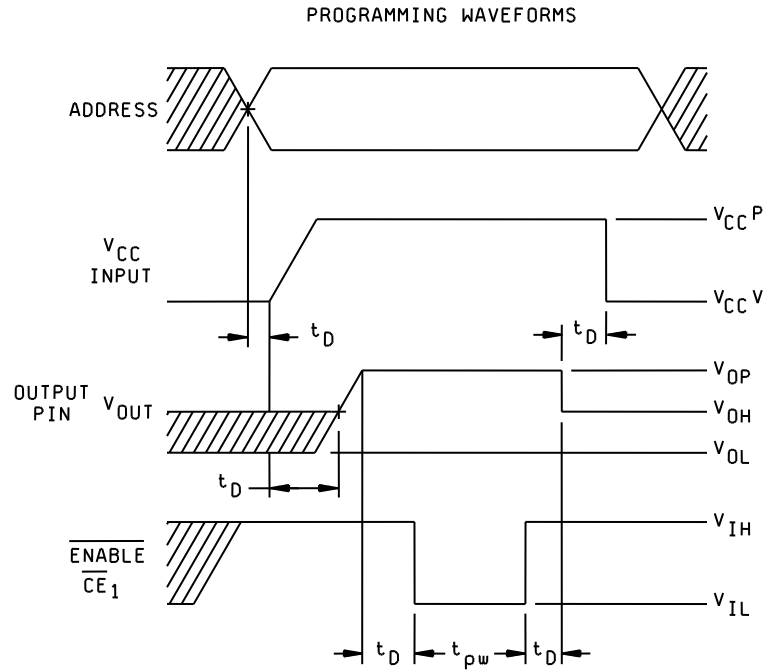


NOTES:

1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVB.

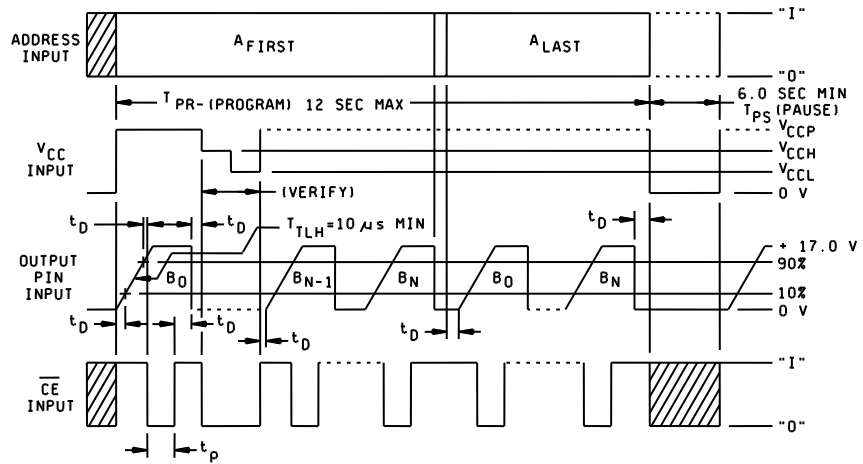
(Device types 03 and 04)

FIGURE 5B. Programming voltage waveforms during programming for circuit B.



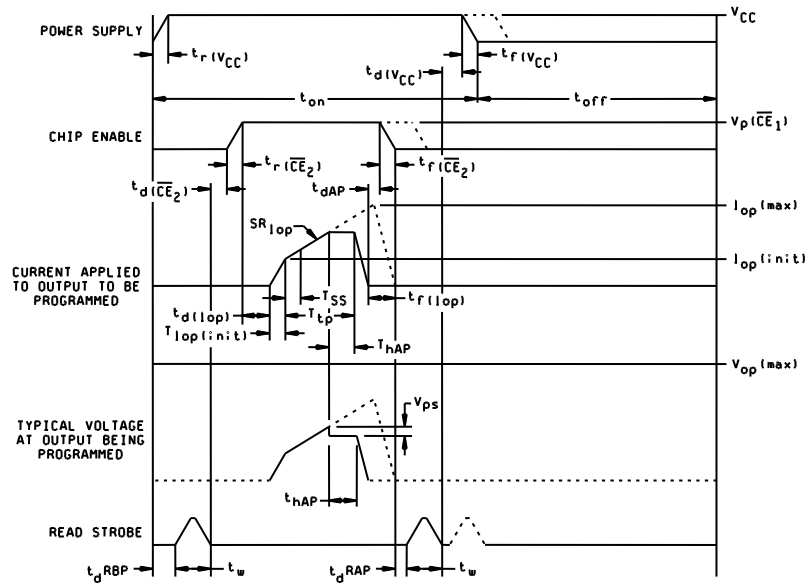
(Device types 01, 02, and 08)

FIGURE 5B. Programming voltage waveforms during programming for circuit B – Continued.



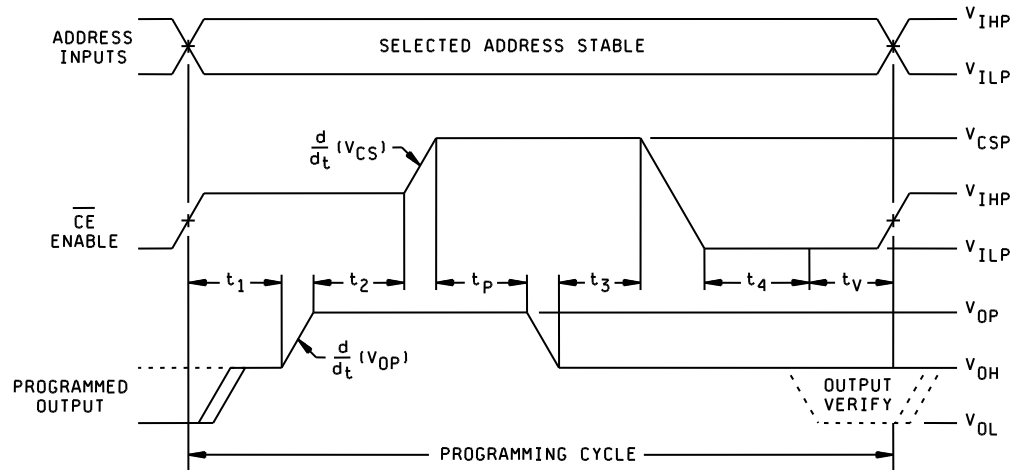
NOTE: All other waveform characteristics shall be as specified in table IVC.

FIGURE 5C. Programming voltage waveforms during programming for circuit C and H.



NOTE: All other waveform characteristics shall be as specified in table IVD.

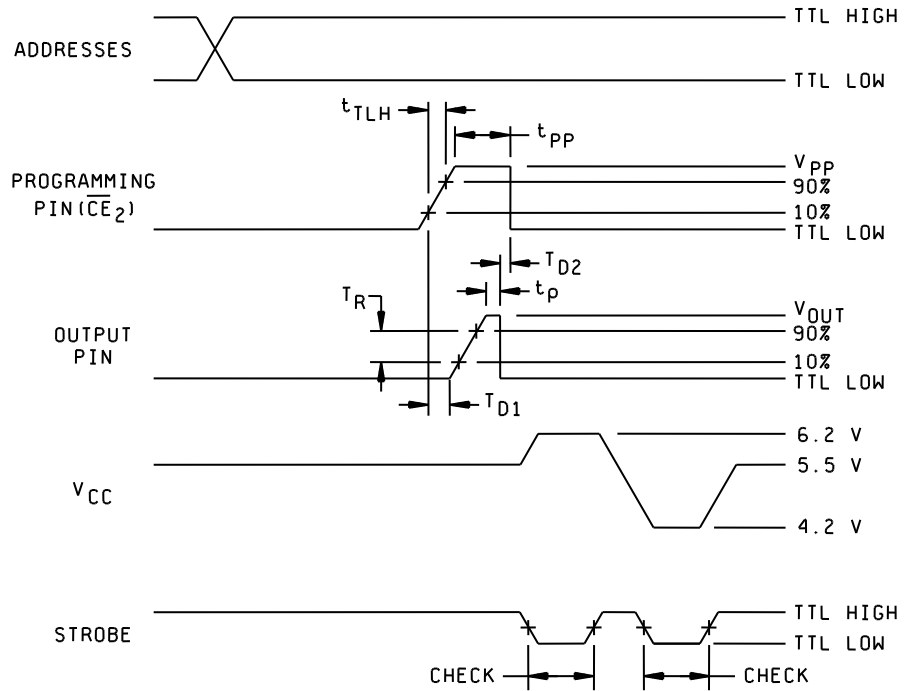
FIGURE 5D. Programming voltage waveforms during programming for circuit D.



## NOTES:

1. All delays between edges are specified from completion of the first edge, not midpoints.
2. Delays  $t_1$ ,  $t_2$ ,  $t_3$ , and  $t_4$  must be greater than 100 ns; maximum delays of 1  $\mu$ s are recommended to minimize heating during programming.
3. During  $t_V$  the output being programmed is switched to the load R and verified.
4. Outputs not being programmed are connected to  $V_{ONP}$  through a resistor which provides output current limiting.
5. All other waveform characteristics shall be as specified in table IVE.

FIGURE 5E. Programming voltage waveforms during programming for circuit E.



NOTES:

1. Output load is 0.2 mA and 12 mA during 6.2 V and 4.2 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVF.

FIGURE 5F. Programming voltage waveforms during programming for circuit F.

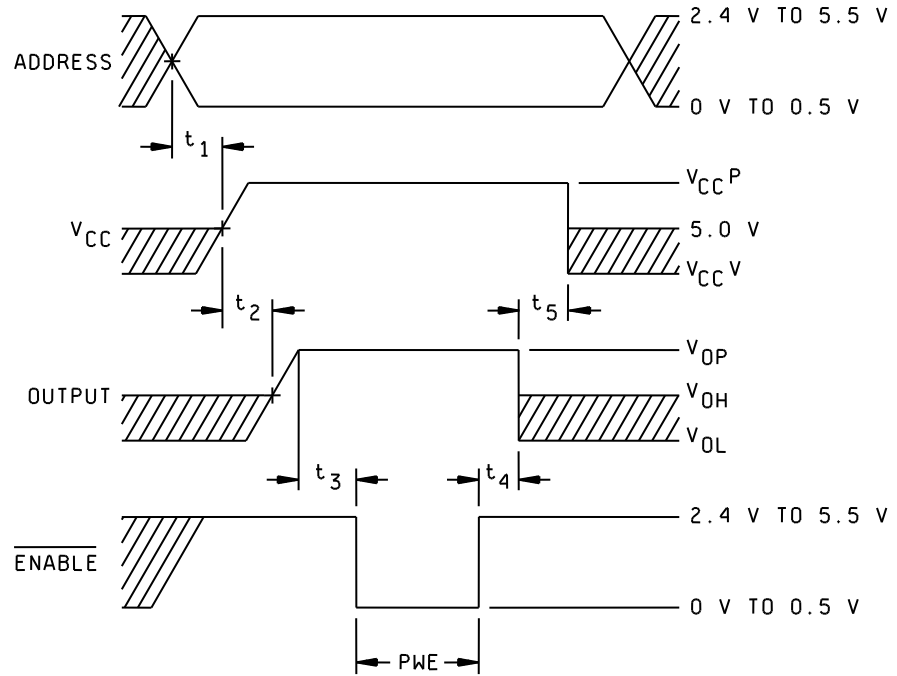
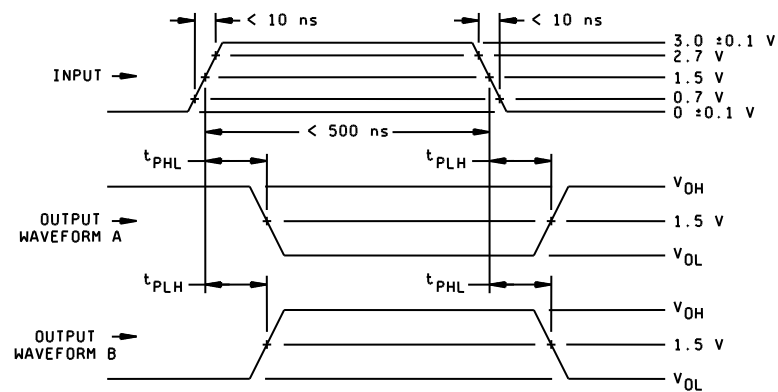
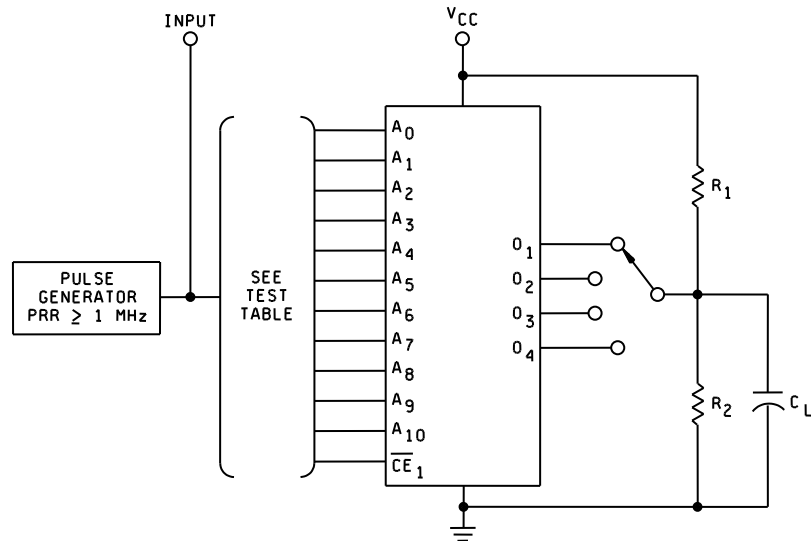


FIGURE 5G. Programming voltage waveforms during programming for circuit G.

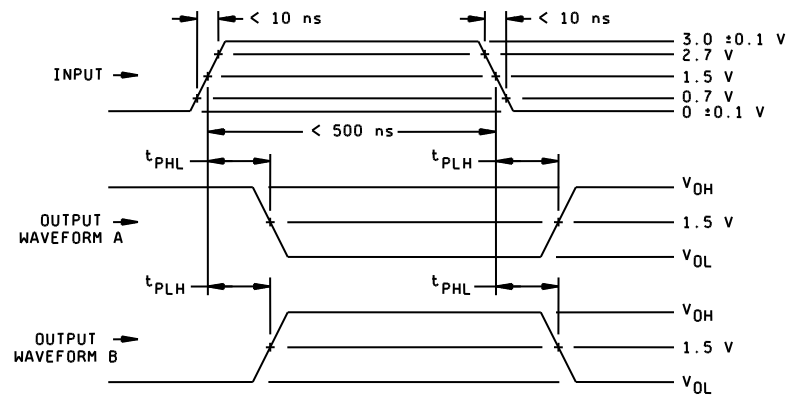
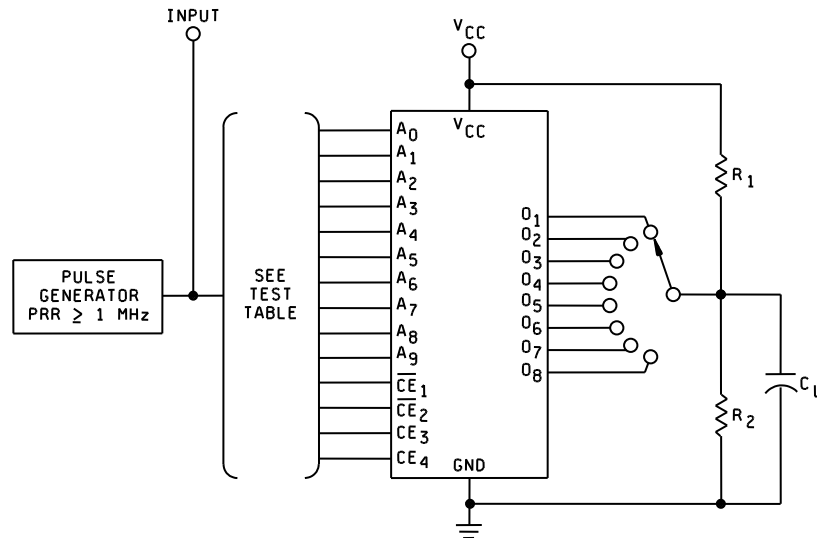
Device types 01, 02, 08, and 10



## NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2.  $C_L = 30 \text{ pF}$  minimum, including jig and probe capacitance;  $R_1 = 330 \Omega \pm 25\%$  and  $R_2 = 680 \Omega \pm 20\%$ .
3. Outputs may be under load simultaneously.

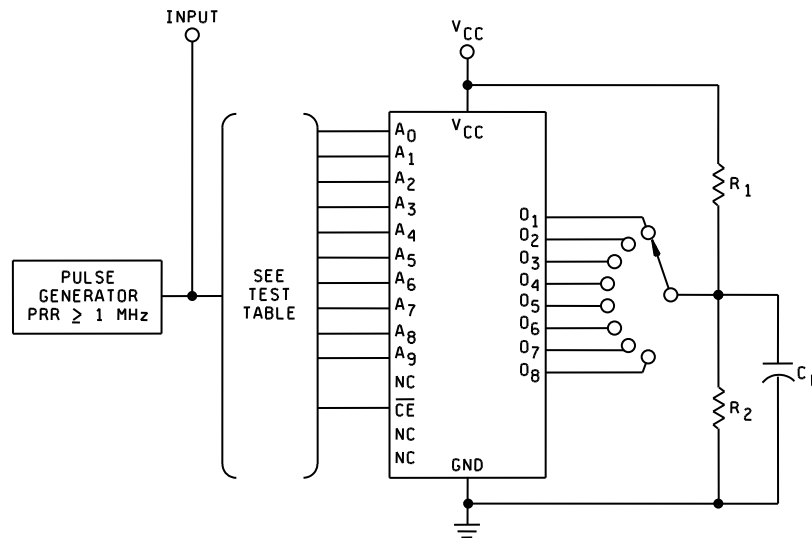
FIGURE 6. Switching time test circuit.



## NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2.  $C_L = 30 \text{ pF}$  minimum, including jig and probe capacitance;  $R_1 = 330 \Omega \pm 25\%$  and  $R_2 = 680 \Omega \pm 20\%$ .
3. Outputs may be under load simultaneously.

FIGURE 6. Switching time test circuit – Continued.



## NOTES:

1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2.  $C_L = 30 \text{ pF}$  minimum, including jig and probe capacitance;  $R_1 = 330 \Omega \pm 25\%$  and  $R_2 = 680 \Omega \pm 20\%$ .
3. Outputs may be under load simultaneously.

FIGURE 6. Switching time test circuit – Continued.

#### 4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
- d. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535. Qualification data for subgroups 7 through 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies faster device type which is manufactured identically (for example, same die, process, and package) to other device types on this specification, then the other device types may be qualified by conducting only group A electrical tests and any electrical specified as additional group C subgroups and submitting data in accordance with MIL-PRF-38535 (for example, groups B, C, and D tests are not required).

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6 shall be omitted.
- c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.3.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.
- d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III) <u>1/</u> , <u>2/</u> , <u>3/</u>	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*, 8
Final electrical test parameters for programmed devices	1*, 2, 3, 7* 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9,
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B end-point electrical parameters subgroup 5 when using the method 5005 QCI option	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D test requirements	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ \* indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. For qualification inspection, at least 50 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the life tests.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.



TABLE III. Group A inspection for device type 01 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases V,X Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		Unit
				A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>10</sub>	GND	$\overline{CE}_1$	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	V <sub>CC</sub>		Min	Max	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T <sub>C</sub> = +125°C and -55°C.																								
9 T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	47	5/	5/	5/	5/	5/	5/	5/	5/	GND	GND	6/	6/	6/	6/	5/	5/	5/	5/	Outputs		125	ns
	t <sub>PLH1</sub>	GALPAT Fig. 6	48	5/	5/	5/	5/	5/	5/	5/	5/	"	GND	"	"	"	"	5/	5/	5/	5/	"		125	"
	t <sub>PHL2</sub>	Sequential Fig. 6	49	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	Z/	"	"	"	"	Z/	Z/	Z/	Z/	"		60	"
	t <sub>PLH2</sub>	Sequential Fig. 6	50	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	Z/	"	"	"	"	Z/	Z/	Z/	Z/	"		60	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																								
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																								

See footnotes at end of table.



TABLE III. Group A inspection for device types 02, 08, and 10 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases V,X,Y Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Meas. terminal	Test limits		Unit			
				A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>10</sub>	GND	$\overline{CE}_1$	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>7</sub>	V <sub>CC</sub>		Min	Max				
1 T <sub>C</sub> = +25°C	I <sub>OS</sub>	3011	54	1/ 10/	1/ 9/	1/	1/ 21/	1/ 13/	1/	1/	1/ 10/	GND	0.5V	GND					1/ 9/	1/ 13/	1/	5.5V	O <sub>4</sub>	-15	-100	mA		
			55	11/	10/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			56																					O <sub>3</sub>	"	"	"	"
			57	12/	"	12/	"	"	"	"	"	"	12/	"	"	"	"	"	"	"	"	"	"	O <sub>2</sub>	"	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = +125°C and V <sub>IC</sub> tests are omitted.																											
3	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = -55°C and V <sub>IC</sub> tests are omitted.																											
7 T <sub>C</sub> = +25°C	Functional tests	4/	58	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs		4/				
8	Same tests, terminal conditions, and limits as for subgroup 7, except T <sub>C</sub> = +125°C and T <sub>C</sub> = -55°C.																											
9 T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	59	5/	5/	5/	5/	5/	5/	5/	5/	GND	GND	6/	6/	6/	6/	5/	5/	5/	5/	Outputs		8/	ns			
	t <sub>PLH1</sub>	GALPAT Fig. 6	60	5/	5/	5/	5/	5/	5/	5/	5/	"	GND	"	"	"	"	5/	5/	5/	5/	"		"	"			
	t <sub>PHL2</sub>	Sequential Fig. 6	61	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	"	"	"	"	7/	7/	7/	7/	"		"	"			
	t <sub>PLH2</sub>	Sequential Fig. 6	62	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	"	"	"	"	7/	7/	7/	7/	"		"	"			
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																											
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																											

See footnotes at end of table.

TABLE III. Group A inspection for device type 03.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit		
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	CE <sub>4</sub>	CE <sub>3</sub>	CE <sub>2</sub>	CE <sub>1</sub>	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max			
1 T <sub>C</sub> = +25°C	V <sub>IC</sub>		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	GND											4.5V	A <sub>7</sub>		-1.5	V		
			2																									A <sub>6</sub>					
			3																										A <sub>5</sub>				
			4																										A <sub>4</sub>				
			5																										A <sub>3</sub>				
			6																										A <sub>2</sub>				
			7																										A <sub>1</sub>				
			8																										A <sub>0</sub>				
			9																											CE <sub>4</sub>			
			10																											CE <sub>3</sub>			
			11																											CE <sub>2</sub>			
			12																											CE <sub>1</sub>			
			13																											A <sub>9</sub>			
			14																											A <sub>8</sub>			
	15																											V <sub>CC</sub>					
	16																																
	17																																
	18																																
	19																																
	20																																
	21																																
	22																																
23																																	
24																																	
	V <sub>OL</sub>	3007	15	1/2	1/	1/	1/	1/	1/	1/	1/	8mA	8mA	8mA		8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	O <sub>1</sub>		0.5	V		
			16	1/16/																							O <sub>2</sub>						
			17																									O <sub>3</sub>					
			18																									O <sub>4</sub>					
			19																									O <sub>5</sub>					
			20																									O <sub>6</sub>					
			21																									O <sub>7</sub>					
			22																									O <sub>8</sub>					
	I <sub>IL</sub>	3009	23	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V															5.5V	A <sub>7</sub>	-1.0	-250	μA			
			24																									A <sub>6</sub>					
			25																									A <sub>5</sub>					
			26																									A <sub>4</sub>					
			27																									A <sub>3</sub>					
			28																									A <sub>2</sub>					
			29																									A <sub>1</sub>					
			30																									A <sub>0</sub>					
			31																									CE <sub>4</sub>					
			32																									CE <sub>3</sub>					
			33																									CE <sub>2</sub>					
			34																									CE <sub>1</sub>					
			35																									A <sub>9</sub>					
			36																									A <sub>8</sub>					
	I <sub>IH1</sub>	3010	37	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V																A <sub>7</sub>		50	μA			
			38																									A <sub>6</sub>					
			39																									A <sub>5</sub>					
			40																									A <sub>4</sub>					
			41																									A <sub>3</sub>					
			42																									A <sub>2</sub>					
			43																									A <sub>1</sub>					
			44																									A <sub>0</sub>					
			45																									CE <sub>4</sub>					
			46																									CE <sub>3</sub>					
			47																									CE <sub>2</sub>					
			48																									CE <sub>1</sub>					
			49																									A <sub>9</sub>					
	I <sub>IH2</sub>		50																								CE <sub>2</sub>		100	μA			
	I <sub>CEX</sub>		51									5.2V	5.2V	5.2V														O <sub>1</sub>					
			52																									O <sub>2</sub>					
			53																									O <sub>3</sub>					
			54																									O <sub>4</sub>					

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit	
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	CE <sub>4</sub>	CE <sub>3</sub>	CE <sub>2</sub>	CE <sub>1</sub>	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max		
1 T <sub>C</sub> = +25°C	I <sub>CEX</sub>		55 56 57 58												GND		5.2V	5.2V			0.5V	0.5V	5.5V	5.5V			5.5V	O <sub>5</sub> O <sub>6</sub> O <sub>7</sub> O <sub>8</sub>		100	μA	
	I <sub>CC</sub>	3005	59	GND	GND	GND	GND	GND	GND	GND	GND	GND									5.2V							V <sub>CC</sub>		185	mA	
2	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = +125°C and V <sub>IC</sub> tests are omitted.																															
3	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = -55°C and V <sub>IC</sub> tests are omitted.																															
7 T <sub>C</sub> = +25°C	Functional tests	4/	60	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	Outputs		4/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T <sub>C</sub> = +125°C and T <sub>C</sub> = -55°C.																															
9 T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	61	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	5.5V	5.5V	GND	GND	5/	5/	5/	Outputs		8/	ns
	t <sub>PLH1</sub>	GALPAT Fig. 6	62	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	"	"	5.5V	5.5V	GND	GND	5/	5/	5/	"		"	"
	t <sub>PHL2</sub>	Sequential Fig. 6	63	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	"	"	"	"	"	"	"	"	"	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"		"	"
	t <sub>PLH2</sub>	Sequential Fig. 6	64	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	"	"	"	"	"	"	"	"	"	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"		"	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																															
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																															

See footnotes at end of table.

TABLE III. Group A inspection for device types 04 and 09.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J.K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit									
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	CE <sub>4</sub>	CE <sub>3</sub>	CE <sub>2</sub>	CE <sub>1</sub>	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max										
1 T <sub>C</sub> = +25°C	V <sub>IC</sub>		1	-10mA	-10mA	-10mA	-10mA																				4.5V	A <sub>7</sub>		-1.5	V									
			2																																					
			3																																					
			4																																					
			5																																					
			6																																					
			7																																					
			8																																					
			9																																					
			10																																					
			11																																					
			12																																					
			13																																					
			VOL	3007	15	1/ 2/ 16/	1/	1/	1/	1/	1/	1/ 18/	1/	1/	19/																									
16																																								
17																																								
18																																								
19																																								
20																																								
21																																								
22																																								
23																																								
24																																								
V <sub>OH</sub>	3006	23	1/	1/ 10/	1/ 9/ 10/	1/ 9/ 23/	1/ 9/	1/ 9/	1/ 9/	1/ 9/ 10/ 20/ 21/	-2mA	-2mA																												
		24																																						
		25																																						
		26																																						
		27																																						
		28																																						
		29																																						
		30																																						
		I <sub>IL</sub>	3009	31	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V																											
				32																																				
33																																								
34																																								
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38																																								
39																																								
40																																								
41																																								
42																																								
43																																								
44																																								
I <sub>IH1</sub>	3010	45	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V																													
		46																																						
		47																																						
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See footnotes at end of table.



TABLE III. Group A inspection for device types 04 and 09 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits			Unit
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	CE <sub>4</sub>	CE <sub>3</sub>	$\overline{\text{CE}}_2$	$\overline{\text{CE}}_1$	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max		
9 T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	85	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/	5.5V	5.5V	GND	GND	5/	5/	5/	Outputs		90	55	ns
	t <sub>PLH1</sub>	GALPAT Fig. 6	86	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	"	5.5V	5.5V	GND	GND	5/	5/	5/	"		90	55	"
	t <sub>PHL2</sub>	Sequential Fig. 6	87	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	"	"	"	"	"	"	"	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"		50	30	"
	t <sub>PLH2</sub>	Sequential Fig. 6	88	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"	"	"	"	"	"	"	"	Z/	Z/	Z/	Z/	Z/	Z/	Z/	"		50	30	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																															
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																															

See footnotes at end of table.

TABLE III. Group A inspection for device type 05.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit									
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	N/C	N/C	$\overline{\text{CE}}$	N/C	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max										
1 T <sub>C</sub> = +25°C	V <sub>IC</sub>		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	GND											4.5V	A <sub>7</sub>		-1.5	V									
			2																																					
			3																																					
			4																																					
			5																																					
			6																																					
			7																																					
			8																																					
			9																																					
			10																																					
			11																																					
VOL	3007	12	1/	1/	1/	1/	1/	1/	1/	1/	1/	1/	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	8mA	0.5V	1/	1/		O <sub>1</sub>		0.5	V				
		13																																						
		14																																						
		15																																						
		16																																						
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		19																																						
		20																																						
VOH	3006	20						1/ 9/	1/ 9/	1/ 9/	1/ 9/ 20/	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	-2mA	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	1/ 9/ 13/ 20/	O <sub>1</sub>	2.4		V		
		21																																						
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		25																																						
		26																																						
		27																																						
I <sub>IL</sub>	3009	28	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	A <sub>7</sub>	-1	-250	μA	
		29																																						
		30																																						
		31																																						
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		33																																						
		34																																						
		35																																						
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		38																																						
I <sub>IH</sub>	3010	39	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	A <sub>7</sub>	50		μA	
		40																																						
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See footnotes at end of table.

TABLE III. Group A inspection for device type 05 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit				
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	N/C	N/C	$\overline{\text{CE}}$	N/C	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max					
1 T <sub>C</sub> = +25°C	I <sub>OZH</sub>		50									5.2V																O <sub>1</sub>		100	μA				
			51																										O <sub>2</sub>						
			52																											O <sub>3</sub>					
			53																											O <sub>4</sub>					
I <sub>OLZ</sub>			54																										O <sub>5</sub>						
			55																										O <sub>6</sub>						
			56																											O <sub>7</sub>					
			57																											O <sub>8</sub>					
I <sub>OS</sub>	3011		58									0.5V																	O <sub>1</sub>		-100	μA			
			59																										O <sub>2</sub>						
			60																											O <sub>3</sub>					
			61																											O <sub>4</sub>					
I <sub>CC</sub>	3005		62																										O <sub>5</sub>						
			63																										O <sub>6</sub>						
			64																											O <sub>7</sub>					
			65																											O <sub>8</sub>					
2	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = +125°C and V <sub>IC</sub> tests are omitted.																																		
3	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = -55°C and V <sub>IC</sub> tests are omitted.																																		
7 T <sub>C</sub> = +25°C	Functional tests	4/	75	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/												Outputs		4/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T <sub>C</sub> = +125°C and T <sub>C</sub> = -55°C.																																		
9 T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	76	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/												Outputs		8/	ns
	t <sub>PLH1</sub>	GALPAT Fig. 6	77	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	"	"											"		"	"
	t <sub>PHL2</sub>	Sequential Fig. 6	78	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	"											"		"	"
	t <sub>PLH2</sub>	Sequential Fig. 6	79	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	"											"		"	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																																		
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																																		

See footnotes at end of table.

TABLE III. Group A inspection for device type 06.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit									
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	N/C	N/C	CE	N/C	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max										
1 T <sub>C</sub> = +25°C	V <sub>IC</sub>		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	GND											4.5V	A <sub>7</sub>		-1.5	V									
			2																																					
			3																																					
			4																																					
			5																																					
			6																																					
			7																																					
			8																																					
			9																																					
			10																																					
			11																																					
	V <sub>OL</sub>	3007		12	1/	1/	1/	1/	1/	1/	1/	1/	1/	8mA	8mA	8mA													O <sub>1</sub>		0.5	V								
				13																																				
				14																																				
				15																																				
				16																																				
				17																																				
				18																																				
				19																																				
				20																																				
	I <sub>IL</sub>	3009		20	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	5.5V	A <sub>7</sub>	-1.0	-250	μA								
				21																																				
				22																																				
				23																																				
				24																																				
				25																																				
				26																																				
				27																																				
				28																																				
				29																																				
	30																																							
	I <sub>IH1</sub>	3010		31	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V		A <sub>7</sub>		50	μA								
				32																																				
				33																																				
				34																																				
				35																																				
				36																																				
				37																																				
				38																																				
				39																																				
				40																																				
	I <sub>IH2</sub>			41																																				
				42																																				
	I <sub>CEX</sub>			43									5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.2V	5.5V	O <sub>1</sub>											
				44																																				
				45																																				
				46																																				
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See footnotes at end of table.

TABLE III. Group A inspection for device type 06 – Continued.

Terminal conditions (outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high  $\geq 2.0$  V, low  $\leq 0.8$  V, or open).

Subgroup	Symbol	MIL-STD-883 method	Cases J,K Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit		
				A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	GND	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	N/C	N/C	$\overline{\text{CE}}$	N/C	A <sub>9</sub>	A <sub>8</sub>	V <sub>CC</sub>		Min	Max			
1	T <sub>C</sub> = +25°C	I <sub>CC</sub>	3006	50	GND	GND	GND	GND	GND	GND	GND				GND								GND		GND	GND	5.5V	V <sub>CC</sub>		185	mA		
2	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = +125°C and V <sub>IC</sub> tests are omitted.																																
3	Same tests, terminal conditions, and limits as for subgroup 1, except T <sub>C</sub> = -55°C and V <sub>IC</sub> tests are omitted.																																
7	T <sub>C</sub> = +25°C	Functional tests	4/	51	4/	4/	4/	4/	4/	4/	4/	4/	4/	4/	GND	4/	4/	4/	4/	4/			4/			4/	4/	Outputs		4/			
8	Same tests, terminal conditions, and limits as for subgroup 7, except T <sub>C</sub> = +125°C and T <sub>C</sub> = -55°C.																																
9	T <sub>C</sub> = +25°C	t <sub>PHL1</sub>	GALPAT Fig. 6	76	5/	5/	5/	5/	5/	5/	5/	5/	6/	6/	6/	GND	6/	6/	6/	6/	6/			GND		5/	5/	5/	Outputs		8/	ns	
		t <sub>PLH1</sub>	GALPAT Fig. 6	77	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	"	"	"	"	"	"	"	"			GND		5/	5/	5/	"		"	"
		t <sub>PHL2</sub>	Sequential Fig. 6	78	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"			7/		7/	7/	7/	"		"	"
		t <sub>PLH2</sub>	Sequential Fig. 6	79	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"			7/		7/	7/	7/	"		"	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = +125°C.																																
11	Same tests, terminal conditions, and limits as for subgroup 9, except T <sub>C</sub> = -55°C.																																

See footnotes at end of table.

TABLE III. Group A inspection – Continued.

- 1/ For programmed devices, select an appropriate address to acquire the desired output state.
- 2/ For unprogrammed device types 01 (circuit A), apply 10.0 V on pin 1 (A<sub>6</sub>) and for unprogrammed device type 02 (circuit A), apply 13.0 V on pins 1 and 2 (A<sub>6</sub>, A<sub>5</sub>); for unprogrammed device types 03, apply 10.0 V on pin 1 (A<sub>7</sub>) and for the unprogrammed device type 04, apply 13.0 V on pins 1 and 2 (A<sub>7</sub>, A<sub>6</sub>) (circuit A).
- 3/ I<sub>OL</sub> = 12 mA for circuits A, C, E, G and H devices; I<sub>OL</sub> = 16 mA for circuits B, D, and F devices.
- 4/ The functional tests shall verify that no fuses are blown for unprogrammed devices or that the truth table specified in the altered item drawing exists for programmed devices (see table II and 3.3.2.2). All bits shall be tested. The functional tests shall be performed with V<sub>CC</sub> = 4.5 V and V<sub>CC</sub> = 5.5 V. Terminal conditions shall be as follows:
- Inputs: H = 3.0 V, L = 0.0 V.
  - Outputs: Output voltage shall be either:
    - H = 2.4 V minimum and L = 0.5 V maximum when using a high speed checker double comparator, or
    - H ≥ 1.0 V and L < 1.0 V when using a high speed checker single comparator.

5/ GALPAT (PROGRAMMED PROM).

This program will test all bits in the array, the addressing and interaction between bits for ac performance t<sub>PLH1</sub> and t<sub>PHL1</sub>. Each bit in the pattern is fixed by being programmed with an “H” or “L”. The GALPAT tests shall be performed with V<sub>CC</sub> = 4.5 V and 5.5 V. For manufacturer-programmed PROM only (see 3.8.2).

When testing device type 10, the t<sub>PHL1</sub> and t<sub>PLH1</sub> limits shall be verified by performing a sequential test pattern outline in footnote 7/.

Description:

- Step 1. Word 0 is read.
- Step 2. Word 1 is read.
- Step 3. Word 0 is read
- Step 4. Word 2 is read.
- Step 5. Word 0 is read.
- Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 1023 or 2047 (as applicable) is reached, then increments to the next word and reads back and forth as in step 1 through step 6 and shall include all words.
- Step 7. Pass execution time = ( n<sup>2</sup> + n ) x cycle time. n = 1024 or 2048 (as applicable).

6/ The outputs are loaded per figure 6.

7/ SEQUENTIAL (PROGRAMMED PROM).

This program will test all bits in the array for t<sub>PHL2</sub> and t<sub>PLH2</sub>. The sequential tests shall be performed with V<sub>CC</sub> = 4.5 V and 5.5 V.

Description:

- Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
- Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t<sub>PHL2</sub> and t<sub>PLH2</sub> are read.
- Step 3. Word 1 is addressed. Same enable sequence as above.
- Step 4. The reading procedure continues until word 1023 or 2047 (as applicable) is reached.
- Step 5. Pass execution times 1024 or 2048 (as applicable) x cycle time.

TABLE III. Group A inspection – Continued.

8/

Device type	t <sub>PHL1</sub> (ns)	t <sub>PLH1</sub> (ns)	t <sub>PHL2</sub> (ns)	t <sub>PLH2</sub> (ns)
01, 02	125	125	60	60
03, 04, 05, 06	90	90	50	50
Circuit F	90	90	50	50
Circuit B device 08	55	55	30	30
Circuit H device 08	90	90	50	50
09	55	55	30	30
10	55	55	30	30

- 9/ For unprogrammed devices (circuit C), apply 10.0 V on pin 15 (A<sub>9</sub>), 0.5 V on pin 2 (A<sub>5</sub>) and 5.0 V to all other address pins for device types 02 and 10; device types 04 and 09, apply 10 V on pin 8 (A<sub>0</sub>) and 5.0 V on pins 7, 6, 5, 4, 3, (A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, A<sub>4</sub>, A<sub>5</sub>); device type 05, apply 10 V on pin 22 (A<sub>9</sub>), 0.5 V on pins 8, 7, 6, 5 (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>) and 5.0 V to all other address pins. For unprogrammed devices (circuit F) apply 12.0 V on pin 5 (A<sub>0</sub>) for device types 02 and 08.
- 10/ For unprogrammed devices (circuit G), apply 10.5 V to pins 1 and 8 (A<sub>6</sub> and A<sub>10</sub>), apply 0.0 V to pin 2 (A<sub>5</sub>) and apply 0.0 V to pin 2 (A<sub>5</sub>) and apply 3.0 V to all other address pins for device types 01 and 02; apply 10.5 V to pin 3 (A<sub>5</sub>), apply to 0.0 V to pins 2 and 8 (A<sub>6</sub> and A<sub>0</sub>), and apply 3.0 V to all other address pins for device types 03 and 04.
- 11/ For unprogrammed devices, apply 12.0 V on pin 1 (A<sub>6</sub>) for device types 02 and 08 ( circuit B ).
- 12/ For unprogrammed devices (circuit G), apply 10.5 V on pin 1 and 8 (A<sub>6</sub> and A<sub>10</sub>), apply 0.0 V to pin 3 (A<sub>4</sub>) and apply 3.0 V to all address pins for device type 02, apply 10.5 V to pin 3 (A<sub>5</sub>), apply 0.0 V to pin 8 (A<sub>0</sub>) and apply 3.0 V to all other address pins for device type 04.
- 13/ For unprogrammed device type 02 (with date codes before 8501), apply 10.0 V pin 5 (A<sub>0</sub>); 0.5 V on pin 16 (A<sub>8</sub>), and 5.0 V on all other address pins; and for unprogrammed device type 04 (with date codes before 8501) (circuit C), apply 10.0 V on pin 22 (A<sub>9</sub>) and 5.0 V on all other address pins.
- 14/ Circuit B, device type 08, apply 2.4 V.
- 15/ For device type 08 and 10: Electrical supply current I<sub>CC</sub> test maximum limit is 185 mA.
- 16/ For unprogrammed devices (circuit B), apply 12.0 V on pins 22 and 1 (A<sub>9</sub> and A<sub>7</sub>) for device types 03 and 04.
- 17/ At the manufacturer's option, this may be performed with V<sub>IN</sub> = 5.5 V and test limits of 50 μA maximum.
- 18/ For unprogrammed devices (circuit F) apply 12.0 V on pin 6 (A<sub>2</sub>) and all other inputs at 0 V for device type 04.
- 19/ I<sub>OL</sub> = 8 mA for circuits A, B, C, D, E, and G devices; I<sub>OL</sub> = 16 mA for circuit F devices.

TABLE III. Group A inspection – Continued.

- 20/ For unprogrammed devices (circuit D), apply 12.0 V on pins 8 and 22 ( $A_0$  and  $A_9$ ), select an appropriate address to acquire the desired output state.
- 21/ For unprogrammed device type 03 (circuit E), apply 13.0 V on pin 4 ( $A_4$ ) and pin 8 ( $A_0$ ); and for unprogrammed device type 04 (circuit E), apply 13.0 V on pin 8 ( $A_0$ ).
- 22/ For unprogrammed device type 02 and 08 (circuit H), apply 5.0 V on pin 18, 0.0V to pins 5, 6, 7 and 8, 3.0V to pins 1, 2, 3, 15, 16 and 17, 9.0V to pin 4.
- 23/ For unprogrammed device type 04 (circuit H) apply 5.0V to pin 24; 0.0V to pins 3, 5, 6, 7, 8, 20 and 21; 3.0V to pins 1, 2, 18, 19, 22 and 23; 9.0V to pin 4.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designator is cross referenced in paragraph 6.7 herein with the manufacturer's symbol or CAGE number.

4.7 Programming procedure for circuit A. The waveforms on figure 5A, the programming characteristics in table IVA and the following procedures shall be used for programming the device.

- a. Connect the device in the electrical configuration for programming. The waveforms on figure 5A and the programming characteristics in table IVA shall apply to these procedures.
- b. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit shall not be used to address the PROM.
- c. Apply  $V_{PL}$  voltage to  $V_{CC}$ .
- d. Bring the  $\overline{CE}_X$  inputs high and the  $CE_X$  inputs low to disable the device. The chip enables are TTL compatible. An open circuit shall not be used to disable the device.
- e. Disable the programming circuitry by applying a voltage of  $V_{OPD}$  to the outputs of the PROM.
- f. Raise  $V_{CC}$  to  $V_{PH}$  with rise time less than or equal to  $t_{TLH}$ .
- g. After a delay equal to or greater than  $t_{D1}$  apply only one pulse with amplitude of  $V_{OPE}$  and duration of  $t_p$  to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
- h. Lower  $V_{CC}$  to  $V_{PL}$  following a delay to  $t_{D2}$  from programming enable pulse applied to an output.
- i. Enable the PROM for verification by applying  $V_{IL}$  to  $\overline{CE}_X$  and  $V_{IH}$  to  $CE_X$ .
- j. Apply  $V_{PHV}$  to  $V_{CC}$  and verify bit is programmed.
- k. Repeat steps 4.7a through 4.7j for all other bits to be programmed in the PROM.
- l. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVA. Programming characteristics for circuit A. 1/

Parameter	Symbol	Limits 2/			Unit
		Min	Recommended	Max	
Address input voltage 3/	V <sub>IH</sub>	2.4	5.0	5.0	V
	V <sub>IL</sub>	0.0	0.4	0.5	"
Programming	V <sub>PH</sub> 4/	10.75	11.0	11.25	V
Voltage to V <sub>CC</sub> low	V <sub>PL</sub>	0.0	0.0	1.5	V
Program verify	V <sub>PHV</sub>	---	5.5	---	V
Verify voltage	V <sub>R</sub> 5/	4.5	---	5.5	V
Programming input low current at V <sub>PH</sub>	I <sub>ILP</sub>	---	-300	-600	μA
Programmed voltage (V <sub>CC</sub> ) transition time	t <sub>TLH</sub>	1	5	10	μs
	t <sub>THL</sub>	1	5	10	"
Programming delay	t <sub>D1</sub>	10	10	20	μs
	t <sub>D2</sub>	1	5	5	"
Programming pulse width	t <sub>p</sub> 6/	90	100	110	μs
Programming duty cycle	PDC	---	30	60	%
Output voltage, enable	V <sub>OPe</sub> 7/	10.5	10.5	11.0	V
Output voltage, disable	V <sub>OPD</sub>	0.0	5.0	5.5	V

1/ During the programming the chip must be disabled for proper operation.

2/ T<sub>C</sub> = +25°C.

3/ No inputs should be left open for V<sub>IH</sub>.

4/ V<sub>PH</sub> source must be capable of supplying one ampere.

5/ It is recommended that post programming dual verification be made at V<sub>R</sub> minimum and V<sub>R</sub> maximum.

6/ Note step j in programming procedure.

7/ V<sub>OPe</sub> source must be capable of supplying 10 mA minimum.

4.8 Programming procedure for circuit B, device types 03 and 04. The waveforms on figure 5B, the programming characteristics in table IVB and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Raise  $V_{CC}$  to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying  $V_{IH}$  to the CE inputs and  $V_{IL}$  to the CE inputs. The chip enable inputs are TTL compatible.
- e. Apply the  $V_{PP}$  pulse to the programming pin ( $CE_2$ ). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by  $T_{D1}$  and leave after the output pin's programming pulse by  $T_{D2}$  (see figure 5B).
- f. Apply only one  $V_{OUT}$  pulse with duration of  $t_P$  to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying  $V_{OUT}$  pulses to each output to be programmed.
- h. Repeat 4.8c through 4.8g for all other bits to be programmed.
- i. Enable the chip by applying  $V_{IL}$  to the  $\overline{CE}$  inputs and  $V_{IH}$  to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at  $V_{CC} = 4.0$  V and 0.2 mA at  $V_{CC} = 7.0$  V at  $T_C = 25^\circ\text{C}$ .
- j. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVB. Programming characteristics for circuit B, device types 03 and 04.

Parameter	Symbol	Conditions	Limits <sup>1/</sup>			Unit
			Min	Recommended	Max	
V <sub>CC</sub> required during programming	V <sub>CCP</sub>		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t <sub>TLH</sub>		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V <sub>PP</sub>		32.5	33	33.5	V
Output programming voltage	V <sub>OUT</sub>		25.5	26	26.5	V
Programming pin pulse width ( $\overline{CE}_2$ )	t <sub>PP</sub>	Chip disabled, V <sub>CC</sub> = 5.5 V		100	180	ns
Pulse width of programming voltage	t <sub>P</sub>	Chip disabled, V <sub>CC</sub> = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I <sub>L</sub>	V <sub>PP</sub> = 33 V, V <sub>OUT</sub> = 26 V, V <sub>CC</sub> = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T <sub>D1</sub>	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T <sub>D2</sub>	Measured at 10% levels	100			ns
Output current during verification	I <sub>OLV1</sub>	Chip enabled, V <sub>CC</sub> = 4.0 V	11	12	13	mA
	I <sub>OLV2</sub>	Chip enabled, V <sub>CC</sub> = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V <sub>IH</sub>		2.4	5.0	5.5	V
	V <sub>IL</sub>		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C	t <sub>P</sub> / t <sub>C</sub>			25	%

<sup>1/</sup> T<sub>C</sub> = +25°C.

4.8.1 Programming procedure for circuit B, device types 01, 02, and 08. The waveforms on figure 5B, (device types 01, 02, and 08), the programming characteristics in table IVB (device types 01, 02, and 08), and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Apply  $V_{IH}$  to  $\overline{CE}_1$  and the binary address of the PROM word to be programmed. Raise  $V_{CC}$  to  $V_{CCP}$ .
- c. After a  $t_D$  delay, apply only one  $V_{OP}$  to the output to be programmed high. Apply  $V_{OP}$  to one output at a time.
- d. After a  $t_D$  delay, a pulse  $\overline{CE}_1$  to a  $V_{IL}$  level for a duration of  $t_p$ .
- e. After a  $t_p$  and  $t_D$  delay, remove  $V_{OP}$  from the programmed output.
- f. Other bits in the same word may be programmed sequentially while the  $V_{CC}$  input is at the  $V_{CCP}$  level by applying  $V_{OP}$  pulses to each output to be programmed and pulsing  $\overline{CE}_1$  to the  $V_{IL}$  level, allowing for proper delays between  $V_{OP}$  and  $\overline{CE}_1$ .
- g. Repeat 4.8.1b through 4.8.1e for all other bits to be programmed.
- h. To verify programming, lower  $V_{CCP}$  to  $V_{CC}$ . Connect a 10 k $\Omega$  resistor between each output and  $V_{CC}$ . Apply  $V_{IL}$  to  $\overline{CE}_1$  input. The programmed outputs should remain in the high state and the unprogrammed outputs should go to the low level.
- i. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVB. Programming characteristics for circuit B, device types 01, 02, and 08.

Parameter	Symbol	Conditions	Limits <sup>1/</sup>			Unit
			Min	Recommended	Max	
V <sub>CC</sub> required during programming	V <sub>CCP</sub>		11.5	11.75	12.0	V
V <sub>OUT</sub> current limit during programming	I <sub>OP</sub>		20	25	30	mA
Output programming voltage	V <sub>OUT</sub>		10.5	11.0	11.5	V
Pulse width of programming voltage	t <sub>P</sub>		9	10	11	μs
Programming delay	t <sub>D</sub>		0	1	10	μs
V <sub>CCP</sub> or V <sub>OUT</sub> transition time	t <sub>TLH</sub>	Rise time of V <sub>CC</sub> or V <sub>OUT</sub>	1	5	10	V/μs
V <sub>CCP</sub> current	I <sub>CCP</sub>		800	900	1000	mA
Low V <sub>CC</sub> for verification	V <sub>CCCL</sub>		4.2	4.3	4.4	V
High V <sub>CC</sub> for verification	V <sub>CCCH</sub>		5.8	6.0	6.2	V
Address input voltage	V <sub>IH</sub>		2.4	3.0	5.5	V
	V <sub>IL</sub>		0.0	0.0	0.5	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C	t <sub>p</sub> / t <sub>c</sub>		25	25	%

<sup>1/</sup> T<sub>C</sub> = +25°C.

4.9 Programming procedure for circuit C and H. The waveforms on figure 5C, the programming characteristics in table IVC and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all device outputs with a 10 k  $\Omega$  resistor to  $V_{CC}$ .  
Apply  $V_{IH}$  to the  $\overline{CE}$  inputs and  $V_{IL}$  to the CE inputs
- c. Address the PROM with the binary address of the selected word to be programmed. Raise  $V_{CC}$  to  $V_{CCP}$ .
- d. After a  $t_D$  delay (10  $\mu$ s), apply only one  $V_{OUT}$  pulse to the output to be programmed.  
Program one output at a time
- e. After a  $t_D$  delay (10  $\mu$ s), pulse  $\overline{CE}$  input to logic "0" for a duration of  $t_p$ .
- f. After a  $t_D$  delay (10  $\mu$ s), remove the  $V_{OUT}$  pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially while the  $V_{CC}$  input is at the  $V_{CCP}$  level by applying  $V_{OUT}$  pulses to each output to be programmed allowing a delay of  $t_D$  between pulses as shown on figure 5C.
- h. Repeat 4.9c through 4.9g for all other bits to be programmed.
- i. To verify programming after  $t_D$  (10  $\mu$ s) delay, lower  $V_{CC}$  to  $V_{CCH}$  and apply a logic "0" level to both  $\overline{CE}$  inputs and logic "1" level to CE inputs. The programmed output should remain in the "1" state. Again, lower  $V_{CC}$  and  $V_{CCL}$  and verify that the programmed output remains in the "1" state.
- j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVC. Programming characteristics for circuit C and H.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Recommended	Max	
Programming voltage	$V_{CCP}$ <u>1/</u>	$I_{CCP} = 375 \pm 75$ mA transient or steady-state	8.5	8.75	9.0	V
Verification upper limit	$V_{CCH}$		5.3	5.5	5.7	V
Verification lower limit	$V_{CCL}$		4.3	4.5	4.7	V
Verify threshold	$V_S$ <u>2/</u>		1.4	1.5	1.6	V
Programming supply current	$I_{CCP}$	$V_{CCP} = +8.75 \pm 0.25$ V	300	350	400	mA
Input voltage high level "1"	$V_{IH}$		2.4		5.5	V
Input voltage low level "0"	$V_{IL}$		0	0.4	0.8	V
Input current	$I_{IH}$	$V_{IH} = +5.5$ V			50	$\mu$ A
Input current	$I_{IL}$	$V_{IL} = +0.4$ V			-500	$\mu$ A
Output programming voltage	$V_{OUT}$ <u>3/</u>	$I_{OUT} = 200 \pm 20$ mA, transient or steady-state	16	17	18	V
Output programming current	$I_{OUT}$	$V_{OUT} = +17 \pm 1$ V	180	200	220	mA
Programming voltage transition time	$t_{TLH}$		10		50	$\mu$ s
$\overline{CE}$ programming pulse width	$t_P$		0.3	0.4	0.5	ms
Pulse sequence delay	$t_D$		10			$\mu$ s
Programming duty cycle	$t_{PR}$ $t_{PR}+t_{PS}$				50	%

1/ Bypass  $V_{CC}$  to GND with a 0.01  $\mu$ F capacitor to reduce voltage spikes.

2/  $V_S$  is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the  $17 \pm 1$  V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4.10 Programming procedure for circuit D. The waveforms on figure 5D, the programming characteristics in table IV D and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Select the word to be programmed by applying the appropriate voltages to the address pins as well as the required voltages to chip enable pins to select the device.
- c. Apply the proper power,  $V_{CC} = 6.5 \text{ V}$ ,  $GND = 0 \text{ V}$ .
- d. Verify that the bit to be programmed is in the "0" logic state.
- e. Enable the chip for programming by application of the chip enable voltage,  $V_{P(CE)} = 21.0 \text{ V}$ ,  $\overline{CE}_2$ ,  $CE_3$ , and  $CE_4$  should be left high, and  $\overline{CE}_1$  should remain low.
- f. Apply  $I_{OP}$  programming current ramp to the output to be programmed. The other outputs shall be left open. Only one output may be programmed at a time. During the rise of the current ramp, the required current will be achieved to program the junction. As programming occurs, a drop in voltage can be sensed at the output of the device. Upon detection of  $V_{ps}$ , the current shall be held for  $t_{hap}$  and then shut off.
- g. Verify that the programmed bits is in the "1" logic state. Lower  $V_{P(CE_1)}$  to 0 V and read the output. Note that the PROM is supplied with fuses generating a low level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.
- h. Lower  $V_{CC}$  to 0 V. The power supply duty cycle shall be equal to or less than 50 percent.
- i. If the bit verifies as not having been programmed at  $V_{CC} = 6.5 \text{ V}$ , repeat the programming ramp sequence up to 15 times until the bit is programmed. If after 16 programming attempts, the bit does not program, the device shall be considered a reject.
- j. If the bit verifies as having been programmed at  $V_{CC} = 6.5 \text{ V}$ , one of the following two conditions shall be followed:
  - (1) If the current required to program was less than  $I_{OP(max)}$ , proceed to 4.10 k.
  - (2) If the current required to program was equal to or greater than  $I_{OP(max)}$ , the device shall be considered a reject and no further attempts at programming other bits shall be attempted.
- k. Repeat 4.10a through 4.10j for all other bits to be programmed.
- l. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVD. Programming characteristics for circuit D.

Parameter	Symbol	Conditions <sup>1/</sup>	Limits			Unit
			Min	Recommended	Max	
Address input voltage	V <sub>IH</sub>	Don't leave inputs open	2.4	5.0	5.0	V
	V <sub>IL</sub>		0	0	0.4	
Chip enable programming voltage	V <sub>P(CE)</sub>	$\overline{CE}_1 = V_{IL}$ , $CE_3 = CE_4 = V_{IH}$ , $V_{P(CE)} = \overline{CE}_2$	20.5	21.0	21.5	V
Programming voltage limit	V <sub>OP(max)</sub>	Programming current ramp voltage limit	24	25	26	V
Power supply	V <sub>CC</sub>		6.3	6.5	6.7	V
Power supply current	I <sub>CC</sub>				250	mA
Chip enable current	I <sub>CE</sub>				150	mA
Initial value of programming current ramp	I <sub>OP(INIT)</sub>		19	20	21	mA
Maximum value of programming current ramp	I <sub>OP(max)</sub>		155	160	165	mA
Programming current ramp (linear slew rate)	SRI <sub>OP</sub>		0.9	1.0	1.1	mA/μs
V <sub>CC</sub> pulse rise time	t <sub>r</sub> (V <sub>CC</sub> )		0.2	2.0		μs
V <sub>CC</sub> pulse fall time	t <sub>f</sub> (V <sub>CC</sub> )		0.2	2.0		μs
Chip enable rise time	t <sub>r</sub> ( $\overline{CE}_2$ )		3.0	4.0		μs
Chip enable fall time	t <sub>f</sub> ( $\overline{CE}_2$ )		0.2	4.0		μs
Programming current ramp fall time	t <sub>f</sub> (I <sub>OP</sub> )			0.1	0.2	μs
Hold time after programming	t <sub>hap</sub>		1.4	1.5	1.6	μs
Time to reach I <sub>OP</sub> initial	t <sub>IOP</sub>		0.5	1.0	2.0	μs
Delay to start V <sub>ps</sub> sense	t <sub>dss</sub>		2.0	3.0	4.0	μs
Delay to chip enable pulse	t <sub>dce</sub>			1.0		μs
Delay to programming ramp	t <sub>d</sub> (I <sub>OP</sub> )		2.0	3.0	10	μs
Delay after programming to CE <sub>1</sub>	t <sub>dRAP</sub>		2.0	3.0	10	μs
Delay to read after programming	t <sub>dRAP</sub>	Programming verification	2.0	3.0		μs

See footnote at end of table.

TABLE IVD. Programming characteristics for circuit D – Continued.

Parameter	Symbol	Conditions <sup>1/</sup>	Limits			Unit
			Min	Recommended	Max	
Delay to V <sub>CC</sub> off	t <sub>D(VCC)</sub>			1.0		μs
Delay to read before programming	t <sub>dRBP</sub>	Initial check	2.0	3.0		μs
Width to read compare strobe	t <sub>W</sub>			1.0		μs
Voltage change at programming	V <sub>ps</sub>	Typical 2.0 V	0.7	2.0		V
Time to program bit	t <sub>tp</sub>	V <sub>ps</sub> sensing circuit will automatically adjust this time				
Duty cycle power		Maximum duty cycle to maintain in T <sub>C</sub> < +85°C		50		%
Case temperature	T <sub>C</sub>		25	85		°C

<sup>1/</sup> T<sub>C</sub> = +25°C.

4.11 Programming procedure for circuit E. The waveforms on figure 5E, the programming characteristics in table IVE and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Terminate all outputs with a  $300\ \Omega$  resistor to  $V_{ONP}$ . Apply  $V_{IHP}$  to the  $\overline{CE}_2$ ,  $CE_3$ , and  $CE_4$  inputs and  $V_{ILP}$  to the  $\overline{CE}_1$  inputs.
- c. Address the PROM with the binary address of the selected word to be programmed. Raise  $V_{CC}$  to  $V_{CCP}$ .
- d. After a delay of  $t_1$ , apply only one  $V_{OP}$  pulse with a duration of  $t_p$ ,  $t_2$ , and  $d(V_{OP}) / dt$  to the output selected for programming. After a delay of  $t_2$  and  $d(V_{OP}) / dt$ , pulse  $\overline{CE}_2$  from  $V_{IHP}$  to  $V_{CEP}$  for the duration of  $t_p$ ,  $2d(V_{CE}) / dt$ , and  $t_3$ ;  $\overline{CE}_2$  is then to go to the  $V_{ILP}$  level.
- e. To verify programming after  $\overline{CE}_1$  has been set to  $V_{ILP}$ , lower  $V_{CC}$  to  $V_{CCL}$  after a delay of  $t_4$ . The programmed output should remain in the logic "1" state.
- f. The outputs should be programmed one output at a time since the internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a low level logic output. Programming a fuse will cause the output to go to a high level logic in the verify mode.
- g. Repeat 4.11c through 4.11f for all other bits to be programmed.
- h. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVE. Programming characteristics for circuit E.

Parameter	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
V <sub>CC</sub> required during programming	V <sub>CCP</sub>		5.0		5.5	V
High level input voltage during programming	V <sub>IHP</sub>		2.4		5.5	V
Low level input voltage during programming	V <sub>ILP</sub>		0.0		0.45	V
Chip enable voltage during programming	V <sub>CEP</sub>	$\overline{CE}_1$ pin	14.5		15.5	V
Output voltage during programming	V <sub>OP</sub>		19.5		20.5	V
Voltage on outputs not to be programmed	V <sub>ONP</sub>		0		V <sub>CCP</sub> +0.3	V
Current on outputs not to be programmed	I <sub>ONP</sub>				20	mA
Rate of output voltage change	d(V <sub>OP</sub> ) / dt		20		250	V/μs
Rate of chip enable voltage change	d(V <sub>CE</sub> ) / dt	$\overline{CE}_1$ pin	100		1000	V/μs
Programming period	t <sub>p</sub>		50		100	μs
V <sub>CC</sub> during programming verification	V <sub>CCL</sub>		4.5		5.0	μs

4.12 Programming procedure for circuit F. The waveforms on figure 5F, the programming characteristics in table IVF and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Raise  $V_{CC}$  to 5.5 volts.
- c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.
- d. Disable the chip by applying  $V_{IH}$  to the  $\overline{CE}$  inputs and  $V_{IL}$  to the  $\overline{CE}$  inputs. The chip enable inputs are TTL compatible.
- e. Apply the  $V_{PP}$  pulse to the programming pin ( $\overline{CE}_2$ ). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by  $T_{D1}$  and leave after the output pin's programming pulse by  $T_{D2}$  (see figure 5F).
- f. Apply only one  $V_{OUT}$  pulse with duration of  $t_p$  to the output selected for programming. The outputs shall be programmed one output at a time since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low level logic in the verify mode.
- g. Other bits in the same word may be programmed sequentially by applying  $V_{OUT}$  pulses to each output to be programmed.
- h. Repeat 4.12c through 4.12g for all other bits to be programmed.
- i. Enable the chip by applying  $V_{IL}$  to the  $\overline{CE}$  inputs and  $V_{IH}$  to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at  $V_{CC} = 4.2$  V and 0.2 mA at  $V_{CC} = 6.2$  V at  $T_C = 25^\circ\text{C}$ .
- j. For classes S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVF. Programming characteristics for circuit E.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Recommended	Max	
V <sub>CC</sub> required during programming	V <sub>CCP</sub>		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t <sub>TLH</sub>		0.34	0.40	0.46	V/μs
Programming voltage on programming pin	V <sub>PP</sub>		32.5	33	33.5	V
Output programming voltage	V <sub>OUT</sub>		25.5	26	26.5	V
Programming pin pulse width ( $\overline{CE}$ )	t <sub>PP</sub>	Chip disabled, V <sub>CC</sub> = 5.5 V		100	180	ns
Pulse width of programming voltage	t <sub>P</sub>	Chip disabled, V <sub>CC</sub> = 5.5 V	1		40	μs
Required current limit of power supply feeding programming pin and output during programming	I <sub>L</sub>	V <sub>PP</sub> = 33 V, V <sub>OUT</sub> = 26 V, V <sub>CC</sub> = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T <sub>D1</sub>	Measured at 10% levels	70	80	90	μs
Required time delay between removal of programming pulse and enabling memory output	T <sub>D2</sub>	Measured at 10% levels	100			ns
Output current during verification	I <sub>OLV1</sub>	Chip enabled, V <sub>CC</sub> = 4.2 V	11	12	13	mA
	I <sub>OLV2</sub>	Chip enabled, V <sub>CC</sub> = 6.2 V	0.19	0.2	0.21	mA
Address input voltage	V <sub>IH</sub>		2.4	5.0	5.5	V
	V <sub>IL</sub>		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C	t <sub>P</sub> / t <sub>C</sub>			25	%

1/ T<sub>C</sub> = +25°C.

4.13 Programming procedure for circuit G. The waveforms on figure 5G, the programming characteristics in table IVG and the following procedures shall apply for programming the device:

- a. Connect the device in the electrical configuration for programming.
- b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more active low chip enable inputs. Note that the address and enable inputs must be driven with TTL logic levels during programming and verification.
- c. Increase  $V_{CC}$  from nominal to  $V_{CCP}$  ( $10.5 \pm 0.5$  V) with a slew rate limit of  $I_{RR}$  (1.0 to 10.0 V/ $\mu$ s). Since  $V_{CC}$  is the source of the current required to program the fuse, as well as the  $I_{CC}$  for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.
- d. Select the output where a logical high is desired by raising that output voltage to  $V_{OP}$  ( $10.5 \pm 0.5$  V). Limit the slew rate to  $I_{RR}$  (1.0 to 10.0 V/ $\mu$ s). This voltage change may occur simultaneously with the  $V_{CC}$  increase to  $V_{CCP}$ , but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 k $\Omega$  minimum (remember that the outputs of the device are disabled at this time).
- e. Enable the device by taking the chip enables to a low level. This is done with a pulse  $PWE$  for 10  $\mu$ s. The 10  $\mu$ s duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
- f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing  $V_{CC}$  to 5.0 V ( $\pm 0.25$  V). The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified  $I_{OL}$  and  $I_{OH}$  limits.
- g. If the device is not to be tested for  $V_{OH}$  over the entire operating range subsequent to programming, the verification of step f is to be performed at a  $V_{CC}$  level of 4.0 volt ( $\pm 0.2$  V).  $V_{OH}$ , during the 4 volt verification, must be at least 2.0 volts. The 4 volt  $V_{CC}$  verification assures minimum  $V_{OH}$  levels over the entire operating range.
- h. Repeat steps 4.13b through 4.13f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of  $V_{CC}$  at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperature. After all selected bits are programmed, the entire contents of the memory should be verified.
- i. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVG. Programming characteristics for circuit G.

Parameter	Symbol	Conditions	Limits <u>1/</u>			Unit
			Min	Recommended	Max	
Required V <sub>CC</sub> for programming	V <sub>CCP</sub>		10.0	10.5	11.0	V
I <sub>CC</sub> during programming	I <sub>CCP</sub>	V <sub>CC</sub> = 11 V			750	mA
Required output voltage for programming	V <sub>OP</sub>		10.0	10.5	11.0	V
Output current while programming	I <sub>OP</sub>	V <sub>OUT</sub> = 11 V			20	mA
Rate of voltage change of V <sub>CC</sub> or output	I <sub>RR</sub>		1.0		10.0	V/μs
Programming pulse width (enabled)	PWE		9	10	11	μs
Required V <sub>CC</sub> for verification	V <sub>CCV</sub>		3.8	4.0	4.2	V
Maximum duty cycle for V <sub>CC</sub> at V <sub>CCP</sub>	MDC			25	25	%
Address setup time	t <sub>1</sub>		100			ns
V <sub>CCP</sub> set-up time	t <sub>2</sub>	<u>2/</u>	5			μs
V <sub>CCP</sub> hold time	t <sub>5</sub>		100			ns
V <sub>OP</sub> setup time	t <sub>3</sub>		100			ns
V <sub>OP</sub> hold time	t <sub>4</sub>		100			ns

1/ T<sub>C</sub> = +25°C.

2/ V<sub>CCP</sub> set-up time may be greater than 0 if V<sub>CCP</sub> rises at the same rate or faster than V<sub>OP</sub>.

## 5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirement for programming the device, including processing option.
- j. Requirements for "JAN" marking.
- k. Packaging Requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-38535) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQC, P.O. Box 3990, Columbus, OH 43218-3990 or email [vqc.chief@dla.mil](mailto:vqc.chief@dla.mil). An online listing of manufacturers qualified to this specification may be found in the Qualified Products Database (QPD) at <http://qpldocs.dla.mil/>.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND .....	Electrical ground (common terminal).
$I_{IN}$ .....	Current flowing into an input terminal.
$V_{IC}$ .....	Input clamp voltage.
$V_{IN}$ .....	Voltage level at an input terminal.

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type	Circuit designator	Fusible links
01 <u>1/</u>	7684 / Harris Semiconductor / CAGE 34371	A	NiCr
01	77S184 / National Semiconductor / CAGE 27014	G	TiW
01 <u>1/</u>	82S184 / Signetics Corporation / CAGE 18324	C	NiCr
02 <u>1/</u>	7685 / Harris Semiconductor / CAGE 34371	A	NiCr
02	77S185 / National Semiconductor / CAGE 27014	G	TiW / W
02, 10	82S185A / Signetics Corporation / CAGE 18324	C	NiCr
02, 08	29651 / Raytheon Company / CAGE 07933	F	NiCr
02	82S185 / e2v aerospace & defense / CAGE 0C7V7	H	ZVE <u>2/</u>
03	77S180 / National Semiconductor / CAGE 27014	G	TiW
03 <u>1/</u>	7680 / Harris Semiconductor / CAGE 34371	A	NiCr
03 <u>1/</u>	82S180 / Signetics Corporation / CAGE 18324	C	NiCr
03	93Z450 / Fairchild Corporation / CAGE 07263	D	ZVE <u>2/</u>
03	27S180 / Advanced Micro Devices, Inc. / CAGE 34335	E	Platinum silicide

See footnote at end of table.

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Military device type	Generic-industry type	Circuit designator	Fusible links
04	77S181 / National Semiconductor / CAGE 27014	G	TiW / W
04	82S181 / e2v aerospace & defense / CAGE 0C7V7	H	ZVE <u>2/</u>
04 <u>1/</u>	7681 / Harris Semiconductor / CAGE 34371	A	NiCr
04, 09	82S181A / Signetics Corporation / CAGE 18324	C	NiCr
04, 09	93Z451 / Fairchild Corporation / CAGE 07263	D	ZVE <u>2/</u>
04	27S181 / Advanced Micro Devices, Inc. / CAGE 34335	E	Platinum silicide
04	29631 / Raytheon Company / CAGE 07933	F	NiCr
05	82S2708 / Signetics Corporation / CAGE 18324	C	NiCr
05	93Z461 / Fairchild Corporation / CAGE 07263	D	ZVE <u>2/</u>
06	93Z460 / Fairchild Corporation / CAGE 07263	D	ZVE <u>2/</u>
02, 08	53S841 / Monolithic Memories, Inc. / CAGE 56364	B	TiW

1/ These generic industry types are no longer manufactured.

2/ Zapped vertical emitter.

6.8 Change from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:  
 Army - CR  
 Navy - EC  
 Air Force - 85  
 DLA - CC

Preparing activity:  
 DLA - CC

Review activities:  
 Army – SM, MI  
 Navy - AS, CG, MC, SH  
 Air Force – 03, 19, 99

(Project 5962-2014-002)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.