23AA02M/23LCV02M

2-Mbit SPI/SDI/SQI 143 Mhz Serial RAM with Optional Battery Backup

Device Selection Table

Part Number	Vcc Range	Temp. Ranges	Battery Backup	Power-Up State Mode	Packages
23AA02M	1.7V-3.6V	I	No	SPI	SN, ST, P
23LCV02M	2.2V-3.6V	I	Yes	SPI	SL, ST, P

Note: 23AA02M is only available in 8-lead while 23LCV02M is only available in 14-lead.

Features

- 2048-Kbit Low-Power SRAM
- Single Voltage Read and Write Operations
  - 1.7V to 3.6V (23AA02M)
  - 2.2V to 3.6V (23LCV02M)
- Serial Interface Architecture
  - SPI compatible: mode 0 and mode 3
  - SDI and SQI supported
- High-Speed Clock Frequency:
  - 143 MHz
- Superior Reliability
  - Built-In Error Correction Code (ECC) Logic
- Low-Power Consumption:
  - Active read current: 3 mA (max @ 40MHz, 3.6V) for SPI/SDI/SQI
  - Standby Current: 70 µA (typical @ 25°C)
- Unlimited Read and Write Cycles
- External Battery Backup Support (23LCV02M)
- Zero Write Time
- Organization
  - 256 x 8-bit Organization
  - User selectable page size (32 bytes or 256 bytes)
- Byte, Page and Sequential Mode for Reads and Writes
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
- RoHS Compliant, Halogen Free

Packages

- 8-Lead PDIP, 8-Lead SOIC and 8-Lead TSSOP
- 14-Lead PDIP, 14-Lead SOIC and 14-Lead TSSOP

Description

The Microchip Technology Inc. 23XX02M[1] is a 2-Mbit Serial SRAM device. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input. Additionally, SDI (Serial Dual Interface) and SQI (Serial Quad Interface) are supported if your application needs faster data rates.

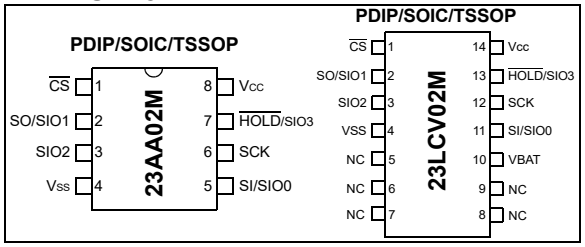
This device also supports unlimited reads and writes to the memory array.

Note 1: 23XX02M is used in this document as a generic part number for the 23AA02M/23LCV02M devices.

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select Input Pin
SO/SIO1	Serial Output/SDI/SQI Pin
SIO2	SQI Pin
VSS	Ground Pin
SI/SIO0	Serial Input/SDI/SQI Pin
SCK	Serial Clock Pin
$\overline{HOLD}$/SIO3	Hold/SQI Pin
VBAT	External Backup Supply Input
Vcc	Power Supply
NC	No Connect

Package Types (not to scale)



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 3.9V

All Inputs and Outputs w.r.t. V_{SS} ..... -0.3V to V_{CC} +0.3V

Storage Temperature ..... -65°C to +150°C

Ambient Temperature under Bias ..... -40°C to +85°C

ESD protection on all pins ..... 2 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

1.1 Power-Up Specifications

All functionalities and DC specifications are included for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 1-1 and Figure 1-1 for more information.

When V_{DD} drops from the operating voltage to below the minimum V_{DD} threshold at power-down, all operations are disabled and the device does not respond to commands (see Figure 1-2).

TABLE 1-1: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Max	Units	Condition
$T_{PU-READ}$ (1)	V_{DD} Min to Read operation	100		µs	
$T_{PU-WRITE}$ (1)	V_{DD} Min to Write operation	100		µs	
T_{PD} (1)	Power-down duration	1		ms	
V_{OFF} (1)	V_{DD} off voltage		0.2	V	0V recommended

Note 1: This parameter is not tested but is ensured by characterization.

FIGURE 1-1: POWER-UP TIMING DIAGRAM

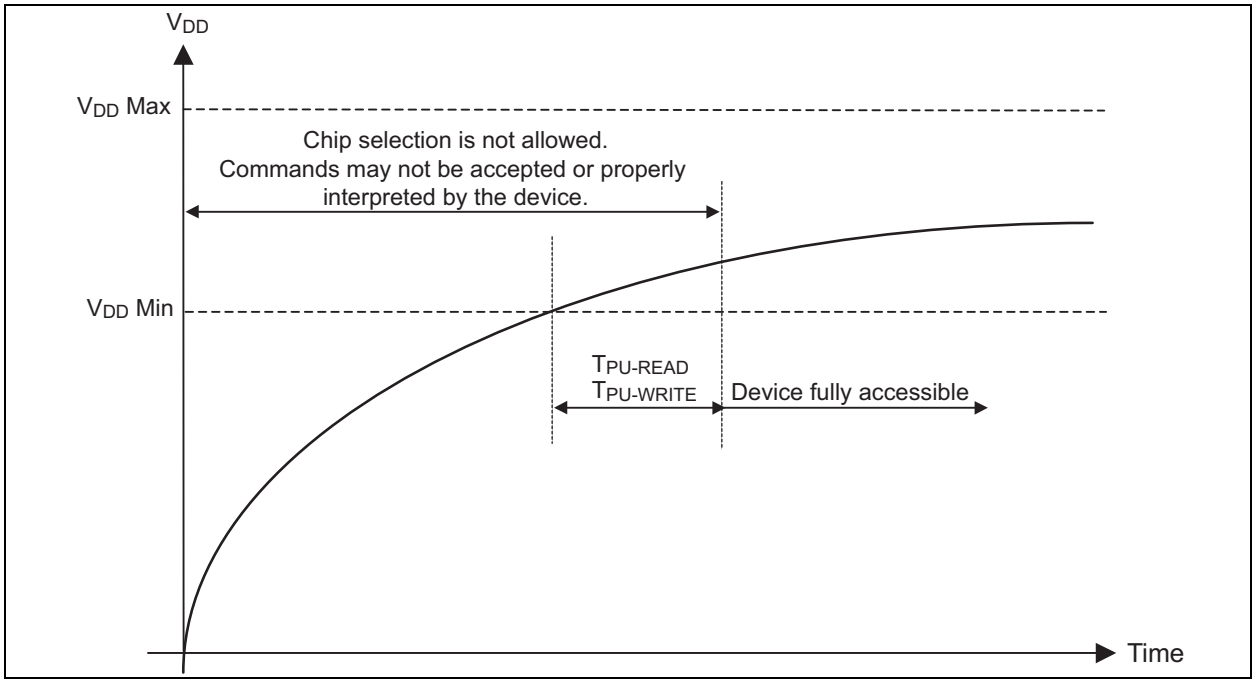

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FIGURE 1-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM

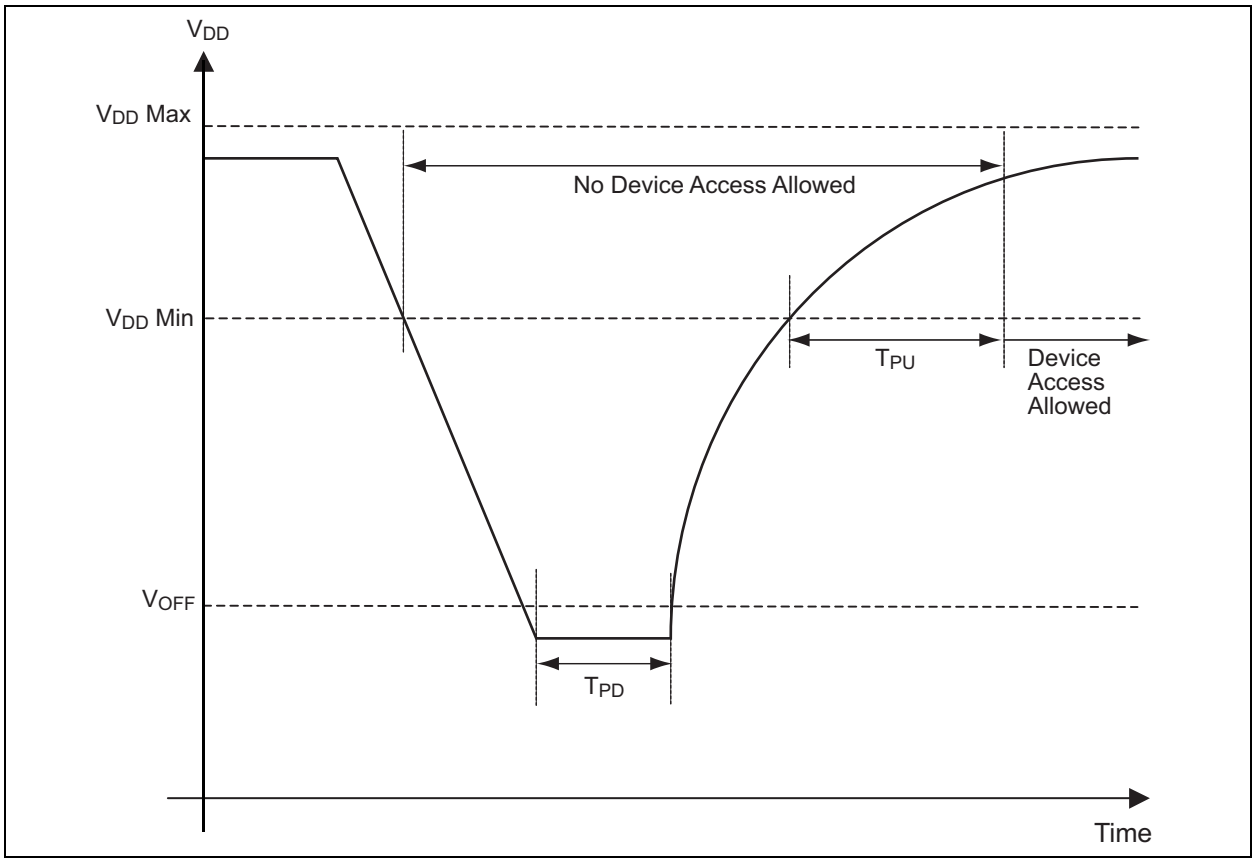

TABLE 1-2: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
D001	VCC	Supply Voltage	1.7	—	3.6	V	23AA02M
			2.2		3.6	V	23LCV02M
D002	VIH	High-level Input Voltage	0.7 VCC	—	—	V	
D003	VIL	Low-level Input Voltage	—	—	0.3 VCC	V	
D004	VOL	Low-level Output Voltage	—	—	0.4	V	IOL = 6 mA
D005	VOH	High-level Output Voltage	VCC - 0.5	—	—	V	IOH = -400 µA
D006	ILI	Input Leakage Current	—	—	1	µA	$\overline{CS}$ = VCC, VIN = VSS OR VCC
D007	ILO	Output Leakage Current	—	—	1	µA	$\overline{CS}$ = VCC, VOUT = VSS OR VCC

Note 1: Typical measurements taken at room temperature (+25°C).

2: This parameter is periodically sampled and not 100% tested.Typical measurements taken at room temperature.

3: This is the limit to which VCC can be lowered without losing RAM data at TA=+25°C. This parameter is periodically sampled and not 100% tested.

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DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C				
Param. No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
D008	IDDR	Operating Current	—	—	3	mA	VCC = 3.6V; SO = O, FCLK = 40 MHz
					10	mA	VCC = 3.6V; SO = O, FCLK = 143 MHz
D009	ISB1	Standby Current	—	70	250	µA	$\overline{CS}$ = VCC, Inputs tied to VCC or VSS, TA = 85°C (Note 1)
D010	CINT	Input Capacitance	—	—	7	pF	VCC = 3.6V, f = 1 MHz, T_A = 25°C (Note 2)
D011	VDR	RAM Data Retention Voltage	—	1.0	—	V	Note 3
D012	VTRIP	VBAT Change Over	1.75	1.85	1.95	V	Note 2
D013	VBAT	VBAT Voltage Range	1.4	—	3.6	V	Note 2
D014	IBAT1	VBAT Current	—	70	250	µA	$\overline{CS}$ = VCC, Inputs tied to VCC or VSS, TA = 85°C (Note 1)

Note 1: Typical measurements taken at room temperature (+25°C).

2: This parameter is periodically sampled and not 100% tested.Typical measurements taken at room temperature.

3: This is the limit to which VCC can be lowered without losing RAM data at TA=+25°C. This parameter is periodically sampled and not 100% tested.

TABLE 1-3: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C					
Param. No.	Sym.	Characteristic	40 MHz		143 MHz		Units	Test Conditions
			Min.	Max.	Min.	Max.		
1	FCLK	Clock Frequency	—	40	—	143	MHz	Note 1
2	TCSS	$\overline{CS}$ Setup Time	5	—	3	—	ns	Note 2
3	TCSH	$\overline{CS}$ Hold Time	5	—	3	—	ns	Note 3
4	TCSD	$\overline{CS}$ Disable Time	20	—	10	—	ns	
5	TSU	Data Setup Time	5	—	2	—	ns	
6	THD	Data Hold Time	5	—	2	—	ns	
7	TR	CLK Rise Time	0.1	—	0.1	—	ns	Note 2 and Note 4
8	TF	CLK Fall Time	0.1	—	0.1	—	ns	Note 2 and Note 4
9	THI	Clock High Time	10	—	2.8	—	ns	
10	TLO	Clock Low Time	10	—	2.8	—	ns	
11	TCLD	Clock Delay Time	5	—	3	—	ns	
12	TV	Output Valid from Clock Low	—	8	—	7	ns	
13	THO	Output Hold Time	0	—	0	—	ns	Note 4
14	TDIS	Output Disable Time	—	9	—	9	ns	

Note 1: Maximum clock frequency for Read Instruction, 03H, is 40 MHz.

2: Maximum Rise and Fall Time may be limited by THI and TLO requirements.

3: Relative to SCK.

4: This parameter is periodically sampled and not 100% tested. Typical measurements taken at room temperature (25°C).

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TABLE 1-3: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C					
Param. No.	Sym.	Characteristic	40 MHz		143 MHz		Units	Test Conditions
			Min.	Max.	Min.	Max.		
15	TCLZ	SCK Low to Output Low-Z	0	—	0	—	ns	
16	TCHH	$\overline{CS}$ Not Active Hold Time	5	—	3	—	ns	Note 3
17	THS	$\overline{HOLD}$ Setup Time	5	—	1.4	—	ns	
18	THH	$\overline{HOLD}$ Hold Time	5	—	1.4	—	ns	
19	THZ	$\overline{HOLD}$ Low to Output High-Z	—	9	—	9	ns	
20	THV	$\overline{HOLD}$ High to Output Valid	—	9	—	9	ns	

Note 1: Maximum clock frequency for Read Instruction, 03H, is 40 MHz.

2: Maximum Rise and Fall Time may be limited by THI and TLO requirements.

3: Relative to SCK.

4: This parameter is periodically sampled and not 100% tested. Typical measurements taken at room temperature (25°C).

TABLE 1-4: AC TEST CONDITIONS

AC Waveform	
Input Pulse Level	0.1 VCC to 0.9 VCC
Input Rise/Fall Time	5 ns
C_L = 30 pF	—
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

FIGURE 1-3: SERIAL INPUT TIMING

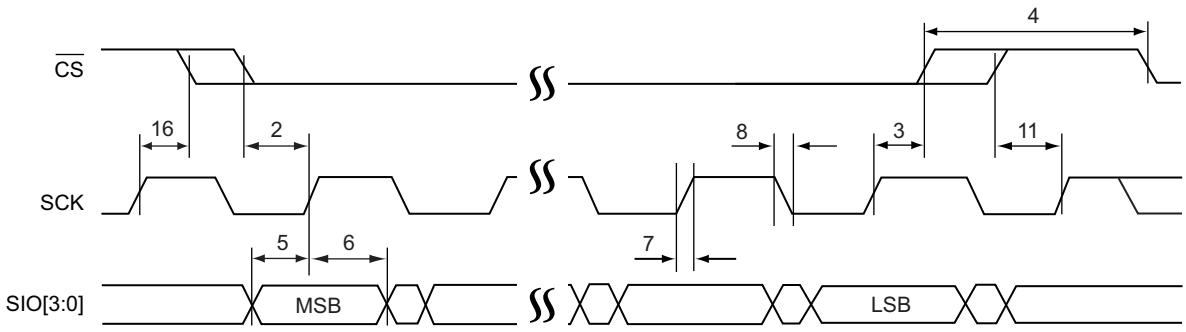

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FIGURE 1-4: SERIAL OUTPUT TIMING

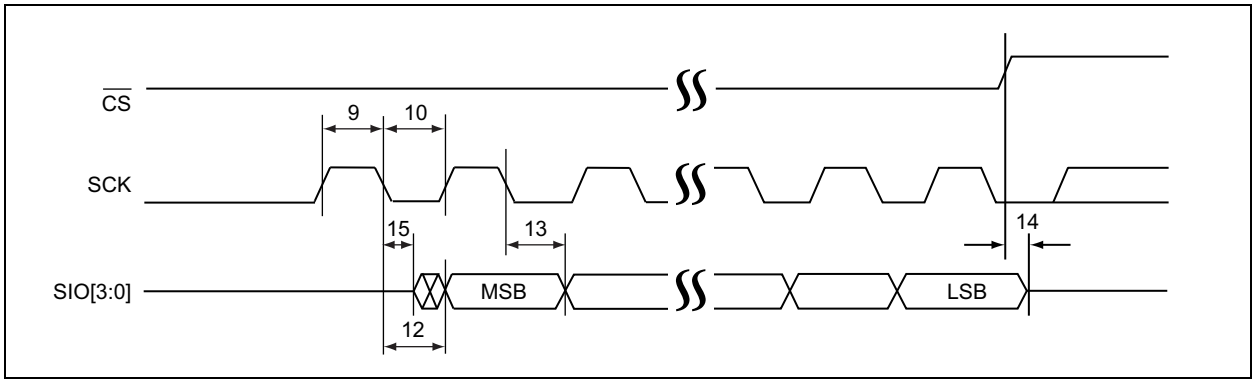
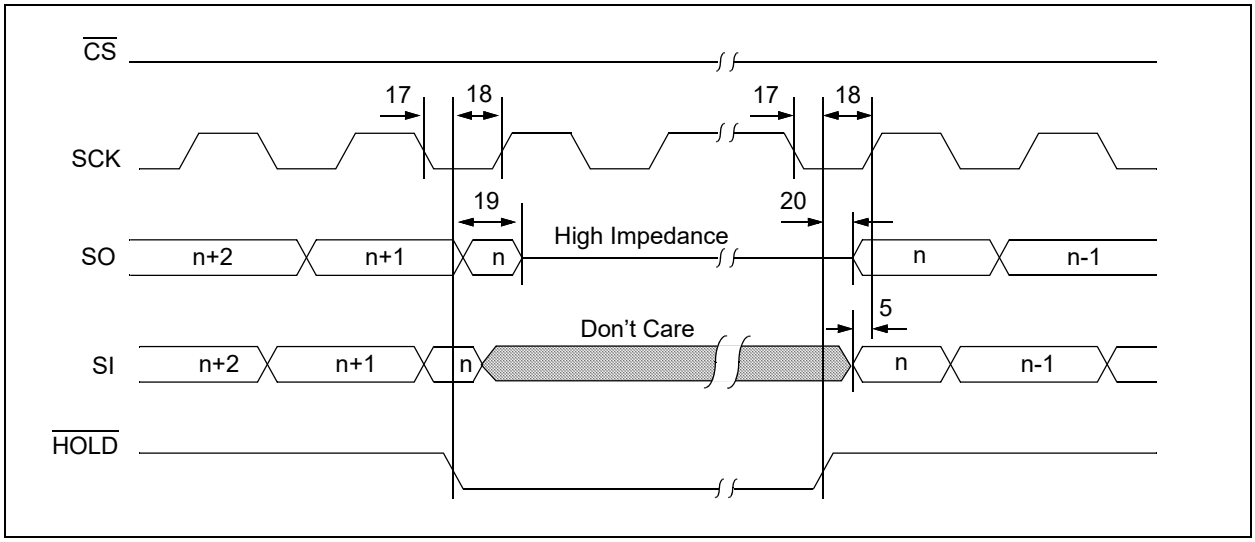


FIGURE 1-5: HOLD TIMING



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2.0 PIN DESCRIPTION

The description of the pins is listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

8-Lead SOIC/PDIP/TSSOP	14-Lead SOIC/PDIP/TSSOP	Pin Name	Pin Function
1	1	$\overline{CS}$	Chip Select
2	2	SO/SIO1	Serial Output, I/O in Dual and Quad mode
3	3	SIO2	Quad I/O Pin in Quad mode
4	4	VSS	Ground
5	11	SI/SIO0	Serial Input, I/O in Dual and Quad mode
6	12	SCK	Serial Clock
7	13	$\overline{HOLD}$/SIO3	$\overline{HOLD}$ Pin in SPI/SDI, I/O Pin in Quad mode
8	14	VCC	+1.7V to +3.6V Power Supply **(23AA02M)**, +2.2V to +3.6V Power Supply **(23LCV02M)**
—	5, 6, 7, 8, 9	NC	No Connect
—	10	VBAT	External Battery Supply Input

2.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. When the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

2.2 SO/SIO1

The SO pin is used to transfer data out of the device. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock. This pin is also an SIO1 pin when the device is in SDI or SQI mode. The SIO1 pin is used both as an input and an output pin during communication. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock. During a write cycle, data are shifted in on this pin after the rising edge of the serial clock.

2.3 SIO2

This pin is used when the device is in SQI mode. The SIO2 pin is used both as an input and an output pin during communication. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock. During a write cycle, data are shifted in on this pin after the rising edge of the serial clock.

2.4 VSS

This pin is a Ground Pin.

2.5 SI/SIO0

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data are latched on the rising edge of the serial clock. This pin is also an SIO0 pin when the device is in SDI or SQI mode. The SIO0 pin is used both as an input and an output pin during communication. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock. During a write cycle, data are shifted in on this pin after the rising edge of the serial clock.

2.6 Serial Clock (SCK)

The SCK is used to synchronize the communication between a host and the device. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin are updated after the falling edge of the clock input.

2.7 $\overline{Hold}$/SIO3

This pin is used as a $\overline{HOLD}$ pin when the device is used in SPI or SDI mode. This pin is also an SIO3 pin when the device is in SQI mode. The SIO3 pin is used both as an input and an output pin during communication. During a read cycle, data are shifted out on this pin after the falling edge of the serial clock. During a write cycle, data are shifted in on this pin after the rising edge of the serial clock.

2.8 VCC

This pin provides power to the device. The normal operating voltage range is from 1.7V to 3.6V for 23AA02M and 2.2V to 3.6V for 23LCV02M.

2.9 VBAT Supply Input

The VBAT pin is used as an input for external backup supply to maintain SRAM data when VCC is below the VTRIP point. If the VBAT function is not being used it is recommended to connect this pin to VSS.

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3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The Microchip Technology Inc. 23XX02M is a 2-Mbit Serial SRAM device. The memory is accessed via a Serial Peripheral Interface (SPI) compatible serial bus. The memory also supports SDI mode, a 2-bit I/O interface and a Serial Quad I/O™ (SQI™), 4-bit I/O interface that allows high-performance operation in a low pin-count package. The bus signals required are a clock input (SCK) plus separate data lines (SI/SIO0, SO/SIO1, SIO2, SIO3). Access to the device is controlled through a Chip Select (CS) input. Communication to the device in SPI and SDI mode can be paused via the hold pin ($\overline{\text{HOLD}}$). While the device is paused, transitions on its inputs will be ignored, allowing the host to service higher priority interrupts.

The 23LCV02M has a VBAT pin, which connects to an external backup battery and allows for non-volatile operation. Automatic switching to the backup battery occurs when VCC supply falls below VTRIP level without loss of data. In addition to the SRAM array, the settings in the STATUS register are also retained by the battery. When VCC voltage is restored, the battery is automatically disconnected, and normal operation is restored.

3.2 Device Operation

The 23XX02M supports Serial Peripheral Interface (SPI) bus protocol, a 2-bit multiplexed SDI bus mode and a 4-bit multiplexed SQI bus mode. The 23XX02M defaults to SPI mode after a power-on reset to provide backward compatibility.

An `EDIO` command instruction configures the device to SDI mode. The dataflow in the SDI mode is similar to the SPI mode, except it uses two multiplexed I/O signals for command, address, and data sequence. The device supports both mode 0 (0,0) and mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred.

The SCK signal is low for mode 0 and SCK signal is high for mode 3. For both modes, the Serial Data I/O (SIO[1:0]) is sampled at the rising edge of the SCK clock signal for input and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as, shown in Figure 3-1. The SDI mode uses two multiplexed signals, SIO[1:0], for both data in and data out, as shown in Figure 3-2. This means the SDI mode doubles the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package. A `RSTIO` command instruction resets the device to SPI mode.

An `EQIO` command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address, and data sequence. The device supports both mode 0 (0,0) and mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus host is in Standby mode and no data are being transferred.

The SCK signal is low for mode 0 and SCK signal is high for mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals, as shown in Figure 3-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 3-3. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package. A `RSTIO` command instruction resets the device to SPI mode.

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FIGURE 3-1: SPI PROTOCOL

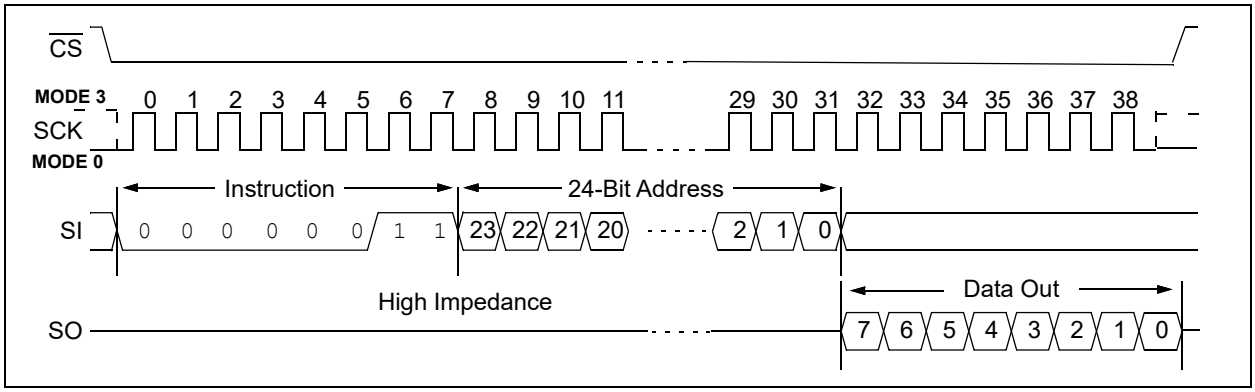


FIGURE 3-2: SDI PROTOCOL

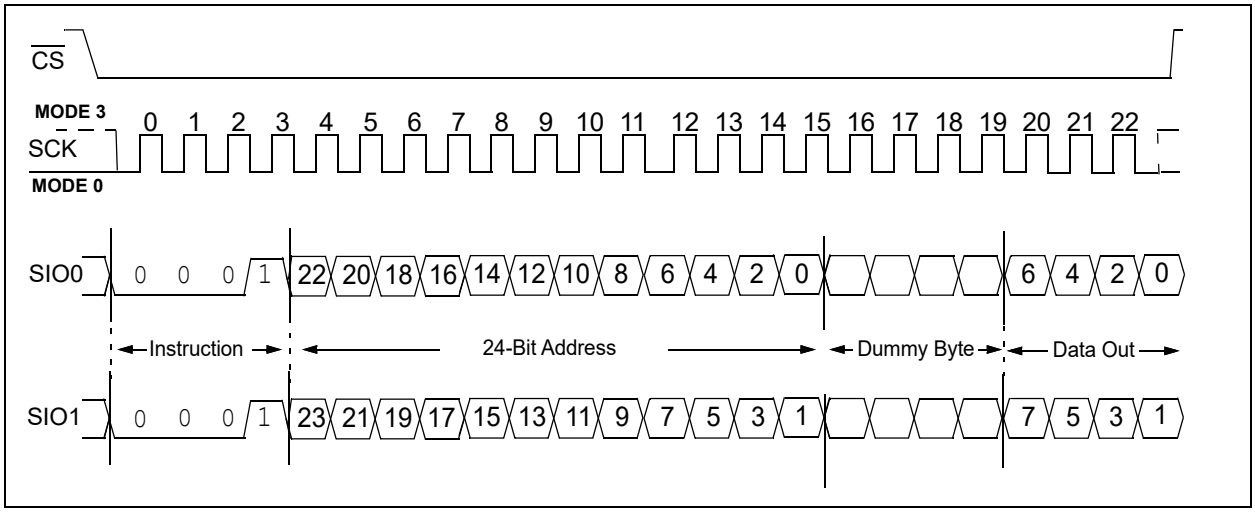
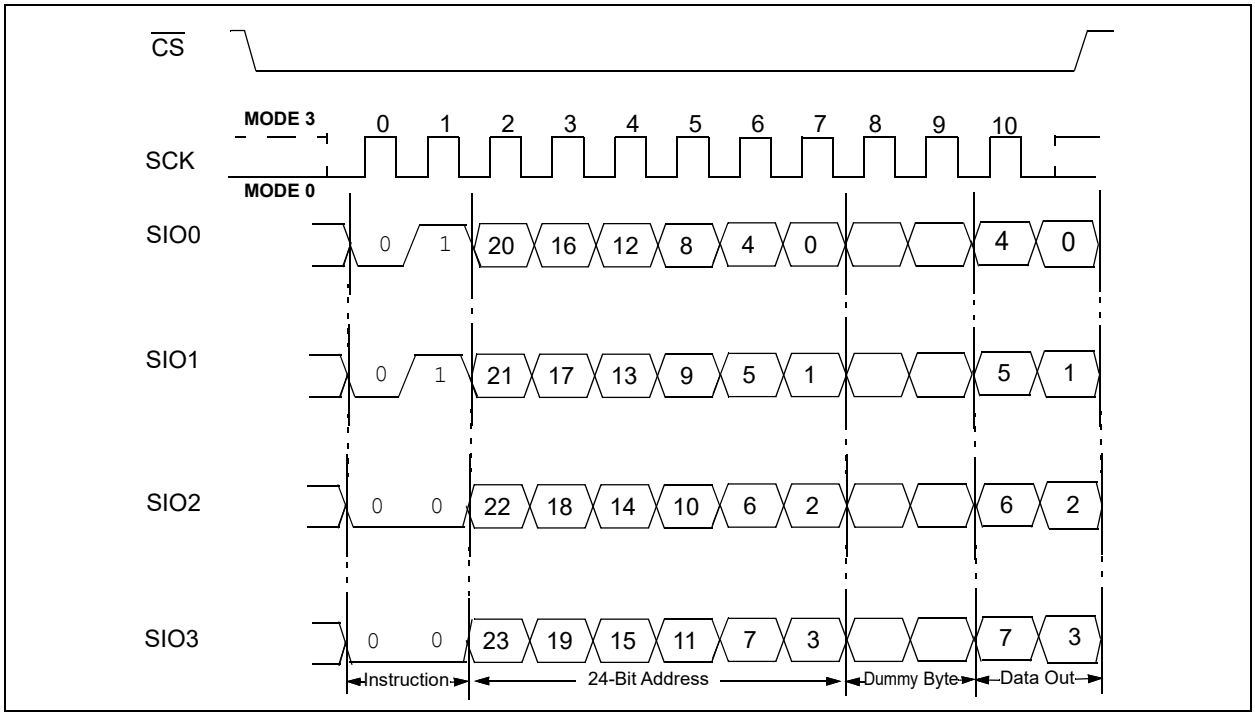


FIGURE 3-3: SQI PROTOCOL



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3.3 INSTRUCTIONS

Instructions are used to read, write and configure the 23XX02M. A complete list of instructions is provided in Table 3-1. All instructions, addresses and data are transferred MSb first, LSb last.

TABLE 3-1: DEVICE OPERATION INSTRUCTIONS FOR 23AA02M

Instruction	Description	Command Byte(1)	Interface			Address Bytes(1, 2)	Dummy Bytes(1)	Data Bytes(1)	Max Frequency
			SPI	SDI	SQI				
READ	Read Memory	0x03	X			3	0	1 to ∞	40 MHz
				X			1		
					X		1		
High-Speed Read	Read Memory	0x0B	X			3	1	1 to ∞	143 MHz
				X			3		
					X		3		
WRITE	Write to Memory	0x02	X	X	X	3	0	1 to ∞	143 MHz
EDIO	Enter Dual I/O mode	0x3B	X			0	0	0	143 MHz
EQIO	Enter Quad I/O mode	0x38	X			0	0	0	143 MHz
RSTIO(3,4)	Reset Dual or Quad I/O mode	0xFF	X	X	X	0	0	0	143 MHz
RDSR	Read STATUS Register	0x05	X			0	0	1 to ∞	143 MHz
				X	X	0	1		
WRSR	Write to STATUS Register	0x01	X	X	X	0	0	2	143 MHz

Note 1: Command Bytes, Address Bytes, Dummy Bytes and Data Bytes are two clock periods in SQI mode, four clock periods in SDI mode and eight clock periods in SPI mode.
2: Address bits above the most significant bit of each density are ignored and can be V_{IL} or V_{IH}.
3: Device accepts eight-clock command in SPI mode, four-clock command in SDI mode and two-clock command in SQI mode.
4: Device accepts RSTIO command with eight clocks with all SIO pins high regardless of current communication mode.

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3.4 $\overline{\text{HOLD}}$ OPERATION

The $\overline{\text{HOLD}}$/SIO3 pin functions as either a hold pin or an I/O pin. The $\overline{\text{HOLD}}$/SIO3 pin functions as a $\overline{\text{HOLD}}$ pin only when the device is in SPI mode or SDI mode. The $\overline{\text{HOLD}}$ pin is used to pause serial sequences underway with the memory without resetting the clocking sequence.

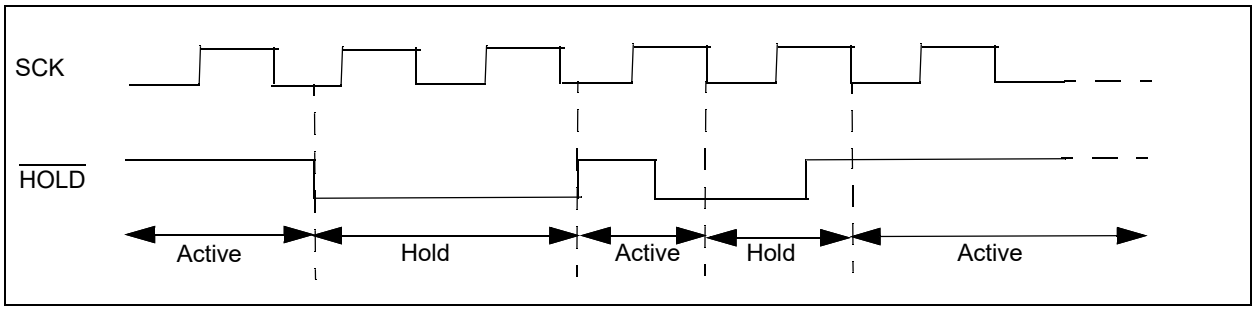
To activate Hold mode, $\overline{\text{CS}}$ must be in active-low state. Hold mode begins when the SCK active-low state coincides with the falling edge of the $\overline{\text{HOLD}}$ signal. Hold mode ends when the $\overline{\text{HOLD}}$ signal's rising edge coincides with the SCK active-low state.

If the falling edge of the $\overline{\text{HOLD}}$ signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the $\overline{\text{HOLD}}$ signal does not coincide with the SCK active-low state, then the device exits Hold mode when the SCK next reaches the active-low state. See Figure 3-4 for Hold Condition waveform.

The SO line will tri-state immediately upon a high-to-low transition of the $\overline{\text{HOLD}}$ pin and will begin outputting again immediately upon a subsequent low-to-high transition of the HOLD pin, independent of the state of SCK.

If $\overline{\text{CS}}$ is driven active-high during a Hold condition, it resets the internal logic of the device. As long as the $\overline{\text{HOLD}}$ signal is low, the memory remains in the Hold condition. To resume communication with the device, $\overline{\text{HOLD}}$ must be driven active-high, and $\overline{\text{CS}}$ must be driven active-low. See Figure 3-4 for Hold timing.

FIGURE 3-4: HOLD CONDITION WAVEFORM



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3.5 STATUS REGISTER

The STATUS register shown in Table 3-2 provides Status bits to indicate if an Error Correction Code (ECC) scheme was used during the previously executed read command and provides mode bits to configure the page size. It also allows the user to configure the output driver to improve signal integrity.

TABLE 3-2: STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
15,14	MODE	00 = Byte operation 10 = Page operation 01 = Sequential operation	01	R/W
13	ECS	Error Correction State Latch bit 1 = The previously executed read command did require the Error Correction Code (ECC) scheme 0 = The previous executed read command did not require the Error Correction Code (ECC) scheme	0	R
12,11	PROT	Indicates current bus protocol 00 = SPI 01 = SDI 10 = SQI	00	R
10,9	RES	Reserved for future use	00	R
8	PAGE SIZE	Sets number of bytes per page 0 = 32 Bytes per Page 1 = 256 Bytes per Page	0	R/W
7,6,5	RES	Reserved for future use	000	R
4,3	SR	Output Slew Rate 00 = 1.44 V/ns 01 = 2.88 V/ns 10 = 4.33 V/ns 11 = 6.00 V/ns	10	R/W
2,1,0	DRV	Output Drive Strength 000 = 12.5% 001 = 25% 010 = 35% 011 = 42.5% 100 = 50% 101 = 60% 110 = 75% 111 = 100%	100	R/W

3.5.1 OUTPUT DRIVE STRENGTH

The DRV bits configure the output drive strength.

3.5.2 OUTPUT SLEW RATE

The SR bits configure the output slew rate.

3.5.3 PAGE SIZE

The Page Size bit configures the page size to be either 32 bytes per page or 256 bytes per page.

3.5.4 PROT

The PROT bits indicate whether the device is currently using SPI, SDI or SQI bus protocol.

3.5.5 ERROR CORRECTION STATE LATCH

The Error Correction State (ECS) bit indicates whether the on-chip Error Correction Code (ECC) logic scheme was invoked during the previous read operation. For more information related to ECC, refer to **Section 3.15 "ERROR CORRECTION CODE (ECC)"**. The ECS bit will be set to logic '0' unless the previously executed read operation required the use of the ECC logic scheme. When this occurs the ECS bit will set to logic '1'.

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The ECS bit will continue to read a logic '1' until another read operation occurs where the use of the ECC logic scheme is not required or a Power-on Reset (PoR) event occurs.

3.5.6 MODE BITS

The mode bits indicate the mode of the read/write operation. The three modes of operation supported are Byte operation, Page operation and Sequential operation.

Byte Operation – is selected when bits 15 and 14 in the STATUS register are set to '00'. In this mode, the read/write operations are limited to only one byte. The command, followed by the 24-bit address, is clocked into the device and the data to/from the device is transferred on the next eight clocks (e.g. Figure 3-5, Figure 3-19).

Page Operation – is selected when bits 15 and 14 in the STATUS register are set to '10'. Page size is determined by bit 8 in the STATUS register. Page size is 32 bytes when bit 8 in the STATUS register is equal to '0' and 256 bytes when bit 8 in the STATUS register is equal to '1'. The 23XX02M has 8,192 pages of 32 bytes/1,024 pages of 256 bytes. In this mode, the read and write operations are limited to within the addressed page (the address is automatically incremented internally). If the data being read or written reach the page boundary, then the internal address counter will increment to the start of the page (e.g. Figure 3-6, Figure 3-20).

Sequential Operation – is selected when bits 15 and 14 in the STATUS register are set to '01'. Sequential operation allows the entire array to be written to and read from. The internal address counter is automatically incremented, and page boundaries are ignored. When the internal address counter reaches the end of the array, the address counter will roll over to 0x00000 (e.g. Figure 3-7, Figure 3-21).

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3.6 READ INSTRUCTION

The Read instruction is supported in SPI mode, SDI mode and SQI mode with clock frequency up to 40 MHz. The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` (0x03) instruction is transmitted to the device, followed by the 24-bit address, and then by dummy cycles, if required (see Table 3-1). After the `READ` instruction, address and dummy are sent, the data stored in the memory at the selected address are shifted out on the output pins. The number of bytes read will depend on the mode of operation of the device (i.e., byte operation, page operation or sequential operation).

If operating in Byte mode, one data byte at the specified address is read out, as shown in Figure 3-5 and Figure 3-8. If the host continues clocking the device, the same data byte will continue to be read out.

If operating in Page mode, the data stored within the page is read out starting with the specified address. Page size is either 32 bytes per page or 256 bytes per page based on the Page Size bit selection in the STATUS register. If the data being read reach the page boundary, then the internal address counter will increment to the start of the page, as shown in Figure 3-6 and Figure 3-9.

If operating in Sequential mode, the data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next highest address after each byte of data is shifted out, as shown in Figure 3-7. When the highest address is reached (3FFFFh), the address counter rolls over to address 00000h, allowing the read cycle to continue indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin.

The device will reject read instructions that have an insufficient number of clocks in the command byte/address byte.

FIGURE 3-5: BYTE READ (SPI MODE)

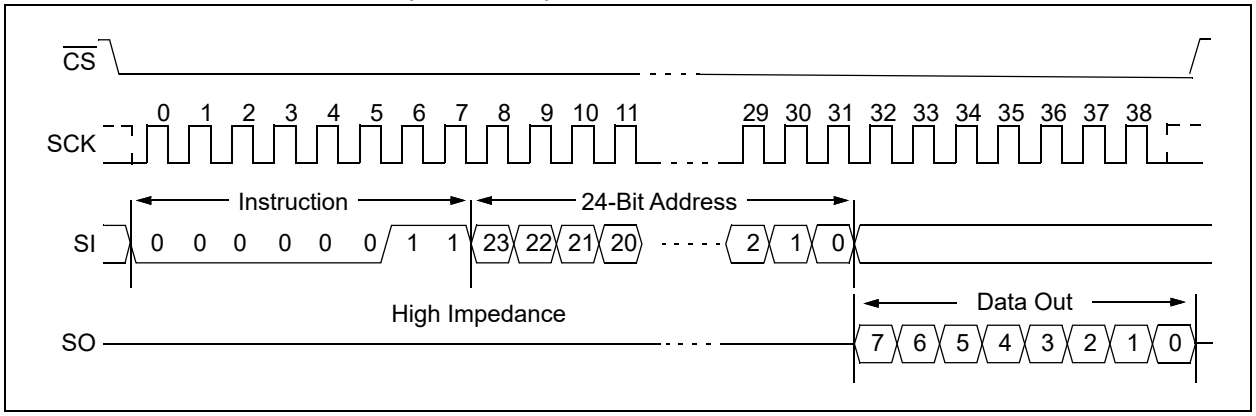

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FIGURE 3-6: PAGE READ (SPI MODE)

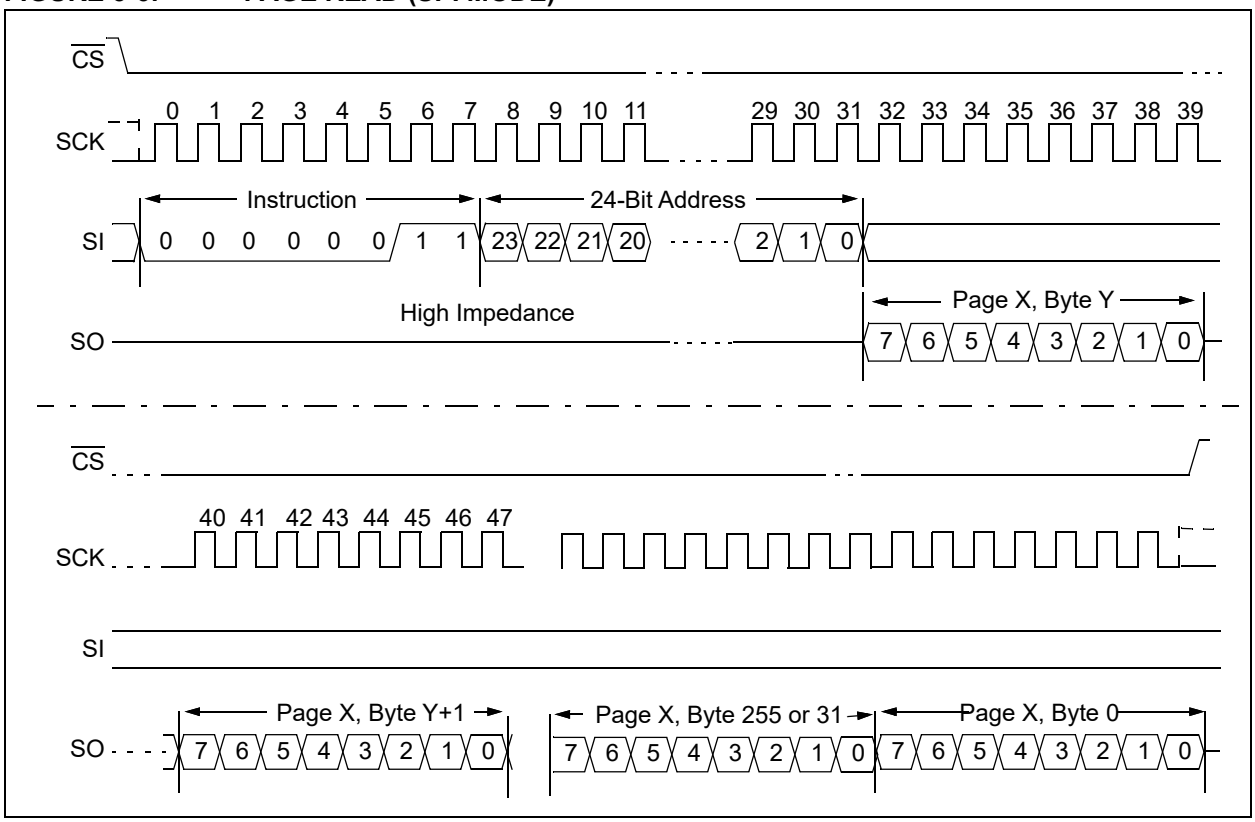

FIGURE 3-7: SEQUENTIAL READ (SPI MODE)

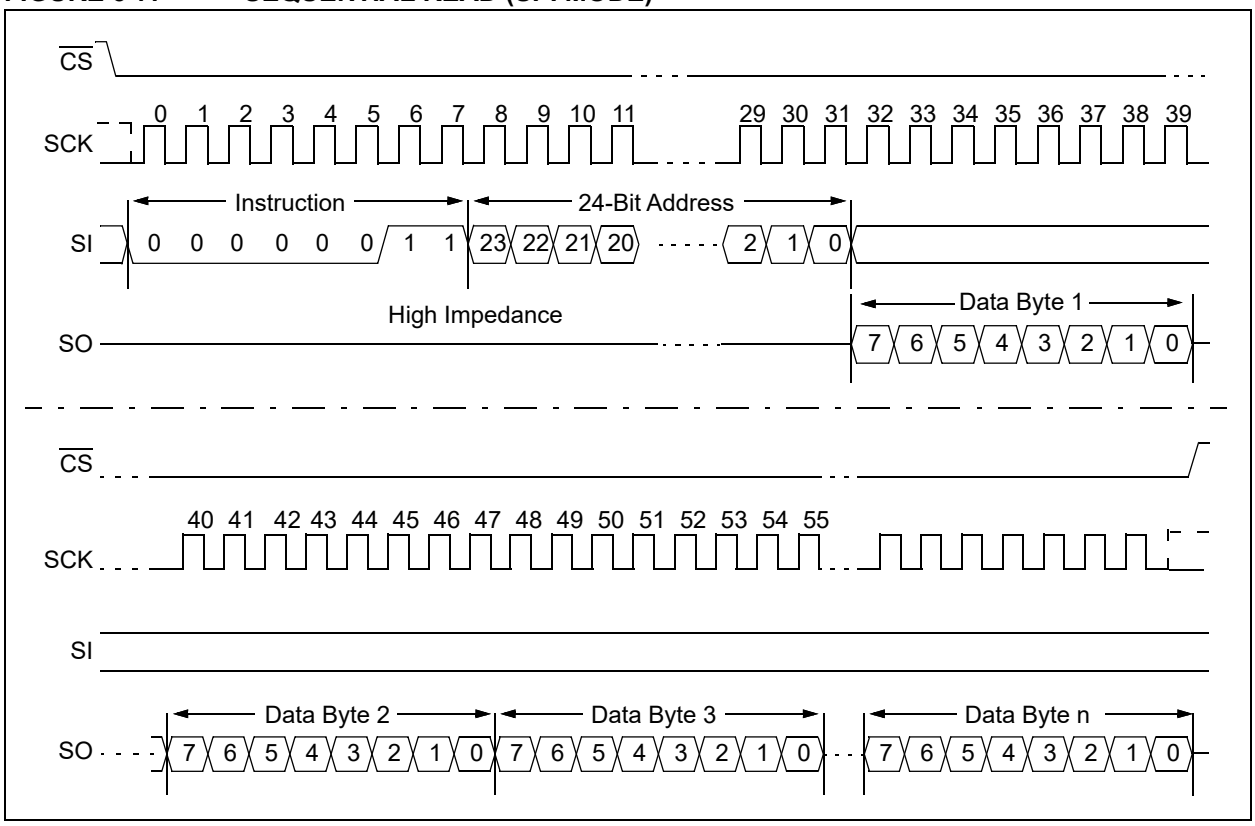

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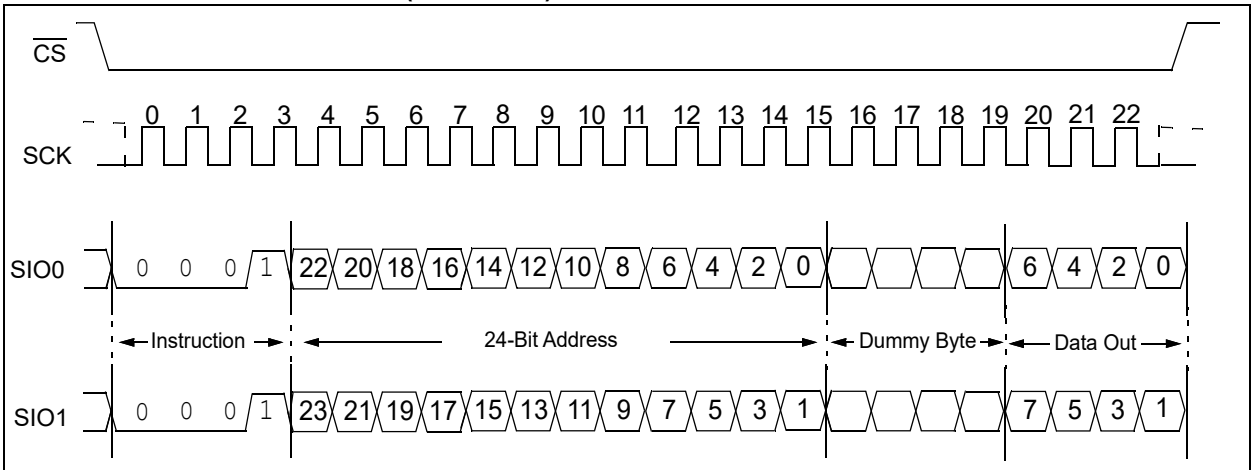
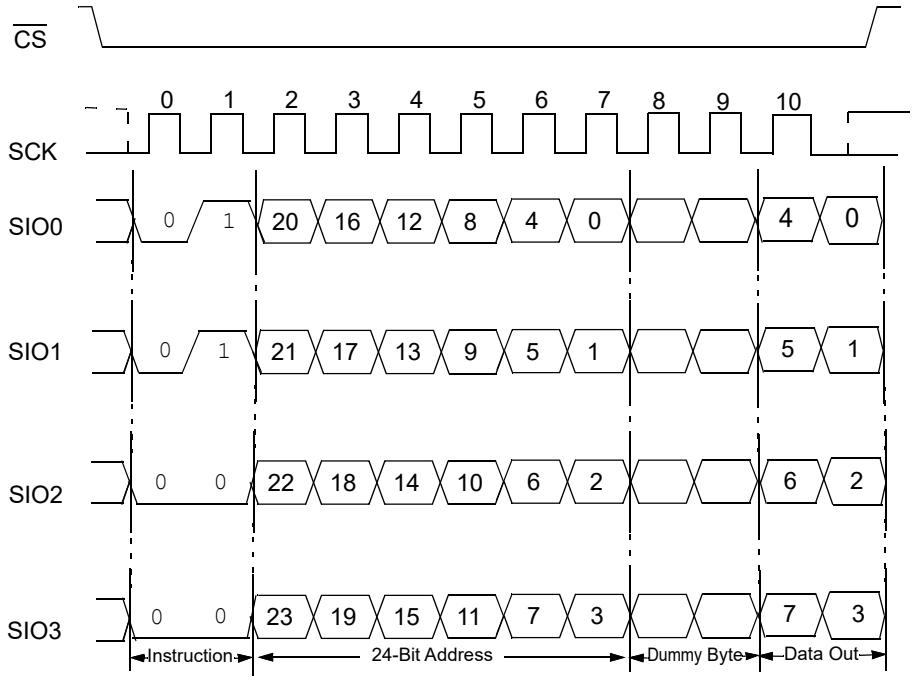
FIGURE 3-8: BYTE READ (SDI MODE)



Note 1: Page and Sequential mode are similar in that additional bytes can be clocked out before the $\overline{CS}$ is brought high.

2: The first byte read after the address will be a dummy byte.

FIGURE 3-9: BYTE READ (SQI MODE)



Note 1: Page and Sequential mode are similar in that additional bytes can be clocked out before the $\overline{CS}$ is brought high.

2: The first byte read after the address will be a dummy byte.

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3.7 HIGH-SPEED READ INSTRUCTION

The High-Speed Read instruction is supported in SPI mode, SDI mode and SQI mode with clock frequency up to 143 Mhz. The device is selected by pulling $\overline{CS}$ low. The 8-bit High-Speed Read (0x0B) instruction is transmitted to the device, followed by the 24-bit address, and then by dummy cycles (see Table 3-1). After the High-Speed Read instruction, address, and dummy are sent, the data stored in the memory at the selected address are shifted out on the output pins. The number of bytes read will depend on the mode of operation of the device (i.e., byte operation, page operation or sequential operation).

If operating in Byte mode, one data byte at the specified address is read out, as shown in Figure 3-10, Figure 3-13 and Figure 3-16.

If operating in Page mode, the data stored within the page is read out starting with the specified address. Page size is either 32 bytes per page or 256 bytes per page based on the Page Size bit selection in the STATUS register. If the data being read reach the page boundary, then the internal address counter will increment to the start of the page, as shown in Figure 3-11, Figure 3-14 and Figure 3-17.

If operating in Sequential mode, the data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next highest address after each byte of data is shifted out, as shown in Figure 3-12, Figure 3-15 and Figure 3-18. When the highest address is reached (3FFFFh), the address counter rolls over to address 00000h, allowing the read cycle to continue indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin.

The device will reject High-Speed Read instructions that have an insufficient number of clocks in the command byte/address byte/dummy byte.

FIGURE 3-10: HIGH SPEED BYTE READ (SPI MODE)

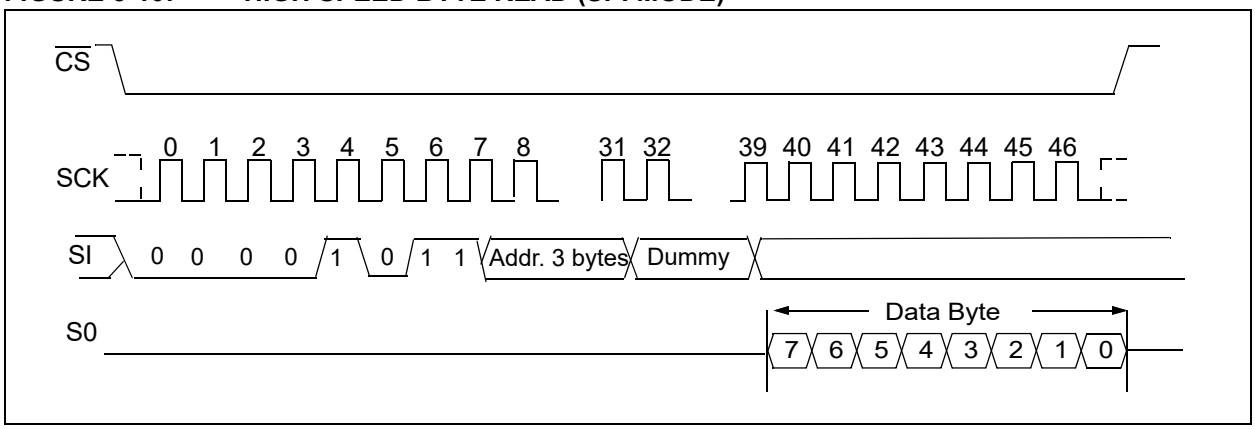

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FIGURE 3-11: HIGH SPEED PAGE READ (SPI MODE)

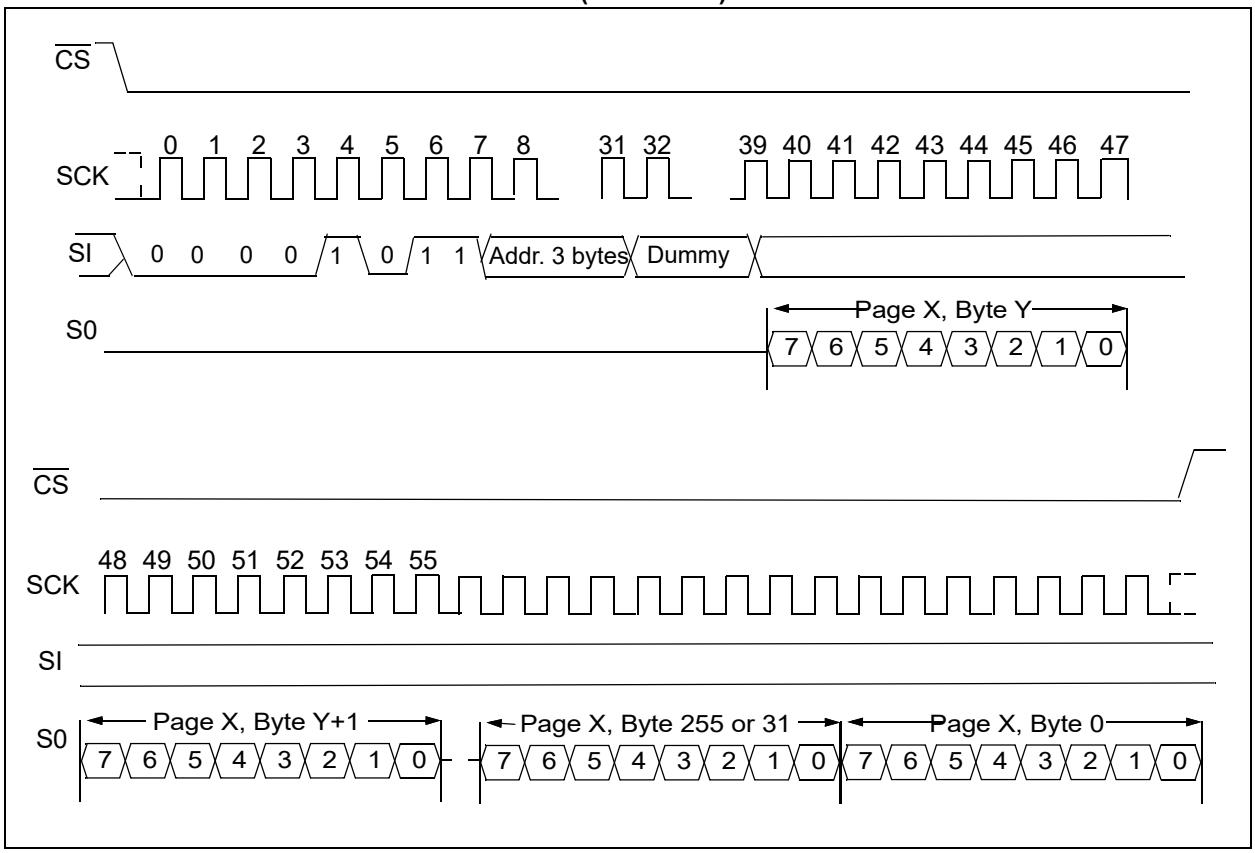

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FIGURE 3-12: HIGH SPEED SEQUENTIAL READ (SPI MODE)

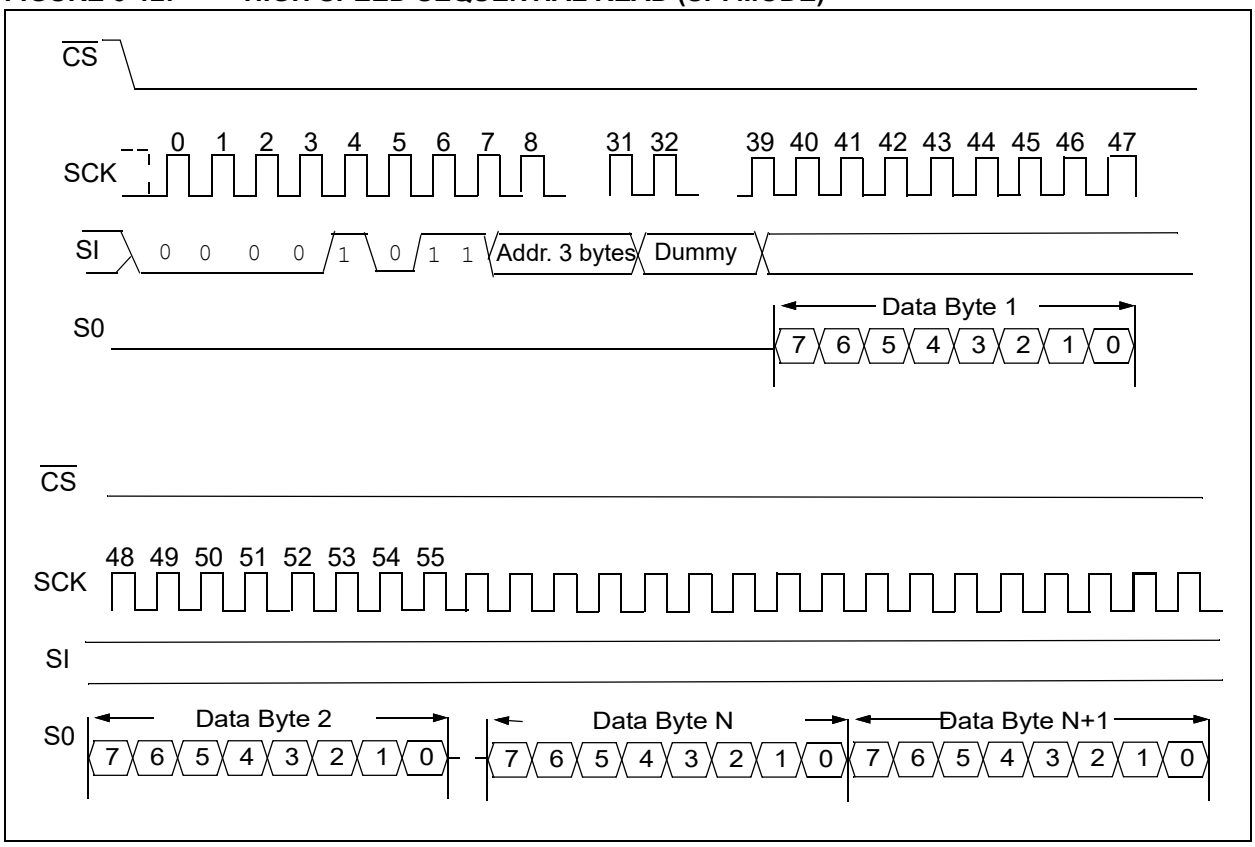

FIGURE 3-13: HIGH SPEED BYTE READ (SDI MODE)

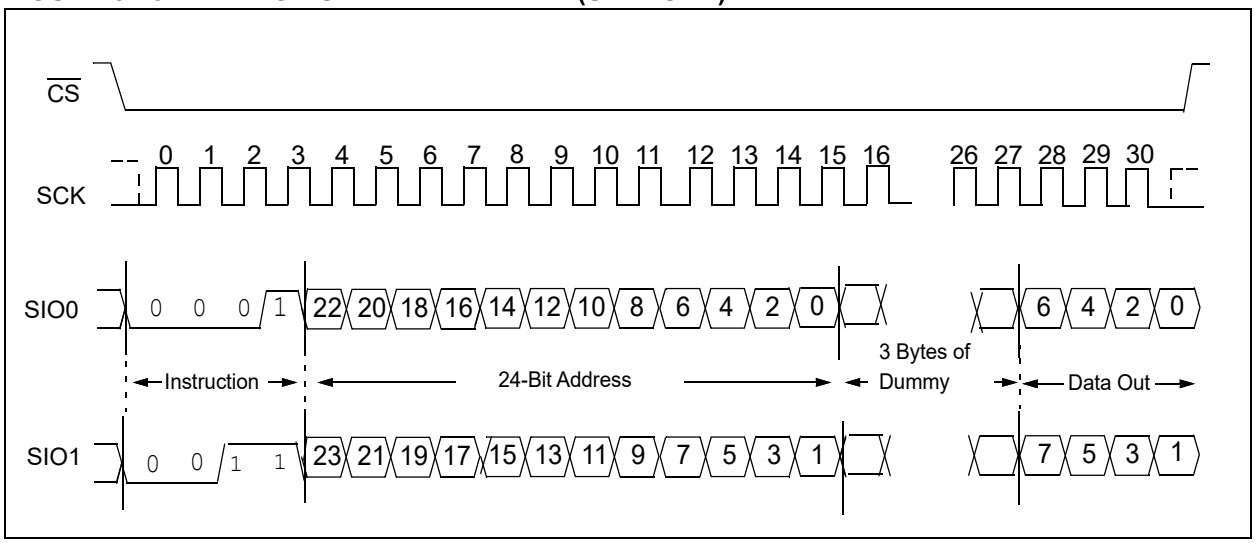

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FIGURE 3-14: HIGH SPEED PAGE READ (SDI MODE)

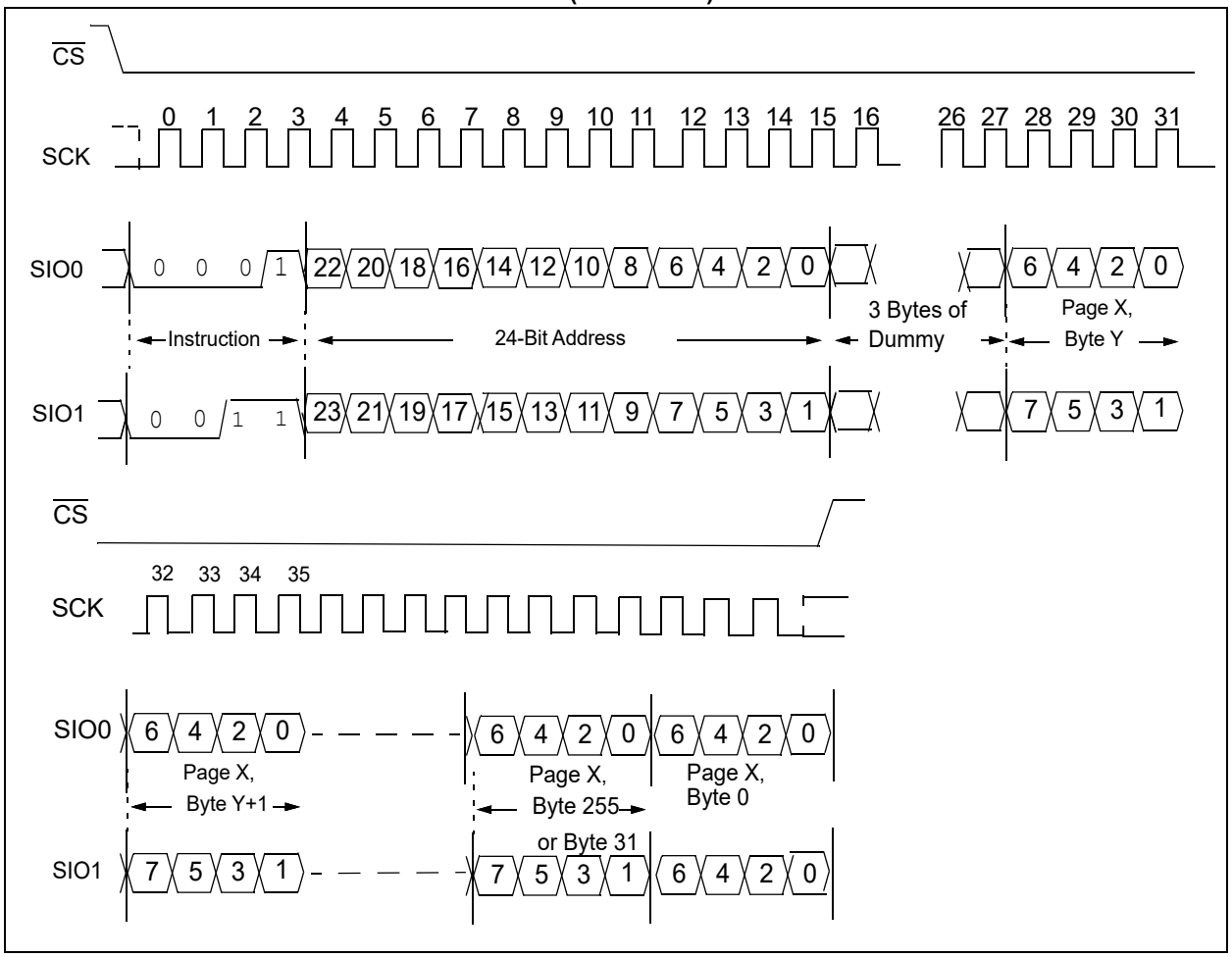

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FIGURE 3-15: HIGH SPEED SEQUENTIAL READ (SDI MODE)

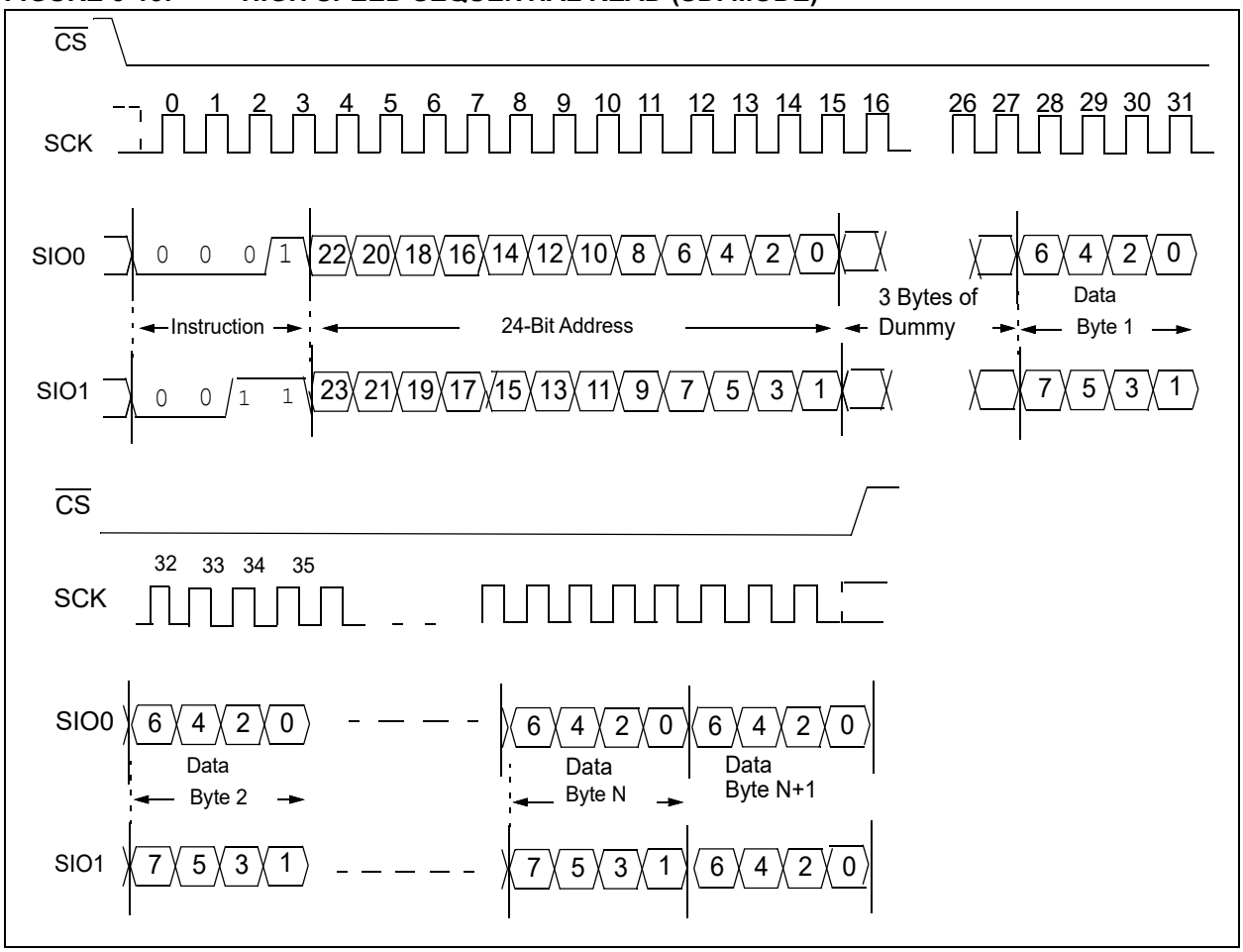

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FIGURE 3-16: HIGH SPEED BYTE READ (SQI MODE)

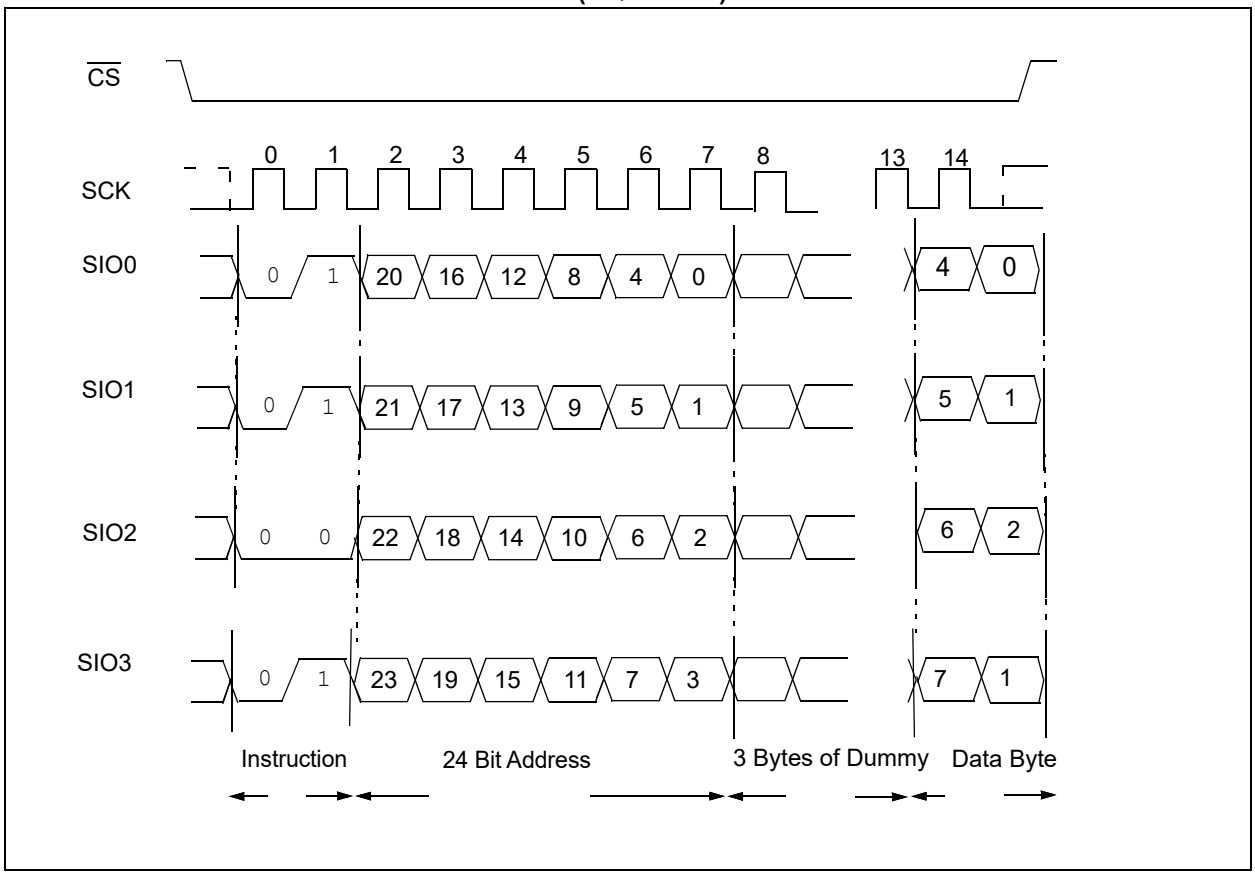

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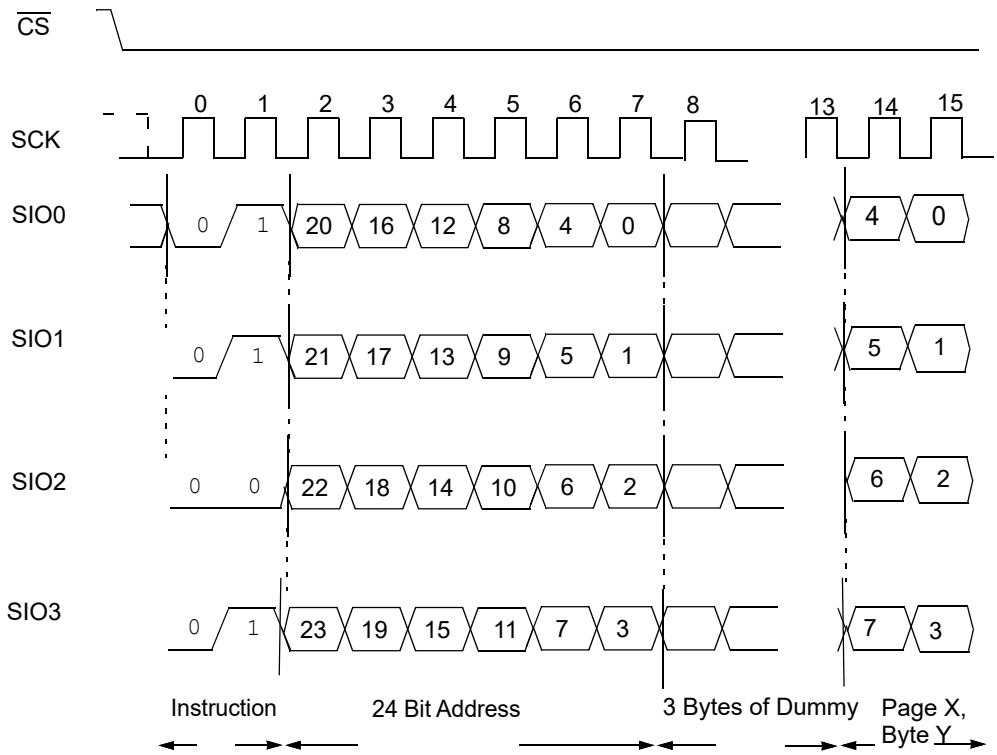
FIGURE 3-17: HIGH SPEED PAGE READ (SQI MODE)



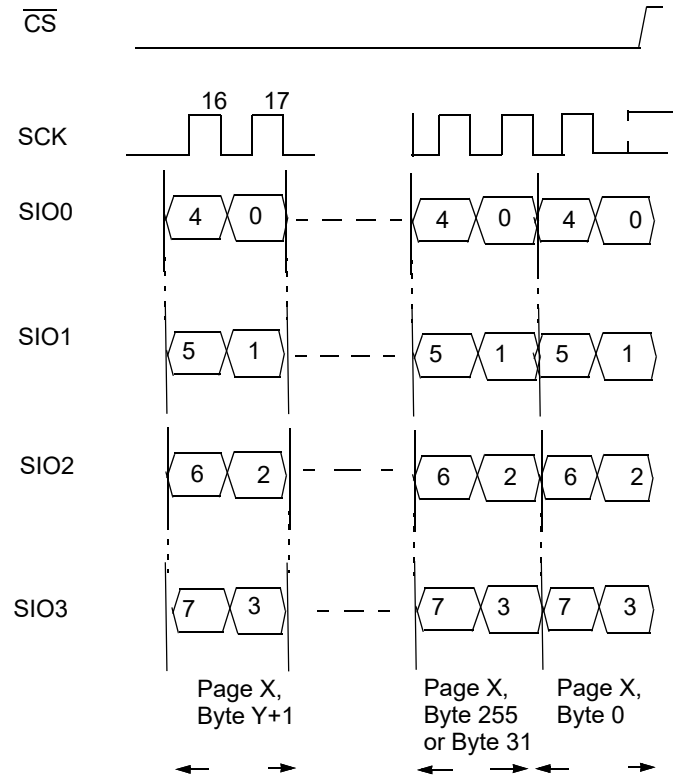


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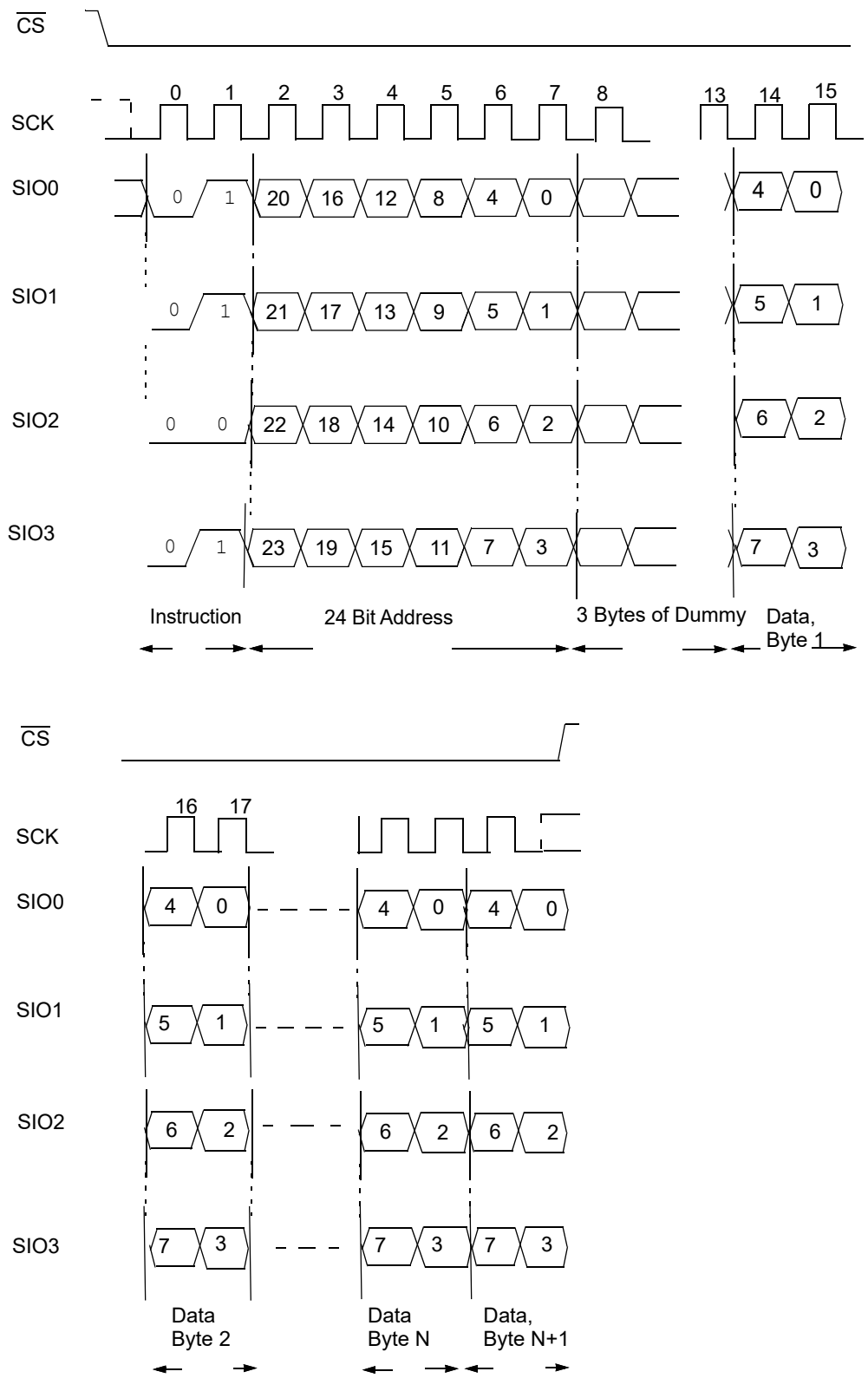
FIGURE 3-18: HIGH SPEED SEQUENTIAL READ (SQI MODE)



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3.8 WRITE INSTRUCTION

The Write instruction is supported in SPI mode, SDI mode and SQI mode with clock frequency up to 143 Mhz. The device is selected by pulling $\overline{CS}$ low. The 8-bit Write (0x02) instruction is transmitted to the device, followed by the 24-bit address, and then by data bytes to write to the device. The number of bytes to write will depend on the mode of operation of the device (i.e., byte operation, page operation or sequential operation).

If operating in Page mode, after the initial data byte is shifted in, additional bytes can be shifted into the device. The Address Pointer is automatically incremented. This operation can continue for the entire page (32 bytes or 256 bytes) before data will start to be overwritten, as shown in Figure 3-20. If operating in Sequential mode, after the initial data byte is shifted in, additional bytes can be clocked into the device, as shown in Figure 3-21. The internal Address Pointer is automatically incremented. When the Address Pointer reaches the highest address, the address counter rolls over to (00000h). This allows the operation to continue indefinitely; however, previous data will be overwritten.

The device will reject a Write instruction that has an insufficient number of clocks in the command byte/address byte/first data byte. The device will accept the Write instruction with a partial data byte by ignoring the partial data byte and writing all of the complete data bytes that it receives.

FIGURE 3-19: BYTE WRITE (SPI MODE)

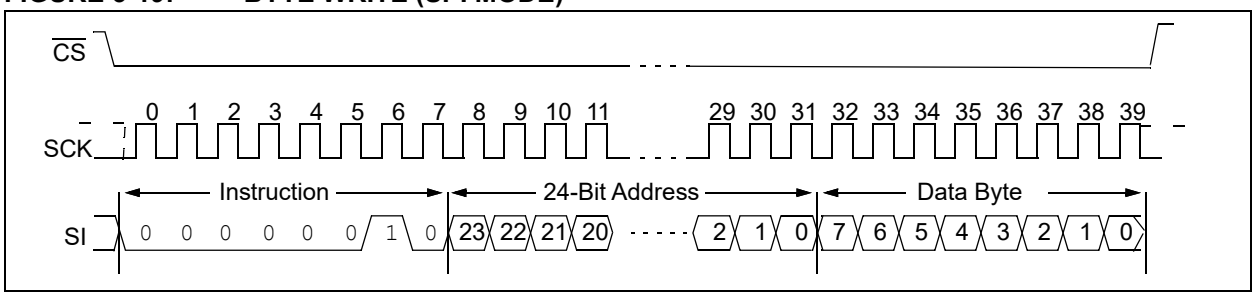

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FIGURE 3-20: PAGE WRITE (SPI MODE)

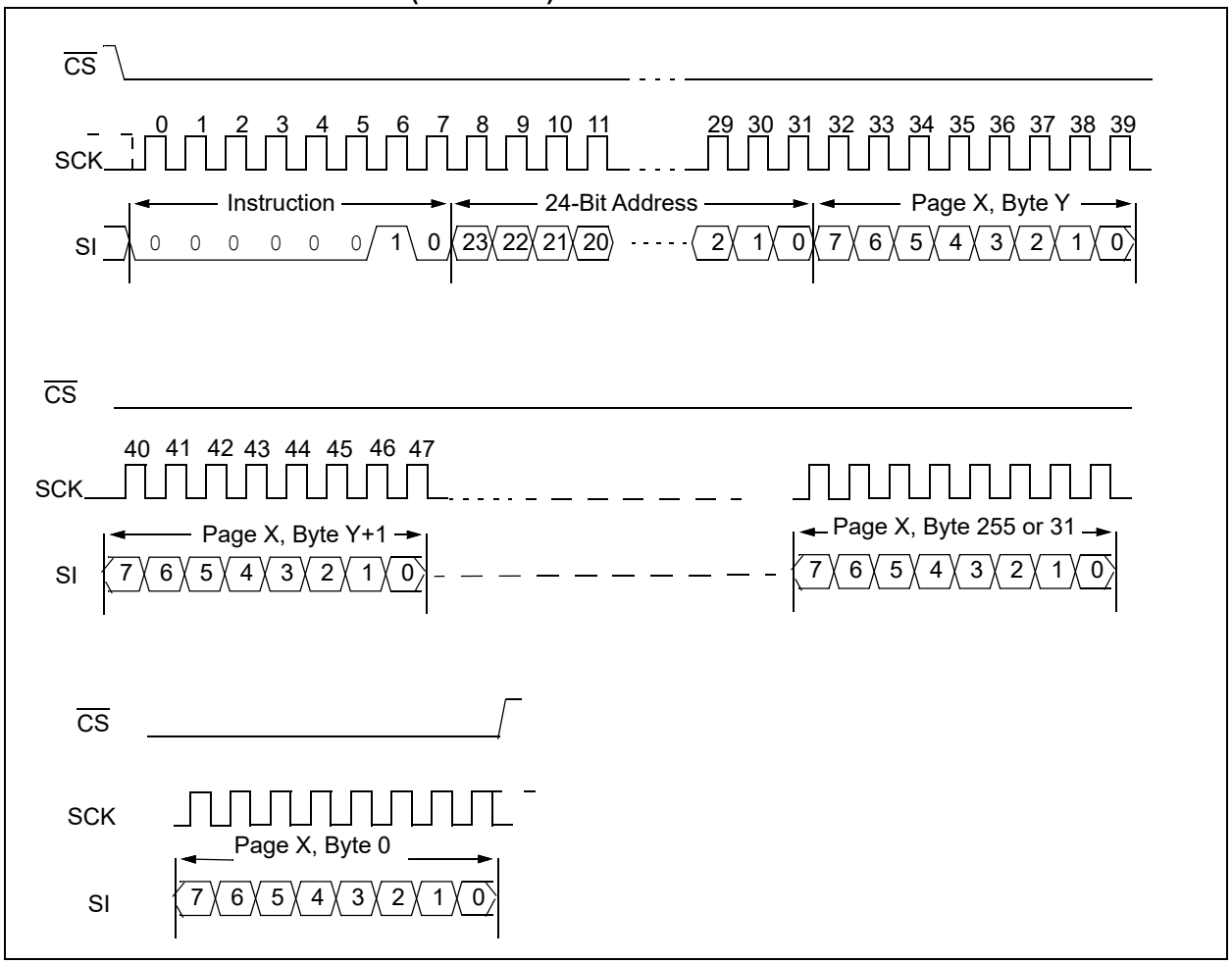

FIGURE 3-21: SEQUENTIAL WRITE (SPI MODE)

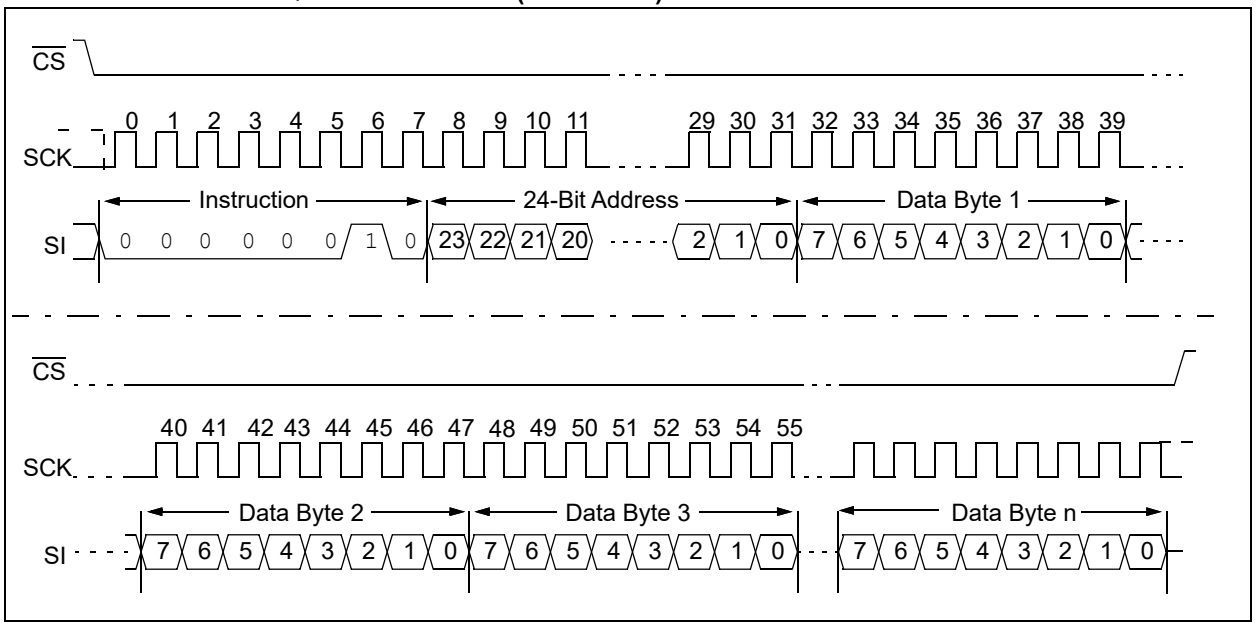

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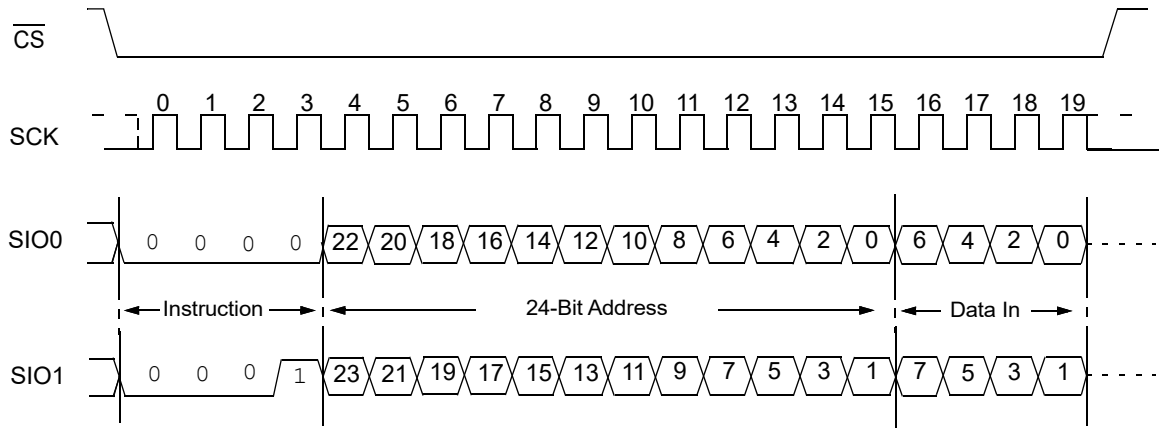
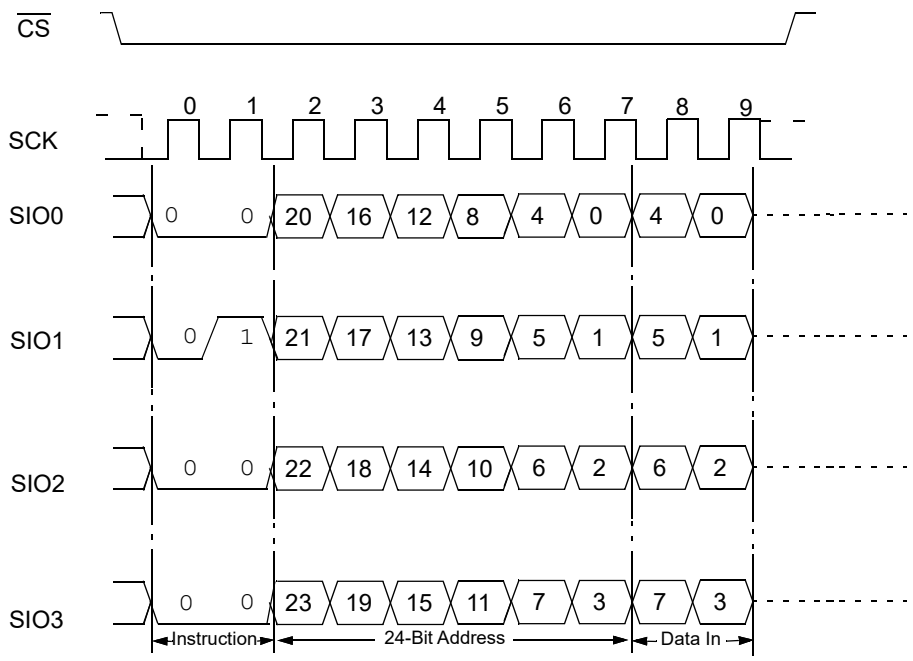
FIGURE 3-22: BYTE WRITE (SDI MODE)



Note 1: Page and sequential mode are similar in that additional bytes can be clocked in before the $\overline{CS}$ is brought high.

FIGURE 3-23: BYTE WRITE (SQI MODE)



Note 1: Page and sequential mode are similar in that additional bytes can be clocked out before the $\overline{CS}$ is brought high.

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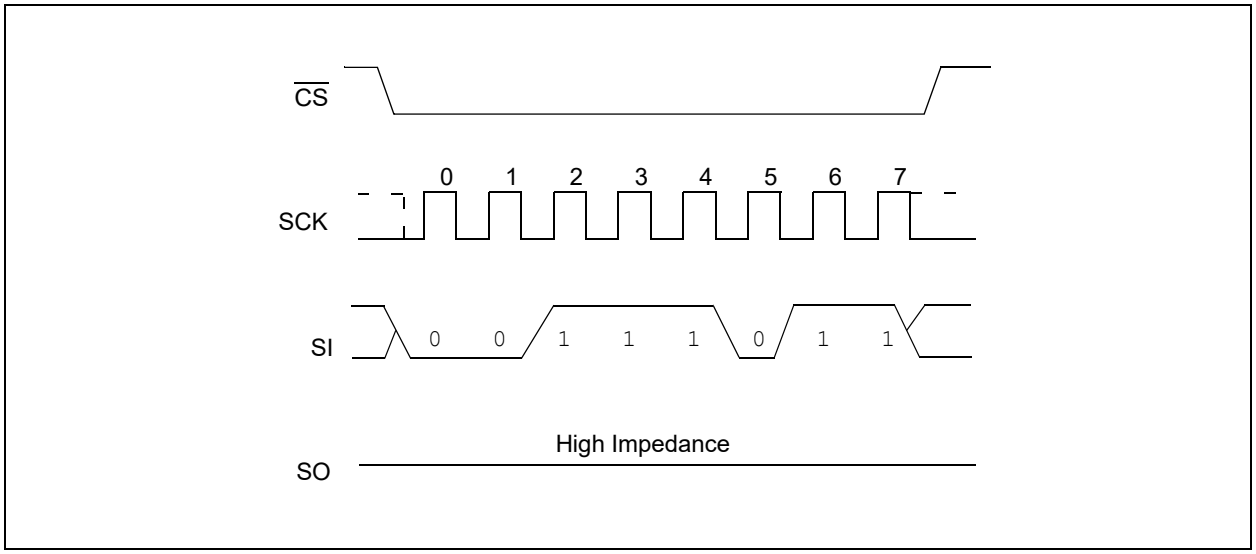
3.9 ENABLE DUAL I/O INSTRUCTION

The Enable DUAL I/O (EDIO) instruction, 3BH, enables the device for SDI bus operation, and the PROT bits <12:11> in the STATUS register will be set to '01'. Upon completion of the instruction, all instructions thereafter are expected to be 2-bit multiplexed input/output (SDI mode) until a power cycle or a "Reset I/O instruction" is executed. See Figure 3-24.

The device will reject an EDIO instruction that has an insufficient number of clocks in the command byte. The device will accept an EDIO instruction with extra clocks, in which case the extra clocks are ignored.

FIGURE 3-24: ENABLE DUAL I/O



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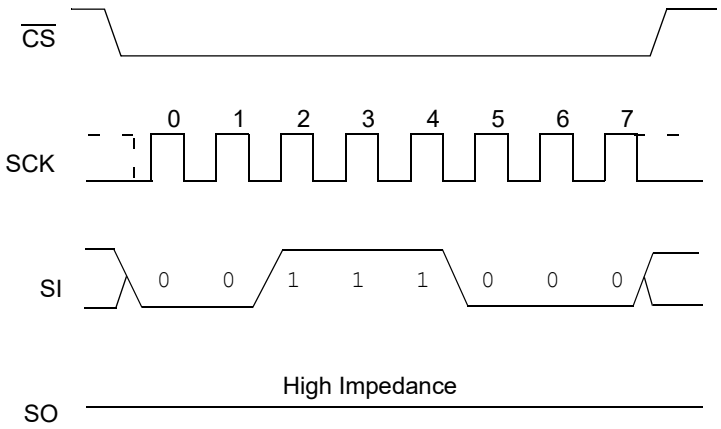
3.10 ENABLE QUAD I/O INSTRUCTION

The Enable Quad I/O (`EQIO`) instruction, 38H, enables the device for SQI bus operation, and the PROT bits <12:11> in the STATUS register will be set to '`10`'. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a "Reset I/O instruction" is executed. See Figure 3-25.

The device will reject an `EQIO` instruction that has an insufficient number of clocks in the command byte. The device will accept an `EQIO` instruction with extra clocks, in which case the extra clocks are ignored.

FIGURE 3-25: ENABLE QUAD I/O



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3.11 RSTIO INSTRUCTION

The Reset IO (RSTIO) instruction, FFH, resets the device for SPI bus operation, and the PROT bits <12:11> in the STATUS register will be cleared to 00. Upon completion of the instruction, all instructions thereafter are expected to be in SPI mode. The RSTIO command must be entered in the current device communication mode. See Figure 3-26 to reset from SDI mode and Figure 3-27 to reset from SQI mode.

The device will accept a RSTIO command with eight clocks with all SIO pins high, regardless of the current communication mode.

The device will reject a RSTIO instruction that has an insufficient number of clocks in the command byte. The device will accept a RSTIO instruction with extra clocks, in which case the extra clocks are ignored.

FIGURE 3-26: RESET I/O (SDI MODE)

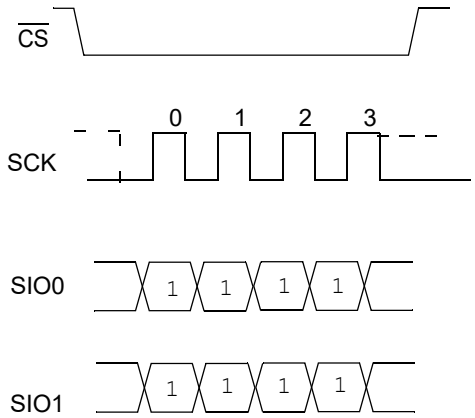
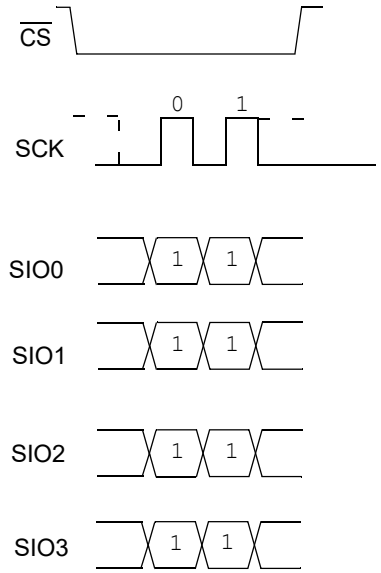


FIGURE 3-27: RESET I/O (SQI MODE)



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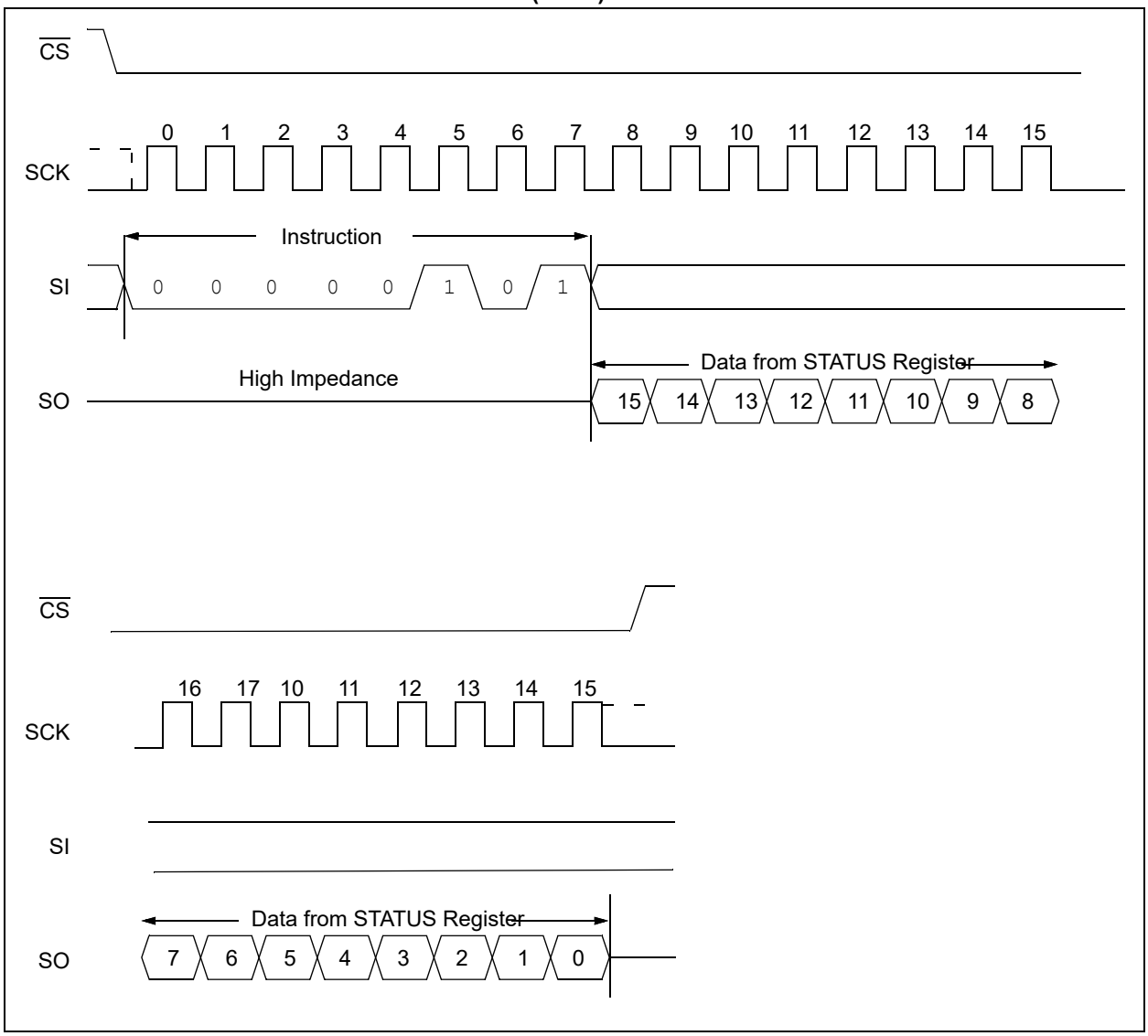
3.12 READ STATUS REGISTER INSTRUCTION

The Read STATUS Register instruction (RDSR) (Figure 3-28) provides access to the STATUS register (Table 3-2). The STATUS register may be read at any time. This instruction is supported in SPI mode, SDI mode and SQI mode. In SPI mode, the Read STATUS Register instruction is issued, followed by a read out of the STATUS register. In SDI and SQI mode, the Read STATUS Register instruction is issued, followed by one dummy cycle and then by a read out of the STATUS register. The STATUS register output stream continues until terminated by a low-to-high transition of the CS pin.

The device will reject a RDSR instruction that has an insufficient number of clocks in the command byte.

FIGURE 3-28: READ STATUS REGISTER (RDSR) - SPI MODE



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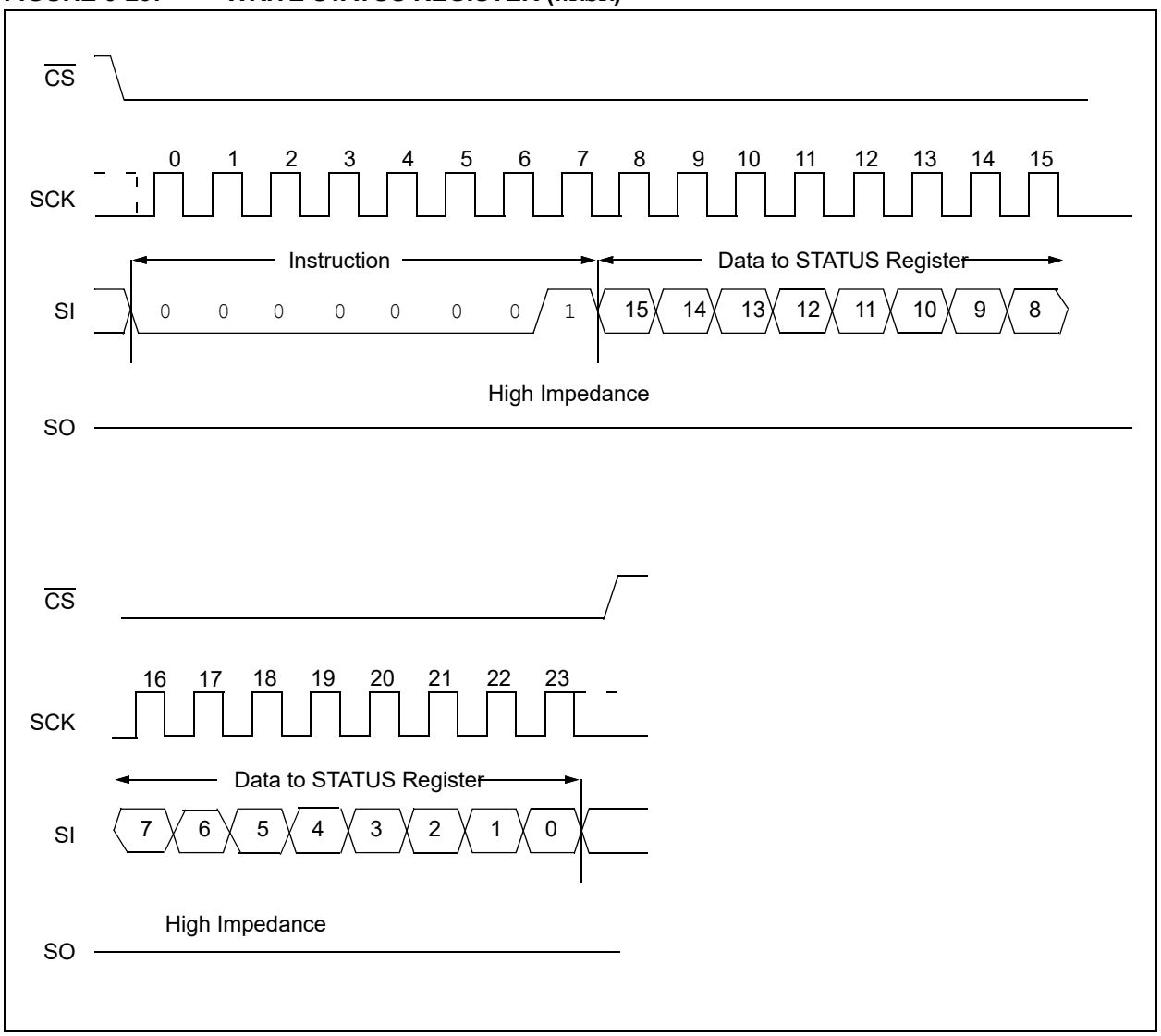
3.13 WRITE STATUS REGISTER INSTRUCTION

The Write STATUS Register instruction (WRSR) (Figure 3-29) allows the user to write to the bits in the STATUS register, as shown in Table 3-2. This allows for setting of the device operating mode. This instruction is supported in SPI mode, SDI mode and SQI mode.

The device will reject a WRSR instruction that has an insufficient number of clocks in the command byte. The device will reject a WRSR instruction with less than eight bits of data.

The device will accept a WRSR instruction with one byte of data, which corresponds to bits 15 to 8 of the STATUS register. The device will accept a WRSR instruction with greater than eight bits of data but less than 16 bits of data, in which case only the first eight bits of data corresponding to STATUS register bits 15 to 8 are accepted. The device will accept a WRSR instruction with greater than 16 bits of data, in which case only the first 16 bits of data corresponding to STATUS register bits 15 to 0 are accepted.

FIGURE 3-29: WRITE STATUS REGISTER (WRSR)



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3.14 VBAT

The 23LCV02M features an internal switch that will maintain the SRAM contents through battery backup. In the event that the VCC supply is not available, the voltage applied to the VBAT pin serves as the backup supply. The VBAT trip point is the point at which the internal switch operates the device from the VBAT supply and is typically 1.85V (VTRIP specification). When VCC falls below the VTRIP point, the system will continue to maintain the SRAM contents. The following conditions apply:

TABLE 3-1: DEVICE POWERED BY POWER SUPPLY OR EXTERNAL BATTERY

Supply condition	READ/WRITE ACCESS	POWERED BY
VCC < VTRIP	NO	VBAT
VCC > VTRIP	YES	VCC

3.15 ERROR CORRECTION CODE (ECC)

The 23XX02M features an effective method of adding reliability to the memory array through the use of Error Correction Code. ECC bits are added to the SRAM data array, which store parity data calculated from the array data. Six extra bits of ECC data are calculated and stored for every four bytes of user data that is written. Upon reading the data at any valid address, the array data in that four-byte block are checked against the ECC bits parity calculation, and any single-bit error, the most common kind, will be corrected automatically. The ECC bits to be stored are calculated during a write to the array. The ECC bits are calculated based on all 32 bits in a four-byte block and are stored near the corresponding 32 data bits (4 bytes) of array data. The ECC bits are stored alongside the array data but are not accessible to the user.

3.15.1 ECC BIT CALCULATION

The ECC bit encoding and decoding are done in logic, generating six parity bits for every 32 bits, or four bytes, of array memory on four-byte boundaries. Any time one or more bytes of memory within a four-byte block of data is written, the ECC bits for all 32 bits are updated and stored simultaneously. During read operations of any particular byte of data, the data in the corresponding four-byte block are calculated and compared against the stored ECC bits. If there is a difference, the ECC mechanism generates a code to indicate which of the 32 data bits is in error and will invert and correct it as it is sent out. This mechanism is effective in correcting any single-bit error, which is the most common type. It cannot fix more than one error in any block of four bytes.

3.16 POWER UP

The serial SRAM enters a known state at power-up. The device is in a low-power state with $\overline{CS}$ = 1. A high-to-low transition is required on the $\overline{CS}$ line to enter an active state. The initial communication mode is SPI for the 23XX02M, and the STATUS register is at the default value, except where VBAT is used, in which case the previous STATUS register setting and communication mode are retained.

If VCC falls below VMIN operating voltage during active communication, such as `WRITE`, then data are not guaranteed and data corruption may occur.

It is possible that, after a brownout condition, a host processor may experience a reset while the memory device may not due to differences in PoR levels. For that reason, it is recommended that the host send the `RSTIO` command before attempting to begin communication with the memory device every time it reboots. The device will accept a `RSTIO` command with eight clocks with all SIO pins high, regardless of current communication mode. Once communication is established in SPI mode, reading or writing data to the array or to the STATUS register, or setting other communication modes can proceed.

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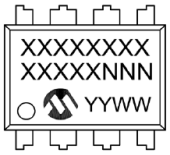
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead PDIP



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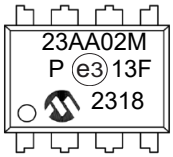
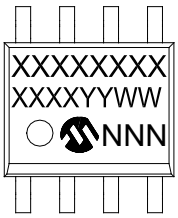


8-Lead SOIC (3.90 mm)



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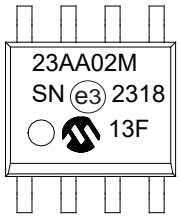
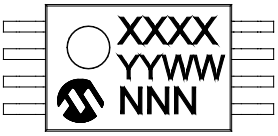


8-Lead TSSOP



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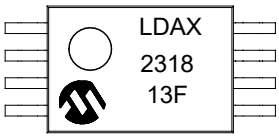

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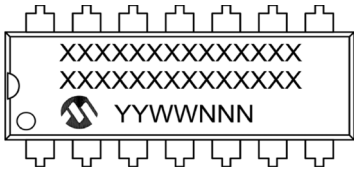
14-Lead PDIP



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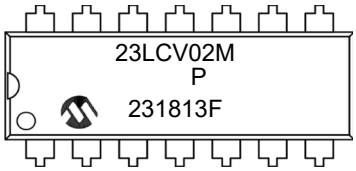
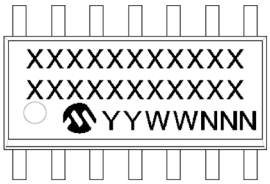


14-Lead SOIC (3.90 mm)



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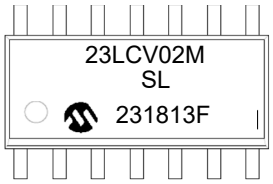
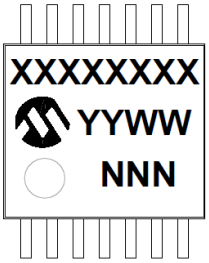
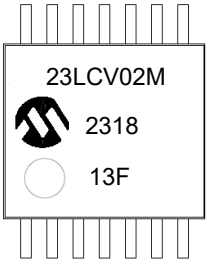


14-Lead TSSOP



Example:



Part Number	1st Line Marking Codes		
	PDIP	SOIC	TSSOP
23AA02M	23AA02M	23AA02M	LDAX
23LCV02M	23LCV02M	23LCV02M	23LCV02M

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	RoHS-compliant JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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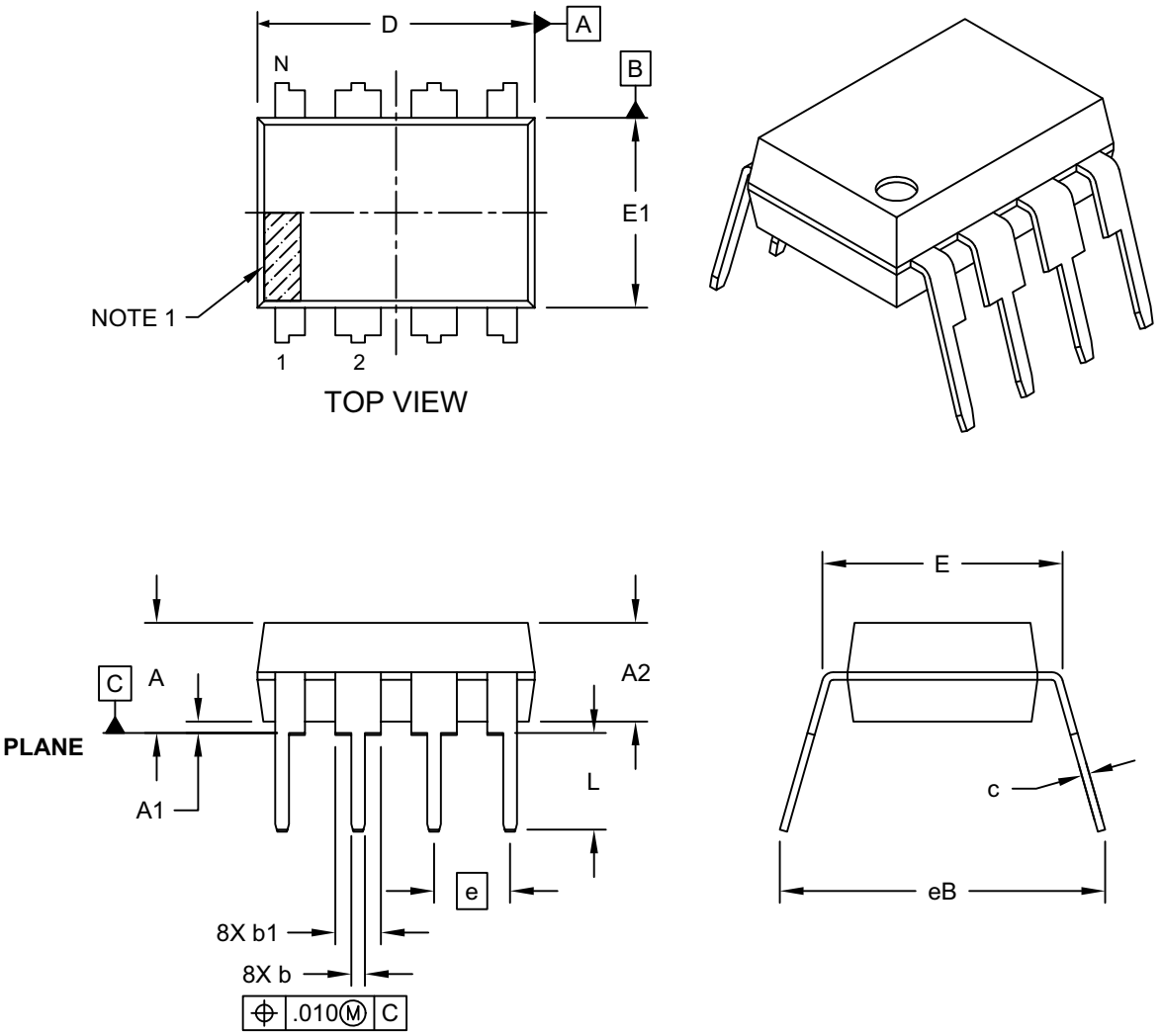
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018-P Rev G Sheet 1 of 2

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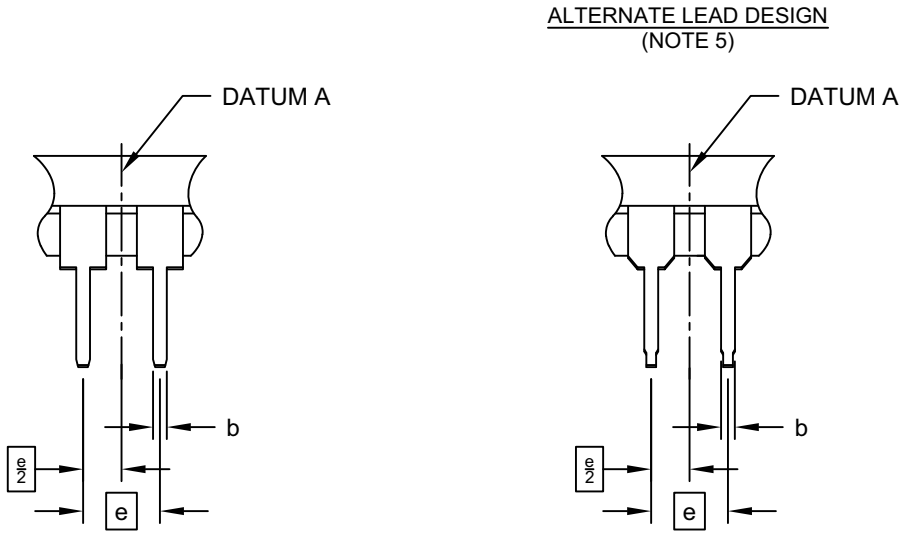
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev G Sheet 2 of 2

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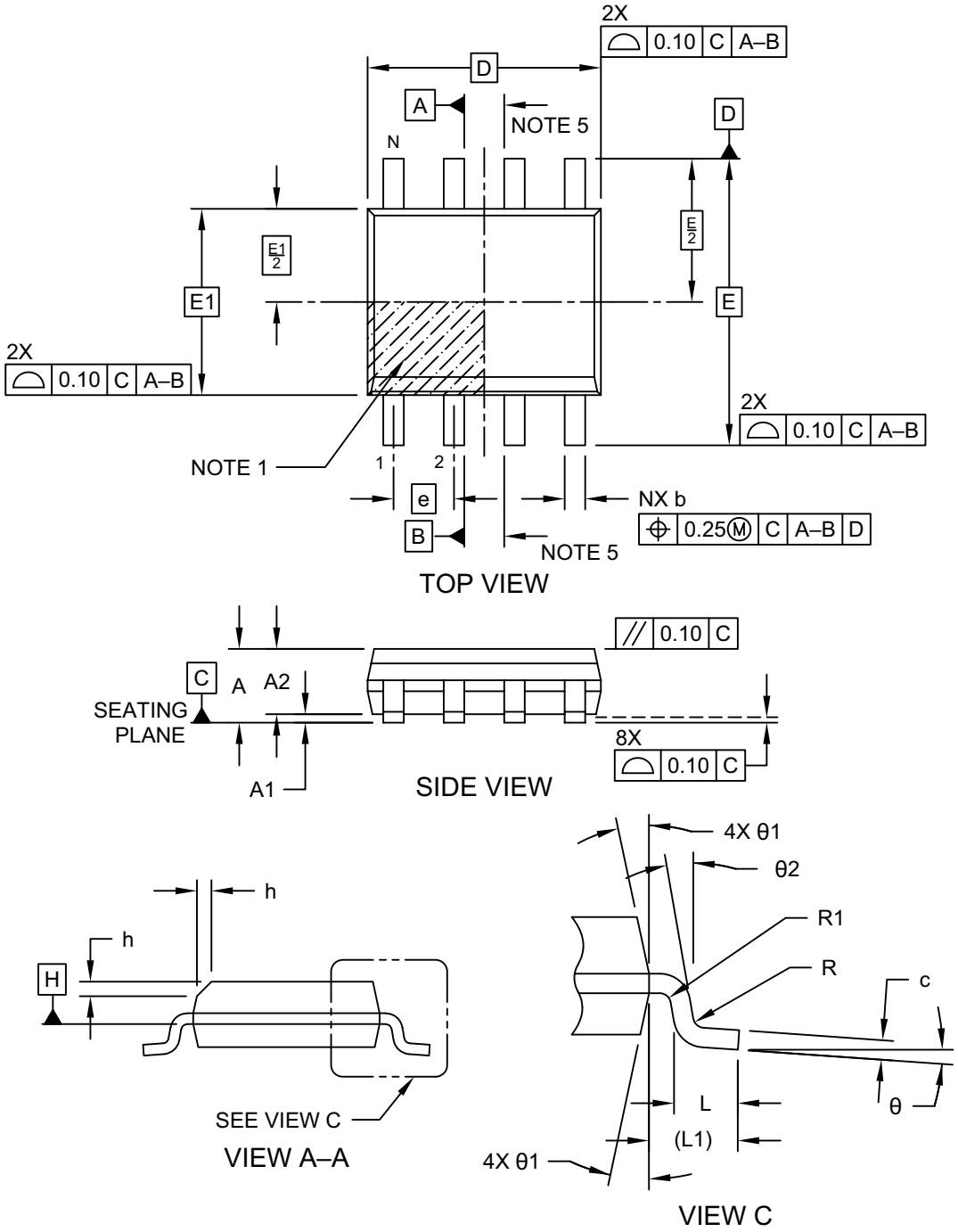
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

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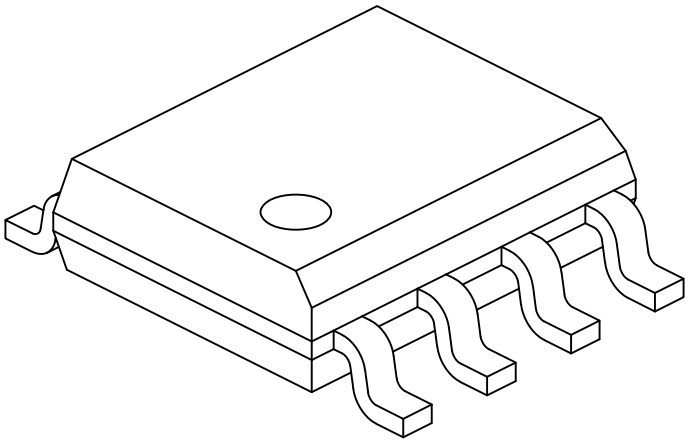
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

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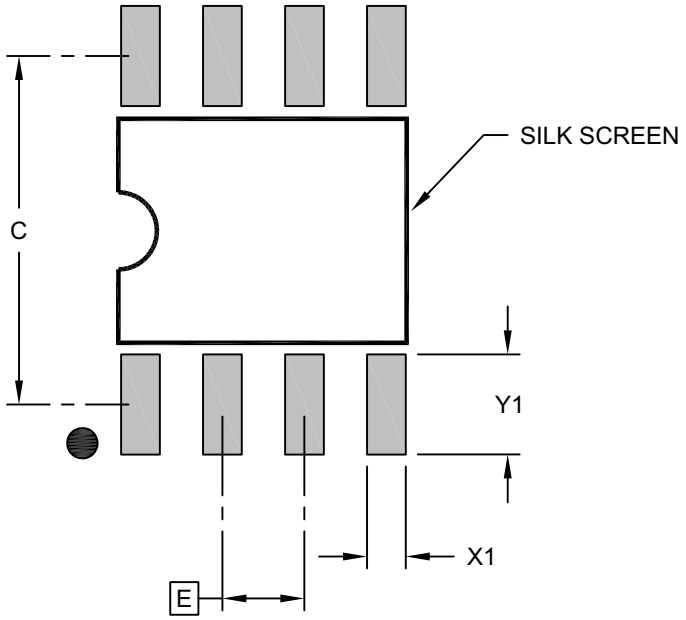
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

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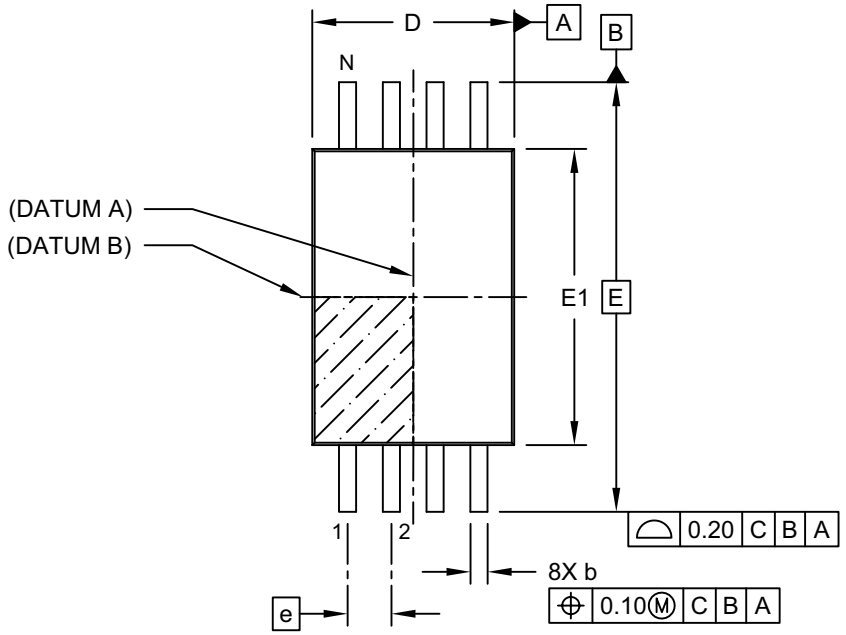
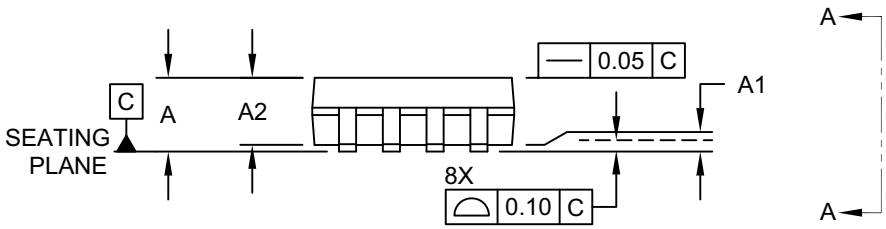
8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

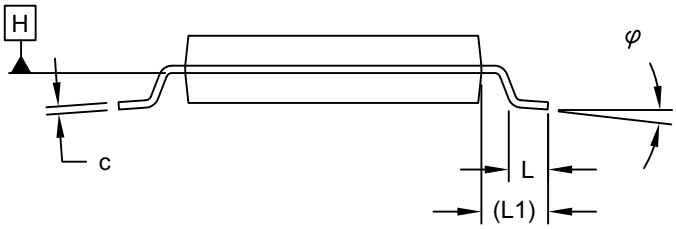
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

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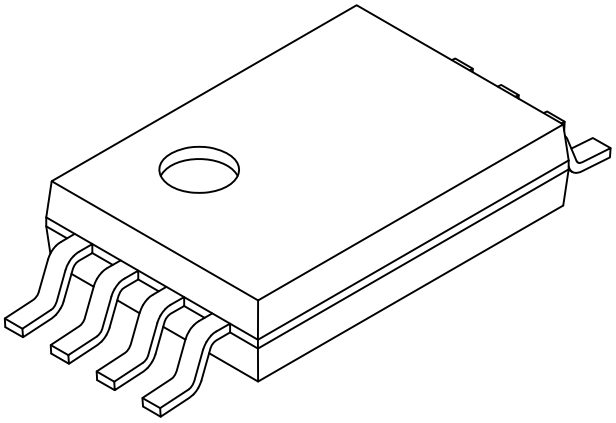
8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

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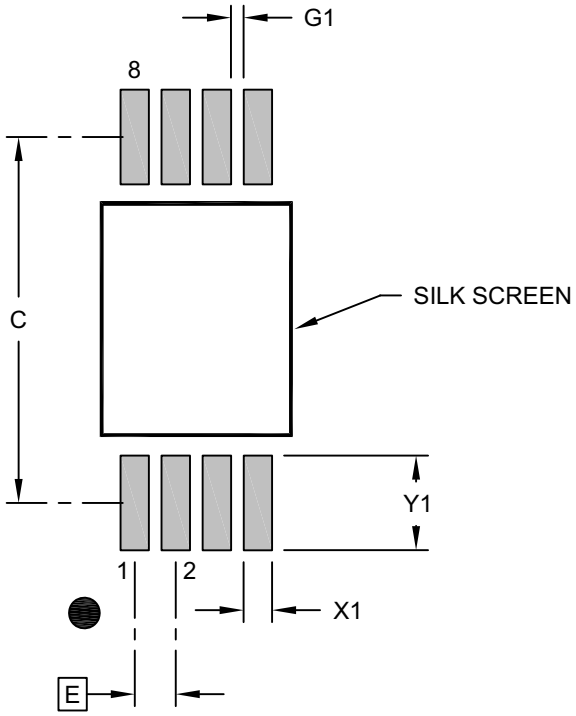
8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

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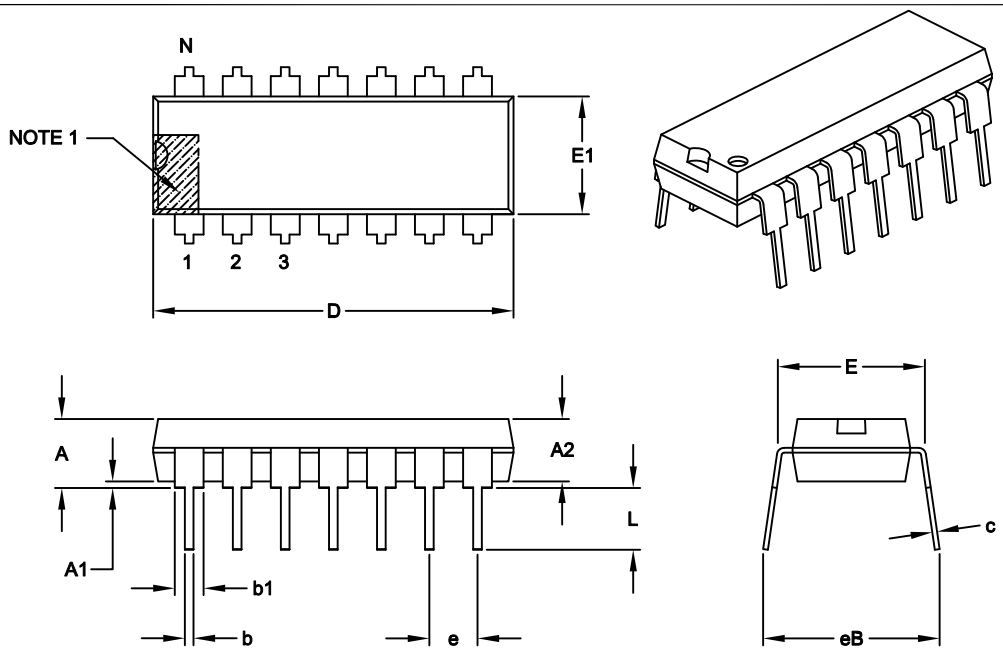
14-Lead Plastic Dual In-Line (P) - .300 In. Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-005B

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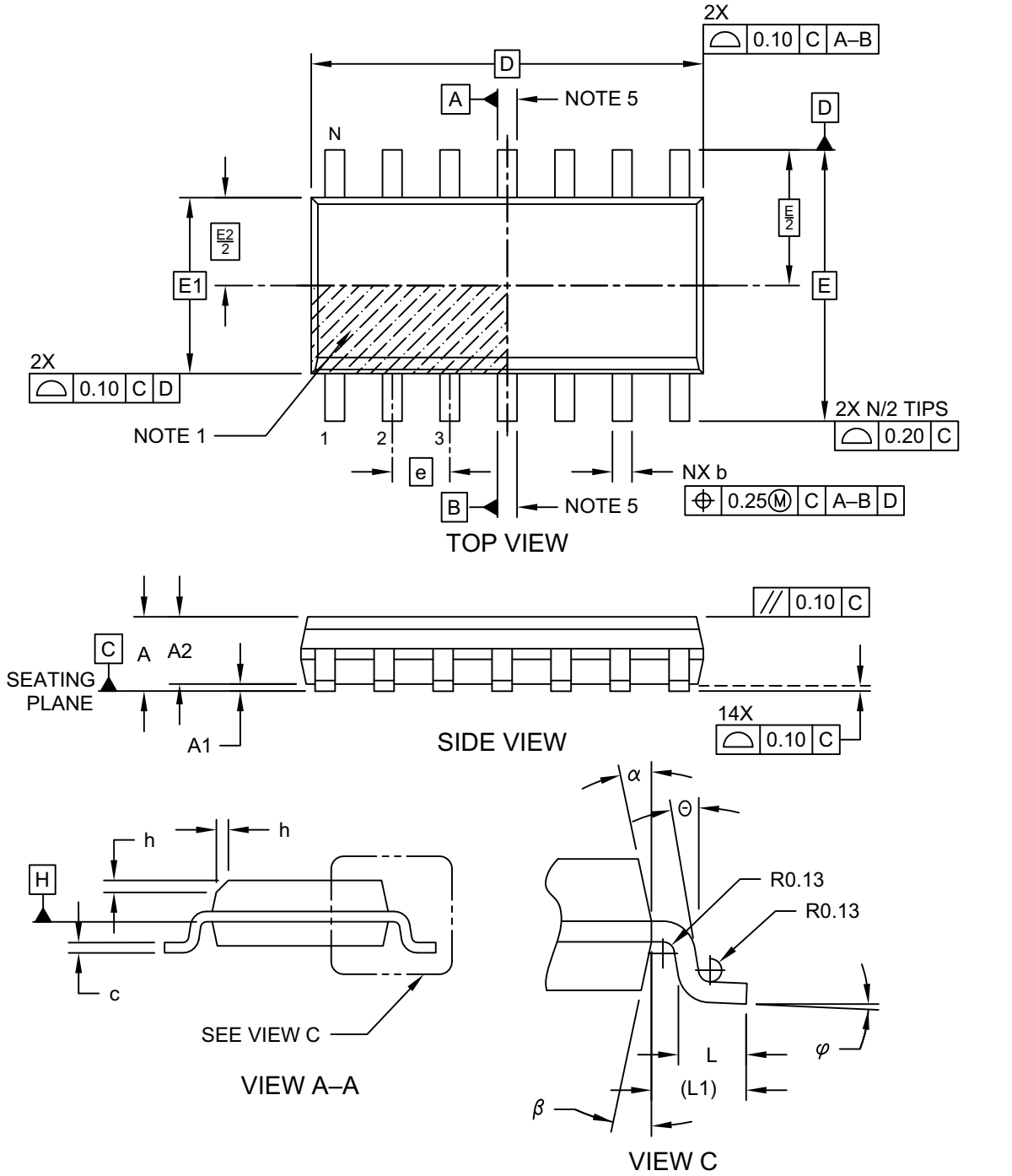
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

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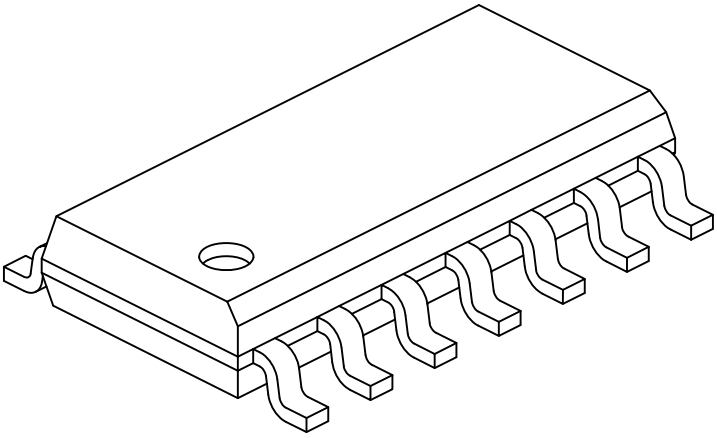
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

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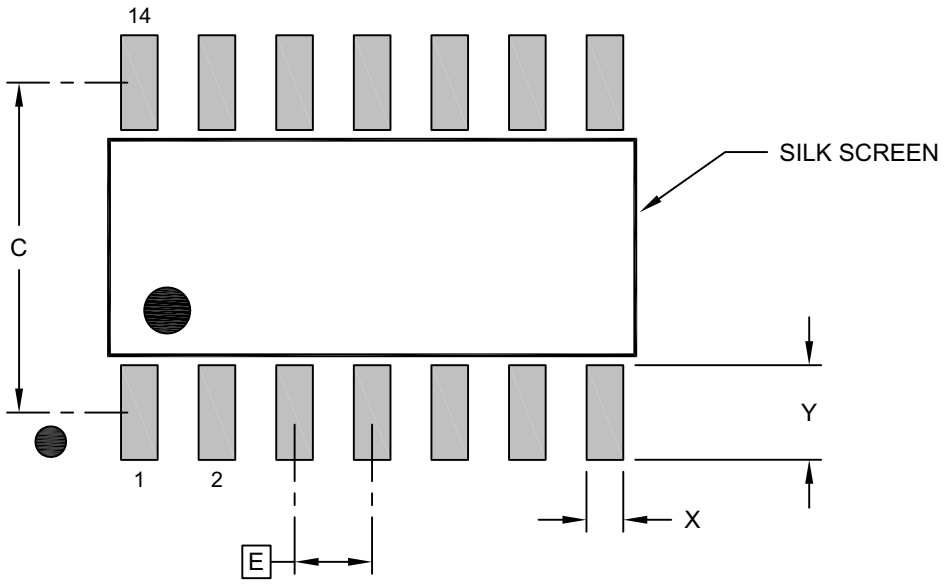
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

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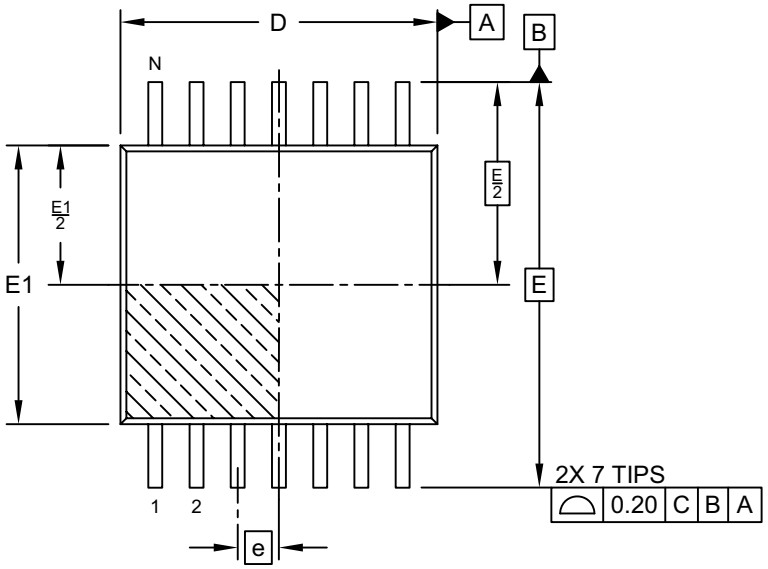
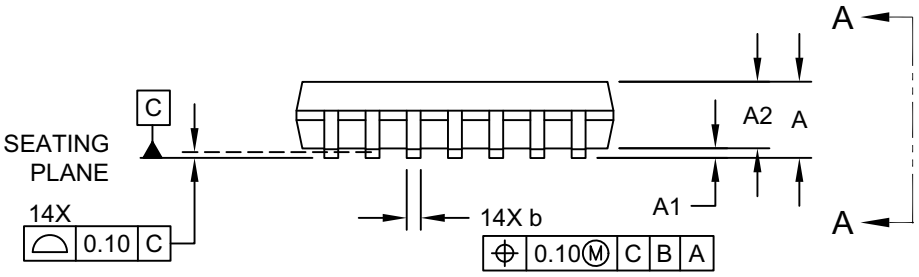
14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

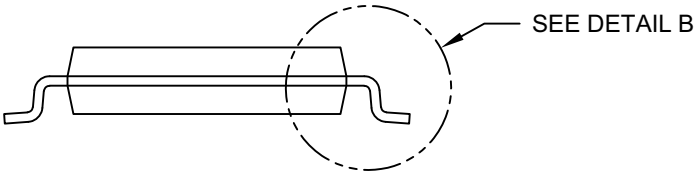
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A–A

Microchip Technology Drawing C04-087-ST Rev F Sheet 1 of 2

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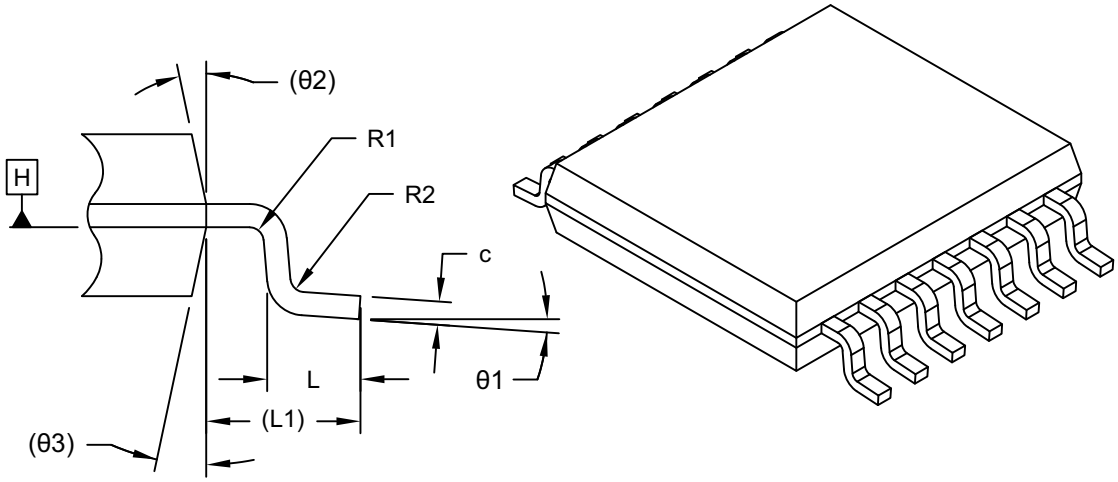
14-Lead Plastic Thin Shrink Small Outline Package [ST] - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087-ST Rev F Sheet 2 of 2

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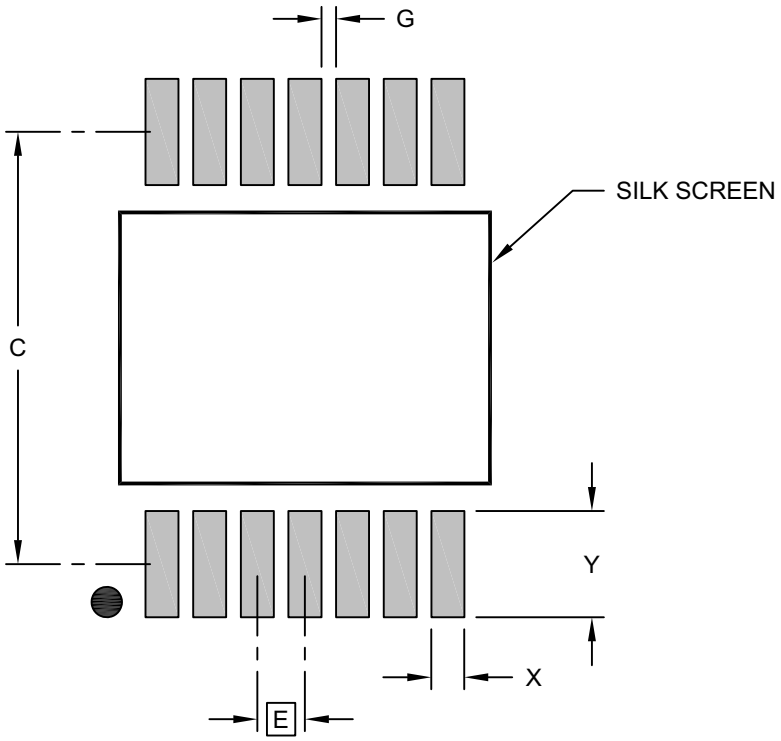

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X14)	X			0.45
Contact Pad Length (X14)	Y			1.45
Contact Pad to Contact Pad (X12)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087-ST Rev F

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APPENDIX A: REVISION HISTORY

Revision A (January 2024)

Initial document release.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	-X	/XX [2]
Device	Tape and Reel Option	Temperature Range	Package

Device[2]:	23AA02M:		2-Mbit, 1.7V - 3.6V, Serial SRAM
	23LCV02M:		2-Mbit, 2.2V - 3.6V, Serial SRAM with Battery Backup
Tape and Reel:	Blank	=	Standard packaging (tube)
	T	=	Tape and Reel[1]
Temperature Range:	I	=	-40°C to +85°C (Industrial)
Package[2]:	P	=	Plastic PDIP (300 mil body), 8-lead
	P	=	Plastic PDIP (300 mil body), 14-lead
	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	SL	=	Plastic SOIC (3.90 mm body), 14-lead
	ST	=	Plastic TSSOP (4.4 mm body), 8-lead
	ST	=	Plastic TSSOP (4.4 mm body), 14-lead

Examples:

a) 23AA02M-I/ST: 2-Mbit, 1.7V-3.6V Serial SRAM, Industrial temp., 8-lead TSSOP package
b) 23LCV02MT-I/SL: 2-Mbit, 2.2V-3.6V Serial SRAM, Industrial temp., Tape and Reel, 14-lead SOIC package
c) 23AA02M-I/P: 2-Mbit, 1.7V-3.6V Serial SRAM, Industrial temp., 8-lead PDIP package
d) 23LCV02M-I/ST: 2-Mbit, 2.2V-3.6V Serial SRAM, Industrial temp., 14-lead TSSOP package
e) 23AA02MT-I/SN: 2-Mbit, 1.7V-3.6V Serial SRAM, Industrial temp., Tape and Reel, 8-lead SOIC package
f) 23LCV02M-I/SL: 2-Mbit, 2.2V-3.6V Serial SRAM, Industrial temp., 14-lead SOIC package
g) 23LCV02M-I/P: 2-Mbit, 2.2V-3.6V Serial SRAM, Industrial temp., 14-lead PDIP package
h) 23AA02M-I/SN: 2-Mbit, 1.7V-3.6V Serial SRAM, Industrial temp., 8-lead SOIC package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: 23AA02M is only available in 8-lead packages while 23LCV02M is only available in 14-lead packages.

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