8-Bit Dual-Supply Level Translator

NL3V8T244, NL3V8T240

The NL3V8T244 / NL3V8T240 are 8−bit configurable dual−supply level translators with 3−state outputs. The A− and B− ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both supply rails are configurable from 0.9 V to 3.6 V allowing universal voltage level translation between the A− to B− ports.

The NL3V8T244 is an 8−bit level translator that allows non−inverting translations from A to B ports. The NL3V8T240 is an 8−bit level translator that allows inverting translations from A to B ports.

The output enable pin ($\overline{OE}$), when High, disables all the output ports by putting them in 3−state. The $\overline{OE}$ pin is designed to track V_{CCA}.

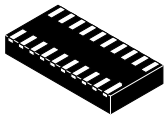
Features

- Wide V_{CCA} and V_{CCB} Operating Range: 0.9 V to 3.6 V
- Balanced Output Drive: ±24 mA @ 3.0 V
- High−Speed w/ Balanced Propagation Delay:
  2.8 ns max at 3.0 to 3.6 V
- Inputs Pins OVT to 3.6 V
- Non−preferential V_{CC} Sequencing
- Outputs at 3−State until Active V_{CC} is Reached
- Partial Power−Off Protection
- Outputs Switch to 3−State with either V_{CC} at GND
- Typical Max Data Rates:
  380 Mbps (≥1.8−V to 3.3−V Translation)
  200 Mbps (≥1.1−V to [1.8−V, 2.5−V, 3.3−V] Translation)
  150 Mbps (≥1.1−V to 1.5−V Translation)
  100 Mbps (≥1.1−V to 1.2−V Translation)
- Small Pb−Free Packaging:
  UDFN20, SOIC−20W, TSSOP−20
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

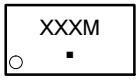
Typical Applications

- Mobile Phones, PDAs, Other Portable Devices
- Automotive
- Industrial

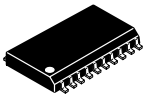
MARKING DIAGRAMS



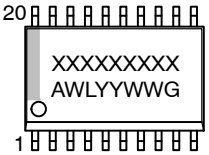
UQFN20
MU SUFFIX
CASE 517AK



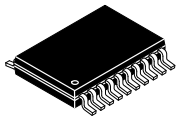
XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package



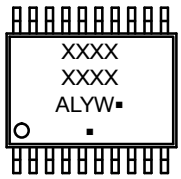
SOIC−20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package



TSSOP−20
DT SUFFIX
CASE 948E



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

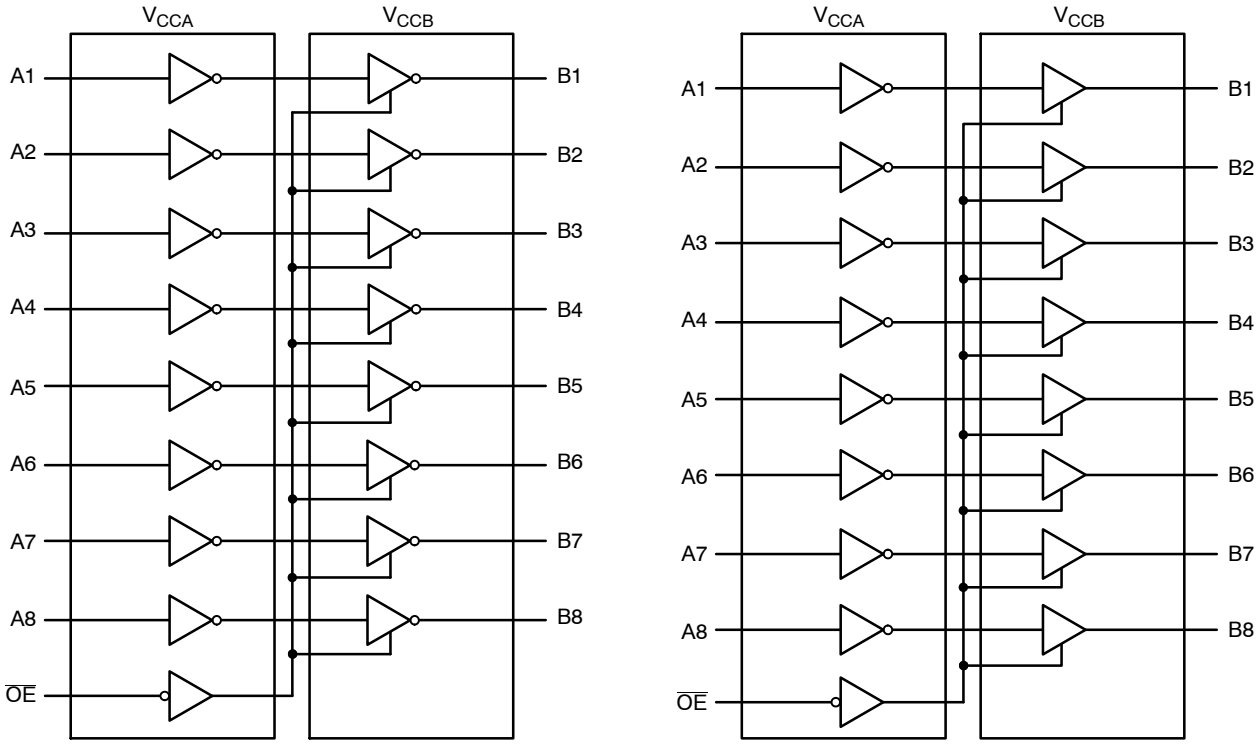
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

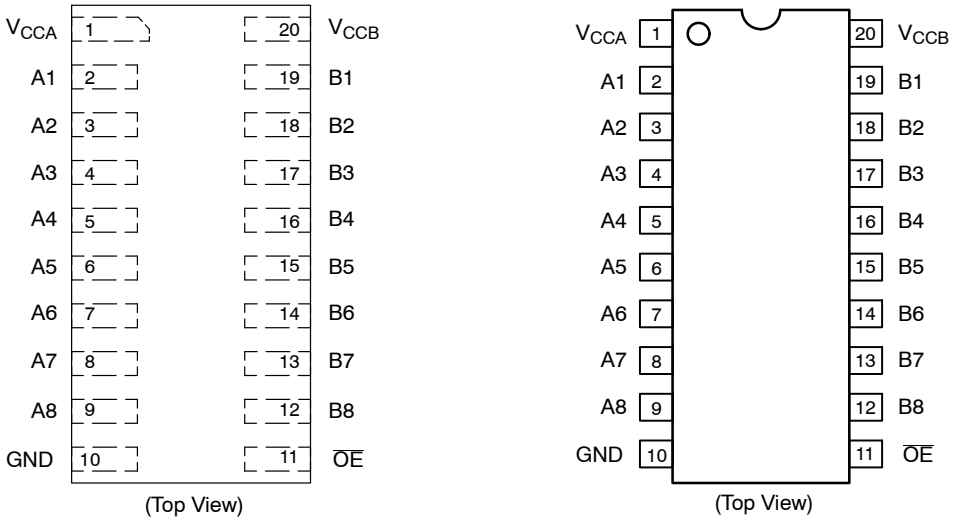
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NL3V8T244 **NL3V8T240**

Figure 1. Logic Diagrams



UDFN20 **SOIC−20W/TSSOP−20**

Figure 2. Pin Assignments (Top View)

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FUNCTION TABLE – NL3V8T244

Inputs		Output
$\overline{OE}$	A_n	B_n
L	L	L
L	H	H
H	X	3–State

FUNCTION TABLE – NL3V8T240

Inputs		Output
$\overline{OE}$	A_n	B_n
L	L	H
L	H	L
H	X	3–State

PIN NAMES

PINS	DESCRIPTION
V_{CCA}	A Port DC Supply
V_{CCB}	B Port DC Supply
GND	Ground
$\overline{OE}$	Output Enable
A1, A2, A3, A4, A5, A6, A7, A8	Input Ports
B1, B2, B3, B4, B5, B6, B7, B8	Output Ports

Application Recommendations

During power−up and power−down, it is recommended that the $\overline{OE}$ pin be connected to V_{CC} through pull−up resistors to ensure high impedance at the I/O ports.

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MAXIMUM RATINGS

Symbol	Rating		Value	Condition	Unit
V_{CCA}, V_{CCB}	DC Supply Voltage		−0.5 to +4.3		V
V_I	DC Input Voltage		−0.5 to +4.3		V
V_O	DC Output Voltage	(Power Down Mode)	−0.5 to +4.3	V_{CCA} = V_{CCB} = 0	V
		(3−State Mode)	−0.5 to +4.3		
		(Active Mode)	−0.5 to V_{CCB}+0.5		
I_{IK}	DC Input Diode Current		−50	V_I < GND	mA
I_{OK}	DC Output Diode Current		−50	V_O < GND	mA
I_O	DC Output Source/Sink Current		±50		mA
I_{CC}	DC Supply Current Per Supply Pin		±100		mA
I_{GND}	DC Ground Current per Ground Pin		±100		mA
T_{STG}	Storage Temperature Range		−65 to +150		°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−20W TSSOP−20 UDFN20		96 150 123	°C/W
P_D	Power Dissipation in Still Air	SOIC−20W TSSOP−20 UDFN20		1302 833 1016	mW
MSL	Moisture Sensitivity Level			Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model		2 1	kV
$I_{LATCHUP}$	Latchup Performance (Note 3)			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm−by−114mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued per JEDEC/JEP172A.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Positive DC Supply Voltage		0.9	3.6	V
V_I	Input Voltage		GND	3.6	V
V_O	Output Voltage	(Power Down Mode)	GND	3.6	V
		(3−State Mode)	GND	3.6	
		(Active Mode)	GND	V_{CCB}	
T_A	Operating Temperature Range		−40	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate		0	5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS – INPUT VOLTAGES

Symbol	Parameter	Test Conditions	Port	V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
						Min	Typ (Note 4)	Max	Min	Max	
V_{IH}	Input HIGH Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	2.0	–	–	2.0	–	V
				2.3 – 2.7		1.6	–	–	1.6	–	
				1.65–1.95		0.65 V_{CCA}	–	–	0.65 V_{CCA}	–	
				1.1 – 1.6		0.7 V_{CCA}	–	–	0.7 V_{CCA}	–	
				0.9		–	0.9 V_{CCA}	–	–	–	
V_{IL}	Input LOW Voltage		$\overline{OE}$, A	2.7 – 3.6	0.9 – 3.6	–	–	0.8	–	0.8	V
				2.3 – 2.7		–	–	0.7	–	0.7	
				1.65–1.95		–	–	0.35 V_{CCA}	–	0.35 V_{CCA}	
				1.1 – 1.6		–	–	0.3 V_{CCA}	–	0.3 V_{CCA}	
				0.9		–	0.1 V_{CCA}	–	–	–	

4. All typical values are at T_A = 25°C.

DC ELECTRICAL CHARACTERISTICS – OUTPUT VOLTAGES

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C			–40°C to +125°C		Unit
					Min	Typ (Note 4)	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_I = V_{IH} or V_{IL}:								V
		I_{OH} = –100 μA	0.9	0.9	–	V_{CCB} – 0.1	–	–	–	
			1.1 – 3.6	1.1 – 3.6	V_{CCB} – 0.1	–	–	V_{CCB} – 0.1	–	
		I_{OH} = –3 mA	1.1	1.1	0.85	–	–	0.85	–	
		I_{OH} = –6 mA	1.4	1.4	1.05	–	–	1.05	–	
		I_{OH} = –8 mA	1.65	1.65	1.2	–	–	1.2	–	
		I_{OH} = –12 mA	2.3	2.3	1.8	–	–	1.8	–	
			2.7	2.7	2.2	–	–	2.2	–	
		I_{OH} = –18 mA	2.3	2.3	1.7	–	–	1.7	–	
			3.0	3.0	2.4	–	–	2.4	–	
		I_{OH} = –24 mA	3.0	3.0	2.2	–	–	2.2	–	
V_{OL}	Output LOW Voltage	V_I = V_{IH} or V_{IL}:								V
		I_{OL} = 100 μA	0.9	0.9	–	0.1	–	–	–	
			1.1 – 3.6	1.1 – 3.6	–	–	0.1	–	0.1	
		I_{OL} = 3 mA	1.1	1.1	–	–	0.25	–	0.25	
		I_{OL} = 6 mA	1.4	1.4	–	–	0.35	–	0.35	
		I_{OL} = 8 mA	1.65	1.65	–	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.3	2.3	–	–	0.4	–	0.4	
			2.7	2.7	–	–	0.4	–	0.4	
		I_{OL} = 18 mA	2.3	2.3	–	–	0.4	–	0.4	
			3.0	3.0	–	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	3.0	–	–	0.55	–	0.55	

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DC ELECTRICAL CHARACTERISTICS – LEAKAGE AND SUPPLY CURRENTS

Symbol	Parameter	Test Conditions	V_{CCA} (V)	V_{CCB} (V)	–40°C to +85°C		–40°C to +125°C		Unit
					Min	Max	Min	Max	
I_I	Input Leakage Current	V_I = 3.6 V or GND	0.9 – 3.6	0.9 – 3.6	–	±1.0	–	±5.0	μA
I_{OZ}	3–State Output Leakage	$\overline{OE}$ = V_{IH}; V_O = GND to 3.6 V	3.6	3.6	–	±1.0	–	±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_I or V_O = 0 to 3.6 V A	0	0.9 – 3.6	–	±1.0	–	±5.0	μA
		B	0.9 – 3.6	0	–	±1.0	–	±5.0	
I_{CCA}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	5.0	–	10	μA
			0	0.9 – 3.6	–	–1.0	–	–5.0	
			0.9 – 3.6	0	–	5.0	–	10	
I_{CCB}	Quiescent Supply Current	V_I = V_{CCA} or GND; I_O = 0	0.9 – 3.6	0.9 – 3.6	–	5.0	–	10	μA
			0	0.9 – 3.6	–	5.0	–	10	
			0.9 – 3.6	0	–	–1.0	–	–5.0	

NOTE: Connect ground before applying supply voltage V_{CCA} or V_{CCB}. This device is designed with the feature that the power–up sequence of V_{CCA} and V_{CCB} will not damage the IC.

AC ELECTRICAL CHARACTERISTICS (Notes 5 and 6)

Symbol	Parameter	V_{CCA} (V)	T_A = –40°C to +85°C					T_A = –40°C to +125°C					Unit
			V_{CCB} (V)					V_{CCB} (V)					
			3.3	2.5	1.8	1.5	1.2	3.3	2.5	1.8	1.5	1.2	
			Max	Max	Max	Max	Max	Max	Max	Max	Max	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to B	3.3	2.9	3.3	4.5	5.6	9.3	3.3	3.8	5.0	6.2	9.5	nS
		2.5	3.6	3.7	4.6	5.7	9.4	4.0	4.0	5.1	6.3	9.6	
		1.8	3.9	4.0	4.9	6.0	9.6	4.3	4.3	5.4	6.6	9.8	
		1.5	4.2	4.3	5.2	6.3	9.8	4.7	4.7	5.8	7.0	10.0	
		1.2	5.1	5.2	6.2	7.1	11.0	5.7	5.8	6.9	7.9	11.2	
t_{PZH}, t_{PZL}	Output Enable, $\overline{OE}$ to B	3.3	3.8	4.7	6.8	8.7	12.4	4.2	5.2	7.5	9.6	12.4	nS
		2.5	4.4	4.8	7.0	8.8	12.4	4.4	5.3	7.7	9.7	12.4	
		1.8	5.1	5.9	7.4	9.2	12.9	5.1	5.9	8.2	10.2	12.9	
		1.5	5.6	6.4	7.7	9.6	13.3	6.2	6.4	8.5	10.6	13.3	
		1.2	7.7	8.7	9.8	11.0	14.7	8.5	8.7	9.8	11.0	14.7	
t_{PHZ}, t_{PLZ}	Output Disable, $\overline{OE}$ to B	3.3	6.2	6.4	8.1	9.3	10.2	6.9	7.1	9.0	10.3	11.3	nS
		2.5	5.2	6.2	8.2	8.8	10.4	5.8	6.9	9.1	10.4	11.5	
		1.8	6.9	6.9	8.7	9.9	10.9	7.6	7.6	9.6	10.9	12.0	
		1.5	7.6	7.4	9.1	10.3	11.3	8.2	8.4	10.1	11.4	12.5	
		1.2	8.6	8.6	9.6	10.6	12.4	9.0	10.1	10.5	10.6	13.7	

5. Propagation delays defined per Figure 3.
6. These parameters are guaranteed by characterization and are not production tested.

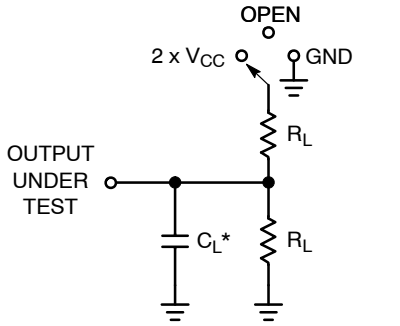
CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 4)	Unit
C_{IN}	Control Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}	2.5	pF
$C_{I/O}$	I/O Pin Input Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}	5.0	pF
C_{PD} (Note 7)	Power Dissipation Capacitance	V_{CCA} = V_{CCB} = 3.3 V, V_I = 0 V or V_{CCA}, f = 10 MHz	12	pF

7. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: $I_{CC(operating)} \cong C_{PD} \times V_{CC} \times f_{IN} \times N_{SW}$ where $I_{CC} = I_{CCA} + I_{CCB}$ and N_{SW} = total number of outputs switching.

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*C_L Includes probe and jig capacitance

Figure 3. AC Test Circuit

Test	Switch	C_L	R_L
t_{PLH}, t_{PHL}	OPEN	15 pF	2 kΩ
t_{PLZ}, t_{PZL}	2 x V_{CC}		
t_{PHZ}, t_{PZH}	GND		
C_L includes probe and jig capacitance Pulse generator Z_O = 50 Ω Input f = 1.0 MHz; t_W = 500 ns			

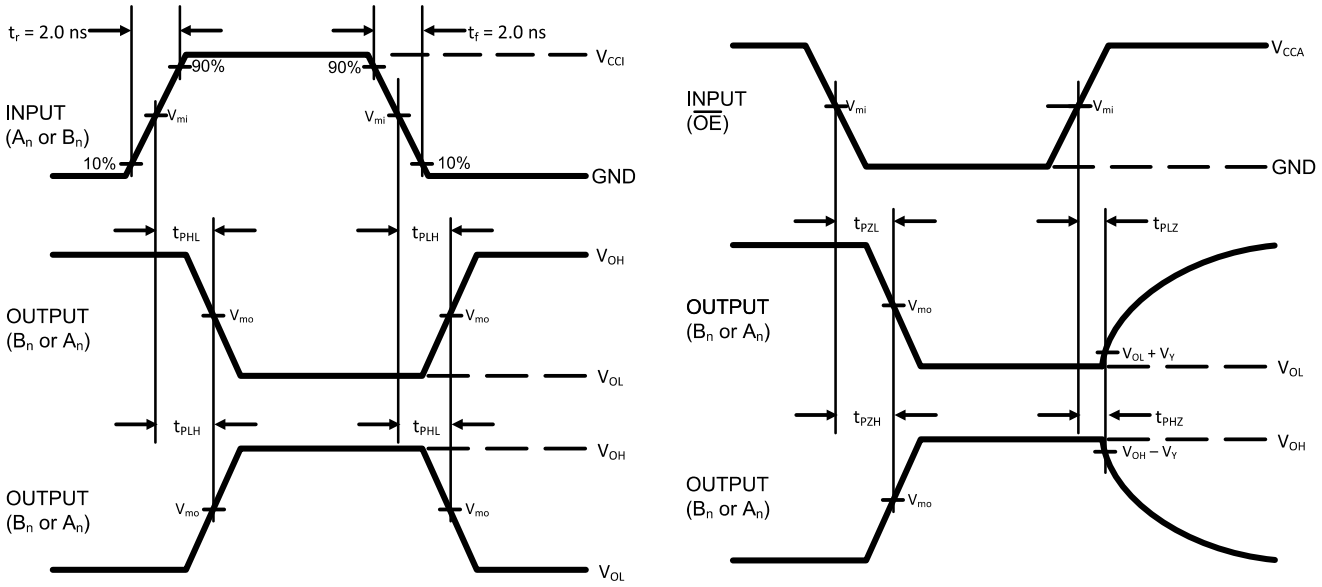


Figure 4. AC Waveforms

Symbol	V_{CC}				
	3.0 V – 3.6 V	2.3 V – 2.7 V	1.65 V – 1.95 V	1.4 V – 1.6 V	1.1 V – 1.3 V
V_{mi}	V_{CCI}/2	V_{CCI}/2	V_{CCI}/2	V_{CCI}/2	V_{CCI}/2
V_{mo}	V_{CCO}/2	V_{CCO}/2	V_{CCO}/2	V_{CCO}/2	V_{CCO}/2
V_Y	0.3 V	0.15 V	0.15 V	0.1 V	0.1 V

8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

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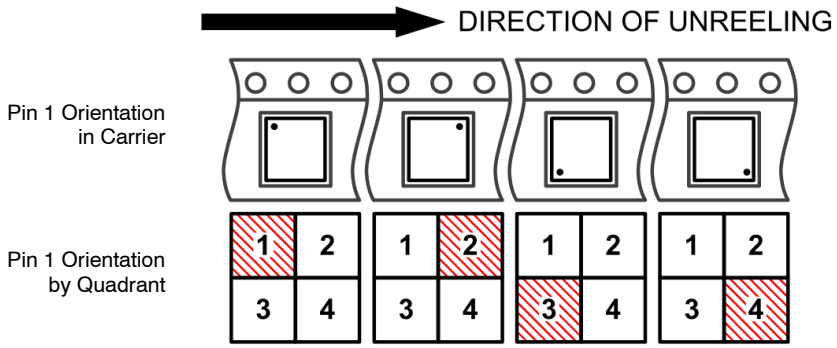
ORDERING INFORMATION

Device	Marking	Package	Pin 1 Quadrant	Shipping†
NL3V8T244DWR2G (Contact **onsemi** sales)	TBD	SOIC−20W	1	1000 Units / Tape & Reel
NL3V8T244DTR2G (Contact **onsemi** sales)	TBD	TSSOP−20	1	2500 Units / Tape & Reel
NL3V8T244MU2TAG	AC	UDFN20	1	3000 Units / Tape & Reel
NL3V8T240MU2TAG	LA	UDFN20	1	3000 Units / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	5/27/2025
1	Updated 16 values in AC Electrical Characteristics table.	5/8/2026

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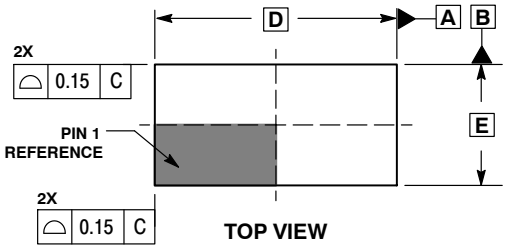
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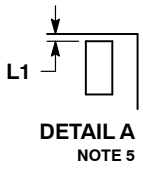


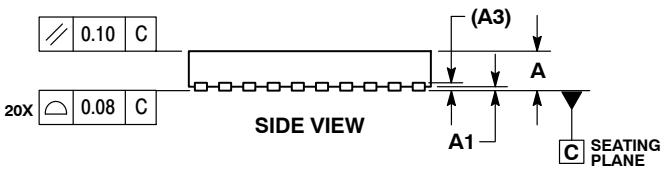
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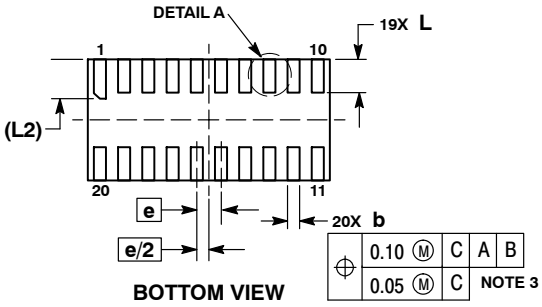
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CASE 517AK
ISSUE O

DATE 14 NOV 2006





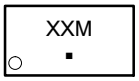




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	4.00 BSC	
E	2.00 BSC	
e	0.40 BSC	
L	0.50	0.60
L1	0.00	0.03
L2	0.60	0.70

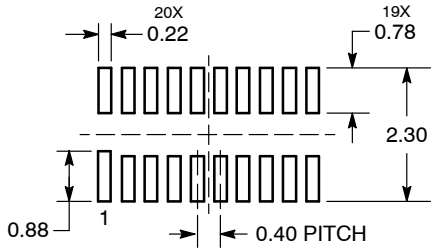
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

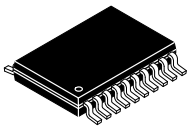
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DESCRIPTION:	**UDFN20 4x2, 0.4P**	**PAGE 1 OF 1**

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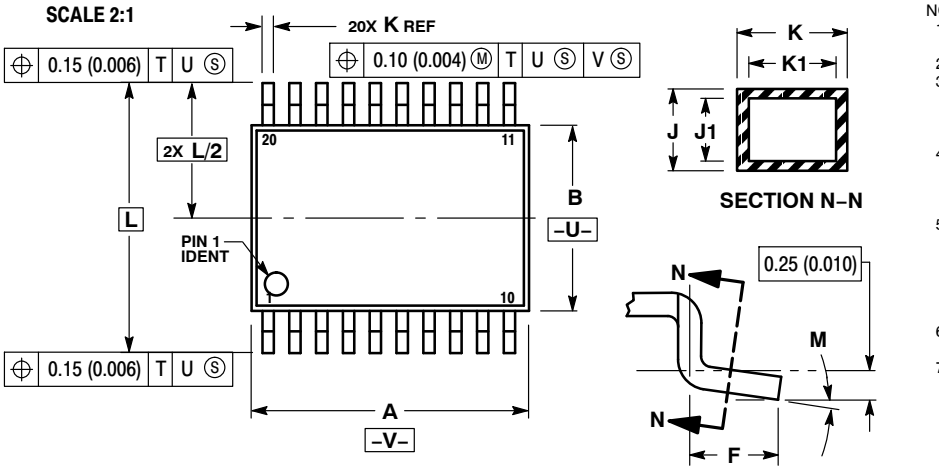
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TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

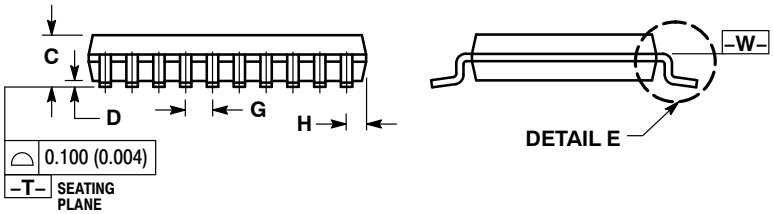


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SECTION N−N

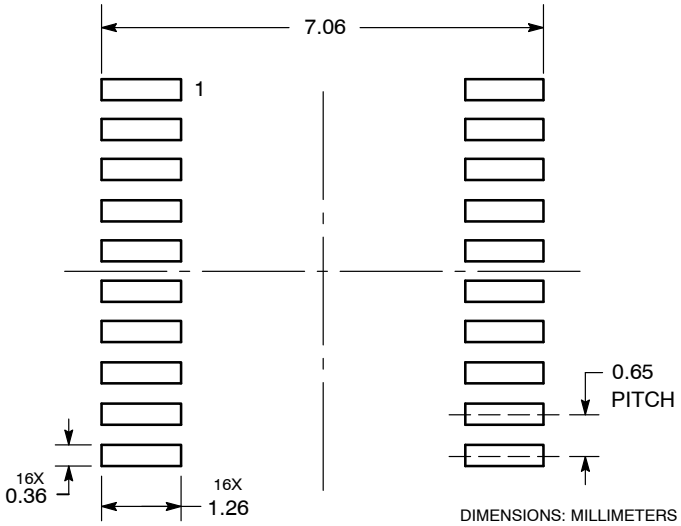
DETAIL E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

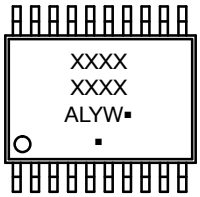
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

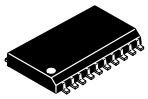
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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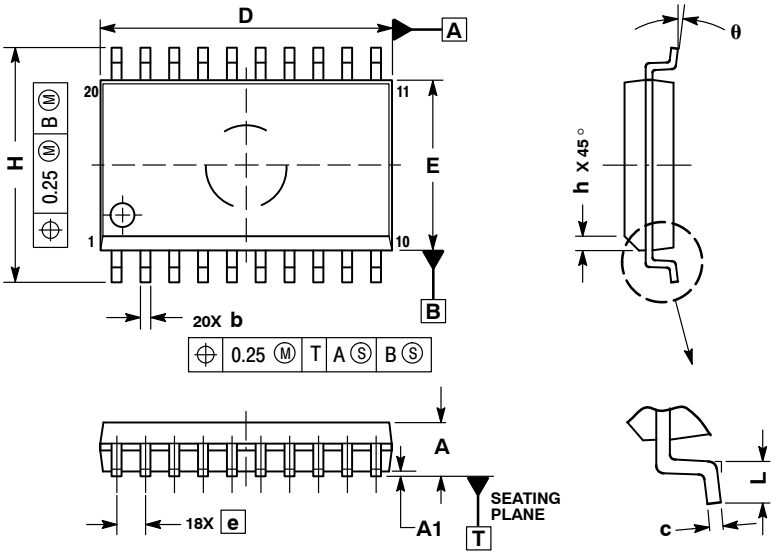
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SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015

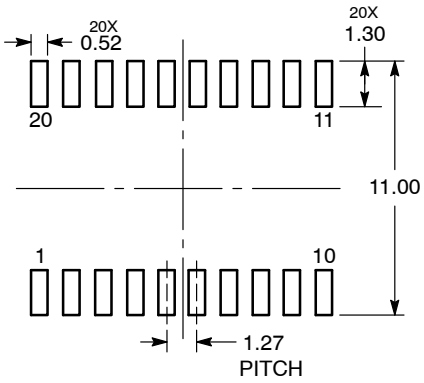
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

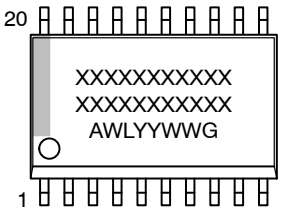
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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