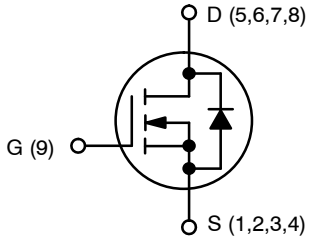
# MOSFET – Power, Single N-Channel, Source-Down
## 30 V, 1.0 mΩ, 294 A
## NTMFSS0D9N03P8

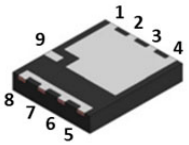
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 1.0 mΩ @ 10 V | 294 A |
| | 1.2 mΩ @ 4.5 V | |

### Features
- Advance 5x6 mm Package with Source Down and Center Gate Design to Improve Power Density, Efficiency, and Thermal Performance
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low $Q_G$ and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen−Free / BFR Free and are RoHS Compliant

### Typical Applications
- ORing
- Motor Drives
- Power Load Switch
- DC−DC




N−CHANNEL MOSFET




TDFN9 5x6
CASE 520AE

### MARKING DIAGRAM


A = Assembly Location
Y = Year Code
W = Work Week Code
ZZ = Assembly Lot Code

### ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Note 2) | Steady State | $T_C$ = 25°C | $I_D$ | 294 | A |
| | | $T_C$ = 85°C | | 212 | |
| Power Dissipation $R_{\theta JC}$ (Note 2) | | $T_C$ = 25°C | $P_D$ | 125 | W |
| | | $T_C$ = 85°C | | 65 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A$ = 25°C | $I_D$ | 46 | A |
| | | $T_A$ = 85°C | | 33 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | $T_A$ = 25°C | $P_D$ | 3.0 | W |
| | | $T_A$ = 85°C | | 1.6 | |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | TBD | A |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 45 A, L = 0.3 mH) | | | $E_{AS}$ | 304 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case − Steady State (Note 2) | $R_{\theta JC}$ | 1.0 | °C/W |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 41 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 $in^2$ pad size, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 500 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D$ = 500 μA, ref to 25°C | | | −37 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 500 μA | | 1.0 | | 3.0 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D$ = 500 μA, ref to 25°C | | | 12 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 30 A | | | 0.62 | 1.0 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 30 A | | | 0.86 | 1.2 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 5 V, $I_D$ = 30 A | | | 175 | | S |
| Gate Resistance | $R_G$ | $T_A$ = 25°C | | | 1 | | Ω |
| **CHARGES & CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 15 V | | | 9000 | | pF |
| Output Capacitance | $C_{OSS}$ | | | | 3010 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 275 | | |
| Threshold Gate Charge | $Q_{G(TH)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 15 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 24 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 12 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V; $I_D$ = 30 A | | | 127 | | nC |
| **SWITCHING CHARACTERISTICS, $V_{GS}$ = 10 V** (Note 5) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V, $I_D$ = 30 A, $R_G$ = 6 Ω | | | 20.4 | | ns |
| Rise Time | $t_r$ | | | | 19.3 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 125.4 | | |
| Fall Time | $t_f$ | | | | 49.5 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A | $T_J$ = 25°C | | 0.75 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.58 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIS/dt = 100 A/μs, $I_S$ = 30 A | | | 68.4 | | ns |
| Charge Time | $t_a$ | | | | 35.2 | | |
| Discharge Time | $t_b$ | | | | 33.2 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 92 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

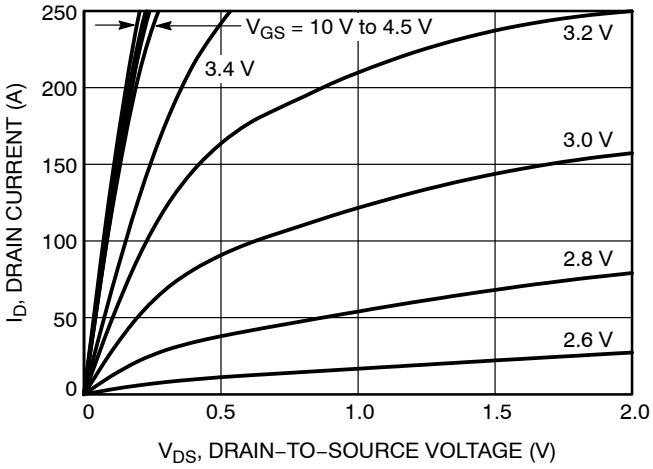



**Figure 1. On−Region Characteristics**

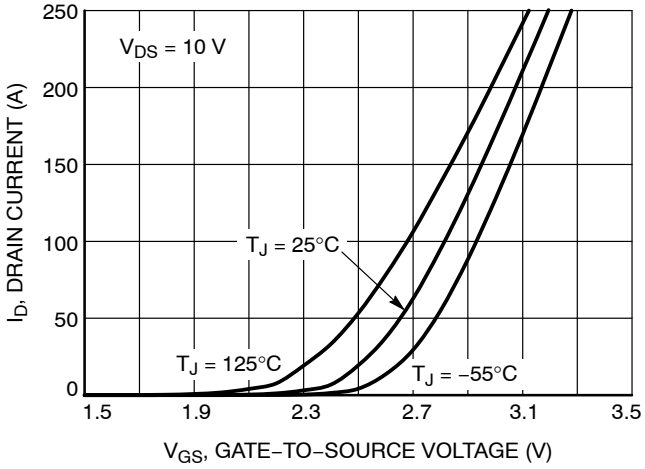



**Figure 2. Transfer Characteristics**

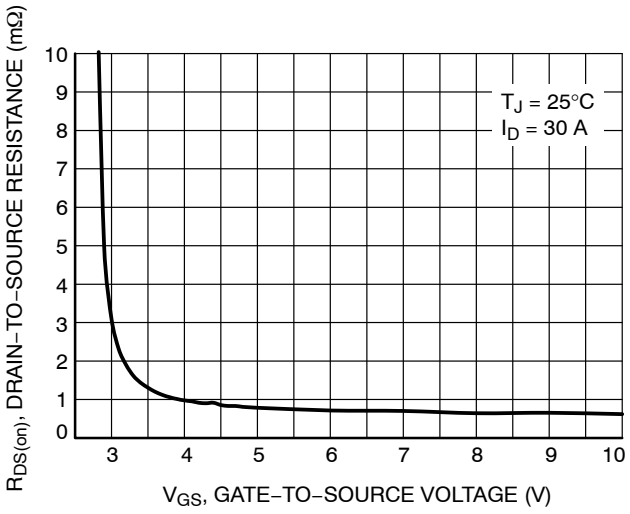



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

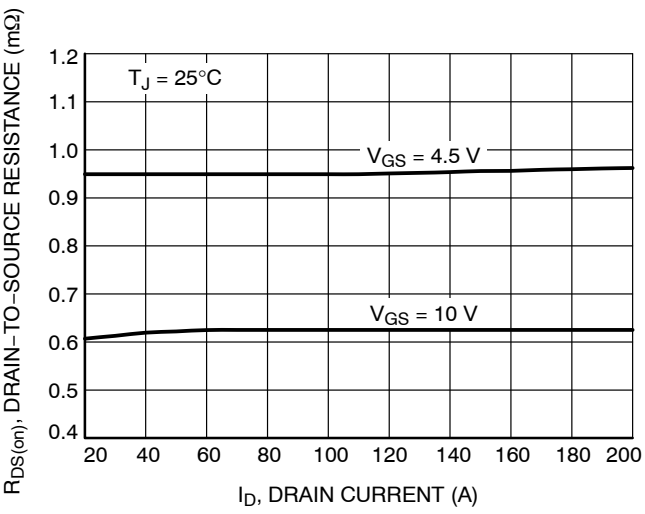



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

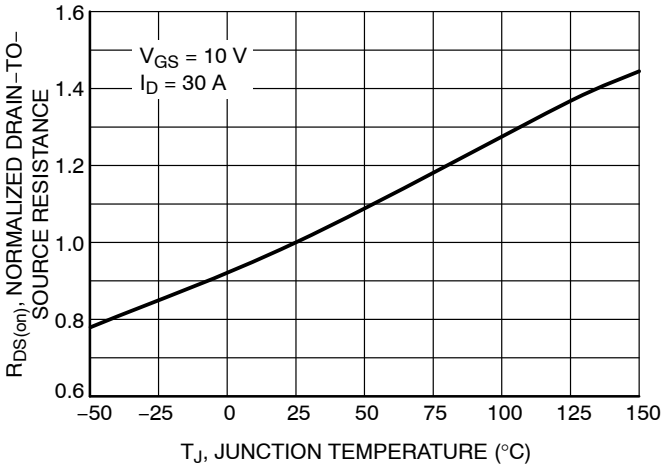



**Figure 5. On−Resistance Variation with Temperature**

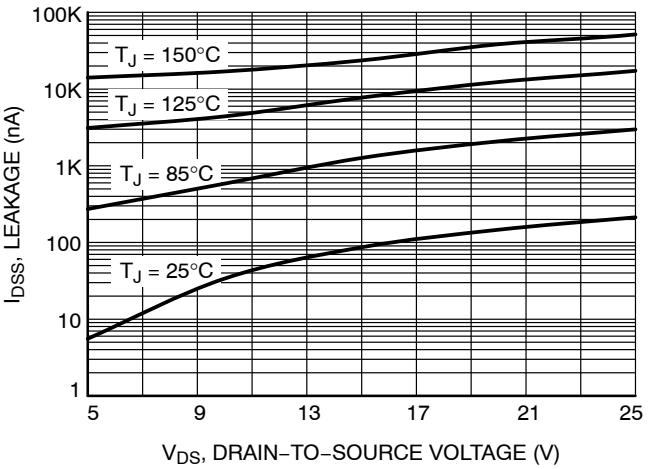



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

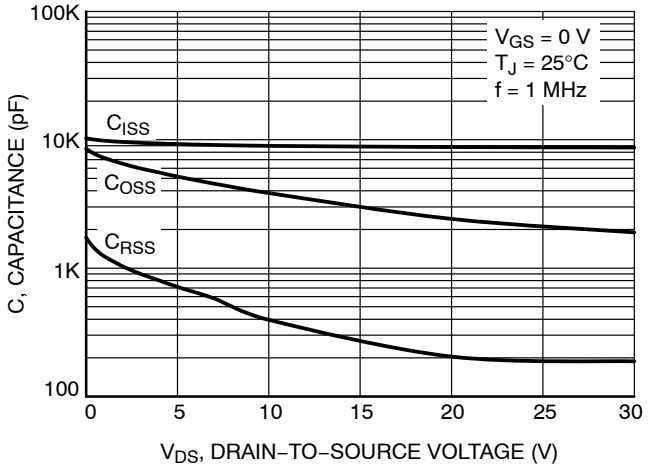



**Figure 7. Capacitance Variation**

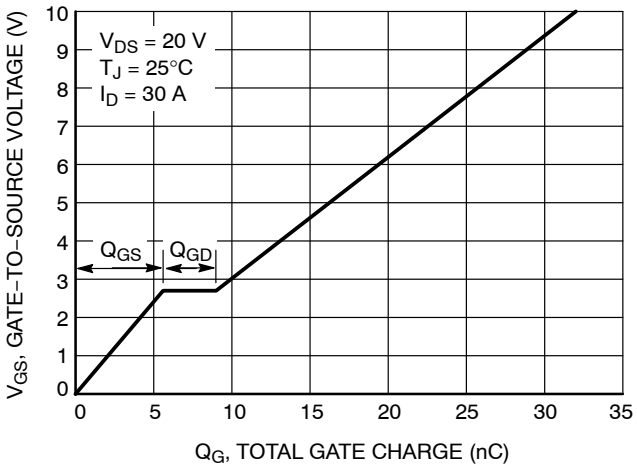



**Figure 8. Gate−to−Source vs. Total Charge**

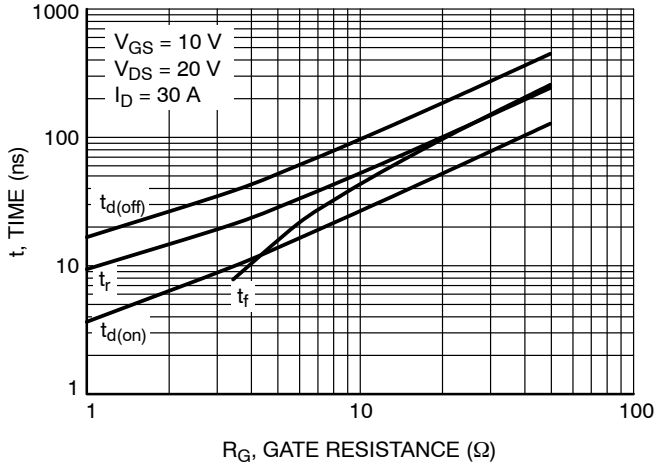



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

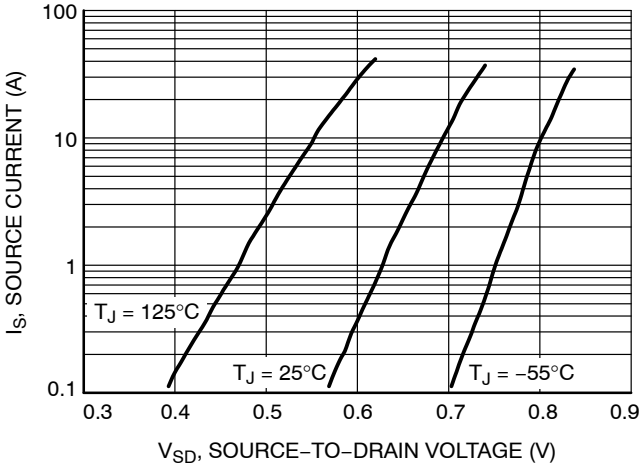



**Figure 10. Diode Forward Voltage vs. Current**

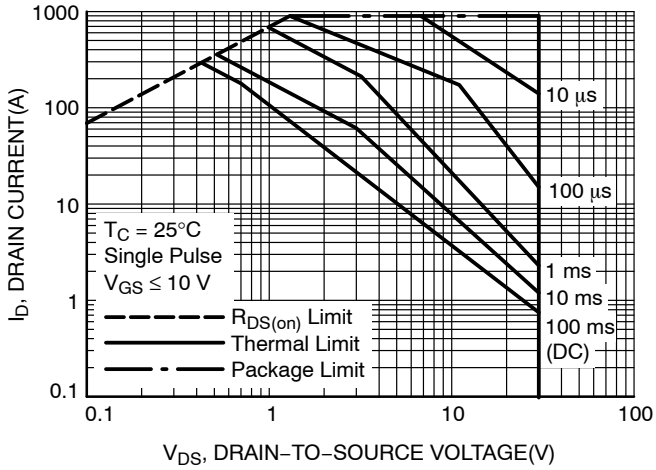



**Figure 11. Safe Operating Area**

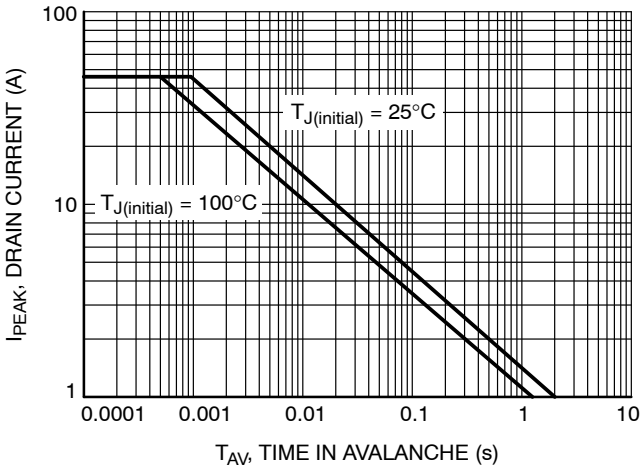



**Figure 12. $I_{PEAK}$ vs. Time in Avalanche**

## TYPICAL CHARACTERISTICS

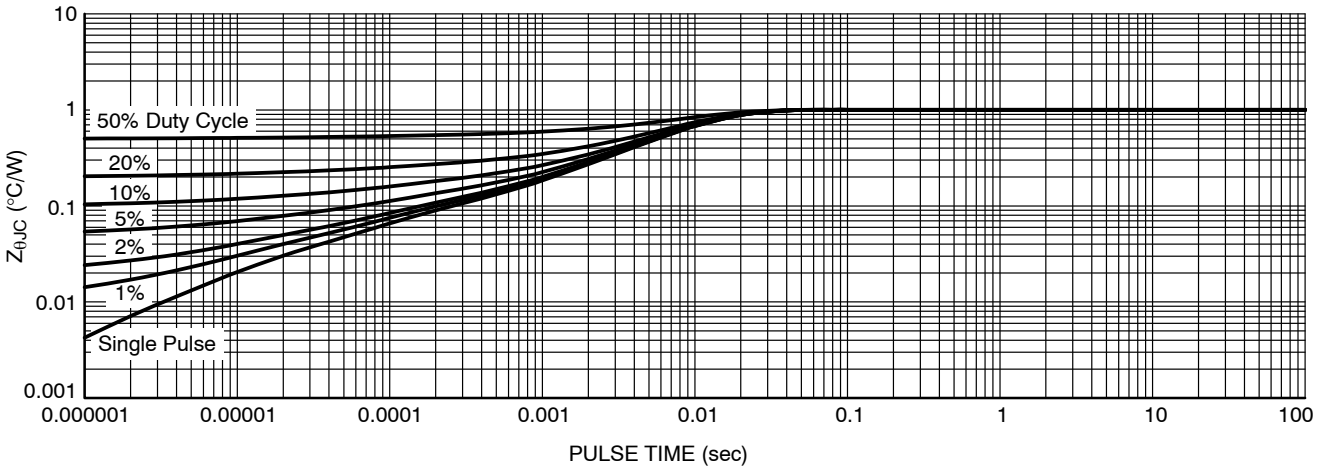
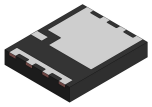



**Figure 13. Thermal Characteristics**

### DEVICE ORDERING INFORMATION

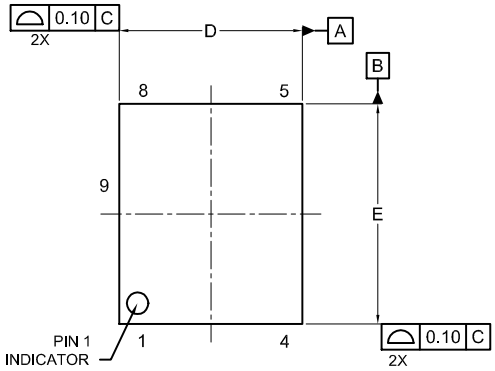
| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NTMFSS0D9N03P8 | 9N03P8 | TDFN9<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

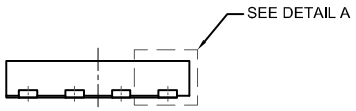


**TDFN9 5x6, 1.27P**
CASE 520AE
ISSUE B

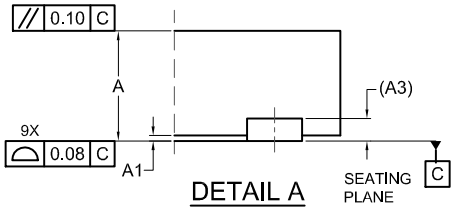
DATE 24 NOV 2022



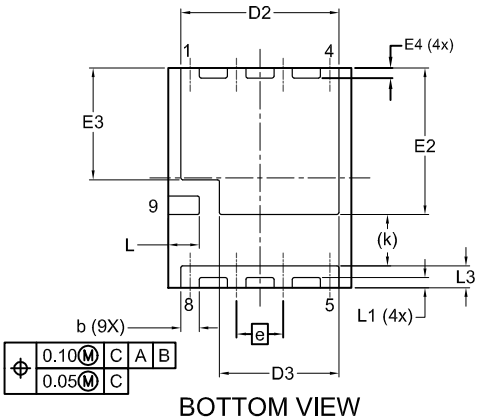

TOP VIEW



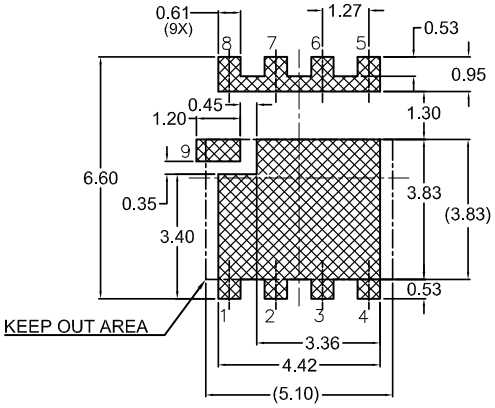

FRONT VIEW




DETAIL A
SCALE: 3:1




BOTTOM VIEW




LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.95 | 1.00 | 1.05 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.45 | 0.50 | 0.55 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 4.10 | 4.30 | 4.50 |
| D3 | 3.16 | 3.26 | 3.36 |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 3.90 | 4.00 | 4.10 |
| E3 | 2.95 | 3.05 | 3.15 |
| E4 | 0.18 | 0.28 | 0.38 |
| e | | 1.27 BSC | |
| k | | 1.40 REF | |
| L | 0.75 | 0.85 | 0.95 |
| L1 | 0.18 | 0.28 | 0.38 |
| L3 | 0.50 | 0.60 | 0.70 |

## GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TDFN9 5x6, 1.27P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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**onsemi Website:** www.onsemi.com

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

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