

MOSFET – Power, Dual, N-Channel, for 1-Cell Lithium-ion Battery Protection

12 V, 7.1 mΩ, 14 A

EFC2J004NUZ

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halide Free and RoHS Compliant

Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	± 8	V
Source Current (DC)	I_S	14	A
Source Current (Pulse) $PW \leq 100 \mu\text{s}$, duty cycle $\leq 1\%$	I_{SP}	60	A
Total Dissipation (Note 1)	P_T	1.5	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

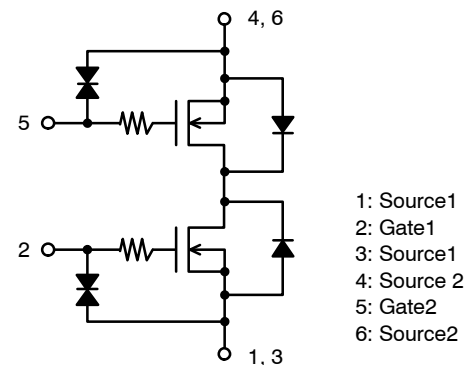
Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	$R_{\theta JA}$	83	$^\circ\text{C/W}$

1. Surface mounted on ceramic substrate ($5000 \text{ mm}^2 \times 0.8 \text{ mm}$).

V_{SSS}	$R_{SS(on)}$ Max	I_S Max
12 V	7.1 mΩ @ 4.5 V	14 A
	7.7 mΩ @ 3.8 V	
	9.5 mΩ @ 3.1 V	
	12.4 mΩ @ 2.5 V	

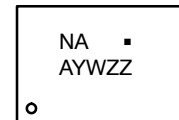
ELECTRICAL CONNECTION

N-Channel



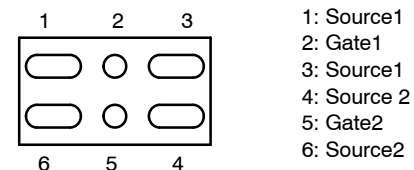
WLCSP6,
2.11x1.18x0.10
CASE 567NP

MARKING DIAGRAM



NA = Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Number
▪ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

EFC2J004NUZ

ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 2)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source to Source Breakdown Voltage	V _{(BR)SSS}	I _S = 1 mA, V _{GS} = 0 V (Figure 1)	12	–	–	V
Zero-Gate Voltage Source Current	I _{SSS}	V _{SS} = 10 V, V _{GS} = 0 V (Figure 1)	–	–	1	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±8 V, V _{SS} = 0 V (Figure 2)	–	–	±1	μA
Gate Threshold Voltage	V _{GS(th)}	V _{SS} = 6 V, I _S = 1 mA (Figure 3)	0.4	–	1.3	V
Static Source to Source On-State Resistance (Note 2)	R _{SS(on)}	I _S = 5 A, V _{GS} = 4.5 V (Figure 4)	3.7	5.4	7.1	mΩ
		I _S = 5 A, V _{GS} = 3.8 V (Figure 4)	4.1	5.9	7.7	mΩ
		I _S = 5 A, V _{GS} = 3.1 V (Figure 4)	4.6	6.7	9.5	mΩ
		I _S = 5 A, V _{GS} = 2.5 V (Figure 4)	5.8	8.4	12.4	mΩ
Turn-ON Delay Time	t _{d(on)}	V _{SS} = 5 V, V _{GS} = 3.8 V, I _S = 5 A, R _g = 10 kΩ (Figure 5)	–	15	–	μs
Rise Time	t _r		–	35	–	μs
Turn-OFF Delay Time	t _{d(off)}		–	100	–	μs
Fall Time	t _f		–	75	–	μs
Total Gate Charge	Q _g	V _{SS} = 6 V, V _{GS} = 4.5 V, I _S = 14 A (Figure 6)	–	36	–	nC
Forward Source to Source Voltage	V _{F(S-S)}	I _S = 3 A, V _{GS} = 0 V (Figure 7)	–	0.76	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Mounted on **onsemi** board.

Test Circuits are Example of Measuring FET1 Side

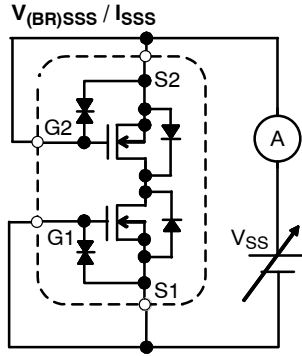


Figure 1. Test Circuit 1

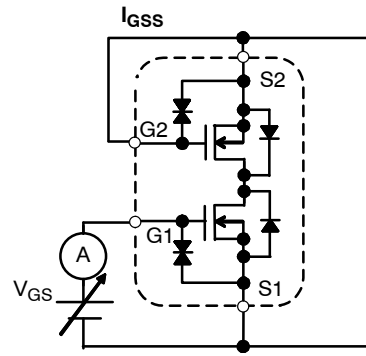


Figure 2. Test Circuit 2

When FET1 is measured, Gate and Source of FET2 are short-circuited.

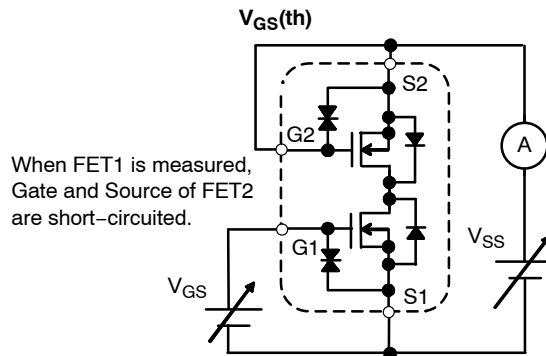


Figure 3. Test Circuit 3

When FET1 is measured, Gate and Source of FET2 are short-circuited.

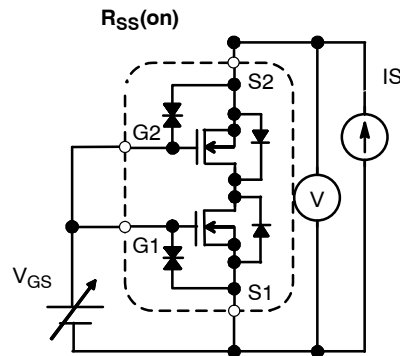


Figure 4. Test Circuit 4

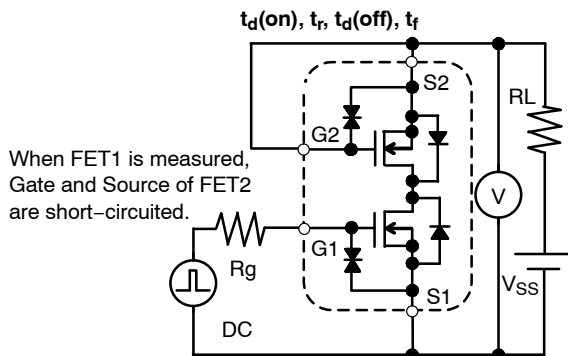


Figure 5. Test Circuit 5

When FET1 is measured, Gate and Source of FET2 are short-circuited.

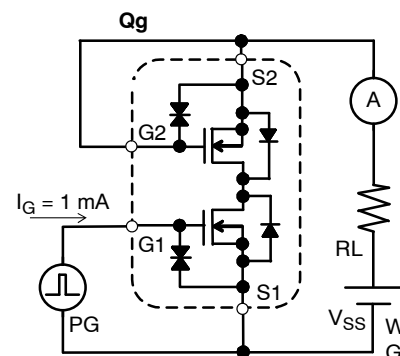


Figure 6. Test Circuit 6

When FET1 is measured, Gate and Source of FET2 are short-circuited.

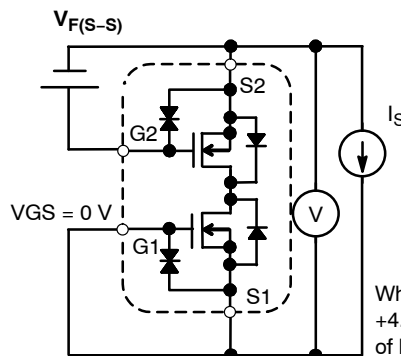


Figure 7. Test Circuit 7

When FET1 is measured, +4.5 V is added to V_GS of FET2.

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

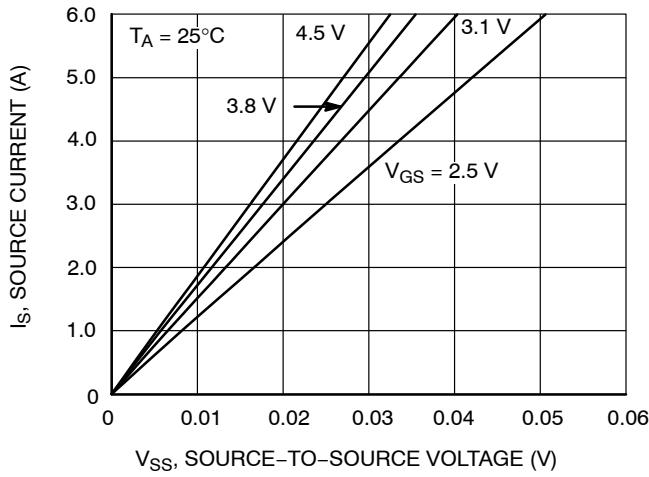


Figure 8. $I_S - V_{SS}$

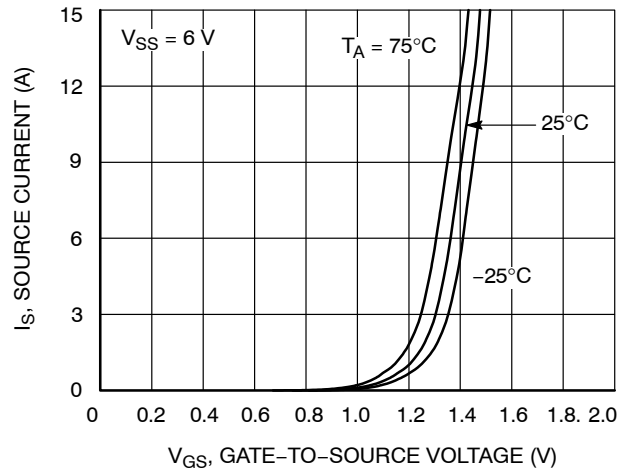


Figure 9. $I_S - V_{GS}$

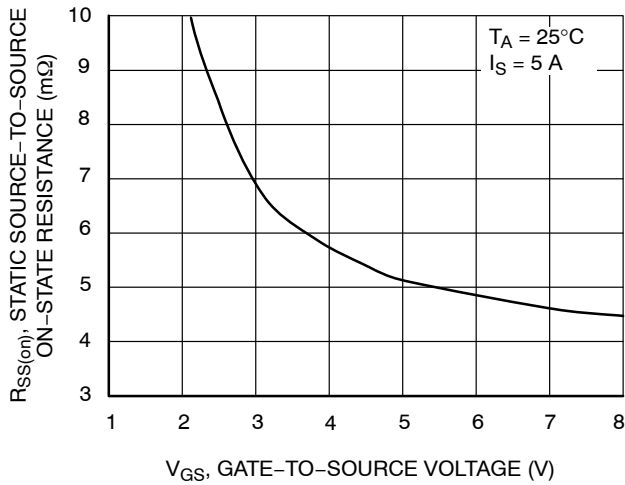


Figure 10. $R_{SS(on)} - V_{GS}$

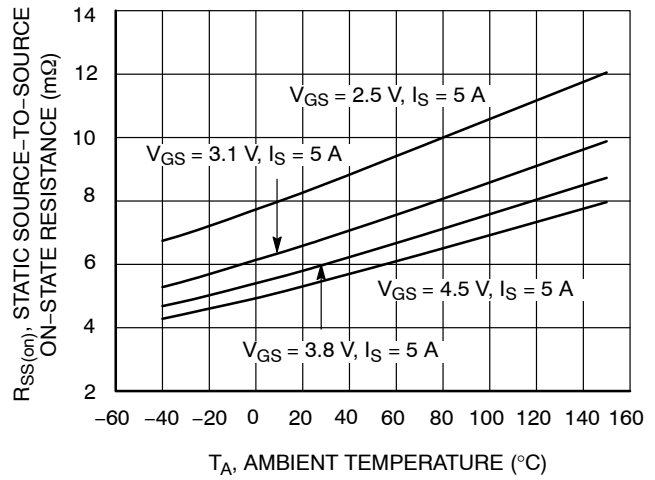


Figure 11. $R_{SS(on)} - T_A$

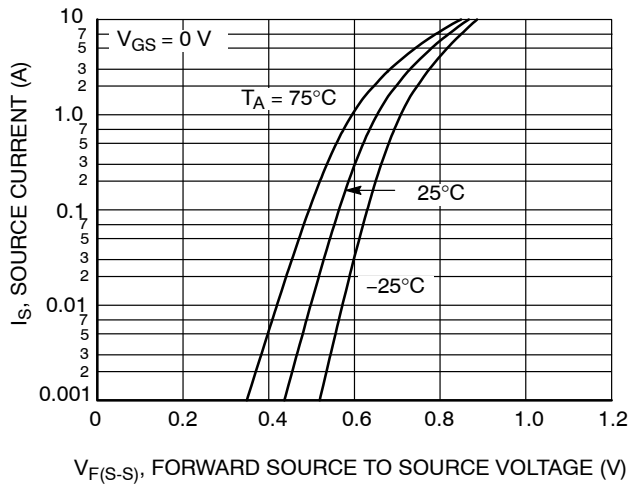


Figure 12. $I_S - V_{F(S-S)}$

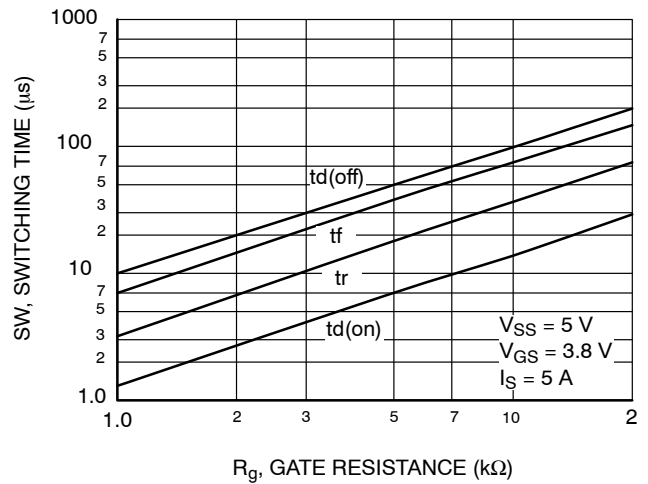


Figure 13. SW Time - R_g

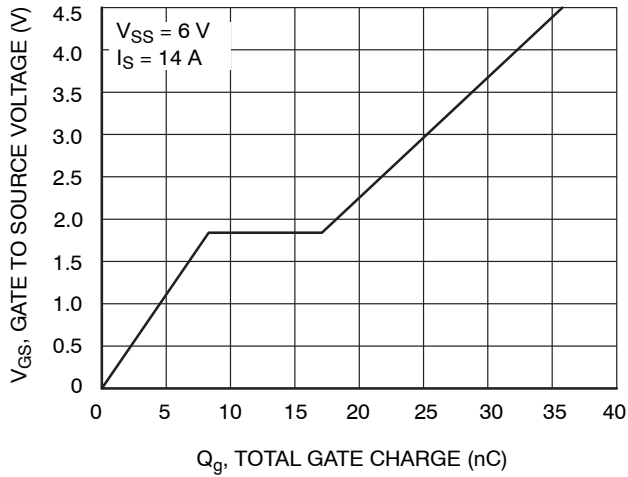


Figure 14. $V_{GS} - Q_g$

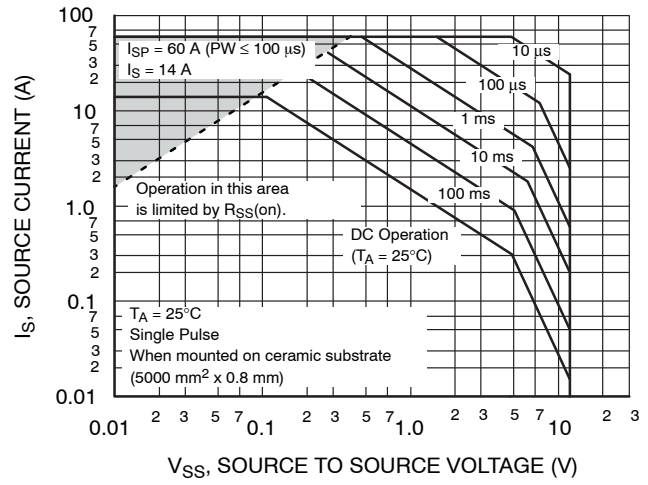


Figure 15. SOA

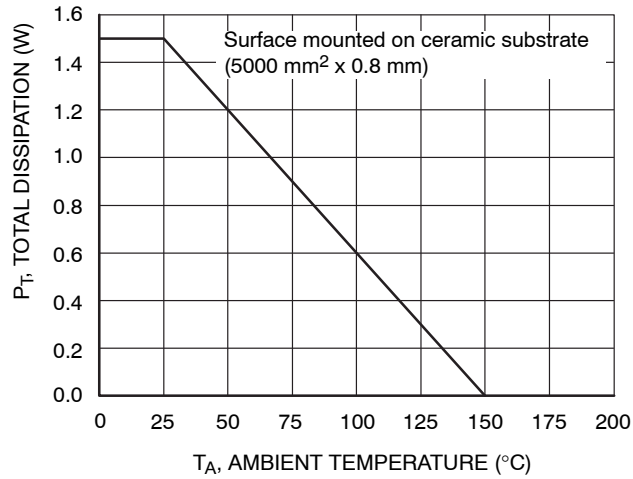


Figure 16. $P_T - T_a$

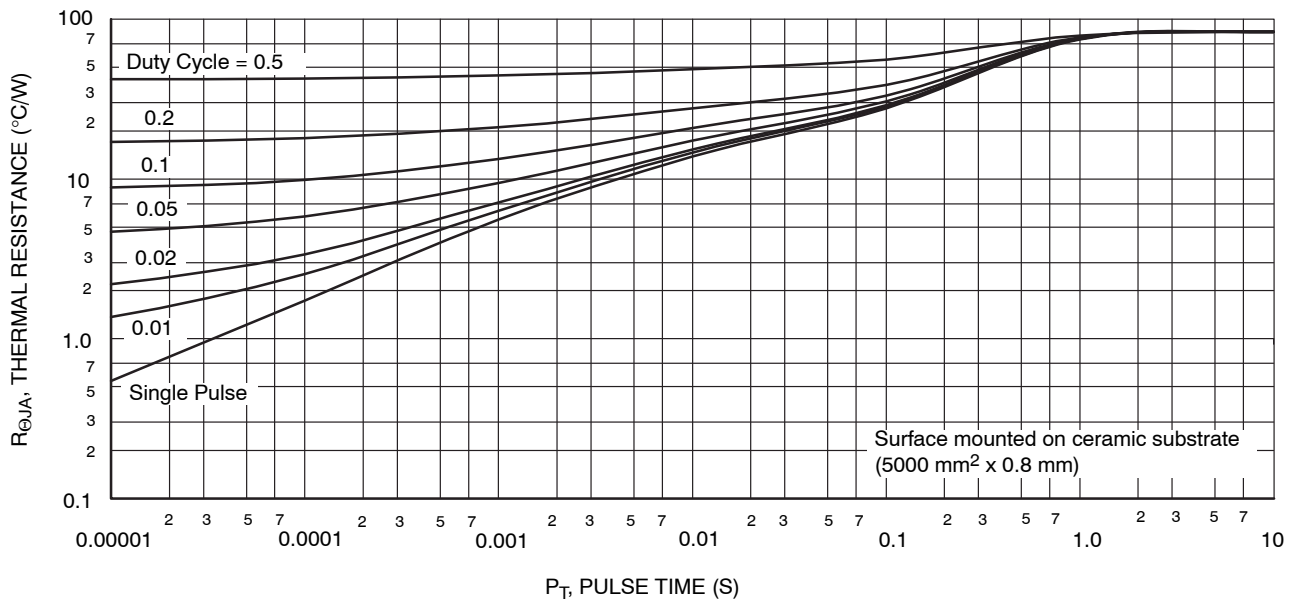


Figure 17. $R_{\theta JA} - \text{Pulse Time}$

EFC2J004NUZ

ORDERING INFORMATION

Device	Marking	Package	Shipping [†] (Qty / Packing)
EFC2J004NUZTDG	NA	WLCSP6, 2.11x1.18x0.10 (Pb-Free / Halogen Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

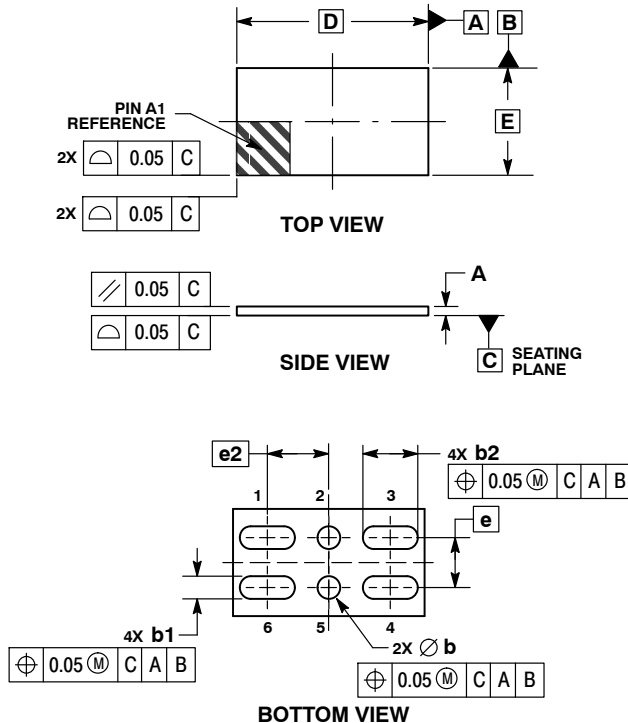
Note on usage: Since the EFC2J004NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.



SCALE 4:1

WLCSP6, 2.11x1.18x0.10
CASE 567NP
ISSUE B

DATE 22 DEC 2016

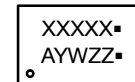


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.08	0.10	0.12
b	0.22	0.25	0.28
b1	0.27	0.30	0.33
b2	0.575	0.605	0.635
D	2.11 BSC		
E	1.18 BSC		
e	0.55 BSC		
e2	0.6775 BSC		

GENERIC
MARKING DIAGRAM*

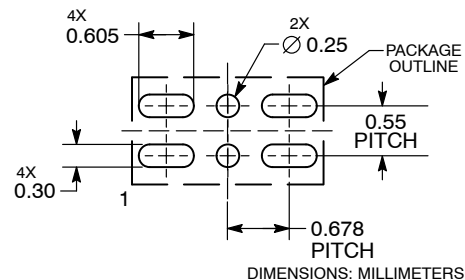


- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Assembly Lot
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	WLCSP6, 2.11X1.18X0.10	PAGE 1 OF 1

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