TLE7185-1E

3-Phase Bridge Driver IC

Automotive Power

Never stop thinking

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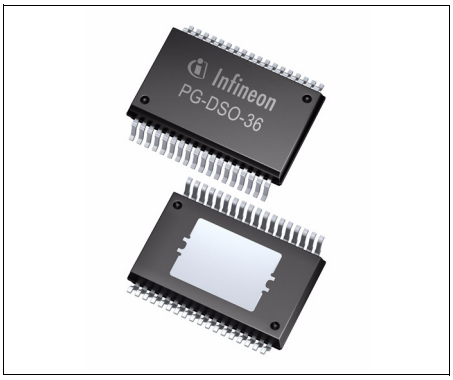
1 Overview



PG-DSO-36-38

Features

- Drives 6 N-Channel Power MOSFETs
- Separate control input for each MOSFET
- Separate Source pin for each MOSFET
- Integrated charge pump for operation at low battery voltages
- Adjustable dead time
- Shoot through protection and Shoot through option
- Analog adjustable Short Circuit Protection levels
- Low quiescent current mode
- 2 bit diagnosis / $\overline{\text{ERR}}$x
- Over temperature warning
- Over voltage warning
- Under voltage warning
- Under voltage lockout
- 0 …95% Duty cycle of High Side MOSFETs
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7185-1E is a driver IC dedicated to control the 6 to 12 external MOSFETs forming the converter for high current 3 phase motor drives in the automotive sector. It incorporates features like short circuit detection, diagnosis and combines it with typical automotive specific requirements.

The TLE7185-1E is especially designed for low battery voltage and therefore it is specified down to 5.5V supply voltage.

Typical applications are cooling fan, water pump, electro-hydraulic and electric power steering. The TLE7185-1E is designed for 12V power net.

Type	Package	Marking
TLE7185-1E	PG-DSO-36-38	TLE7185-1E

2 Block Diagram

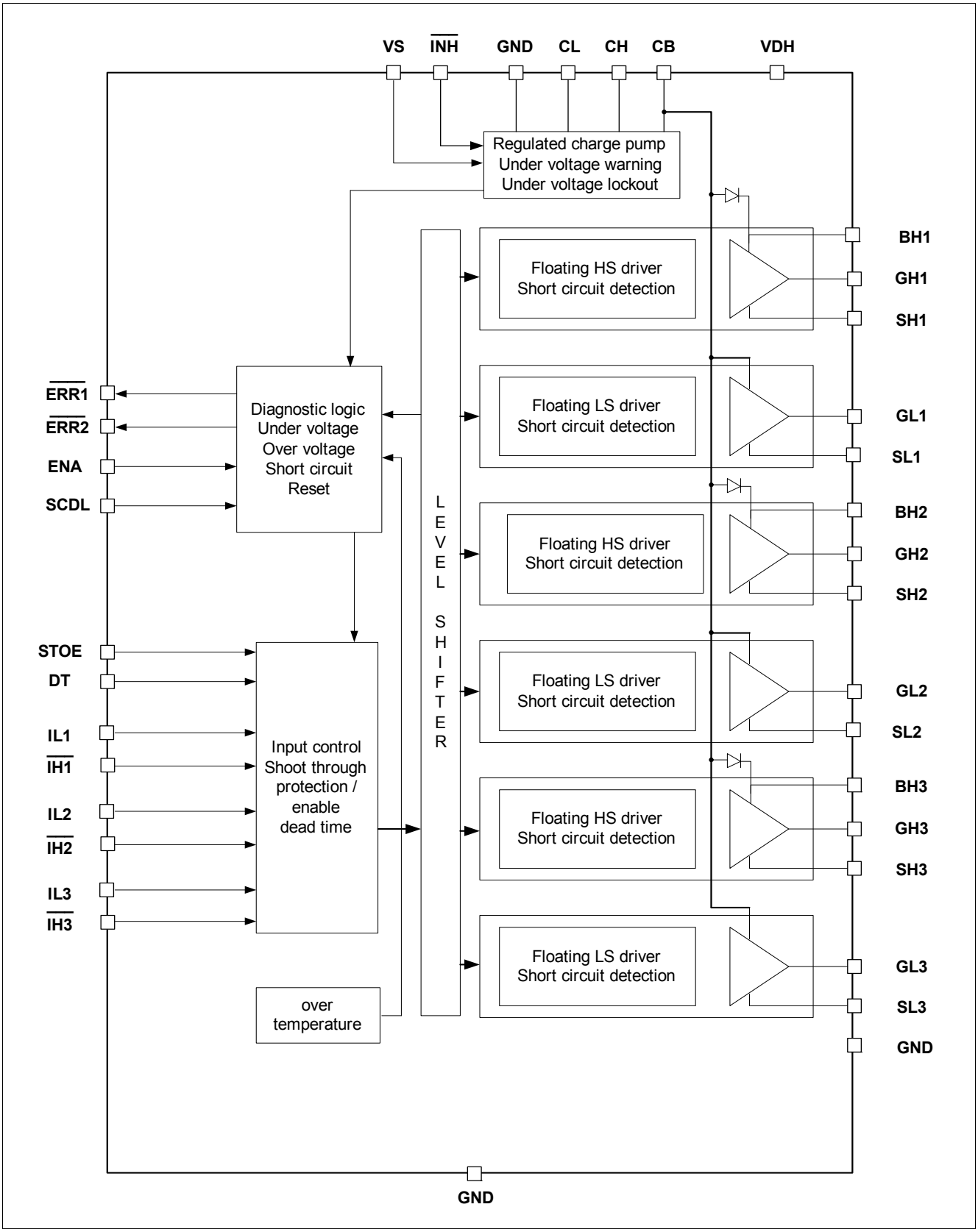


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment TLE7185-1E

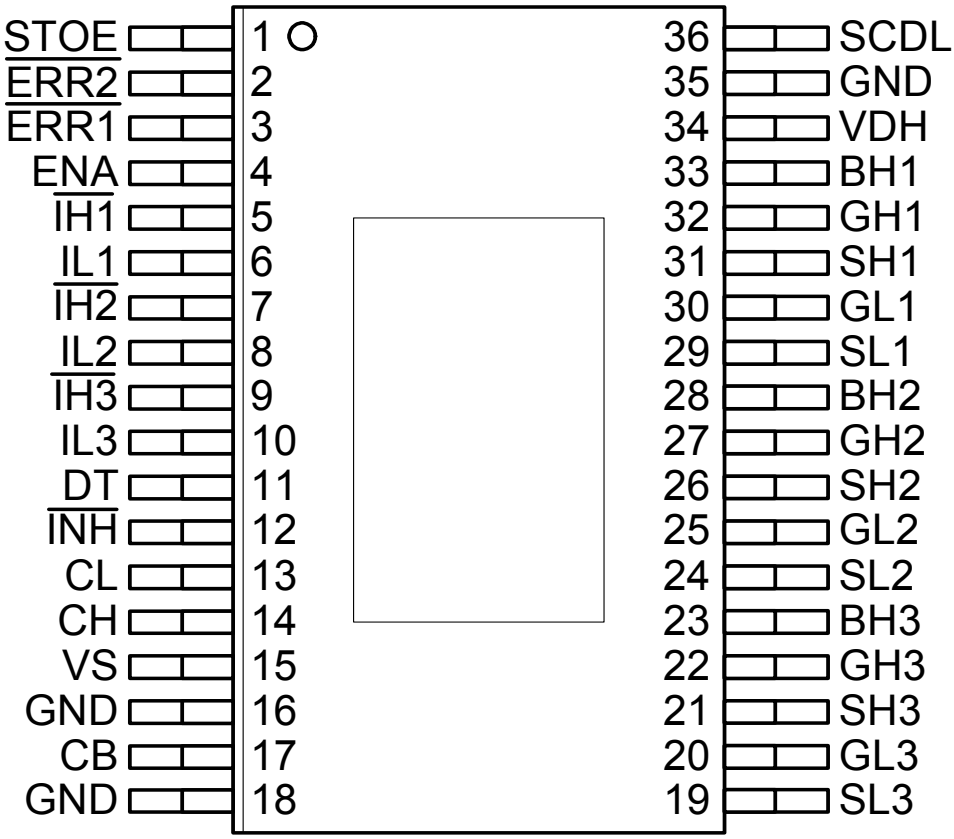


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	STOE	Input pin to enable shoot through option in all 3 half bridges (active high)
2	$\overline{\text{ERR2}}$	Open drain error output 2
3	$\overline{\text{ERR1}}$	Open drain error output 1
4	ENA	Input pin for reset of $\overline{\text{ERRx}}$ registers + active switch off of external MOSFETs, set HIGH to enable operation
5	$\overline{\text{IH1}}$	Input for high side switch 1 (active low)
6	IL1	Input for low side switch 1 (active high)
7	$\overline{\text{IH2}}$	Input for high side switch 2 (active low)
8	IL2	Input for low side switch 2 (active high)
9	$\overline{\text{IH3}}$	Input for high side switch 3 (active low)
10	IL3	Input for low side switch 3 (active high)
11	DT	Input pin for adjustable dead time function, connect to GND via resistor
12	$\overline{\text{INH}}$	Input pin to activate (high) / deactivate (low) the complete Driver IC
13	CL	Charge pump capacitor - terminal
14	CH	Charge pump capacitor + terminal
15	VS	Supply Pin
16	GND	
17	CB	Output of charge pump; connect to buffer capacitor
18	GND	
19	SL3	Pin for source connection of high side MOSFET 3
20	GL3	Output pin for gate of low side MOSFET 3
21	SH3	Pin for source connection of high side MOSFET 3
22	GH3	Output pin for gate of high side MOSFET 3
23	BH3	Pin for + terminal of the bootstrap capacitor of phase 3
24	SL2	Pin for source connection of high side MOSFET 2
25	GL2	Output pin for gate of low side MOSFET 2
26	SH2	Pin for source connection of high side MOSFET 2
27	GH2	Output pin for gate of high side MOSFET 2
28	BH2	Pin for + terminal of the bootstrap capacitor of phase 2
29	SL1	Pin for source connection of high side MOSFET 1
30	GL1	Output pin for gate of low side MOSFET 1
31	SH1	Pin for source connection of high side MOSFET 1
32	GH1	Output pin for gate of high side MOSFET 1
33	BH1	Pin for + terminal of the bootstrap capacitor of phase 1
34	VDH	Voltage input common drain high side for short circuit detection
35	GND	
36	SCDL	Input pin for adjustable Short Circuit Detection function, connect to GND via resistor
Cooling Tab	GND	Should be connected to GND

All GND pins and Cooling Tab should be interconnected.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-0.3	45	V	–
4.1.2	Supply voltage	V_{SR1}	-1.0	45	V	t < 60s, 5x
4.1.3	Supply voltage	V_{SR2}	-4.0	45	V	$R_{VS} \geq 4.7\Omega$;; 500ms, 5x
4.1.4	Voltage range at VDH	V_{VDH}	-0.3	55	V	–
4.1.5	Voltage range at VDH	V_{VDHR1}	-4.0	55	V	$R_{VDH} \geq 10\Omega$; 500ms, 5x
4.1.6	Voltage range at $\overline{IHx}$, ILx, ENA, $\overline{INH}$, STOE	V_{DP}	-0.3	18	V	–
4.1.7	Voltage range at $\overline{ERRx}$	V_{ERR}	-0.3	18	V	$R_{ERR} \geq 5k\Omega$
4.1.8	Voltage range at SCDL	V_{SCDL}	-0.3	18	V	$R_{SCDL} \geq 10k\Omega$
4.1.9	Voltage range at DT	V_{DT}	-0.3	6	V	–
4.1.10	Voltage range at BHx	V_{BH}	-0.3	55	V	–
4.1.11	Voltage range at GHx	V_{GH}	-0.3	55	V	–
4.1.12	Voltage range at GHx	V_{GHP}	-7.0	55	V	t<1µs / f=50kHz
4.1.13	Voltage range at SHx	V_{SH}	-2.6	45	V	–
4.1.14	Voltage range at SHx	V_{SHP}	-7.0	45	V	t<1µs / f=50kHz
4.1.15	Voltage range at GLx	V_{GL}	-1.0	18	V	–
4.1.16	Voltage range at GLx	V_{GLP}	-7.0	18	V	t<0.5µs /f=50kHz
4.1.17	Voltage range at SLx	V_{SL}	-1.0	5.0	V	–
4.1.18	Voltage range at SLx	V_{SLP}	-7.0	7.0	V	t<0.5µs /f=50kHz
4.1.19	Voltage difference Gxx-Sxx	V_{GS}	-0.3	15	V	–
4.1.20	Voltage difference BHx-SHx	V_{BS}	-0.3	15	V	–
4.1.21	Minimum bootstrap capacitor C_{BS}	C_{BS}	330	–	nF	–
4.1.22	Voltage range at CL	V_{CL}	-0.3	25	V	–
4.1.23	Voltage range at CH, CB	V_{CHB}	-0.3	25	V	–
4.1.24	Voltage difference CH-CL	V_{CHL}	-0.3	25	V	–
Temperatures						
4.1.25	Junction temperature	T_j	-40	150	°C	–
4.1.26	Storage temperature	T_{stg}	-55	150	°C	–
Power Dissipation						
4.1.27	Power Dissipation (DC) @ TCASE=135°C	P_{tot}	–	3	W	–
ESD Susceptibility						

Absolute Maximum Ratings (cont'd)[1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.28	ESD Resistivity[2)]	V_{ESD}	-2	2	kV	–
4.1.29	CDM[3)]	V_{CDM}	-500	500	V	–

1) Not subject to production test, specified by design.

2) ESD susceptibility HBM according to EIA/JESD 22-A 114B

3) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage[1)]	V_S	5.5	32	V	–
4.2.2	Quiescent current[2)]	I_Q	–	22	µA	V_S,V_{DH}<15V; INH=Low; T_j<85°C
4.2.3	Supply current at Vs (device disabled)	$I_{Vs(0)}$	–	20	mA	–
4.2.4	Supply current at Vs (device enabled)	$I_{Vs(1)}$	–	80	mA	6xQ_Gxf_{PWM}≤30mA; V_s=5.5..16V;
4.2.5	Supply current at Vs (device enabled)	$I_{Vs(2)}$	–	45	mA	6xQ_Gxf_{PWM}≤30mA; Vs=16..32V;
4.2.6	Duty cycle HS	D_{HS}	0	95	%	f_{PWM}=20kHz; continuous operation; C_{BSx}≥330nF
4.2.7	Duty cycle LS	D_{LS}	0	100	%	
4.2.8	Charge pump capacitor	C_{CP}	1.0	4.7	µF	–
4.2.9	Buffer capacitor	C_{CB}	1.0	4.7	µF	–

1) For wake up of driver min. 6.5V Vs are required

2) total current consumption from power net (Vs and VDH)

The limitations in the PWM frequency are given by thermal constraints and limitations in the duty cycle (charging time of bootstrap capacitor).

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	–	5	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	29	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) **Exposed Heatslug Package use this sentence**: Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Default State of Inputs

Table 1 Default State of Inputs (if left open)

Characteristic	State	Remark
Default state of ILx	Low	Low side MOSFETs off
Default state of $\overline{IHx}$	High	High side MOSFETs off
Default state of ENA	Low	Device outputs disabled
Default state of $\overline{INH}$	Low	Sleep mode, I_Q < 22 µA
Default state of STOE	Low	Shoot through option is disabled

Note: To activate the driver both $\overline{INH}$ and ENA must be pulled high. To allow shoot through all ILx pins must be pulled high, all $\overline{IHx}$ must be pulled low and STOE must be pulled high

5 Description and Electrical Characteristics

5.1 MOSFET Driver

5.1.1 Output Stages

The 3 low side and 3 high side powerful push-pull output stages of the TLE7185-1E are all floating blocks, each with its own source pin. This allows the direct connection of the output stage to the source of each single MOSFET, allowing a perfect control of each gate-source voltage even when 200A are driven in the bridge with rise and fall times below 1µs.

All 6 output stages have the same output power and thanks to the used bootstrap principle they can be switched all up to 30kHz.

To ensure high gate voltages even at low battery voltages, the driver IC has an integrated charge pump. It allows operation of normal level MOSFETs down to 5.5V supply.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 5.2.1**.[1)]

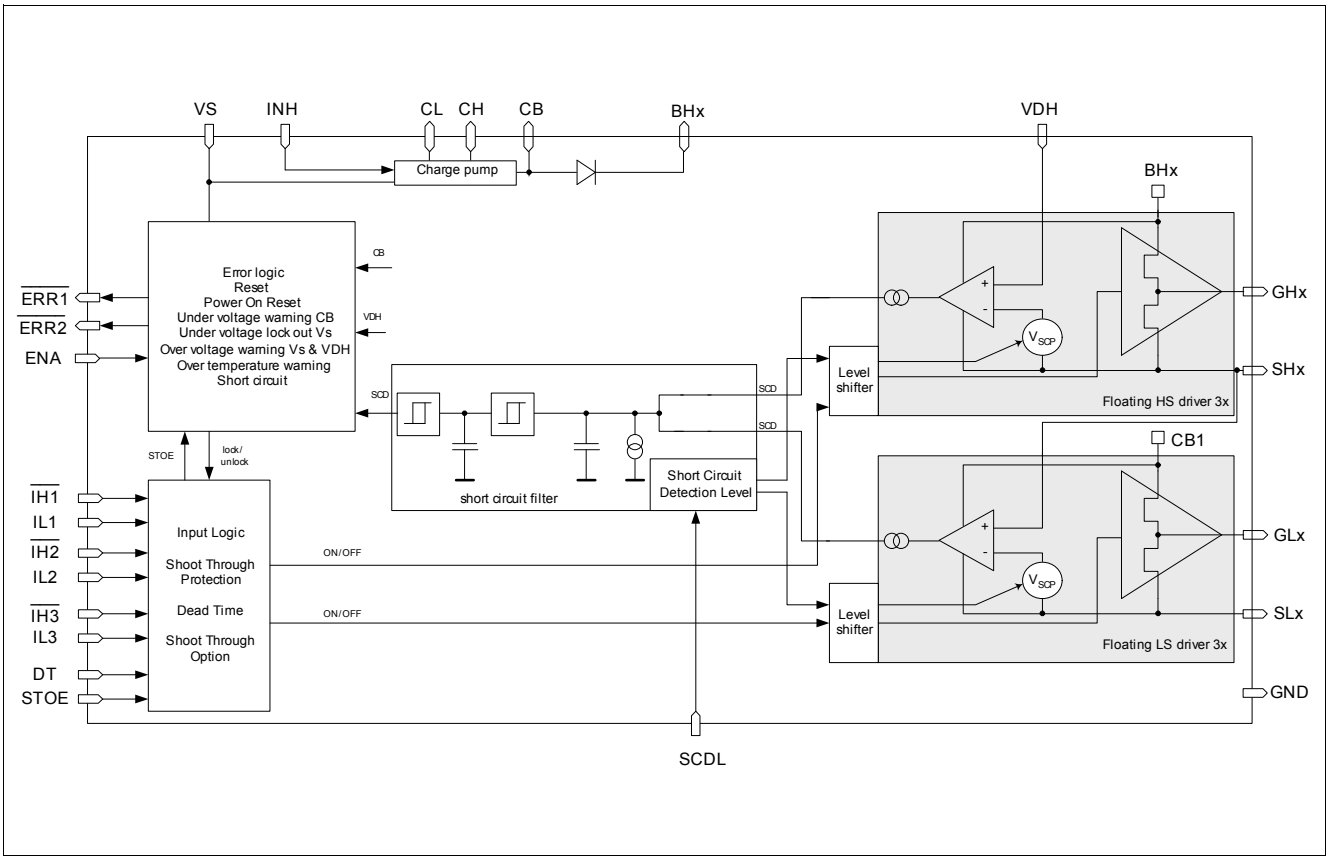


Figure 3 Block Diagram of Driver Stages including Short Circuit Detection

5.1.2 Operation at Vs<12V - Integrated Charge Pump

The TLE7185-1E provides a feature tailored to the requirements in 12V automotive applications. Often the operation of an application has to be assured even at 9V supply voltage or lower. Normally bridge driver ICs

1) The high side outputs are not designed to be used for low side MOSFETs; the low side outputs are not designed to be used for high side MOSFETs

provide in such conditions clearly less than 9V to the gate of the external MOSFETs, increasing their R_{DSon} and the associated power dissipation.

The TLE7185-1E has a charge pump circuitry for external capacitors.

The operation of the charge pump is independent upon the pulse pattern of the MOSFETs.

The output of the charge pump is regulated to about 12V.

The output of the charge pump supplies the output stages for the low side MOSFETs with sufficient voltage to assure 10V at the MOSFETs´ gate even if the supply voltage is below 10V.

It supplies as well the bootstrap circuitry for the high side output stages. Off course the bootstrap principle leads to the fact that the bootstrap capacitors needs to be charged regularly. The charging time for the bootstrap capacitor is specified (duty cycle HS) as well as the current consumption from the bootstrap capacitor in permanent “on” condition.

The charge pump is only deactivated when the device is put into sleep mode via $\overline{\text{INH}}$.

During Start Up of the device it is not allowed to have any PWM patterns at the ILx and $\overline{\text{IHx}}$ pins until the charge pumps have ramped up to their final values or it is recommended to keep the ENA pin low.

The size of the charge pump capacitor (pump capacitors C_{CP} as well as buffer capacitor C_{CB}) can be varied between 1 µF and 4.7 µF. Yet, larger capacitor values result in higher charge pump voltages and less voltage ripple on the charge pump buffer capacitor CB. Besides the capacitance values the ESR of the buffer capacitor CB determines the voltage ripple as well. It is recommended to use buffer capacitor CB that has small ESR.

Please. see also **Chapter 5.1.3** for capacitor selection.

5.1.3 Sleep Mode

When the $\overline{\text{INH}}$ pin is set to low, the driver will be set to sleep mode. The $\overline{\text{INH}}$ pin switches off the complete supply structure of the device and leads finally to an under voltage shut down of the complete driver. Enabling the device with the $\overline{\text{INH}}$ pin means to switch on the supply structure. The device will run through power on reset during wake up. It is recommended to perform a Reset by ENA after Wake up to remove possible ERR signals; Reset is performed by keeping one or more ENA pins low until the charge pump voltages have ramped up.

Enabling and disabling with the $\overline{\text{INH}}$ pin is not very fast. For fast enable / disable the ENA pin is recommended.

When the TLE7185-1E is in $\overline{\text{INH}}$ mode ($\overline{\text{INH}}$ is low) or when the supply voltage is not available on the Vs pin, then the driver IC is not supplied, the charge pump is inactive and the charge pump buffer capacitor as well as the bootstrap capacitors are discharged.

5.1.4 Electrical Characteristics

Electrical Characteristics MOSFET drivers

V_S = 5.5 to 32V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Inputs							
5.1.1	Low level input voltage of ILx; $\overline{\text{IHx}}$; ENA; STOE	V_{I_LL}	–	–	1.0	V	–
5.1.2	High level input voltage of ILx; $\overline{\text{IHx}}$; ENA; STOE	V_{I_HL}	2.0	–	–	V	–
5.1.3	Input hysteresis of $\overline{\text{IHx}}$; ILx; ENA; STOE	dV_I	100	–	–	mV	–
5.1.4	$\overline{\text{IHx}}$ pull up resistors	R_{IH}	20	–	45	kΩ	pulled to 5V

Electrical Characteristics MOSFET drivers

V_S = 5.5 to 32V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.5	ILx; ENA; STOE pull down resistors	R_{IL}	20	–	45	kΩ	–
5.1.6	$\overline{INH}$ pull down resistor	R_{IL_INH}	30	–	75	kΩ	–
5.1.7	Low level input voltage of $\overline{INH}$	V_{INHL}	–	–	0.75	V	–
5.1.8	High level input voltage of $\overline{INH}$	V_{INHH}	2.5	–	–	V	–
Charge pump							
5.1.9	Charge pump output voltage	V_{CB}	11	–	13.5	V	V_s=7..32V; $6xQ_Gxf_{PWM}$≤30mA
5.1.10	Charge pump frequency	f_{CP}	38	55	72	kHz	–
MOSFET driver output							
5.1.11	Output source resistance	R_{Sou}	–	–	13.5	Ω	–
5.1.12	Output sink resistance	R_{Sink}	–	–	9.0	Ω	–
5.1.13	High level output voltage	V_{Gxx}	–	–	13.5	V	V_S<32V, $6xQ_Gxf_{PWM}$≤30mA
5.1.14	High level output voltage	V_{Gxx}	9	10	–	V	V_s=7V, $6xQ_Gxf_{PWM}$≤30mA, D.C.=94%; f_{PWM}=20kHz
5.1.15	High level output voltage	V_{GUV}	–	–	1.2	V	$\overline{INH}$=low or UVLO[1)]
5.1.16	Pull down resistor at BHx to GND	R_{INH}	30	–	80	kΩ	$\overline{INH}$=low or UVLO
5.1.17	Pull down resistor at CB to GND	R_{CBUV}	10	–	30	kΩ	$\overline{INH}$=low or UVLO
5.1.18	Bias current into BHx	I_{BH}	–	–	120	µA	V_{BSx}>5V; no switching
5.1.19	Bias current out of SHx	I_{SH}	–	40	–	µA	$\overline{INH}$=ENA=high; $\overline{IHx}$ =high; V_{BSx}=5V..13.0V
5.1.20	Bias current out of SLx	I_{SL}	–	–	1	mA	0V≤V_{SH}≤V_S+1V; no switching; V_{BSx}≥5V
5.1.21	Programmable internal dead time	t_{DT}	0.08 0.25 0.62 1.0 2.0	0.14 0.41 1.05 1.85 3.82	0.20 0.57 1.45 2.7 5.6	µs	R_{DT}=0 Ω R_{DT}=10 kΩ R_{DT}=47 kΩ R_{DT}=100 kΩ R_{DT}=1000 kΩ
5.1.22	Max. internal dead time	t_{DT_MAX}	2.3	–	6.4	µs	DT pin open
5.1.23	Input propagation time (low on)	$t_{P(ILN)}$	0	–	200	ns	C_{Load}=11nF; R_{Load}=1Ω
5.1.24	Input propagation time (low off)	$t_{P(ILF)}$	0	–	200	ns	
5.1.25	Input propagation time (high on)	$t_{P(IHN)}$	0	–	200	ns	
5.1.26	Input propagation time (high off)	$t_{P(IHF)}$	0	–	200	ns	
5.1.27	Absolute input propagation time difference between above propagation times	$t_{P(an)}$	–	–	100	ns	

Electrical Characteristics MOSFET drivers

V_S = 5.5 to 32V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Wake up / Inhibit							
5.1.28	$\overline{INH}$ propagation time to disable the output stages	t_{INH_Pdis}	–	–	10	µs	–
5.1.29	Wake up time; $\overline{INH}$ low to high	t_{INH_Pen1}	–	–	20	ms	V_s=6.5..8V Driver fully functional; ENA=low; C_{CB}=4.7µF
5.1.30	Wake up time; $\overline{INH}$ low to high	t_{INH_Pen2}	–	–	10	ms	V_s=8..32V Driver fully functional; ENA=low; C_{CB}=4.7µF

1) Not subjected to production test; specified by design

5.2 Protection and Diagnostic Functions

5.2.1 Short Circuit Protection

The TLE7185-1E provides a short circuit protection for the external MOSFETs. It is a monitoring of the drain-source voltage of the external MOSFETs. As soon as this voltage is higher than the short circuit detection level, a timer will start to run.

The short circuit detection level is programmable from outside by applying a voltage divider at the SCDL pin. The applied voltage at this pin will be used as short circuit detection level up to the specified maximum level. Above this level the short circuit detection is deactivated.

After a delay t_{SCP} all external MOSFETs will be switched off until the driver is reset by the ENA pin. The error flag is set.

The drain-source voltage monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding input is set to "on" and the dead time is expired.

For safety reasons a pull up resistor at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to high levels. In this case, the SCD is deactivated an error signal is set. This function is self clearing when the voltage at SCDL returns to the specified level.

The short circuit detection filter is realized with a capacitor, which is discharged with a current source with X µA. In case the output stage is switched on and the VDS of the MOSFET is still above SCDL, the capacitor is charged with a current source with Y µA. If this capacitor is charged to a specific voltage level, the short circuit is detected, the $\overline{ERR}$ signals are set and the MOSFETs switched off. The SCD charge and discharge ratio is defined as (Y-X)/X.

This ratio defines down to which duty cycle the short circuit can be detected.

It has to be considered that the high side and the low side output of one phase are working with the same capacitor, defining the maximum switching time, which is allowed without short circuit detection. This maximum allowed switching time in normal operation is defined by $d_{noSCD}/2*f_{PWM}$.

This behavior is specified as “maximum duty cycle for no short circuit detection” and “minimum duty cycle for periodic short circuit detection”

5.2.2 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs are not "on" at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7185-1E is fixed to a minimum value if the DT pin is connected to GND. This function assures a minimum dead time if the input signals coming from the µC are faulty.

The dead time can be increased beyond the internal fixed dead time by connecting the DT pin via a dead time resistor R_{DT} to GND - the larger the dead time resistor the larger the dead time (for details pls. see the “Dynamic Characteristic” table in the MOSFET driver section).

The exact dead time of the bridge is usually controlled by the PWM generation unit of the µC.

In addition to this dead time, the TLE7185-1E provides a locking mechanism, avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection.

If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored.

5.2.3 Shoot Through Option

The TLE7185-1E offers the possibility to switch off the Shoot Through Protection by setting the STOE pin to high and in the same time all $\overline{\text{IHX}}$ to low and all ILX to high. Only if all 7 conditions are fulfilled in the same time, the Shoot Through Protection and the Short Circuit Detection is deactivated and allows to switch on all 6 external MOSFETs.

If STOE is set to high, an error signal is set.

5.2.4 Under Voltage Lock Out on Vs

The TLE7185-1E has an integrated under voltage lock out, to assure that the behavior of the device is predictable in all supply voltage ranges.

If the supply voltage at VS reaches the under voltage lock out level for a minimum specified filter time, the gate-source voltage of all external MOSFETs will be actively pulled to low. In this situation the short circuit detection of this output stage is deactivated to avoid a latching shut down of the driver. Furthermore, the charge pump will be deactivated.

As soon as the supply voltage recovers, the output stage condition will be aligned to the input patterns automatically. This allows to continue operation of the motor in case of under voltage shut down without a reset by the µC.

5.2.5 Under Voltage warning on CB

In addition to the under voltage lockout, the TLE7185-1E provides an integrated under voltage warning.

The purpose of this warning is to inform the user about possible low gate voltages.

If the voltage of a charge pump buffer capacitor CB reaches the under voltage warning level for a minimum specified filter time, an Errors signal is set.

As soon as the charge pump buffer voltage recovers, the Error signal will be removed automatically.

5.2.6 Over Voltage Warning on Vs and / or VDH

The TLE7185-1E has an integrated over voltage warning to avoid destruction of the IC at high supply voltages. The voltage is observed at the VS and the VDH pin. When one of them or all of them exceed the over voltage warning level for more than the specified filter time an Error signal is set. It is in the responsibility of the user to react to this signal to avoid damage of the driver by exceeding the max ratings. The Errors signal is self clearing.

The basic driver functions will work even above this over voltage warning level as long as no maximum rating is violated. At such high voltages, the specified values will not be guaranteed.

5.2.7 Over Temperature Warning

If the junction temperature is exceeding the over temperature level an error signal is given as warning. The driver IC will continue to operate in order not to disturb the application.

The warning is removed automatically when the junction temperature is cooling down.

It is in the responsibility of the user to protect the device against over temperature destruction.

5.2.8 $\overline{\text{ERR}}$ Pins

The TLE7185-1E has two status pins to provide diagnostic feedback to the µC. The outputs of these pins are open drain outputs with integrated pull up resistors to the internal 5V supply (see **Figure 4**). The outputs are either high or low.

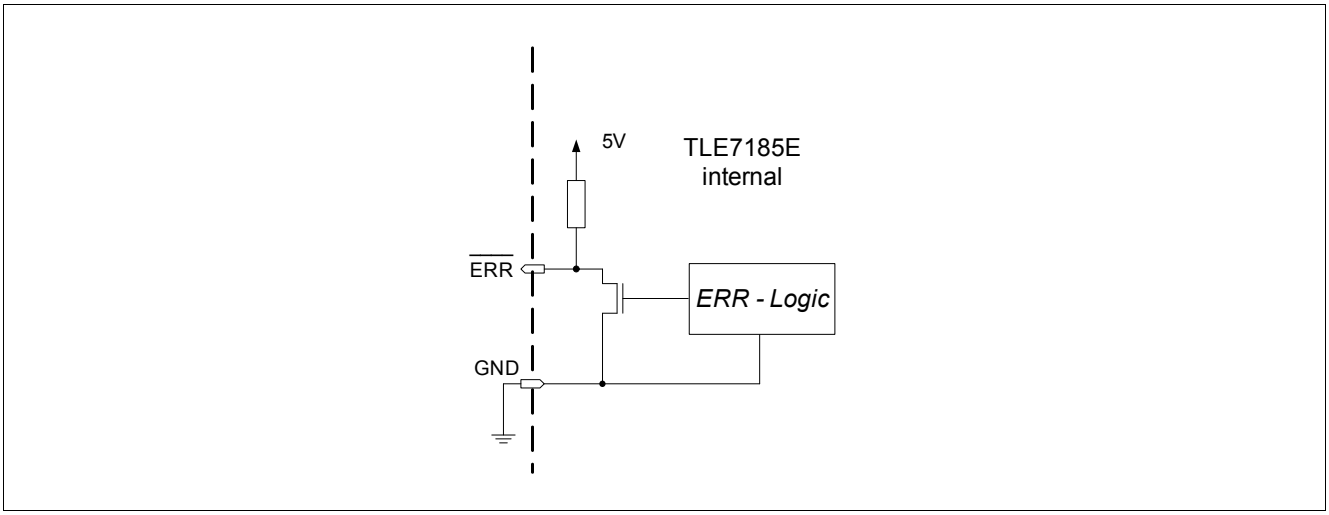


Figure 4 Structure of ERR output

Table 2 Overview of error conditions

$\overline{\text{ERR1}}$	$\overline{\text{ERR2}}$	Driver conditions	Driver action	Restart
High	High	no errors	Fully functional	–
High	Low	Over temperature	Warning only	Self clearing
Low	High	Over voltage VS/VDH or under voltage CB	Warning only	Self clearing
Low	High	Under voltage lockout based on Vs	Deactivation of driver output and charge pump	Self clearing
Low	Low	STOE pin High	Warning only	Self clearing
Low	Low	SCDL open pin	Warning only; SCD deactivated;	Self clearing
Low	Low	Short circuit detection	All MOSFETs actively switched off	Reset at ENA needed

Reset of ERROR Registers and Disable

The TLE7185-1E can be reseted by the enable pin ENA. If the ENA pin is pulled to low for a specified minimum time, the error registers are cleared. During reset (ENA = low) the driver outputs are disabled and the external MOSFETs are switched off actively. Furthermore, the Short Circuit Detection SCD is deactivated as long as ENA = low.

During disable (ENA = low) any error is shown. However, the Short circuit detection error is reset (error is cleared) and can not reoccur as the output stages which drive the external MOSFETs are disabled.

In case of under voltage lockout, the $\overline{\text{ERR}}$ pins deviate from the table above as the charge pump is not active and the TLE7185E is not biased properly.

5.2.9 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 5.5 to 32V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
ERR pins							
5.2.1	$\overline{\text{ERRx}}$ output (open drain)	V_{ERR}	–	–	0.6	V	I=100µA
5.2.2	Fall time $\overline{\text{ERRx}}$ (80 - 20 %)	$t_{f(ERR)}$	–	–	1	µs	C_{LOAD}=100pF; V_S=7V; R_{Load}=100kΩ
5.2.3	Internal pull up resistor $\overline{\text{ERRx}}$	$R_{f(ERR)}$	15	22	35	kΩ	pulled to 5V
Over temperature							
5.2.4	Over temperature warning	$T_{j(OW)}$	160	170	180	°C	–
5.2.5	Hysteresis for over temperature warning	$dT_{j(OW)}$	10	–	20	°C	–
Short circuit protection							
5.2.6	Short circuit protection detection level	V_{SCP}	0.3	–	2	V	programmed by SCDL pin
5.2.7	Short circuit protection detection Accuracy	A_{SCP}	-30	–	+30	%	0.3V≤V_{SCDL}<1.2V
5.2.8	Short circuit protection detection Accuracy	A_{SCP}	-10	–	+10	%	1.2V≤V_{SCDL}≤2.0V
5.2.9	Filter time of short circuit protection	$t_{SCP(off)}$	5	–	12	µs	–
5.2.10	Maximum duty cycle for no periodic short circuit detection	d_{noSCD}	–	–	12	%	static short circuit applied; only one input switched ($\overline{\text{IHx}}$ or ILx), f_{PWM}=40kHz
5.2.11	Minimum duty cycle for periodic short circuit detection	d_{pSCD}	28	–	–	%	
5.2.12	Internal pull up resistor SCDL	R_{SCDL}	80	140	200	kΩ	pulled to 5V
5.2.13	SCDL open pin detection level	V_{SCPOP}	2.0	–	2.5	V	–
5.2.14	Filter time of SCDL open pin	t_{SCPOP}	1	–	3	µs	–
5.2.15	SCDL open pin detection level hysteresis	V_{SCOPH}		0.3		V	–
Over- and under voltage							
5.2.16	Over voltage warning at Vs and/or VDH	V_{OV}	32	–	35	V	V_s and/or V_{VDH} increasing
5.2.17	Over voltage warning filter time	t_{OV}	10	–	25	µs	–
5.2.18	Over voltage warning hysteresis	V_{H_OV}	2	–	4	V	–
5.2.19	Under voltage lockout at Vs	V_{UVLO}	–	–	5.5	V	V_s decreasing
5.2.20	Under voltage lockout filter time	t_{UVLO}	1	–	4	µs	–
5.2.21	Under voltage lockout hysteresis	V_{UVLOH}	–	0.25	–	V	–
5.2.22	Under voltage warning at CB	V_{UV}	9.5	–	10.5	V	V_{CB} decreasing
5.2.23	Under voltage warning filter time	t_{UV}	10	–	20	µs	–
5.2.24	Under voltage warning hysteresis	V_{UVH}	–	0.25	–	V	–

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 5.5 to 32V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Reset and Enable							
5.2.25	Reset time to clear $\overline{\text{ERR}}$ registers	t_{Res1}	3.0	–	–	µs	–
5.2.26	Low time of ENA signal without reset	t_{Res0}	–	–	0.5	µs	–
5.2.27	ENA propagation time	$t_{PENA\_H\text{-}L}$	–	–	1.5	µs	high to low
5.2.28	Return time to normal operation at auto-restart	t_{AR}	–	–	1.0	µs	–

6 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as electro-hydraulic or electric power steering. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

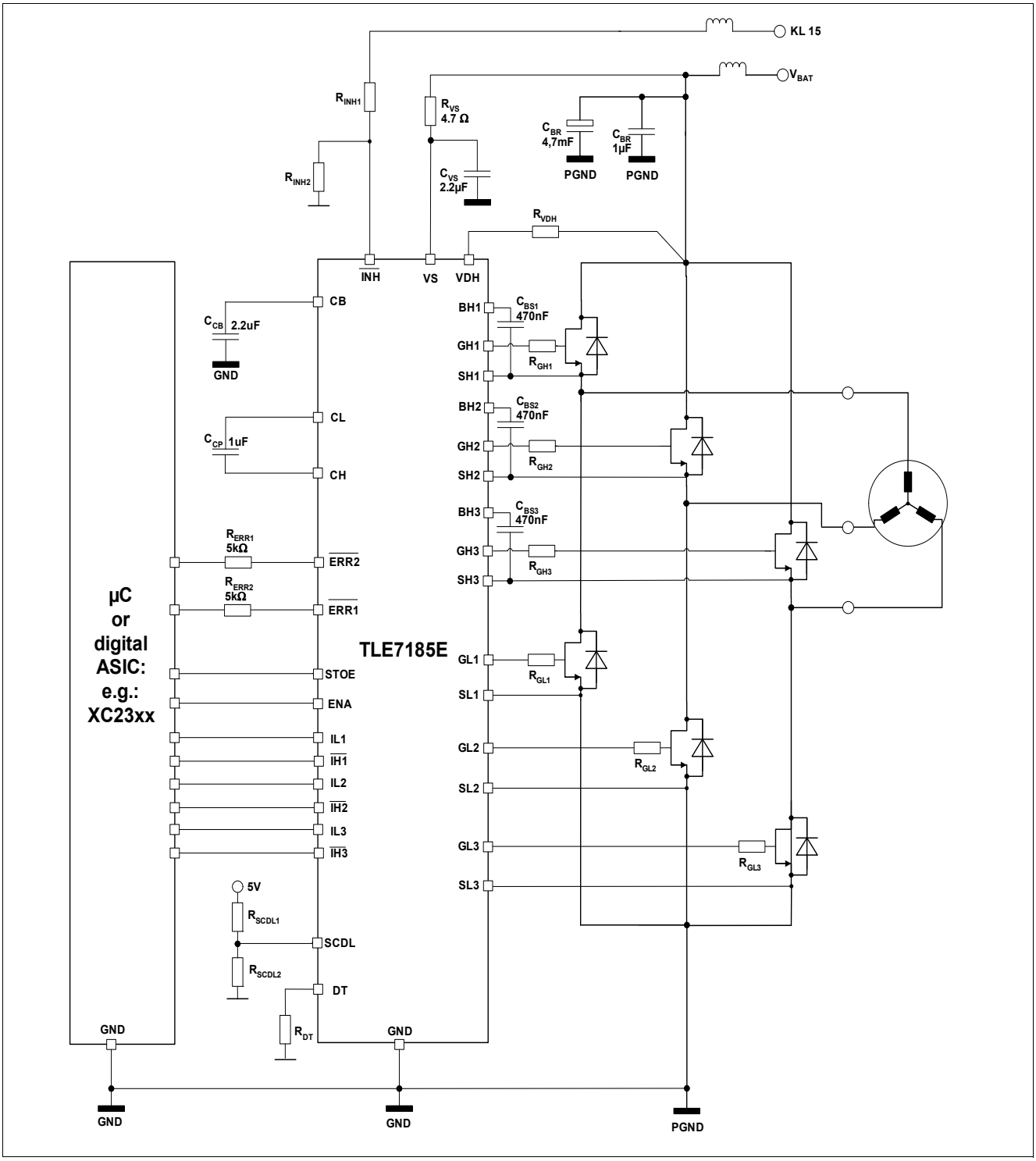


Figure 5 Application Circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

7 Package Outlines

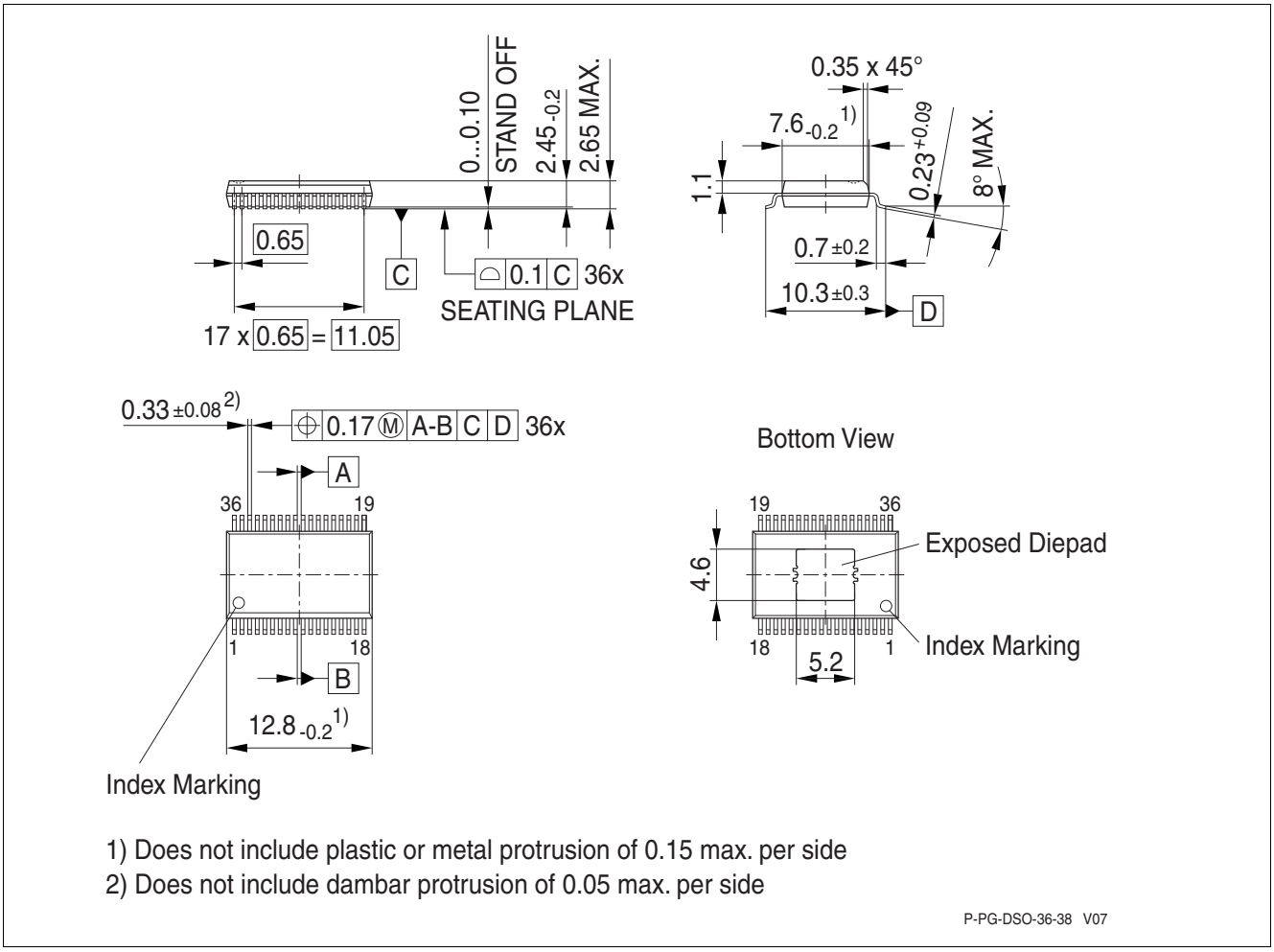


Figure 6 PG-DSO-36-38

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

8 Revision History

Version	Date	Changes
Rev. 2.4	2010-07-16	Change of Name and Marking
Rev. 2.3	2009-08-18	Parameter **Chapter 5.1.8** High level input voltage $\overline{\text{INH}}$ minimum value to 2.5V
Rev. 2.2	2009-01-13	chapter 7: package outline updated (Stand-off reduced)
Rev. 2.1	2008-10-08	parameter 5.1.20 R_{SHSL} deleted

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