REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Superseded drawing with 5962-38294.	1990 OCT 29	M.A. Frye

This drawing 5962-89691, is superseded by drawing 5962-38294 as of 29 OCT 1990. Specific part substitution information is included in 5962-38294.

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	A																							
	SHEET	1																							

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

PREPARED BY: Kenneth Rico

CHECKED BY: Charles Reysing

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 14 NOVEMBER 1989

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL CMOS, 8K x 8 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89691

SHEET 1 OF 1

DESC FORM 193
SEP 87

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REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

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SIZE	CAGE CODE	5962-89691
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SHEET 1 OF 21

DESC FORM 193
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5962-E1401

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89691	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	(See 6.6)	8K X 8 CMOS SRAM (low power)	25 ns
02	(See 6.6)	8K X 8 CMOS SRAM	25 ns
04	(See 6.6)	8K X 8 CMOS SRAM	20 ns
06	(See 6.6)	8K X 8 CMOS SRAM	15 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x 0.610" x 0.232"), dual-in-line package
Y	C-12 (32-terminal, 0.560" x 0.458" x 0.120"), rectangular chip carrier package
Z	See figure 1, (28-pin, 1.490" x 0.310", x 0.200"), dual-in-line package
U,N	C-11A (28-terminal, 0.560" x 0.358" x 0.075"), rectangular chip carrier package
T	F-11 (28-lead, 0.740" x 0.380" x 0.090"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc 1/
Input voltage	-0.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X, Y, U, N, and T	See MIL-M-38510, appendix C
Case Z	12°C/Watt
Junction temperature (T_J)	+150°C 2/

1/ All voltages referenced to V_{SS} unless otherwise specified.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage (V_{IH})	2.2 V dc to V_{CC} +0.5 V dc
Input low voltage (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	$I_O = -4.0$ mA, $V_{IL} = 0.8$ V $V_{CC} = 4.5$ V, $V_{IH} = 2.2$ V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	$I_O = 8.0$ mA, $V_{IL} = 0.8$ V $V_{CC} = 4.5$ V, $V_{IH} = 2.2$ V	1, 2, 3	All		0.4	V
High impedance output leakage current	I_{OZ}	$\overline{OE} = 2.4$ V $V_{CC} = 5.5$ V $V_O =$ GND and V_{CC}	1, 2, 3	02,04, 06	-10.0	10.0	µA
				01	-5.0	5.0	
Input leakage current	I_{IH}	$V_{IN} = 5.5$ V $V_{CC} = 5.5$ V	1, 2, 3	02,04, 06		10.0	µA
				01		5.0	
	I_{IL}	$V_{IN} =$ GND $V_{CC} = 5.5$ V	1, 2, 3	02,04 06	-10.0		µA
				01	-5.0		
Operating supply current	I_{CC1}	$V_{CC} = 5.5$ V, $\overline{CE} = 0.8$ V $CE_2 = 2.4$ V, $\overline{OE} = 2.4$ V $f = 1/t_{AVQV}$	1, 2, 3	01		110	mA
				02,04, 06		135 150	
Standby supply current (TTL)	I_{CC2}	$V_{CC} = 5.5$ V, $\overline{CE1} = 2.4$ V $CE2 = 0.8$ V, $f = 0$ Hz $\overline{OE} = 2.4$ V	1, 2, 3	01		20	mA
				02,04, 06		40	
Standby supply current (CMOS)	I_{CC3}	$V_{CC} = 5.5$ V, $\overline{CE1} = V_{CC} - 0.3$ V or CE2 = GND +0.3 V $f = 0$ Hz	1, 2, 3	01		10	mA
				02,04 06		20	
Data retention supply current	I_{CC4}	$V_{CC} = 2.0$ V, $\overline{CE1} \ge V_{CC} - 0.2$ V $CE2 \le 0.2$ V Applies only to devices with data retention.	1, 2, 3	01		300	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input capacitance 2/ 3/	C_{IN}	f = 1 MHz, V_{IN} = 0 V, T_A = +25°C, See 4.3.1c	4	All		10	pF
Output capacitance 2/ 3/	C_{OUT}	f = 1 MHz, V_{OUT} = 0 V, T_A = +25°C, See 4.3.1c	4	All		12	pF
Functional tests		See 4.3.1d	7, 8	All			
Read/write cycle time	t_{AVAV}	4/ 5/	9, 10,11	01	25		ns
				02	25		
				04	20		
				06	15		
Address access time	t_{AVQV}		9, 10, 11	01		25	ns
				02		25	
				04		20	
				06		15	
Output hold from address change	t_{AVQX}		9, 10, 11	All	0		ns
Output enable to output active 3/ 6/	t_{OLQX}		9, 10, 11	01, 02, 04, 06	0		ns
Output enable to output valid	t_{OLQV}		9, 10, 11	01		15	ns
				02		15	
				04		15	
				06		12	
Chip enable access time	t_{ELQV}		9, 10, 11	01		25	ns
				02		25	
				04		20	
				06		15	
Chip disable to output disable 3/ 6/	t_{EHQZ}		9, 10, 11	01		15	ns
				02		15	
				04		15	
				06		10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4/ 5/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write recovery time	t_{WHAV}		9, 10, 11	All	0		ns
Chip enable to end-of-write	t_{ELWH}		9, 10, 11	01	20		ns
				02	20		
				04	15		
				06	13		
Chip enable to output active 3/ 6/	t_{ELQX}		9, 10, 11	01, 02, 04, 06	3		ns
End-of-write to data active 3/ 6/	t_{WHQX}		9, 10, 11	01, 02, 04, 06	0		ns
Chip enable to data retention 3/	t_{CDR}	Applies only to devices with data retention	9, 10, 11	01	0		ns
Recovery from data retention mode 3/	t_R	Applies only to devices with data retention	9, 10, 11	01	25		ns
Address valid to end-of-write	t_{AVWH}		9, 10, 11	01	20		ns
				02	20		
				04	15		
				06	15		
Address valid to write enable	t_{AVWL}		9, 10, 11	All	0		ns
Output disable to output inactive 3/	t_{OHQZ}		9, 10, 11	01		15	ns
				02		15	
				04		15	
				06		10	
Write enable pulse width	t_{WLWH}		9, 10, 11	01	20		ns
				02	20		
				04	15		
				06	13		
Data set-up to end-of-write	t_{DVWH}		9, 10, 11	01	15		ns
				02	15		
				04	12		
				06	10		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4/ 5/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Data hold after end-of-write	t_{WHDX}		9, 10, 11	All	0		ns
Address valid to chip enable	t_{AVEL}		9, 10, 11	All	0		ns

1/ All voltages referenced to ground. Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 50 ns pulse width.
2/ Effective capacitance calculated from $C = \Delta Q/\Delta V$ = 3 volts and V_{CC} = 5.0 V, or measured with capacitance meter.
3/ Tested initially and after any design or process changes which could affect these parameters, and therefore shall be guaranteed to the limits specified in table I.
4/ For timing waveforms, see figure 4.
5/ AC measurements assume transition time $\le$ 5 ns, input levels are from ground to 3.0 V, and output load $C_L > 30$ pF and 1 /TTL gate except as noted on figure 5. Timing reference levels are 1.5 V.
6/ This parameter measured ±500 mV from steady-state.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B,9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**,7***, (8A,8B)***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c.
*** See 4.3.1d.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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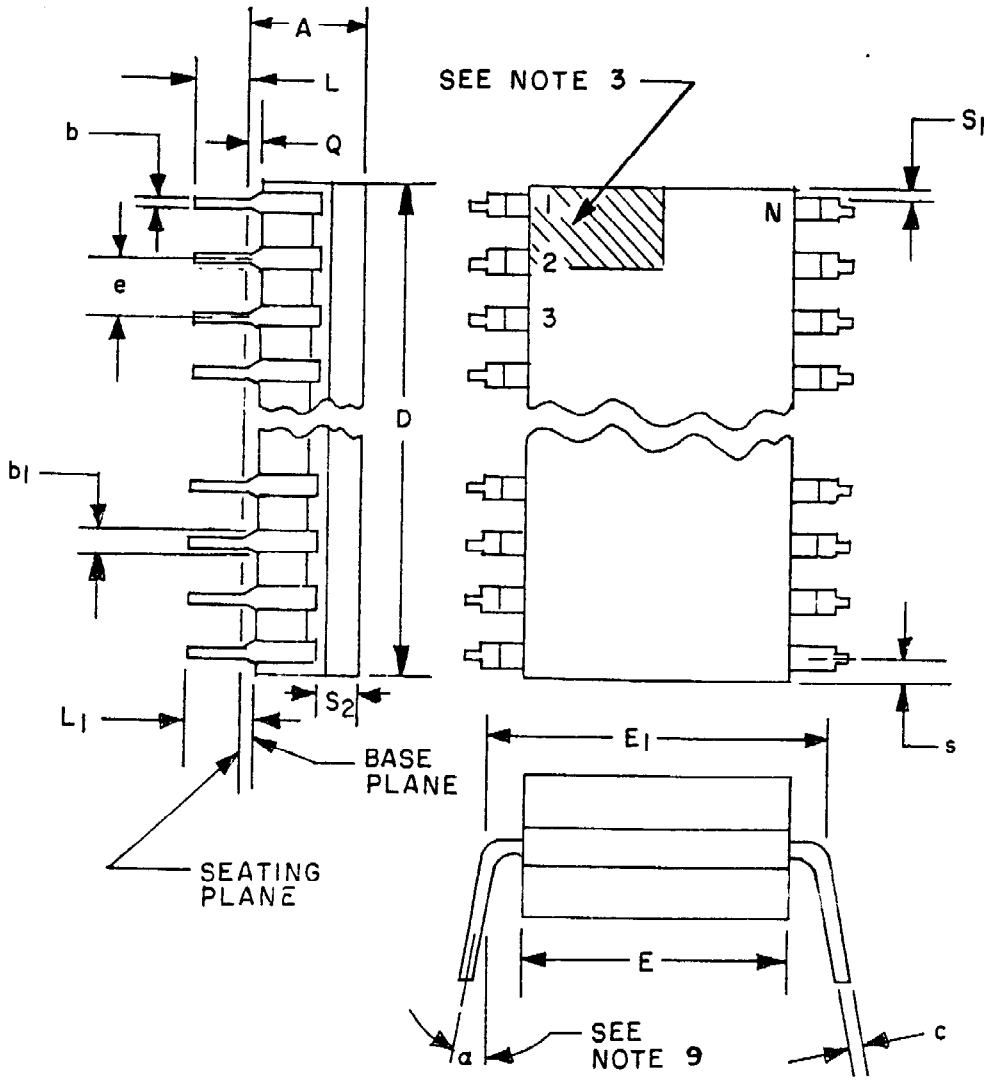

FIGURE 1. Case Z (28-pin, 1.490" x 0.310" x 0.200"), dual-in-line package.

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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.200	---	5.08	
b	.014	.023	0.36	0.58	10
b_1	.030	.070	0.76	1.78	4, 10
c	.008	.015	0.20	0.38	10
D	---	1.490	---	37.89	6
E	.220	.310	5.59	7.87	6
E_1	.290	.320	7.37	8.13	9

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
e	.100 BSC		2.54 BSC		7, 11
L	.125	.200	3.18	5.08	
L_1	.150	---	3.81	---	
Q	.015	.060	0.38	1.52	5
S	---	.100	---	2.54	8
S_1	.005	---	0.13	---	8
S_2	.005	---	0.13	---	13
α	0°	15°	0°	15°	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
4. The minimum limit for dimension b_1 may be .023 (0.58 mm) for leads number 1, 14, 15, and 28 only.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. This dimension allows for off-center lid, meniscus and glass overrun.
7. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 28.
8. Applies to all four corners (leads number 1, 14, 15, and 28) shall apply.
9. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
10. All leads - Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
11. Twenty-six spaces.
12. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
13. Not applicable for configuration 1.
14. Configurations 1 and 3 may be used (see MIL-M-38510 appendix C for dual-in-line packages, for configuration styles).

FIGURE 1. Case Z (28-pin, 1.490" x 0.310" x 0.200"), dual-in-line package - Continued.

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Device types	01, 02, 04, and 06		
Case outlines	X, Z, T, and N	U	Y
Terminal number	Terminal symbol		
1	NC	A_4	NC
2	A_{12}	A_5	NC
3	A_7	A_6	A_{12}
4	A_6	NC	A_7
5	A_5	A_7	A_6
6	A_4	A_8	A_5
7	A_3	A_9	A_4
8	A_2	A_{10}	A_3
9	A_1	A_{11}	A_2
10	A_0	A_{12}	A_1
11	I/O	I/O	A_0
12	I/O	I/O	NC
13	I/O	I/O	I/O
14	V_{SS}	V_{SS}	I/O
15	I/O	I/O	I/O
16	I/O	I/O	V_{SS}
17	I/O	I/O	NC
18	I/O	I/O	I/O
19	I/O	I/O	I/O
20	$\overline{CE}_1$	$\overline{CE}_1$	I/O
21	A_{10}	A_0	I/O
22	$\overline{OE}$	$\overline{OE}$	I/O
23	A_{11}	A_1	CE_1
24	A_9	A_2	A_{10}
25	A_8	A_3	$\overline{OE}$
26	CE_2	CE_2	NC
27	$\overline{WE}$	$\overline{WE}$	A_{11}
28	V_{CC}	V_{CC}	A_9
29	---	---	A_8
30	---	---	CE_2
31	---	---	$\overline{WE}$
32	---	---	V_{CC}

FIGURE 2. Terminal connections.

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MODE	$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	DQ
STANDBY	H	X	X	X	HIGH Z
STANDBY	X	L	X	X	HIGH Z
READ	L	H	H	L	D OUT
READ	L	H	H	H	HIGH Z
WRITE	L	H	L	X	D IN

H = logic "1" state, L = logic "0" state.
X = logic "don't care state, and Z = high impedance state.

FIGURE 3. Truth table.

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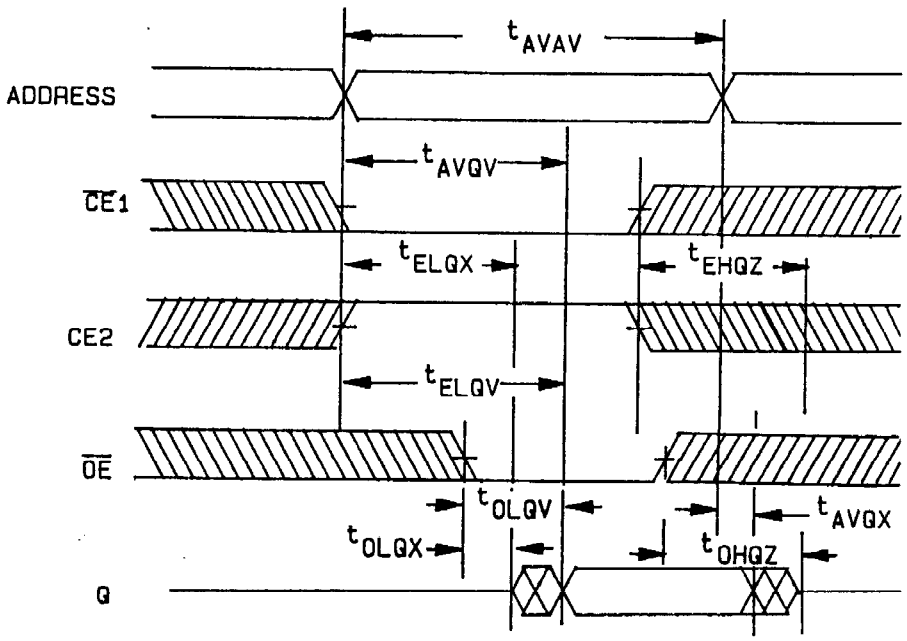
Read Cycle



NOTES:
1. $\overline{WE}$ is held high during the read cycle.
2. Timing measurement reference level is 1.5 V.

FIGURE 4. Timing waveform diagram.

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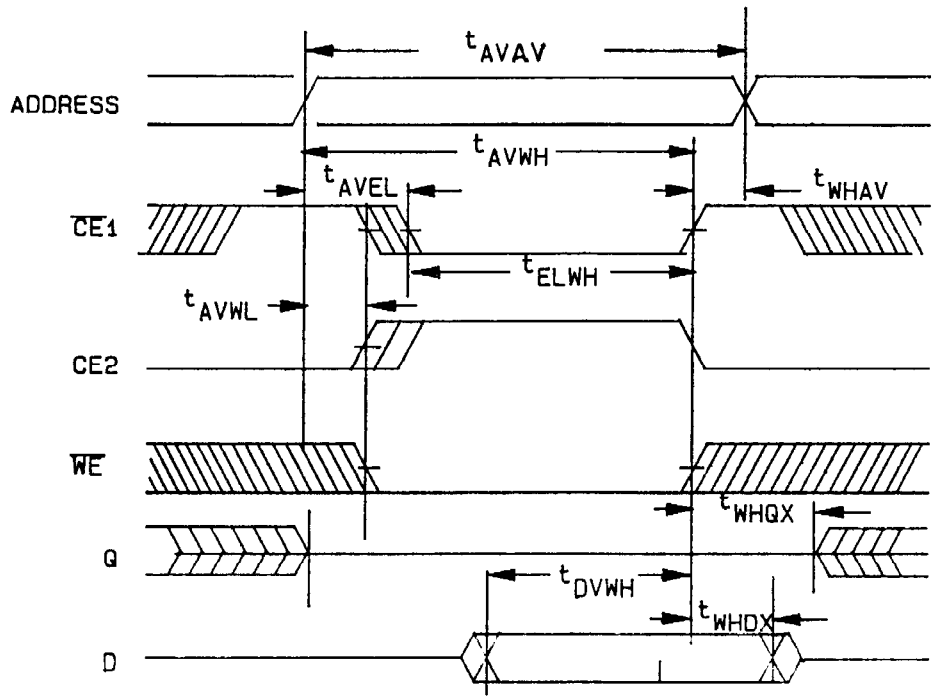
Write cycle 1

($\overline{CE1}$ or CE2 controlled)



NOTES:
1. Either $\overline{CE1}$ or CE2 may be used to control the write cycle. If $\overline{CE1}$ is used, CE2 should be high when $\overline{WE}$ is low. If CE2 is used, $\overline{CE1}$ should be low when $\overline{WE}$ is low.
2. In a $\overline{CE1}$ or CE2 controlled write cycle, the outputs assume a high impedance state, whether $\overline{OE}$ is high or low.
3. Timing measurement reference is 1.5 V.

FIGURE 4. Timing waveform diagram - Continued.

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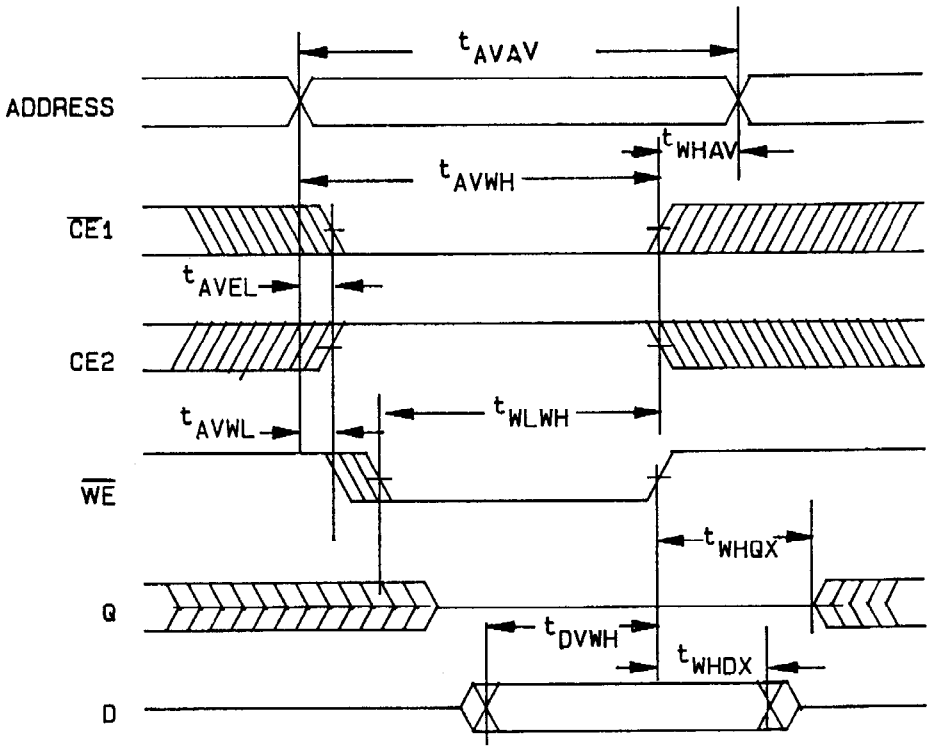
Write cycle 2
($\overline{WE}$ controlled)



NOTES:
1. In the $\overline{WE}$ controlled write cycle, while $\overline{WE}$ is low, it will force the the outputs into a high impedance state, whether $\overline{OE}$ is high or low.
2. Timing measurement reference level is 1.5 V.

FIGURE 4. Timing waveform diagram - Continued.

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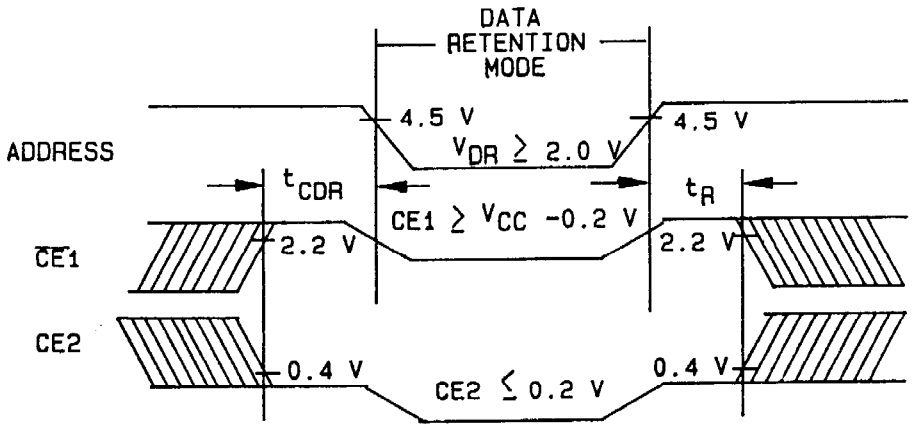
Data retention cycle



NOTE: Either $\overline{CE1}$ or CE2 may be used to begin data retention mode.

FIGURE 4. Timing waveform diagram - Continued.

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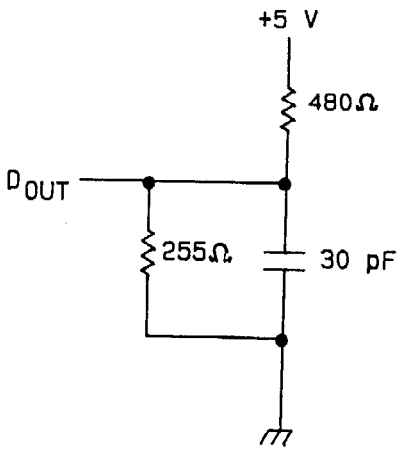
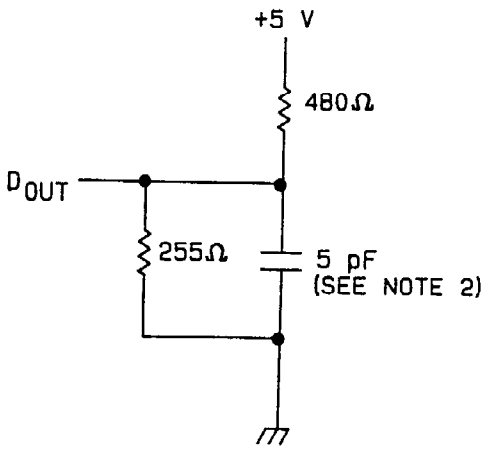


A OUTPUT LOAD



B OUTPUT LOAD

FOR t_{OLQX}, t_{EHQZ}, t_{ELQX}, t_{OHQZ}, AND t_{WHQX}

NOTE:
1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.

FIGURE 5. Output load circuits.

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4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input or output capacitance. Sample size is fifteen devices, all input and output terminals tested and no failures.

d. Subgroups 7 and 8 tests sufficient to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

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6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8969101XX	75569	P4C164L-25DWMB
5962-8969101ZX	75569	P4C164L-25CMB
5962-8969101UX	75569	P4C164L-25LMB
5962-8969101TX	75569	P4C164L-25FMB
5962-8969102XX	75569 6Y440 65786 34649	P4C164-25DWMB MT5C6408CW-25 883C CY7C186-25DMB MC5104-25/B
5962-8969102YX	6Y440	MT5C6408ECW-25 883C
5962-8969102ZX	75569 6Y440 65786	P4C164-25CMB MT5C6408C-25 883C CY7C185-25DMB
5962-8969102UX	65786 75569	CY7C186-LMB P4C164-25LMB
5962-8969102NX	6Y440	MT5C6408EC-25 883C

See footnote at end of table.

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Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8969102TX	65786 75569	CY7C186-25KMB P4C164-25FMB
5962-8969104XX	6Y440 65786 75569	MT5C6408CH-20 883C CY7C186-20DMB P4C164-20DWMB
5962-8969104YX	6Y440	MT5C6408ECW-20 883C
5962-8969104ZX	75569 6Y440 65786	P4C164-20CMB MT5C6408C-20 883C CY7C185-20DMB
5962-8969104UX	65786 75569	CY7C186-20LMB P4C164-20LMB
5962-8969104NX	6Y440	MT5C6408EC-20 883C
5962-8969104TX	75569	P4C164-20FMB
5962-8969106XX	6Y440 65786	MT5C6408CH-15 883C CY7C186-15DMB
5962-8969106YX	6Y440	MT5C6408ECW-15883C
5962-8969106ZX	6Y440 65786	MT5C6408C-15 883C CY7C185-15DMB
5962-8969106UX	65786	CY7C186-15LMB
5962-8969106NX	6Y440	MT5C6408EC-15 883C
5962-8969106TX	65786	CY7C186-15KMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

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Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 N. First Street San Jose, CA 95134
6Y440	Micron Technology 2805 E Columbia Road Boise, ID 83706
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051
75569	Performance Semiconductor Corporated 610 East Weddell Drive Sunnyvale, CA 94089

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