mXT336UD-MAUHA1 1.0

maXTouch 336-node Touchscreen Controller

Functional Safety

- IEC/UL 60730 Class B support
- Self diagnostics at power-on and as periodic tests during operation
- Heartbeat (alive) signal output to host

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 14 X (transmit) lines and 24 Y (receive) lines for use by a touchscreen (see Section 3.2.1 “Permitted Configurations”)
- A maximum of 336 nodes can be allocated to the touch sensor
- Touchscreen size of 7.11 inches (16:9 aspect ratio), assuming a sensor electrode pitch of 6.5 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 10 concurrent touches tracked in real time

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, IPS and OLED
- Synchronization with display refresh timing capability
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- 10 mm glass (or 5 mm PMMA) with bare finger (dependent on screen size, touch size, configuration and stack-up)
- 6 mm glass (or 3 mm PMMA) with multi-finger 5 mm glove (2.7 mm PMMA equivalent) (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- P2P mutual capacitance measurements supported for extra sensitive multi-touch sensing
- Noise suppression technology to combat ambient, charger, and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Burst Frequency
  - Controlled Tx burst frequency drift over process and temperature range
- Scan Speed
  - Configurable to allow for power and speed optimization
- Touch panel failure detection
  - Automatic touch sensor diagnostics during run time to support the implementation of safety critical features
  - Diagnostics reported using dedicated output pin or by standard Object Protocol messages
  - Configurable test limits

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- I^2C slave with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz)

- Interrupt to indicate when a message is available
- Additional SPI Debug Interface to read the raw data for tuning and debugging purposes

Power Supply

- Digital (Vdd) 3.3V nominal
- Digital I/O (VddIO) 3.3V nominal
- Analog (AVdd) 3.3V nominal
- High voltage internal X line drive (XVdd) 6.6 V with internal voltage pump (XVdd connected to Vdd if voltage pump not used)

Package

- 56-pin XQFN 6 × 6 × 0.4 mm, 0.35 mm pitch

Operating Temperature

- –40°C to +85°C

Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

PIN CONFIGURATION

Pin Configuration – 56-pin XQFN

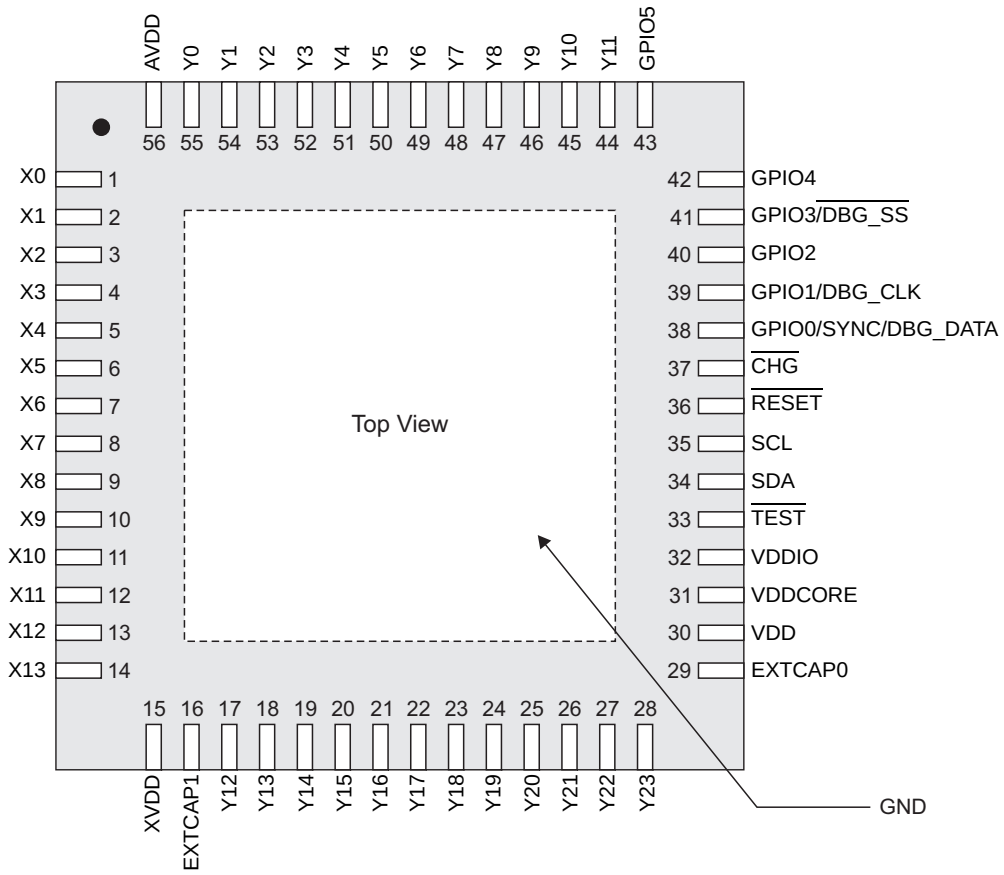


TABLE 1: PIN LISTING – 56-PIN XQFN

Pin	Name	Type	Supply	Description	If Unused...
1	X0	S	XVdd	X line connection	Leave open
2	X1	S	XVdd	X line connection	Leave open
3	X2	S	XVdd	X line connection	Leave open
4	X3	S	XVdd	X line connection	Leave open
5	X4	S	XVdd	X line connection	Leave open
6	X5	S	XVdd	X line connection	Leave open
7	X6	S	XVdd	X line connection	Leave open
8	X7	S	XVdd	X line connection	Leave open
9	X8	S	XVdd	X line connection	Leave open
10	X9	S	XVdd	X line connection	Leave open
11	X10	S	XVdd	X line connection	Leave open
12	X11	S	XVdd	X line connection	Leave open
13	X12	S	XVdd	X line connection	Leave open
14	X13	S	XVdd	X line connection	Leave open
15	XVDD	P	–	X line drive power	–
16	EXTCAP1	P	–	Voltage doubler – connect to EXTCAP0 via capacitor; see Section 2.2.5 “XVdd”	Leave open
17	Y12	S	AVdd	Y line connection	Leave open
18	Y13	S	AVdd	Y line connection	Leave open
19	Y14	S	AVdd	Y line connection	Leave open
20	Y15	S	AVdd	Y line connection	Leave open
21	Y16	S	AVdd	Y line connection	Leave open
22	Y17	S	AVdd	Y line connection	Leave open
23	Y18	S	AVdd	Y line connection	Leave open
24	Y19	S	AVdd	Y line connection	Leave open
25	Y20	S	AVdd	Y line connection	Leave open
26	Y21	S	AVdd	Y line connection	Leave open
27	Y22	S	AVdd	Y line connection	Leave open
28	Y23	S	AVdd	Y line connection	Leave open
29	EXTCAP0	P	–	Voltage doubler – connect to EXTCAP1 via capacitor; see Section 2.2.5 “XVdd”	Leave open
30	VDD	P	–	Digital power	–
31	VDDCORE	P	–	Digital core power	–
32	VDDIO	P	–	Digital IO interface power	–
33	$\overline{\text{TEST}}$	–	VddIO	Reserved for factory use; pull up to VddIO	–
34	SDA	OD	VddIO	I^2C Serial Data	–
35	SCL	OD	VddIO	I^2C Serial Clock	–
36	$\overline{\text{RESET}}$	I	VddIO	Reset low. Pull up to VddIO. Connection to host system is recommended	Pull up to VddIO
37	$\overline{\text{CHG}}$	OD	VddIO	State change interrupt. Pull up to VddIO Note: Briefly set (~100 ms) as an input after power-up/ reset for diagnostic purposes	–

TABLE 1: PIN LISTING – 56-PIN XQFN (CONTINUED)

Pin	Name	Type	Supply	Description	If Unused...
38	GPIO0	I/O	VddIO	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Connect to test point Input: Connect to GND Output: Leave open
	SYNC	I		External synchronization: (VSync or HSync)	
	DBG_DATA	O		Debug Data	
39	GPIO1	I/O	VddIO	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Connect to test point Input: Connect to GND Output: Leave open
	DBG_CLK	O		Debug Clock	
40	GPIO2	I/O	Vdd	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Input: Connect to GND Output: Leave open
41	GPIO3	I/O	Vdd	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Connect to test point Input: Connect to GND Output: Leave open
	$\overline{\text{DBG\_SS}}$	O		Debug SS line	
42	GPIO4	I/O	Vdd	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Input: Connect to GND Output: Leave open
43	GPIO5	I/O	Vdd	General purpose IO; see Section 2.2.9 "GPIO Pins" (1)	Input: Connect to GND Output: Leave open
44	Y11	S	AVdd	Y line connection	Leave open
45	Y10	S	AVdd	Y line connection	Leave open
46	Y9	S	AVdd	Y line connection	Leave open
47	Y8	S	AVdd	Y line connection	Leave open
48	Y7	S	AVdd	Y line connection	Leave open
49	Y6	S	AVdd	Y line connection	Leave open
50	Y5	S	AVdd	Y line connection	Leave open
51	Y4	S	AVdd	Y line connection	Leave open
52	Y3	S	AVdd	Y line connection	Leave open
53	Y2	S	AVdd	Y line connection	Leave open
54	Y1	S	AVdd	Y line connection	Leave open
55	Y0	S	AVdd	Y line connection	Leave open
56	AVDD	P	–	Analog power	–
Pad	GND	P	–	Exposed pad must be connected to GND	–

Note 1: Use of the GPIO pin not supported for functional safety purposes under IEC/UL 60730 Class B.

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

1.0 OVERVIEW OF MXT336UD-MAUHA1

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer applications. The mXT336UD-MAUHA1 features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT336UD-MAUHA1 uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT336UD-MAUHA1 features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT336UD-MAUHA1 allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in active mode and Self Capacitance Touch as the default in idle mode. Note that other types of scans (such as P2P mutual capacitance scans and other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has a greater resolution than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

  Self capacitance and P2P mutual capacitance measurements allow for the detection of touches in extreme scenarios, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two companion microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing and postprocessing to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT336UD-MAUHA1 provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.
- **Functional Safety** – The device is designed with functional safety applications in mind (for example, for the home appliance market). Specifically, the device complies with the IEC/UL 60730 standard for Class B safety specification:
  - Self diagnostics at power-on and Periodic testing during operation to detect faults for immediate action by the host system (see Table 1-1)
  - Heartbeat (alive) signal output to host
  - Enhanced I^2C communications for error detection and reporting

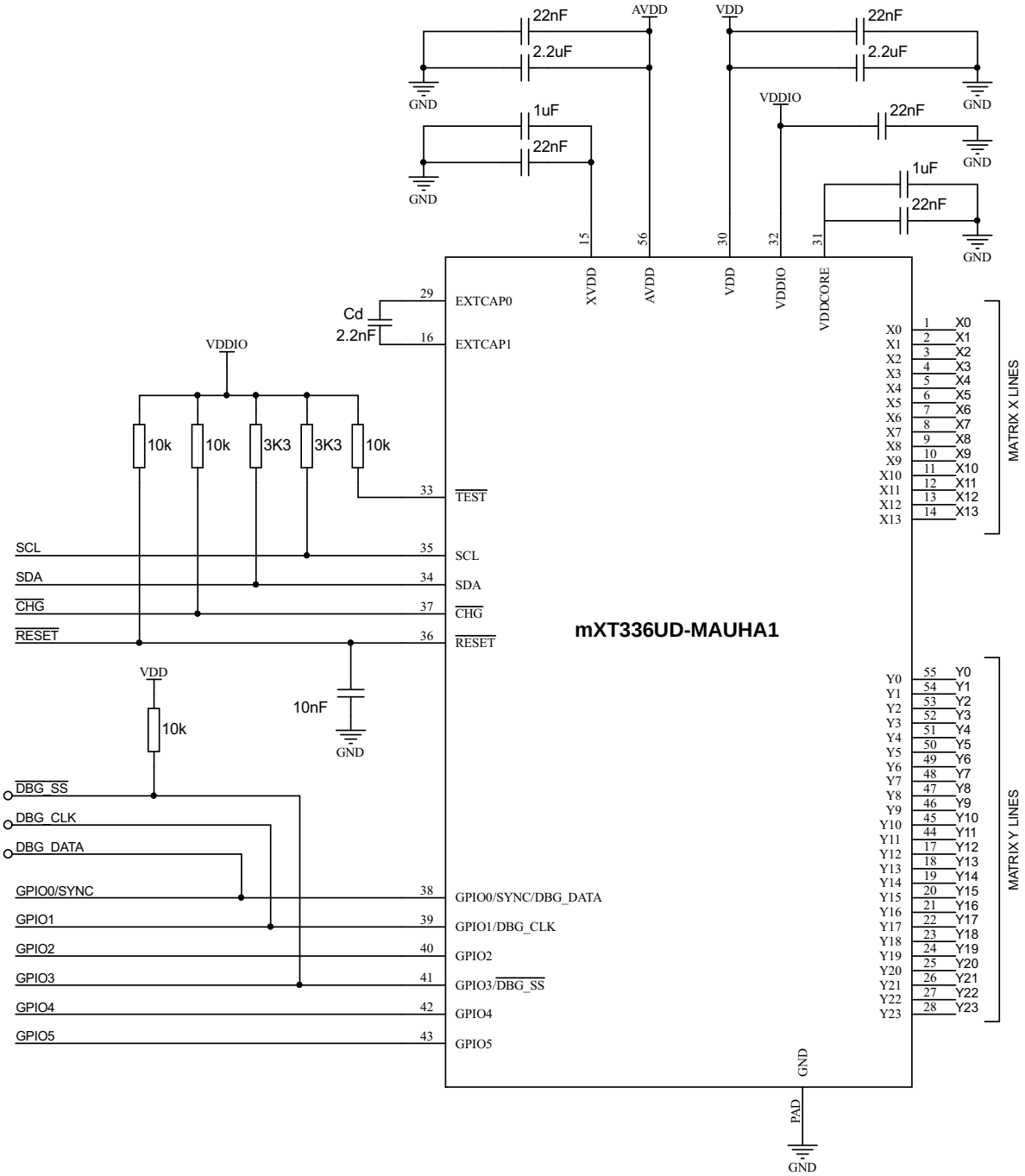
TABLE 1-1: FUNCTIONAL SAFETY TESTS

Tests	Power-on Test (POST)	Periodic Runtime Test (BIST)
CPU register tests	Yes	Yes
Missing and unexpected interrupt tests	Yes	Yes
Internal clock tests	Yes	Yes
Flash memory tests	Yes	Yes
RAM tests	Yes	Yes
Factory data	Yes	Yes
Software related tests (1)	Yes	Yes
Brown-out detection (BOD) tests	Yes	–
Analog and digital front-end tests (2)	–	Yes
Signal Limit and Pin Fault tests (2)	–	Yes

Note 1: Includes flow execution tests (specifically, all safety-related modules are executed).
2: Several tests detect both internal and external defects, including a number of touch sensor faults.

2.0 SCHEMATIC

2.1 56-pin XQFN



Notes:

1. The schematic shown assumes that the voltage doubler is used. If low voltage operation is required, capacitor Cd must be omitted (see Section 2.2.5 “XVdd")
2. See “Pin configuration” for information on I/O pin supply
3. See Section 2.2 “Schematic Notes”

2.2 Schematic Notes

2.2.1 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in Table 2-1. This information is also indicated in "Pin configuration".

TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS

Power Supply	Pins
XVdd	X sense pins
AVdd	Y sense pins
Vdd	GPIO2, GPIO3/$\overline{\text{DBG\_SS}}$, GPIO4, GPIO5
VddIO	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$, $\overline{\text{CHG}}$ SCL, SDA, GPIO0/SYNC/DBG_DATA, GPIO1/DBG_CLK

2.2.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.2.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematic are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I^2C SDA and SCL lines (shown on the schematic), as the values of these resistors depend on the speed of the I^2C interface. See Section 7.6 "I2C Specification" for details.

Note that if a VddIO supply at the low end of the allowable range is used, the I^2C pull-up resistor values may need to be reduced.

2.2.4 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.2.5 XVDD

XVdd power can be supplied either as high voltage (using an internal voltage pump) or as low voltage (connected directly to the Vdd supply). The operating mode should be chosen according to the final application.

The voltage pump requires one external capacitor:

- EXTCAP0 must be connected to EXTCAP1 via a capacitor (Cd). The capacitor must be placed as close as possible to the EXTCAP*n* pins.
- The capacitor on XVDD should be rated at least 10 V if the voltage doubler is used.

Capacitor Cd should provide a capacitance of 2.2 nF.

If low voltage XVdd is required (that is, the XVdd voltage doubler is not required):

- Capacitor Cd must be omitted and EXTCAP0 and EXTCAP1 left unconnected.
- XVDD must be connected directly to the Vdd supply.

CAUTION! The device may be permanently damaged if the XVDD supply pin is shorted to Ground or high current is drawn from it.

2.2.6 AVDD

A diode from AVDD to VDD is present in the device. If AVDD and VDD are driven from different supplies, the Vdd supply must be powered up earlier than AVdd.

2.2.7 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.2.8 SYNC PIN

The mXT336UD-MAUHA1 has a single SYNC pin that can be used for either frame synchronization or pulse synchronization, but not both.

IMPORTANT!	Use of the SYNC pin is not covered for functional safety purposes under IEC/UL 60730 Class B.

2.2.9 GPIO PINS

The mXT336UD-MAUHA1 has 6 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

IMPORTANT!	Use of the GPIO pins is not covered for functional safety purposes under IEC/UL 60730 Class B.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object.

By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor or else the internal resistor should be pulled up using the GPIO Configuration T19 object. Note that this does not apply if the GPIO pin is shared with a debug line; see Section 2.2.10 “SPI Debug Interface” for advice on how to treat an unused GPIO pin in this case.

Alternatively, the GPIO pin can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used for GPIO purposes, although any alternative function can still be used.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO0 cannot be used if the SYNC function is in use.
- The SPI Debug Interface functionality is shared with some of the GPIO pins. See Section 2.2.10 “SPI Debug Interface” for more details on the SPI Debug Interface and how to handle these pins if they are totally unused.

2.2.10 SPI DEBUG INTERFACE

IMPORTANT!	Use of the SPI Debug Interface is not covered for functional safety purposes under IEC/UL 60730 Class B.

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 6.1 “SPI Debug Interface”.

The debug lines may share pins with other functionality. If the circuit is designed to use the SPI Debug Interface, then any alternative functionality cannot be used. Specifically:

- The DBG_CLK line shares functionality with GPIO1; therefore GPIO1 cannot be used if the SPI Debug Interface is in use.
- The DBG_DATA line shares functionality with GPIO0; therefore GPIO0 cannot be used if the SPI Debug Interface is in use.
- The $\overline{\text{DBG\_SS}}$ line shares functionality with GPIO3, so GPIO3 cannot be used.
- The pull-up resistor for $\overline{\text{DBG\_SS}}$ in the schematics is optional and should be present only if the line is used as $\overline{\text{DBG\_SS}}$.

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines should not be connected to power or GND. For this reason, where these pins are shared with GPIO pins and they are totally unused (that is, they are not being used as debug or GPIO pins), they should be set as outputs using the GPIO Configuration T19 object.

3.0 SENSOR LAYOUT

NOTE	The specific electrode designs used in Microchip touchscreens may be the subject of various patents and patent applications. Further information is available on request.

IMPORTANT!	The device is currently under development. Functionality described here may be subject to change or is not yet implemented. You are advised to consult Microchip concerning any designs based on the information below

3.1 Electrodes

The device supports various configurations of touch electrodes as summarized below:

- Touchscreen: 1 touchscreen panel occupies a rectangular matrix of up to 14 X × 24 Y lines maximum (subject to other configurations).

3.2 Sensor Matrix Layout

When designing the physical layout of the touch panel, the following rules must be obeyed:

- **General layout rules:**
  - The Multiple Touch Touchscreen T100 object should be a regular rectangular shape in terms of the lines it uses.
- **Additional layout rules for Multiple Touch Touchscreen T100:**
  - The Multiple Touch Touchscreen T100 object ***must*** start at (X0, Y0).
  - For mutual capacitance measurements (see Table 3-1):

    The touchscreen must contain a minimum of 3 X lines. If Dual X Drive is enabled for use in the Noise Suppression T72 object, the minimum is 4 X lines.

    The touchscreen must contain a minimum of 3 Y lines.
  - For self capacitance measurements (see Table 3-2):

    The touchscreen must contain a minimum of 6 X lines.

    The number of Y lines must be one of 24, 23, 20, 19, 16, 15, 12, 11, 8 or 7.

3.2.1 PERMITTED CONFIGURATIONS

The permitted X/Y configurations are shown in Table 3-1 and Table 3-2.

TABLE 3-1: PERMITTED TOUCHSCREEN CONFIGURATIONS – MUTUAL CAPACITANCE SENSING

Number of X Lines \ Number of Y Lines	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
14	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
13	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
12	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
11	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
10	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
9	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
8	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
7	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
6	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
5	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
4	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
2																								
1																								

Key: Y – Configuration supported; X – Configuration supported, but only if dual X is *not* used; (blank) – Configuration not supported

TABLE 3-2: PERMITTED TOUCHSCREEN CONFIGURATIONS – SELF CAPACITANCE SENSING

Number of X Lines \ Number of Y Lines	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
14	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
13	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
12	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
11	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
10	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
9	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
8	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
7	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
6	Y	Y			Y	Y			Y	Y			Y	Y			Y	Y						
5																								
4																								
3																								
2																								
1																								

Key: Y — Configuration supported; (blank) — Configuration not supported

3.3 Screen Size

Table 3-3 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 3-3: TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)		
			4.5 mm Pitch	5.5 mm Pitch	6.5 mm Pitch
16:10	X = 14, Y = 23	322	4.77	5.83	6.89
16:9	X = 14, Y = 24	336	4.92	6.02	7.11
4:3	X = 14, Y = 20	280	4.18	5.11	6.04
2:1	X = 12, Y = 24	288	4.75	5.81	6.87

Note 1: The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio.

4.0 POWER-UP / RESET REQUIREMENTS

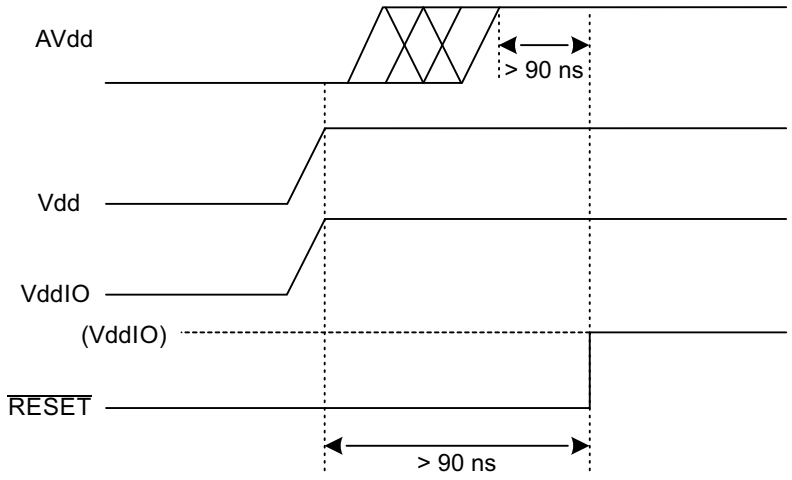
4.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in $\overline{\text{RESET}}$ (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 4-1. See Section 7.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

A diode from AVDD to VDD is present in the device. If AVDD and VDD are driven from different supplies, the Vdd supply must be powered up earlier than AVdd.

FIGURE 4-1: POWER SEQUENCING ON THE MXT336UD-MAUHA1



Note: When using external $\overline{\text{RESET}}$ at power-up, VddIO must not be enabled after Vdd

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the $\overline{\text{RESET}}$ line low.

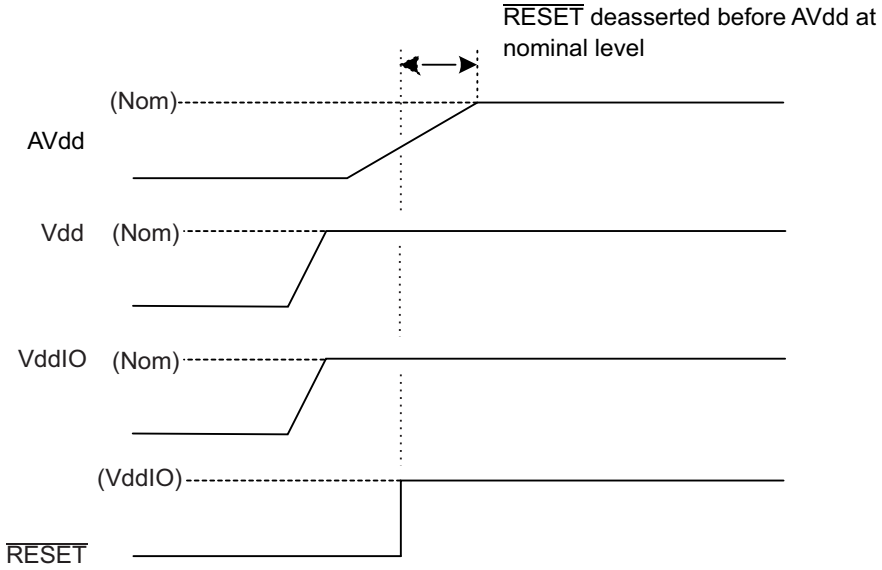
After power-up, the device typically takes TBD ms before it is ready to start communications.

NOTE	Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the $\overline{\text{RESET}}$ line is released before the AVdd supply has reached its nominal voltage (see Figure 4-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in Deep Sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

FIGURE 4-2: POWER SEQUENCING ON THE MXT336UD-MAUHA1 – LATE RISE ON AVDD



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After the host has released the RESET pin, the device typically takes TBD ms before it is ready to start communications. It is recommended to connect the RESET pin to a host controller to allow the host to initiate a full hardware reset without requiring the mXT336UD-MAUHA1 to be powered down.

WARNING	The device should be reset only by using the RESET line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up and power-down. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

NOTE	The voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes TBD ms. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The CHG line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should never be driven by the host.

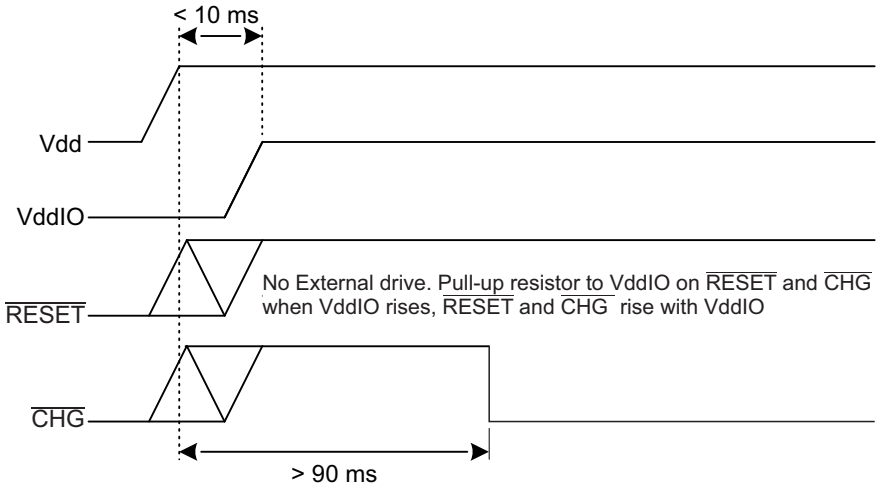
At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

4.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 4-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The RESET and CHG pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, RESET and CHG will rise with VddIO. The internal POR system ensures reliable boot up of the device and the CHG line will go low approximately TBD ms after Vdd to notify the host that the device is ready to start communication.

FIGURE 4-3: POWER-UP SEQUENCE



5.0 PCB DESIGN CONSIDERATIONS

5.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT336UD-MAUHA1. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

5.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT336UD-MAUHA1 applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

5.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION!	If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

5.3 Power Supply

5.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

5.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

5.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.2 “Schematic Notes”.

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

5.3.4 VOLTAGE PUMP

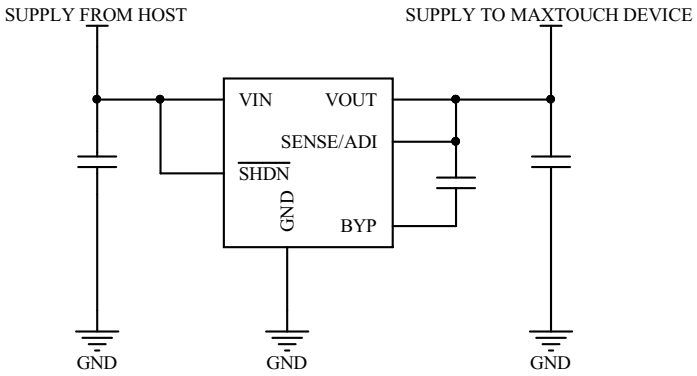
The traces for the voltage pump capacitor between EXTCAP0 and EXTCAP1 (Cd on the schematic in Section 2.0 “Schematic”) should be kept as short and as wide as possible for best pump performance. They should also be routed as parallel and as close as possible to each other in order to reduce emissions, and ideally the traces should be the same length.

5.3.5 VOLTAGE REGULATORS

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 5-1 shows an example circuit for an LDO.

FIGURE 5-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, good load regulation and step response. The voltage regulators listed in Table 5-1 have been tested and found to work well with maXTouch devices. If it is desired to use an alternative LDO, however, certain performance criteria should be verified before using the device. These are:

- Stable with high value multi-layer ceramic capacitors on the output
- Low output noise – ideally less than 100 μV_{RMS} over the range 10 Hz to 1 MHz
- Good load transient response – this should be less than 35 mV peak when a load step change of 100 mA is applied at the device output terminal
- No-load stable – Some LDOs become unstable if the output current falls below a certain minimum. If this is the case, then this minimum must be lower than the minimum current consumed by the mXT336UD-MAUHA1 (for example, in deep sleep).

TABLE 5-1: SUITABLE LDO REGULATORS

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP5504	300
Microchip Technology Inc.	MCP1725	500
Microchip Technology Inc.	MIC5514	300
Microchip Technology Inc.	MIC5323	300

Note: Some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturer's datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

5.3.6 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

5.3.7 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

5.4 Guard Track

A guard track (Ground) should be routed between the X and Y tracks, as well as between the X/Y tracks and Ground. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation.

A guard track is also needed between any self capacitance X/Y lines and mutual capacitance only X/Y lines.

5.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground. This should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- MXTAN0208 – *Design guide for PCB Layouts for maXTouch Touch Controllers*

5.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

5.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

5.7.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

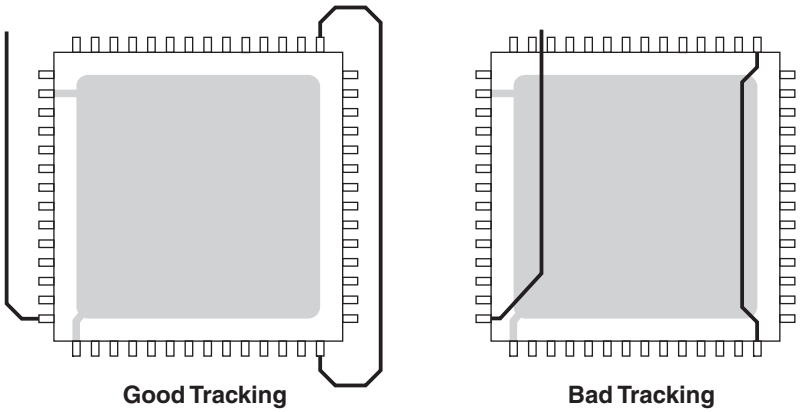
A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

5.7.2 QFN PACKAGE RESTRICTIONS

The central pad on the underside of the QFN device should be connected to ground. Do not run any tracks underneath the body of the device on the top layer of the PCB, only ground. Figure 5-2 shows examples of good and bad tracking.

FIGURE 5-2: EXAMPLES OF GOOD AND BAD TRACKING

Note: The number of pins and their functions is shown for example purposes only and may not reflect the actual number or function on the device.



5.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer’s datasheet for more information.

6.0 DEBUGGING AND TUNING

6.1 SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. These lines should be routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.2.10 “SPI Debug Interface” for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	The touch controller will take care of the pin configuration. When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used.

6.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

6.3 Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no pin short (X to Y, or X lines to power or GND) before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines could damage the device.

In addition to one-off hardware tests, the Self Test T25 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic test can be run at a user-specified interval and reports pass and/or fail messages (as determined by the device configuration). Reporting is achieved either by standard Self Test T25 object protocol messages or by a dedicated hardware GPIO pin, configured using the GPIO Configuration T19 object.

IMPORTANT!	For compliance with IEC/UL 60730 Class B safety specification, reporting should be achieved using Self Test T25 object protocol messages and not by a hardware GPIO pin.

7.0 SPECIFICATIONS

7.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
AVdd	3.6V
Maximum continuous combined pin current, all GPIO*n* pins	40 mA
Voltage forced onto any pin	–0.3 V to (Vdd, VddIO or AVdd) + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Operating temperature	–40°C to +85°C
Storage temperature	–60°C to +150°C
Vdd	3.3 V
VddIO	1.8 V to 3.3 V
AVdd	3.3 V
XVdd with internal voltage doubler	2 × Vdd
XVdd low voltage operation (without internal voltage doubler)	Connected to Vdd
Temperature slew rate	10°C/min

7.2.1 DC CHARACTERISTICS

7.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	3.0	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise

7.2.1.2 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits	1.71	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Vdd					
Operating limits	2.7	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 µs to fall

7.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits – voltage doubler enabled	–	2 × Vdd	–	V	
Operating limits – voltage doubler disabled	–	Vdd	–	V	

7.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

7.3 Timing Specifications

7.3.1 BURST FREQUENCY TOLERANCE

The burst frequency is directly correlated to the system clock. The burst frequency tolerance depends on the tolerance of the system's oscillator (see Table 7-1).

TABLE 7-1: OSCILLATOR TOLERANCE

Min Drift	Nominal	Max Drift	Notes
–5%	40 MHz (calibrated)	+5%	Minimum/Maximum drift over temperature is specified as percentage below/above nominal frequency

7.4 Touchscreen Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.Single node
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
	With Internal Voltage Pump	Maximum recommended load on each X line: (2) Cpx + (*num_Y* × Cm) < 240 pF
	With Internal Voltage Pump and Dual X	Maximum recommended load on each X line: (2) Cpx + (2 × *num_Y* × Cm) < 120 pF
Cpy	Mutual capacitance load to Y	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 130 pF on each X or Y line. (1)
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 14.8 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
ΔCpy	Self capacitance imbalance on Y	

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

2: *num_Y* = Number of active Y lines defined by Multiple Touch Touchscreen T100.

7.5 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	–	–	1	µA	
$\overline{\text{RESET}}$	Internal pull-up resistor	9	10	16	kΩ	
GPIOs	Internal pull-up/pull-down resistor					
Input (All input pins connected to the Vdd power rail)						
Vil	Low input logic level	–0.3	–	0.3 × Vdd	V	
Vih	High input logic level	0.7 × Vdd	–	Vdd	V	
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	VddIO = 1.8 V to Vdd Iol = max 0.4 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd Ioh = 0.4 mA
Output (All output pins connected to the Vdd power rail)						
Vol	Low output voltage	0	–	0.2 × Vdd	V	Iol = max 0.4 mA
Voh	High output voltage	0.8 × Vdd	–	Vdd	V	Ioh = 0.4 mA

7.6 I²C Specification

Parameter	Value
Address	0x4A
I²C specification (1)	Revision 6.0
Maximum bus speed (SCL) (2)	400 kHz
Standard Mode (3)	100 kHz
Fast Mode (3)	400 kHz

Note 1: More detailed information on I²C operation is available from www.nxp.com/documents/user_manual/UM10204.pdf.

2: In systems with heavily laden I²C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

3: The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of capacitance loading on the lines.

7.7 Thermal Packaging

7.7.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	33.7	°C/W	Still air	56-pin XQFN 6 × 6 × 0.4 mm
θ_{JC}	Junction to case thermal resistance	10.1	°C/W		56-pin XQFN 6 × 6 × 0.4 mm

7.7.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W) (see Section 7.7.1 “Thermal Data”)
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 7.7.1 “Thermal Data”)
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

7.8 ESD Information

Parameter	Value	Reference Standard
Human Body Model (HBM)	±2000 V	JEDEC JS–001
Charge Device Model (CDM)	±250 V	JEDEC JS–001

7.9 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

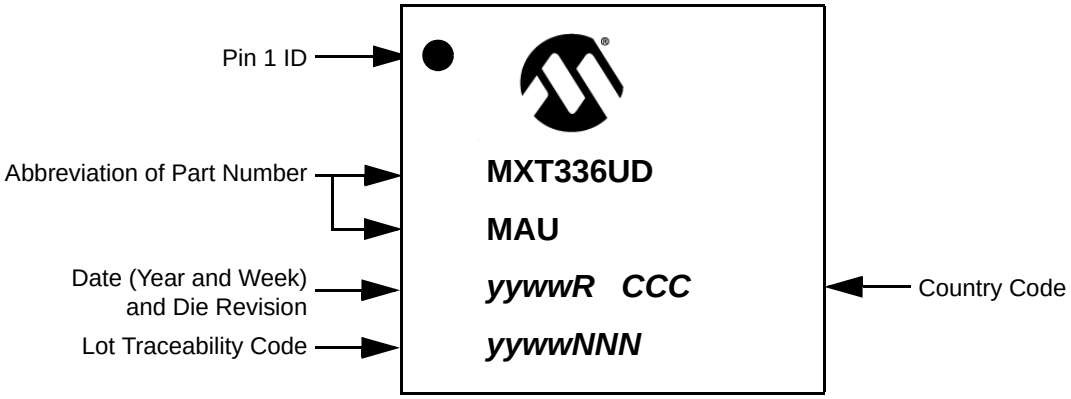
7.10 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	QFN	260°C	IPC/JEDEC J-STD-020

8.0 PACKAGING INFORMATION

8.1 Package Marking Information

8.1.1 56-PIN XQFN

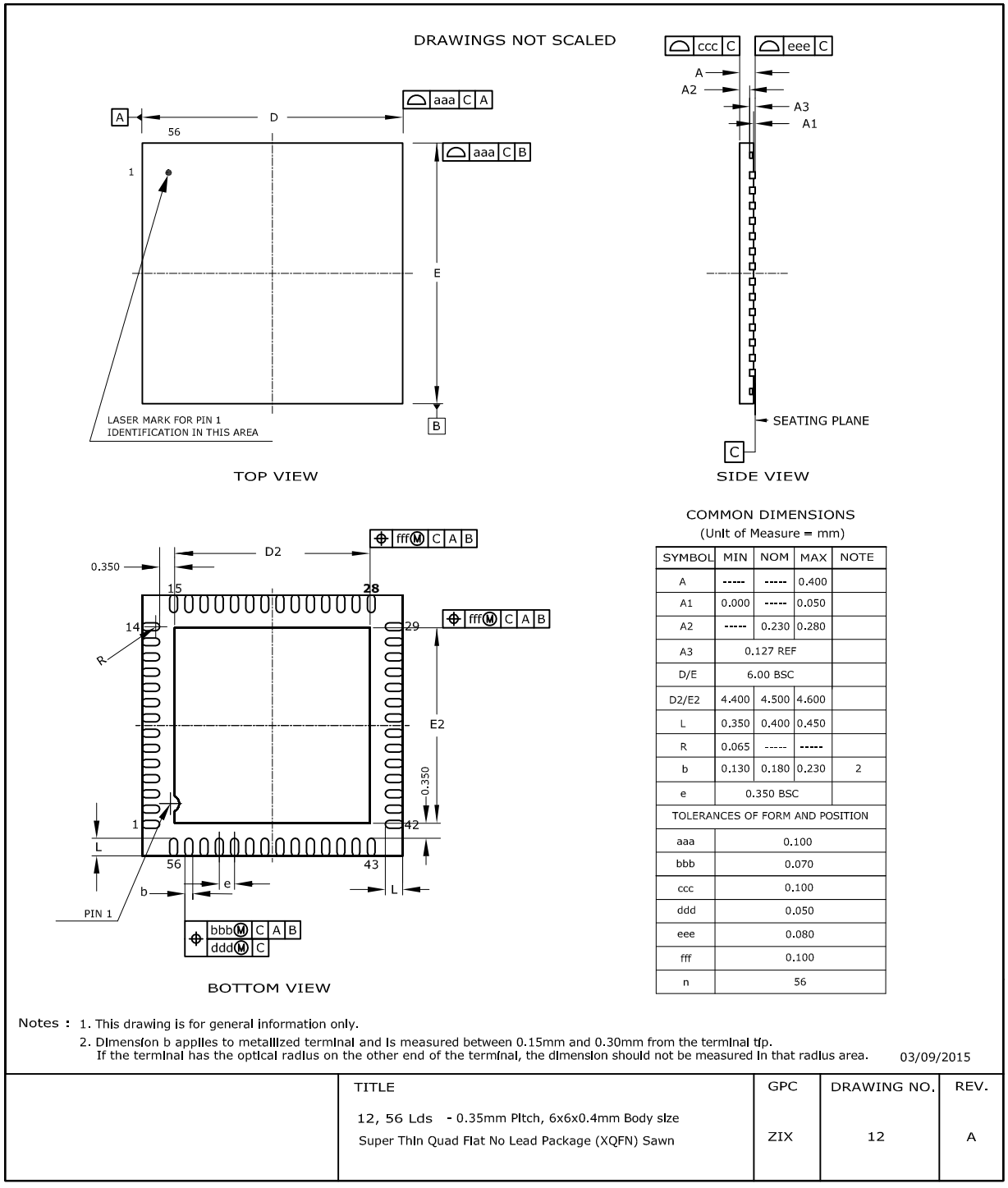


8.1.2 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in "Product Identification System". That section also lists example part numbers for the device.

8.2 Package Details

8.2.1 56-PIN XQFN 6 × 6 × 0.4 MM



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	0.400	
A1	0.000	-----	0.050	
A2	-----	0.230	0.280	
A3	0.127 REF			
D/E	6.00 BSC			
D2/E2	4.400	4.500	4.600	
L	0.350	0.400	0.450	
R	0.065	-----	-----	
b	0.130	0.180	0.230	2
e	0.350 BSC			
TOLERANCES OF FORM AND POSITION				
aaa	0.100			
bbb	0.070			
ccc	0.100			
ddd	0.050			
eee	0.080			
fff	0.100			
n	56			

Notes : 1. This drawing is for general information only.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

03/09/2015

	TITLE	GPC	DRAWING NO.	REV.
	12, 56 Lds - 0.35mm Pitch, 6x6x0.4mm Body size Super Thin Quad Flat No Lead Package (XQFN) Sawn	ZIX	12	A

APPENDIX A: REVISION HISTORY

Revision A (January 2020)

Initial edition for firmware revision 0.2 – Advance Information

PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT336UD-MAUHA1.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[X]	[XXX]
Device	Package	Temperature Range	Tape and Reel Option	Pattern

Device:	Base device name		
Package:	A	=	QFP (Plastic Quad Flatpack)
	CC	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C2	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	NH	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C4	=	X1FBGA (Extra Thin Fine-pitch Ball Grid Array)
	MA	=	XQFN (Super Thin Quad Flat No Lead Sawn)
	MA5	=	XQFN (Super Thin Quad Flat No Lead Sawn)
Temperature Range:	U	=	–40°C to +85°C (Grade 3)
	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Tape and Reel Option:	*Blank*	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel (1)
Pattern:	Extension, QTP, SQTP, Code or Special Requirements (Blank Otherwise)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT336UD-MAUHA1 (Supplied in trays)	0.2	56-pin XQFN 6 × 6 × 0.4 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT336UD-MAURHA1 (Supplied in tape and reel)		

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

ISBN: 978-1-5224-5408-3

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