

MOSFET
OptiMOS™ 7 Power-Transistor, 25 V

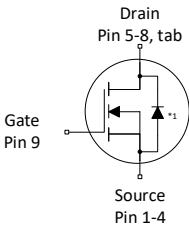
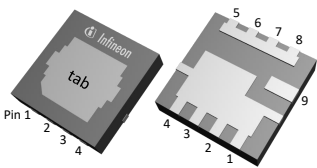
Features

- N-channel, logic level
- Optimized for hard-switching topologies
- Optimized for best FOM_{oss}
- Excellent Miller ratio for dv/dt ruggedness
- Very low on-resistance R_{DS(on)}
- Superior thermal resistance, dual-side cooling feature
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

PG-WHTFN-9 (3x3)



*1: Internal body diode

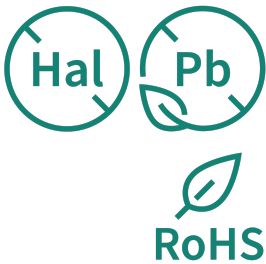


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	0.46	mΩ
I_D	440	A
Q_{oss}	38	nC
$Q_G (0V...10V)$	57	nC

Part number	Package	Marking	Related links
IQEH46NE2LM7UCGSC	PG-WHTFN-9	X	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	440	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$
				311		$V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
				242		$V_{GS}=4.5\text{ V}$, $T_C=100\text{ °C}$
				57		$V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1760	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	340	mJ	$I_D=20\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	-	-	150	W	$T_C=25\text{ °C}$
				2.5		$T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.0	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		0.7	-		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	60		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.4	1.7	2.0	V	$V_{DS}=V_{GS}$, $I_D=432\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=22\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=22\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=16\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.41	0.46	m Ω	$V_{GS}=10\text{ V}$, $I_D=20\text{ A}$
			0.61	0.76		$V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance	R_G	-	0.75	-	Ω	-
Transconductance	g_{fs}	55	110	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4700	6100	pF	$V_{GS}=0\text{ V}$, $V_{DS}=12\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		1800	-		
Reverse transfer capacitance	C_{rss}		81	-		
Turn-on delay time	$t_{d(on)}$	-	7.0	-	ns	$V_{DD}=12\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r		2.0			
Turn-off delay time	$t_{d(off)}$		29			
Fall time	t_f		4.4			

Table 6 Gate charge characteristics ⁶⁾

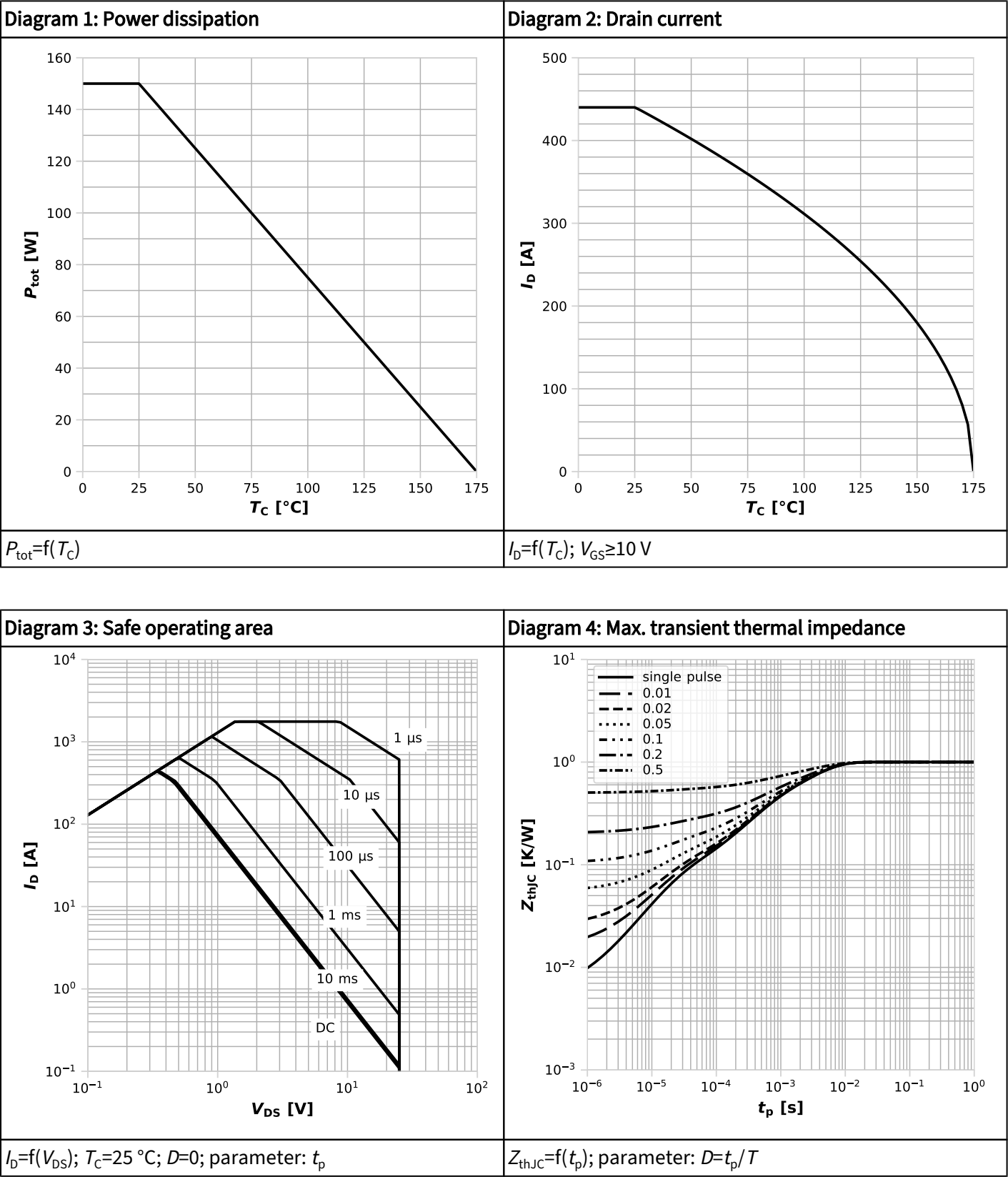
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	13.3	-	nC	$V_{DD}=12\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		8.1		nC	
Gate to drain charge	Q_{gd}		4.2		nC	
Switching charge	Q_{sw}		9.4		nC	
Gate charge total	Q_g		27		nC	
Gate plateau voltage	$V_{plateau}$		2.8		V	
Gate charge total	Q_g	-	57	-	nC	$V_{DD}=12\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	38	-	nC	$V_{DS}=12\text{ V}$, $V_{GS}=0\text{ V}$

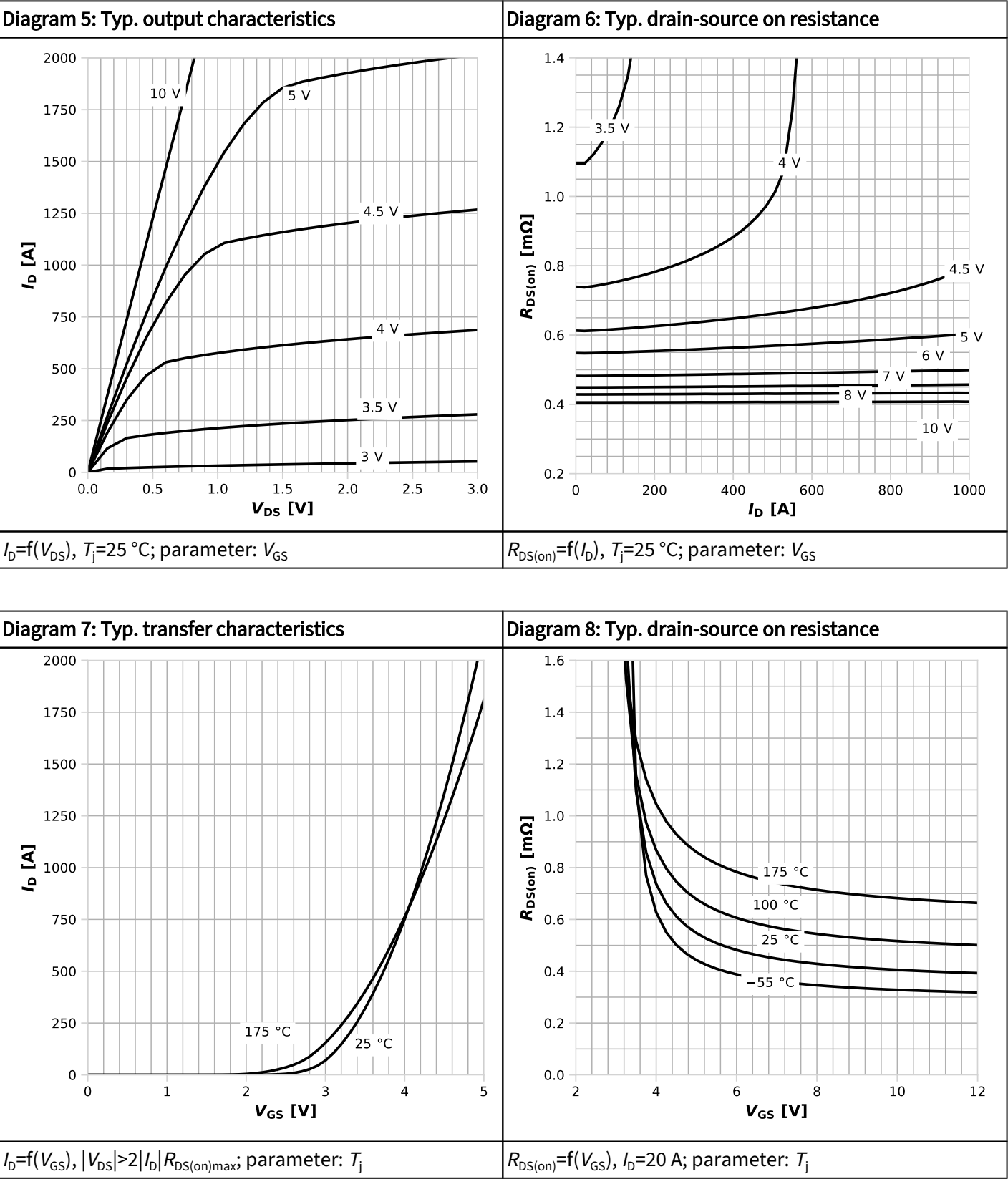
⁶⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	138	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			1760		
Diode forward voltage	V_{SD}	-	0.76	1.0	V	$V_{GS}=0\text{ V}$, $I_F=20\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	25	-	ns	$V_R=12\text{ V}$, $I_F=20\text{ A}$, $di_F/dt=400\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		88		nC	

4 Electrical characteristics diagrams





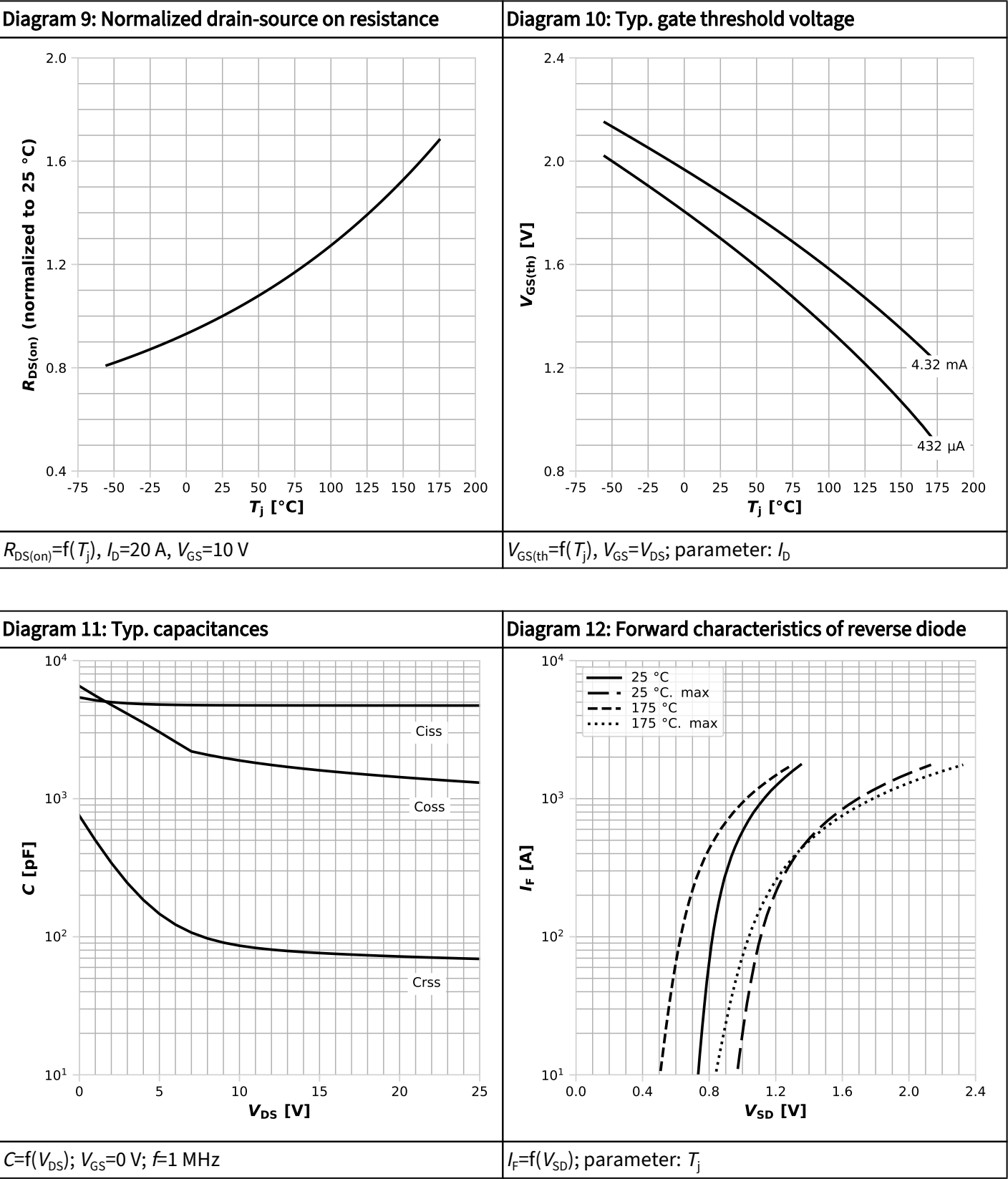
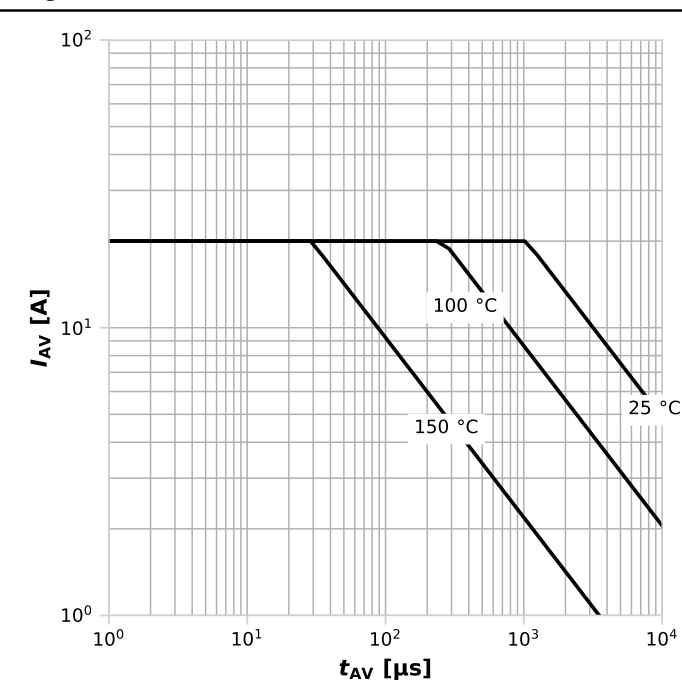
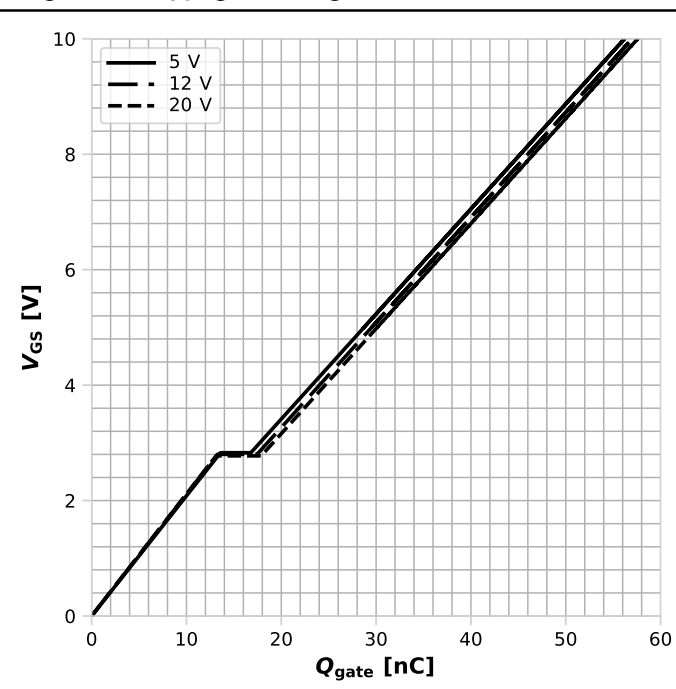


Diagram 13: Avalanche characteristics



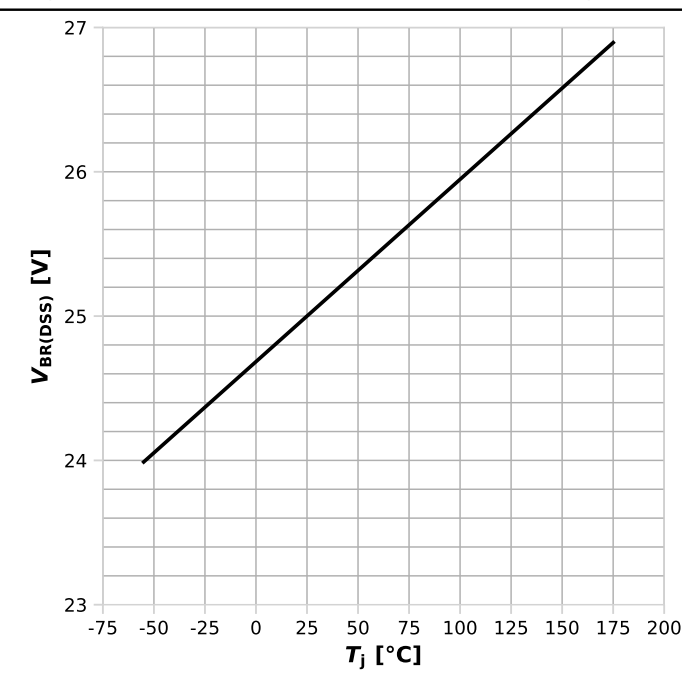
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



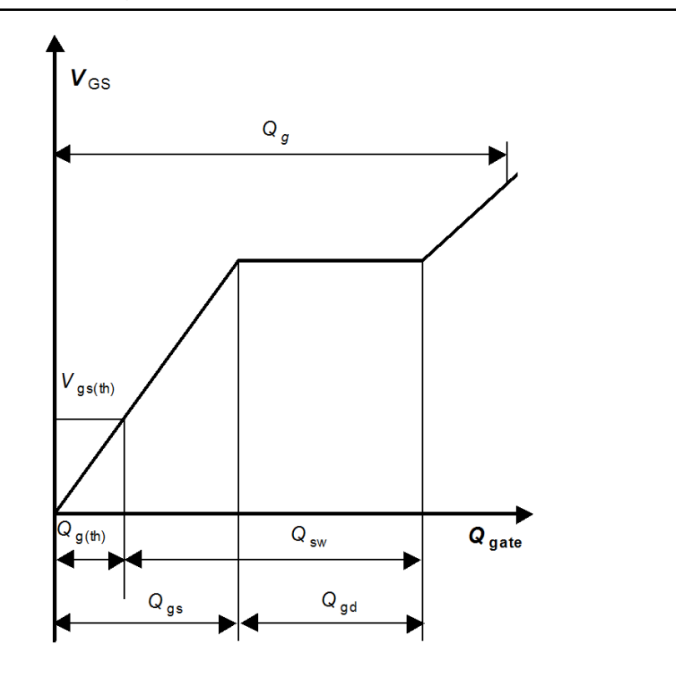
$V_{GS}=f(Q_{gate})$, $I_D=20\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package outlines

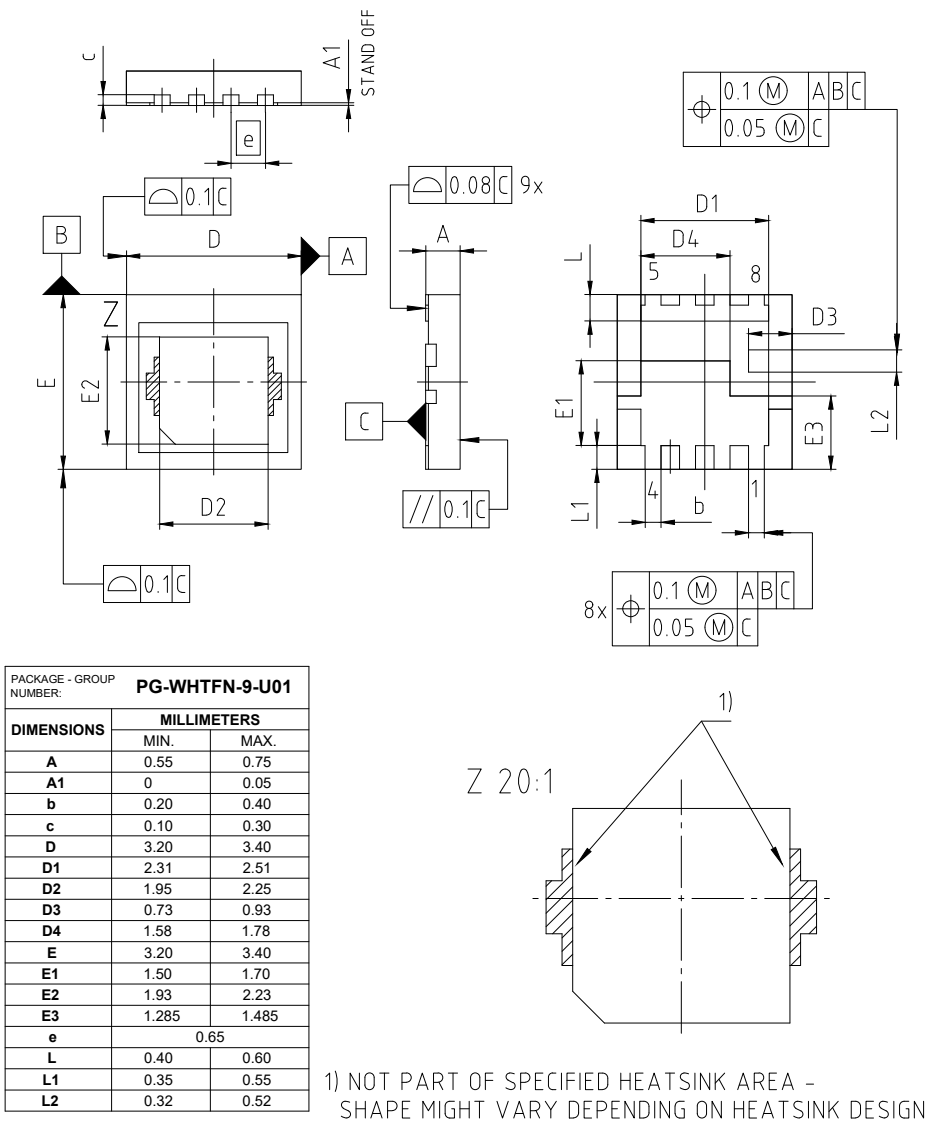


Figure 1 Outline PG-WHTFN-9, dimensions in mm

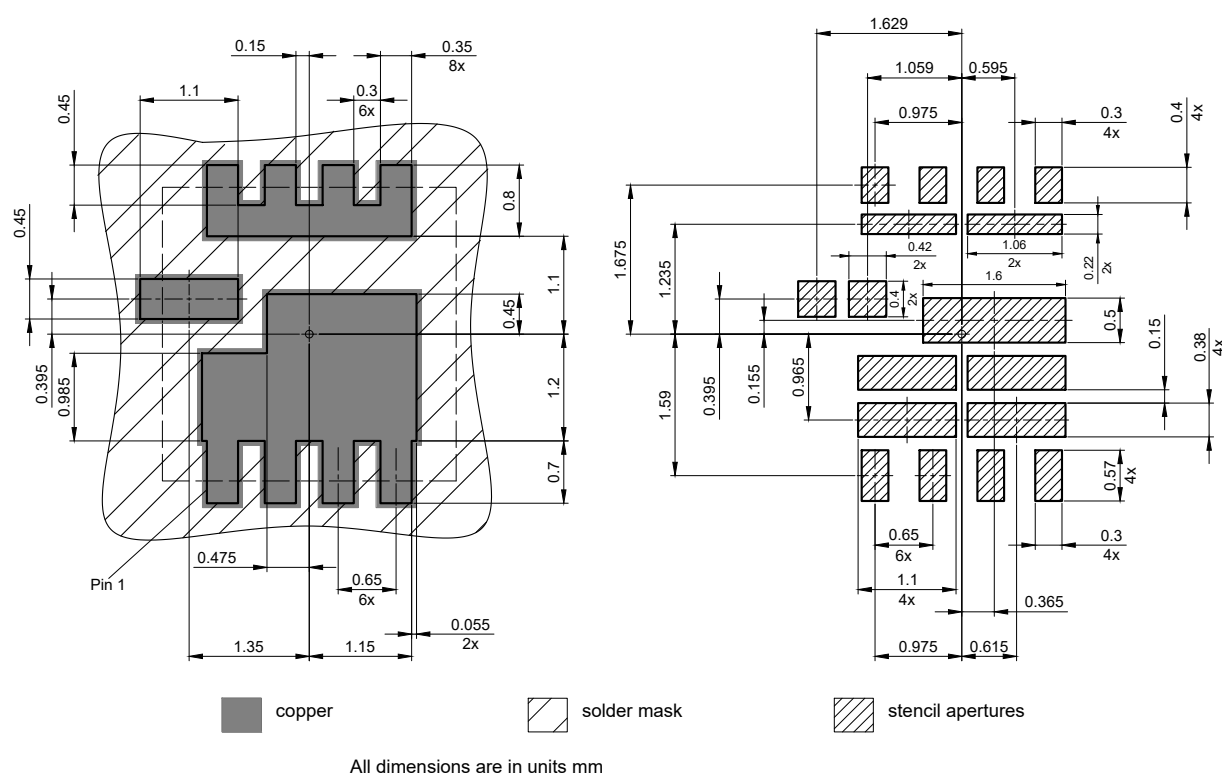


Figure 2 Footprint drawing PG-WHTFN-9, dimensions in mm

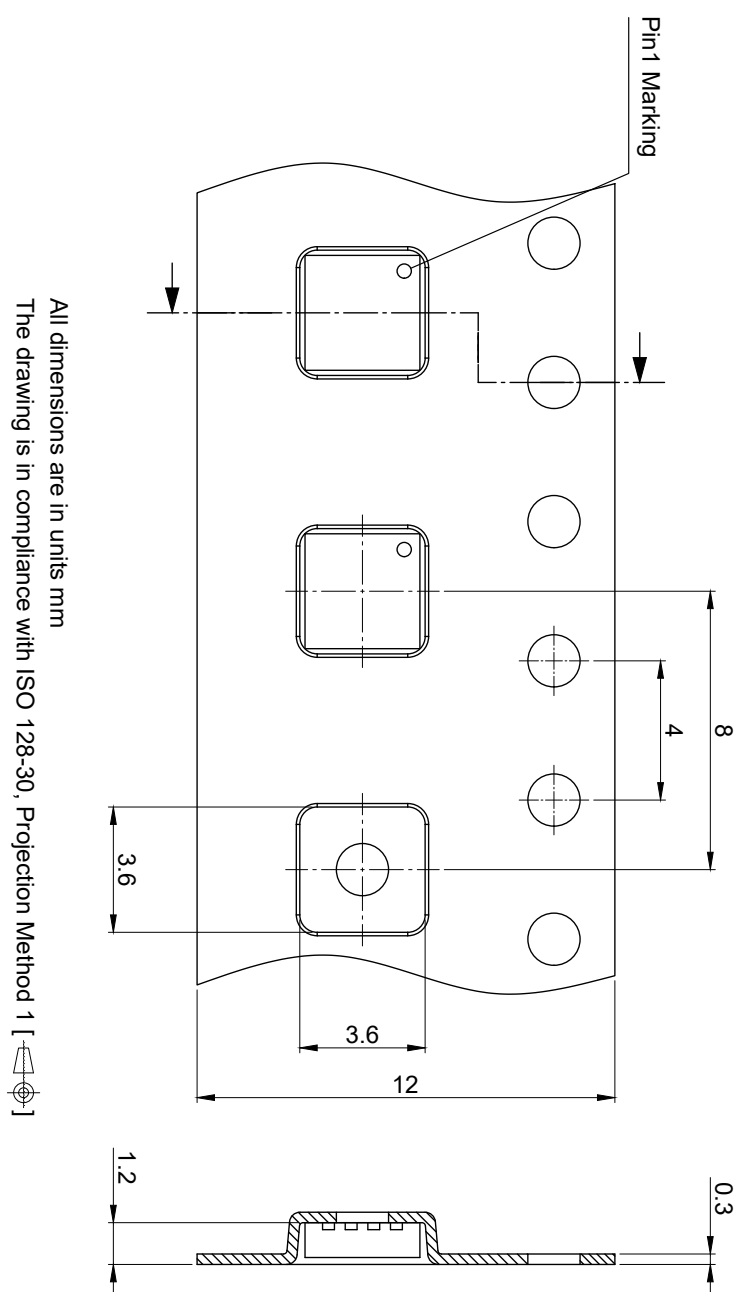


Figure 3 Packaging variant PG-WHTFN-9, dimensions in mm

Revision history

IQEH46NE2LM7UCGSC

Revision 2025-08-05, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-08-05	Release of final datasheet

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