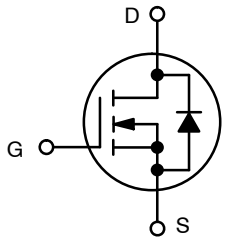
MOSFET – Power, Single N-Channel

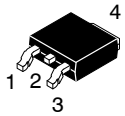
60 V, 27.4 mΩ, 17 A

NVD5C688NL

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	27.4 mΩ @ 10 V	17 A
	40 mΩ @ 4.5 V	



N-CHANNEL MOSFET



DPAK
CASE 369C
STYLE 2

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	±16	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25 °C	I_D	17	A
		T_C = 100 °C		12	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25 °C	P_D	18	W
		T_C = 100 °C		9.0	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25 °C	I_D	7.0	A
		T_A = 100 °C		5.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25 °C	P_D	2.9	W
		T_A = 100 °C		1.45	
Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		I_{DM}	77	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	20	A
Single Pulse Drain-to-Source Avalanche Energy (T_J = 25 °C, $I_{L(pk)}$ = 1 A)			E_{AS}	48	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

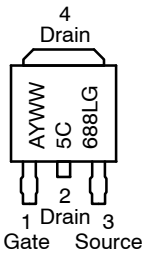
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	8.05	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	51.6	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
5C688L = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125 °C			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 15 μA		1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.4		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A			22.8	27.4	mΩ
		V_{GS} = 4.5 V, I_D = 10 A			32	40	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 10 A			20		S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			400		pF
Output Capacitance	C_{oss}				170		
Reverse Transfer Capacitance	C_{rss}				12		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = 48 V, I_D = 10 A	V_{GS} = 4.5 V		3.4		nC
			V_{GS} = 10 V		7.0		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 10 A			0.9		nC
Gate-to-Source Charge	Q_{GS}				1.5		
Gate-to-Drain Charge	Q_{GD}				1.1		
Plateau Voltage	V_{GP}				2.9		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 10 A, R_G = 2.5 Ω			8		ns
Rise Time	t_r				42		
Turn-Off Delay Time	$t_{d(off)}$				11		
Fall Time	t_f				24		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25 °C		0.9	1.2	V
			T_J = 125 °C		0.8		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 10 A			17		ns
Charge Time	ta				8		
Discharge Time	tb				9		
Reverse Recovery Charge	Q_{RR}				10		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

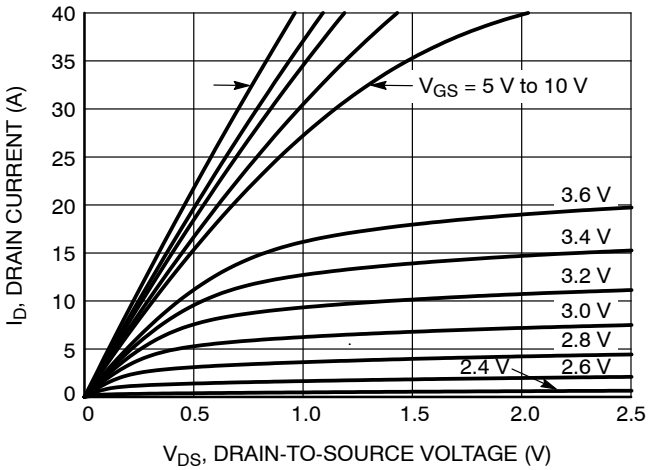

Figure 1. On-Region Characteristics

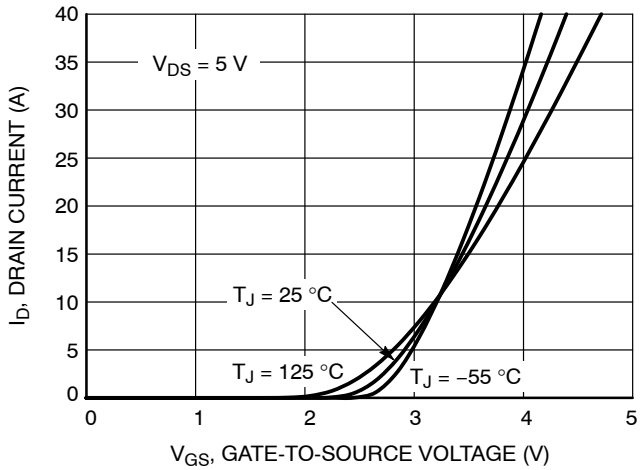

Figure 2. Transfer Characteristics

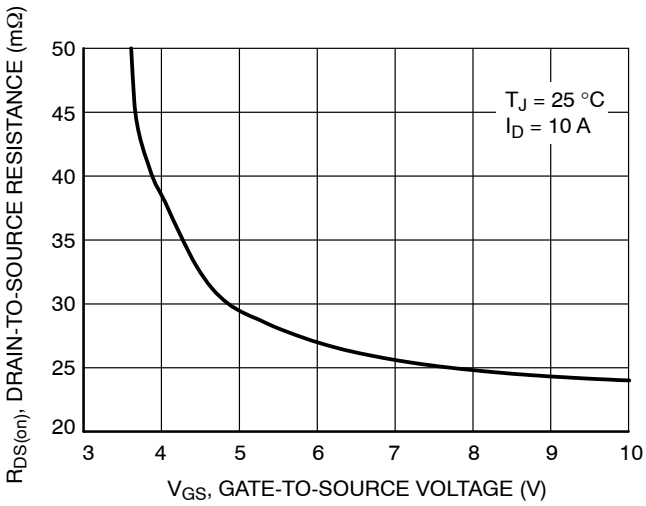

Figure 3. On-Resistance vs. Gate-to-Source Voltage

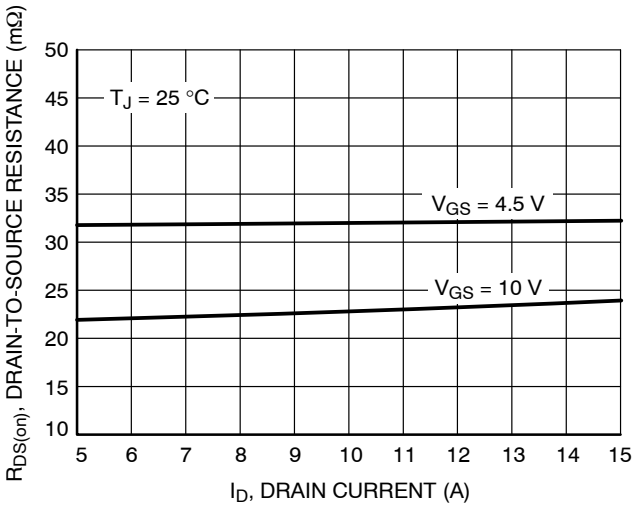

Figure 4. On-Resistance vs. Drain Current and Gate Voltage

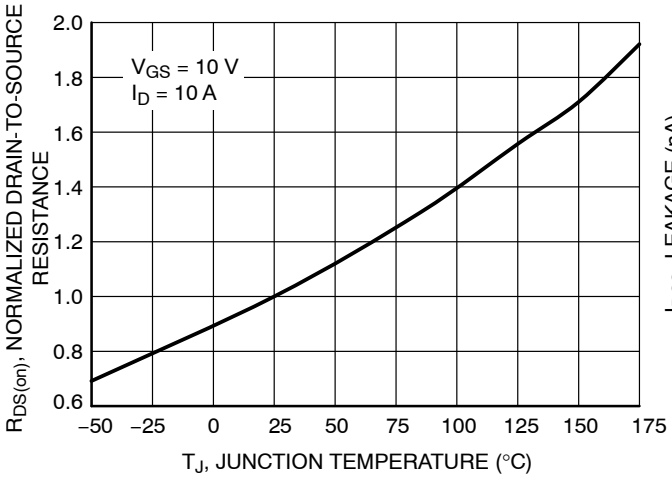

Figure 5. On-Resistance Variation with Temperature

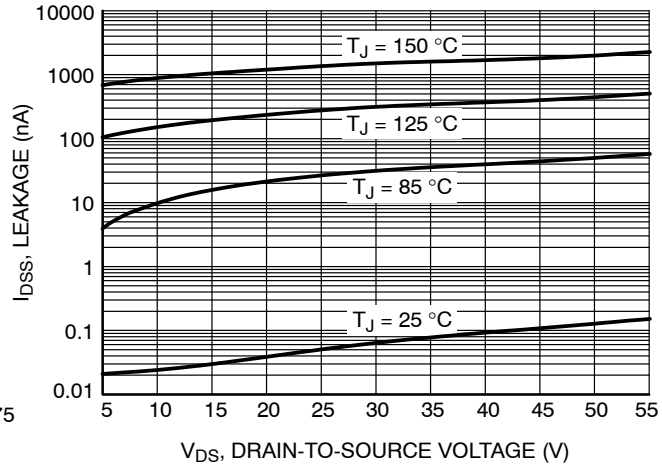

Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

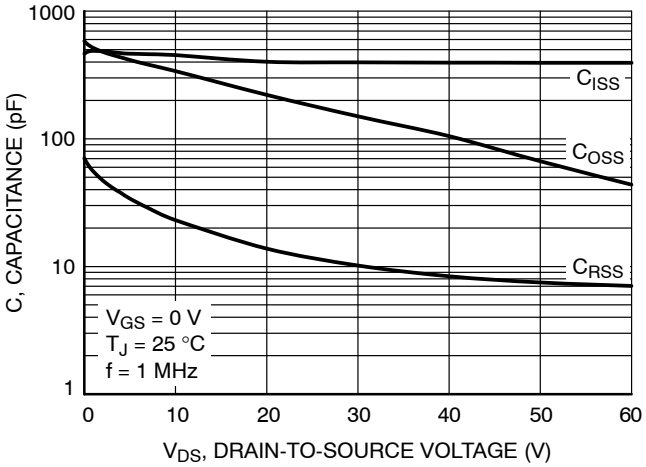

Figure 7. Capacitance Variation

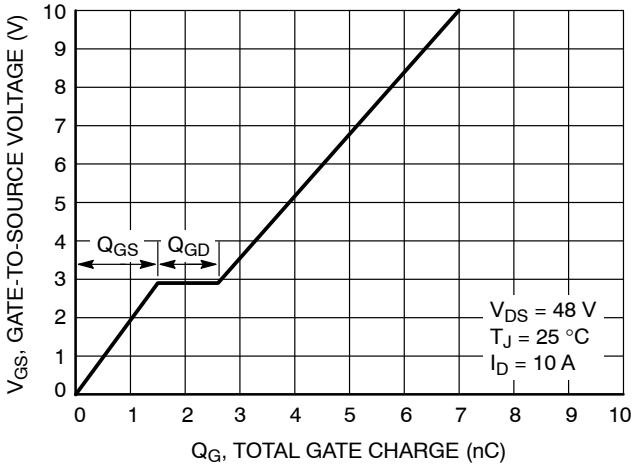

Figure 8. Gate−to−Source vs. Total Charge

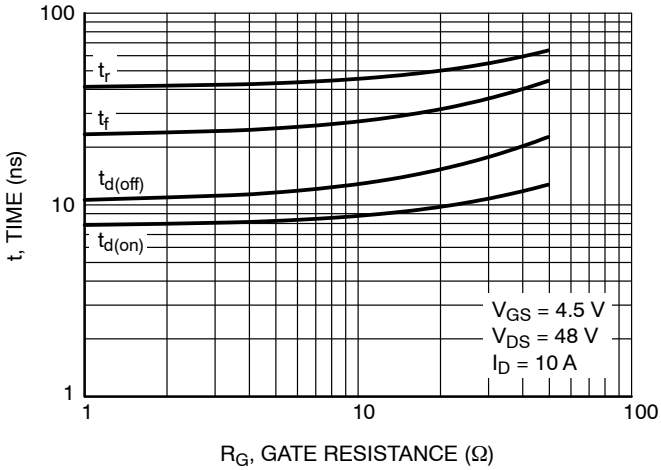

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

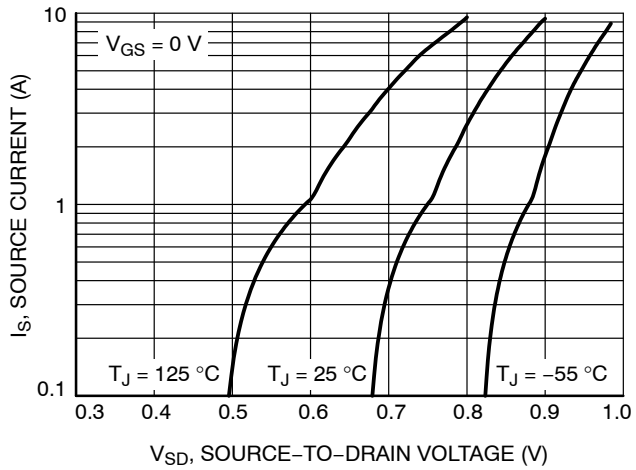

Figure 10. Diode Forward Voltage vs. Current

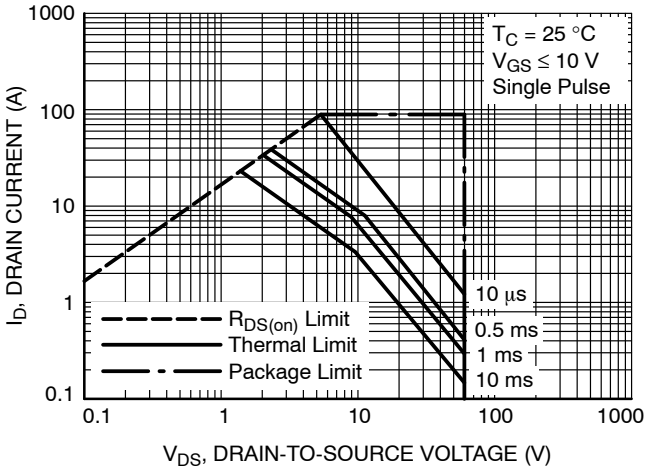

Figure 11. Maximum Rated Forward Biased Safe Operating Area

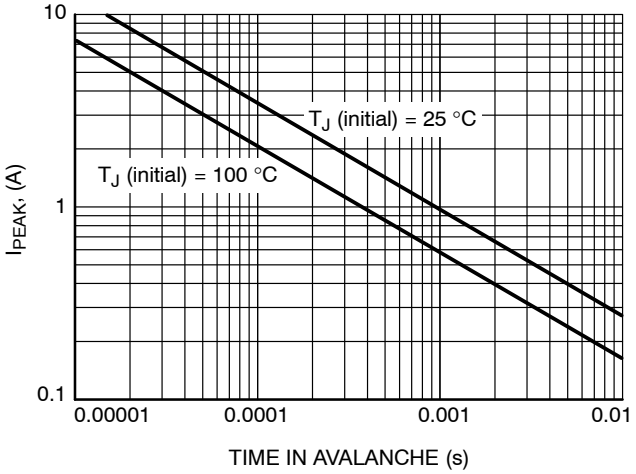

Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

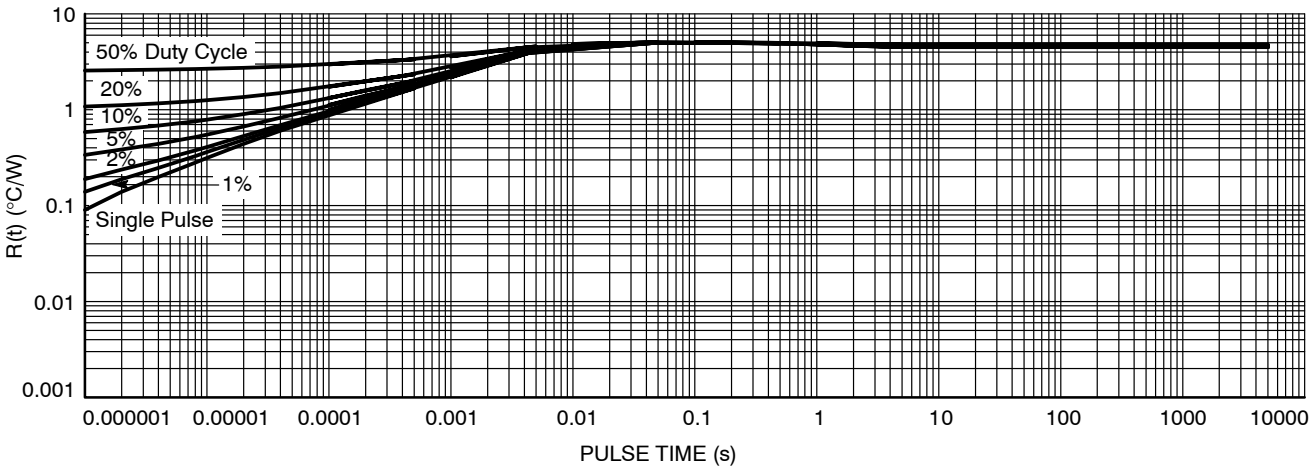

Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping†
NVD5C688NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranding to **onsemi** format.	3/16/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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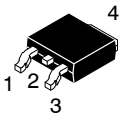
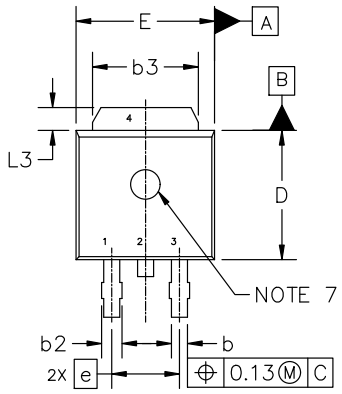


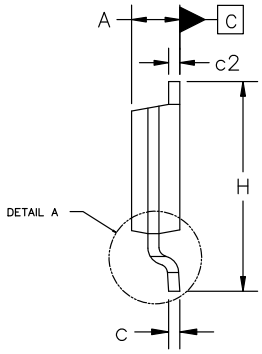
SCALE 1:1

DPAK–3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE K

DATE 14 MAY 2026

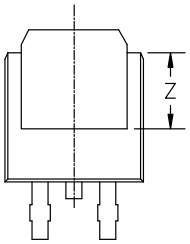


TOP VIEW

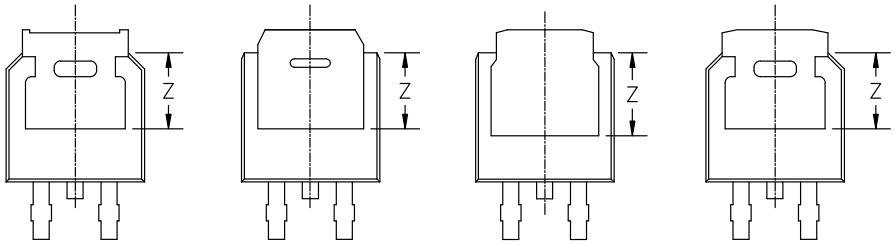


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



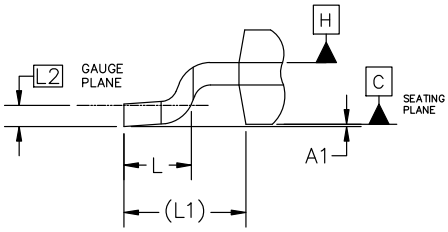
BOTTOM VIEW



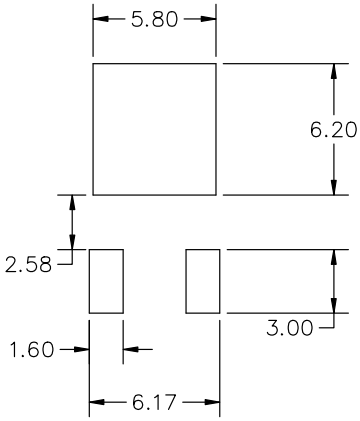
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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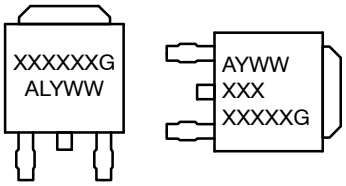
CASE 369C
ISSUE K

DATE 13 MAY 2026

GENERIC
MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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