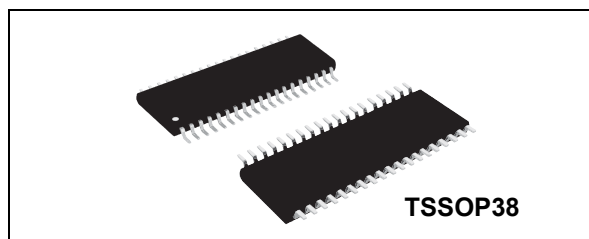


## Digital controller for lighting and power conversion applications with 6 programmable PWM generators, 96 MHz PLL, DALI

Datasheet - production data



### Features

- 6 programmable PWM generators (SMEDs) (state machine event driven)
  - 10 ns event detection and reaction
  - Max. 1.3 ns PWM resolution
  - Single, coupled and two coupled operational modes
  - Up to 3 internal/external events per SMED
- DALI (digital addressable lighting interface)
  - Interrupt driven hardware encoder
  - Bus frequency: 1.2, 2.4 or 4.8 kHz
  - IEC 60929 and IEC 62386 compliant plus 24-bit frame extension
  - Configurable noise rejection filter
  - Reverse polarity on Tx/Rx lines
- 4 analog comparators
  - 4 internal 4-bit references
  - 1 external reference
  - Less than 50 ns propagation time
  - Continuous comparison cycle
- 8 analog-to-digital converters (ADCs)
  - 10-bit precision, with operational amplifier to extend resolution to 12-bit equivalent
  - Sequencer functionality
  - Input impedance: 1 M $\Omega$
  - Configurable gain value: x 1 or x 4
- Integrated microcontroller
  - Advanced STM8<sup>®</sup> core with Harvard architecture and 3-stage pipeline
  - Max. f<sub>CPU</sub>: 16 MHz
- Memories
  - Flash and E<sup>2</sup>PROM with read while write (RWW) and error correction code (ECC)
  - Program memory: 32 Kbytes Flash; data retention 15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 Kbyte true data E<sup>2</sup>PROM; data retention: 15 years at 85 °C after 100 kcycles at 85 °C
  - RAM: 2 Kbytes
  - ROM: 2 Kbytes
- Clock management
  - Internal 96 MHz PLL
  - Low-power oscillator circuit for external crystal resonator or direct clock input
  - Internal, user-trimmable 16 MHz RC and low-power 153.6 kHz RC oscillators
  - Clock security system with clock monitor
- Basic peripherals
  - System and auxiliary timers
  - IWDG/WWDG watchdog, AWU, ITC
- Reset and supply management
  - Multiple low-power modes (wait, slow, auto-wakeup, Halt) with user definable clock gating
  - Low consumption power-on and power-down reset
- I/O
  - 12 multifunction bidirectional GPIO with highly robust design, immune against current injection
  - 6 fast digital input DIGIN, with configurable pull-up
- Communication interfaces
  - UART asynchronous with SW flow control
  - I<sup>2</sup>C master/slave fast-slow speed rate
- Operating temperature
  - -40 °C up to 105 °C.

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# 1 Description

The STLUX385A device is part of the STLUX™ family of STMicroelectronics® digital devices tailored for lighting and power conversion applications. The STLUX385A has been successfully integrated in a wide range of architectures and applications, starting from simple buck converters for driving multiple LED strings, boost for power factor corrections, half-bridge resonant converters for high power dimmable LED strings and up to full bridge controllers for HID lamp ballasts.

## 2 Introducing SMED

The heart of the STLUX385A device is the SMED (state machine event driven) technology which allows the device to operate six independently configurable PWM clocks with a maximum resolution of 1.3 ns. A SMED is a powerful autonomous state machine, which is programmed to react to both external and internal events and may evolve without any software intervention. The SMED reaction time can be as low as 10.4 ns, giving the STLUX385A the ability of operating in time critical applications. The SMED offers superior performance when compared to traditional, timer based, PWM generators.

Each SMED is configured via the STLUX385A internal microcontroller. The integrated controller extends the STLUX385A reliability and guarantees more than 15 years of both operating lifetime and memory data retention for program and data memory after cycling.

A set of dedicated peripherals complete the STLUX385A:

- 4 analog comparators with configurable references and 50 ns max. propagation delay. It is ideal to implement zero current detection algorithms or detect current peaks.
- 10-bit ADC with configurable op amp and 8-channel sequencer.
- DALI: hardware interface that provides full IEC 60929 and IEC 62386 slave interface.
- 96 MHz PLL for high output signal resolution.

## Documentation

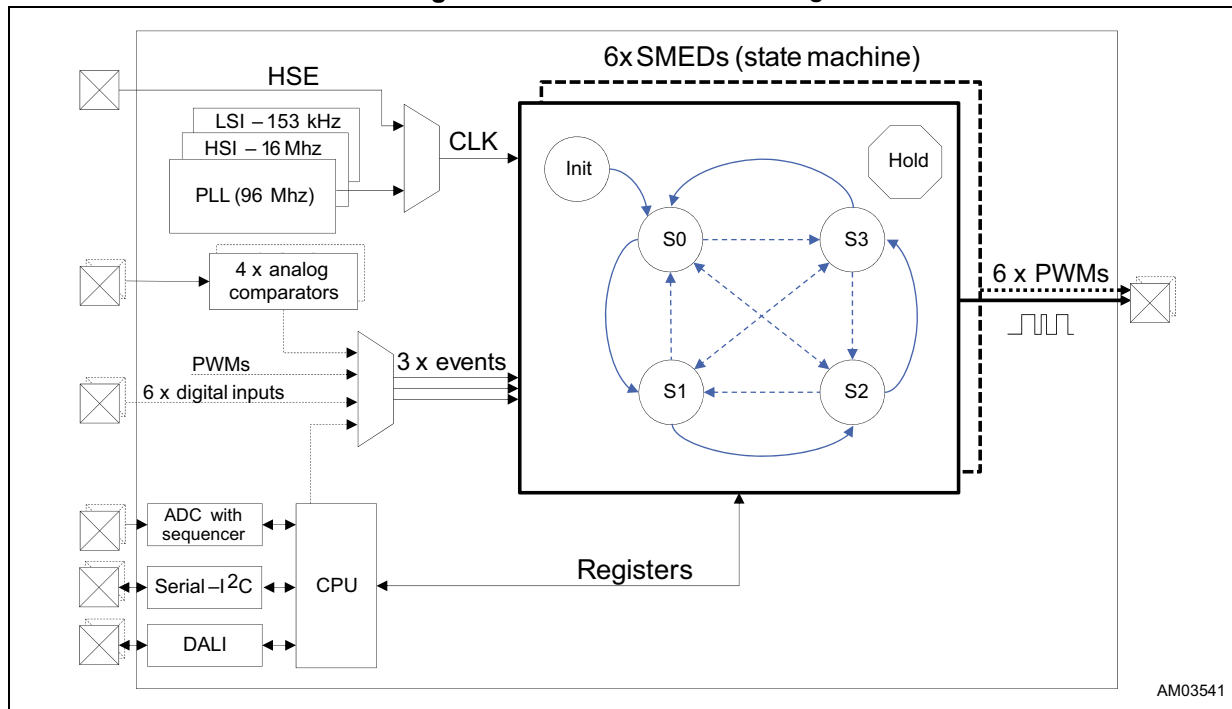
This datasheet contains the description of features, pinout, pin assignment, electrical characteristics, mechanical data and ordering information.

- For information on programming, erasing and protection of the internal Flash memory, please refer to the STM8S reference in the programming manual “How to program STM8S and STM8A Flash program memory and data EEPROM” (PM0051).
- For information on the debug and SWIM (single wire interface module) refer to the “STM8 SWIM communication protocol and debug module” user manual (UM0470).
- For information on the STM8 core, please refer to the “STM8 CPU programming manual” (PM0044).

### 3 System architecture

The STLUX385A device generates and controls PWM signals by means of a state machine, called SMED (state machine event driven). [Figure 1](#) gives an overview of the internal architecture.

**Figure 1. STLUX385A internal design**



The core of the device is the SMED unit: a hardware state machine driven by system events. The SMED includes 4 states (S0, S1, S2 and S3) available during running operations. A special HOLD state is provided as well. The SMED allows the user to configure, for every state, which system events trigger a transaction to a new state. During a transaction from one state to the other, the PWM output signal level can be updated.

Once a SMED is configured and running, it becomes an autonomous unit, so no interaction is required since the SMED automatically reacts to system events.

Thanks to the SMED's 96 MHz operating frequency and their automatic dithering function, the PWM maximum resolution is 1.3 ns.

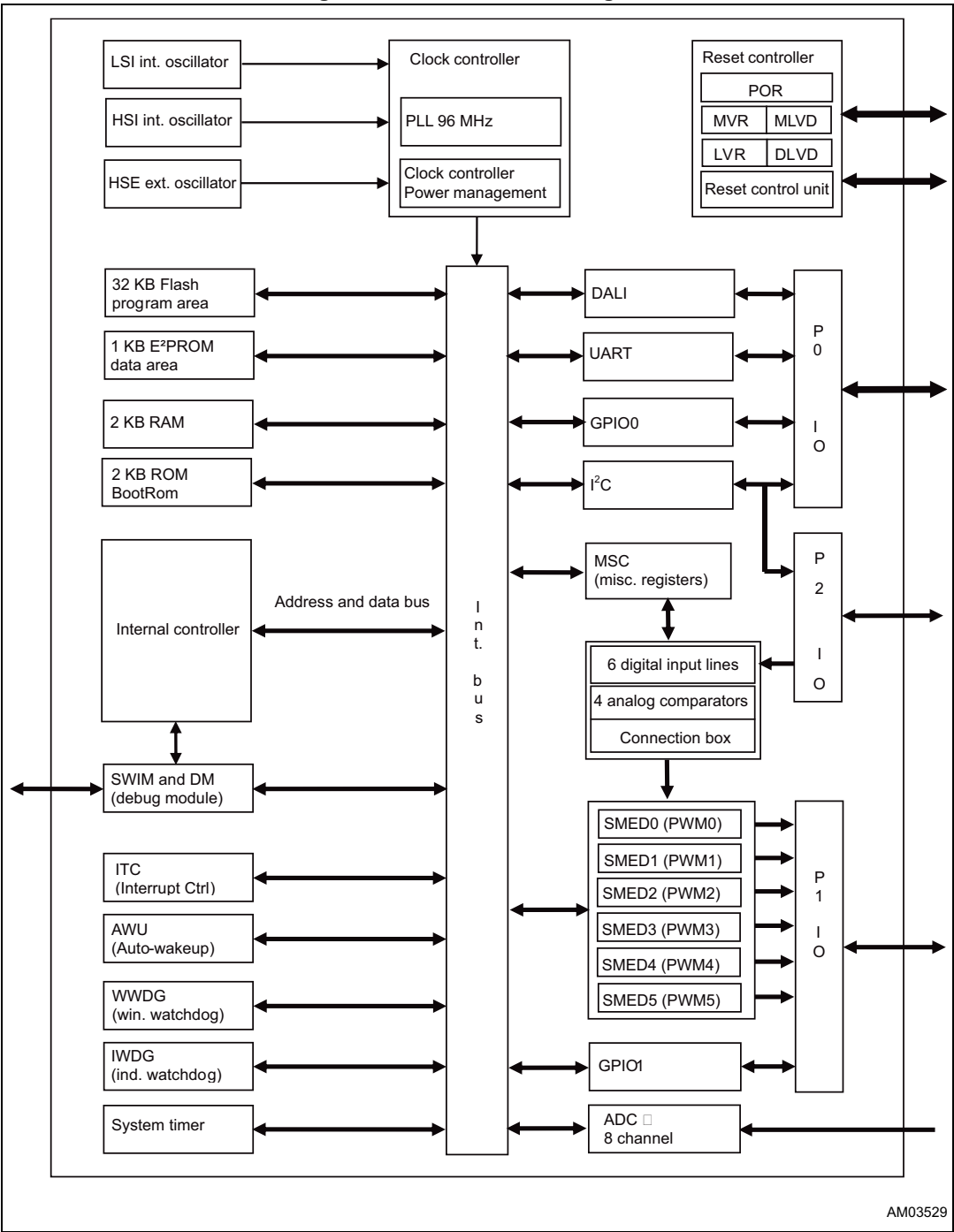
The STLUX385A device has 6 SMEDs available. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The STLUX385A also integrates a low-power STM8 microcontroller which is used to configure and monitor the SMED activity and to supply external communication such as DALI. The STM8 controller has full access to all the STLUX385A subsystems, including the SMEDs. The STLUX385A device also features a sequential ADC, which can be configured to continuously sample up to 8 channels.

[Section : Block diagram](#) illustrates the overall system block and shows how SMEDs have been implemented in the STLUX385A architecture.

Block diagram

Figure 2. Internal block diagram



## 4 Product overview

[Section 4.1](#) describes the features implemented in the product device.

### 4.1 SMED (state machine event driven): configurable PWM generator

The SMED is an advanced programmable PWM generator signal. The SMED (state machine event driven) is a state machine device controllable by both external events (primary I/O signals) and internal events (counter timers), which generate an output signal (PWM) depending on the evolution of the internal state machine.

The PWM signal generated by the SMED is therefore shaped by external events and not by a single timer. This mechanism allows controlled high frequency PWM signals to be generated.

The SMED is also autonomous: once it has been configured by the STLUX385A internal controller, the SMED can operate without any software interaction.

The STLUX385A device provides 6 SMED units. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The main features of a SMED are described here below:

- Configurable state machine generating a PWM signal
- More than 10.4 ns PWM native resolution
- Up to 1.3 ns PWM resolution when using SMED dithering
- 6 states available in each SMED: IDLE, S0, S1, S2, S3 plus a special HOLD state
- Transactions triggered by synchronous and asynchronous external events or internal timer
- Each transaction can generate an interrupt
- Fifteen registers available to configure the state machine behavior
- Four 16-bit configurable time registers, one for each running state (T0, T1, T2, T3)
- Internal resources accessible through the processor interface
- Eight interrupt request lines

#### 4.1.1 SMED coupling schemes

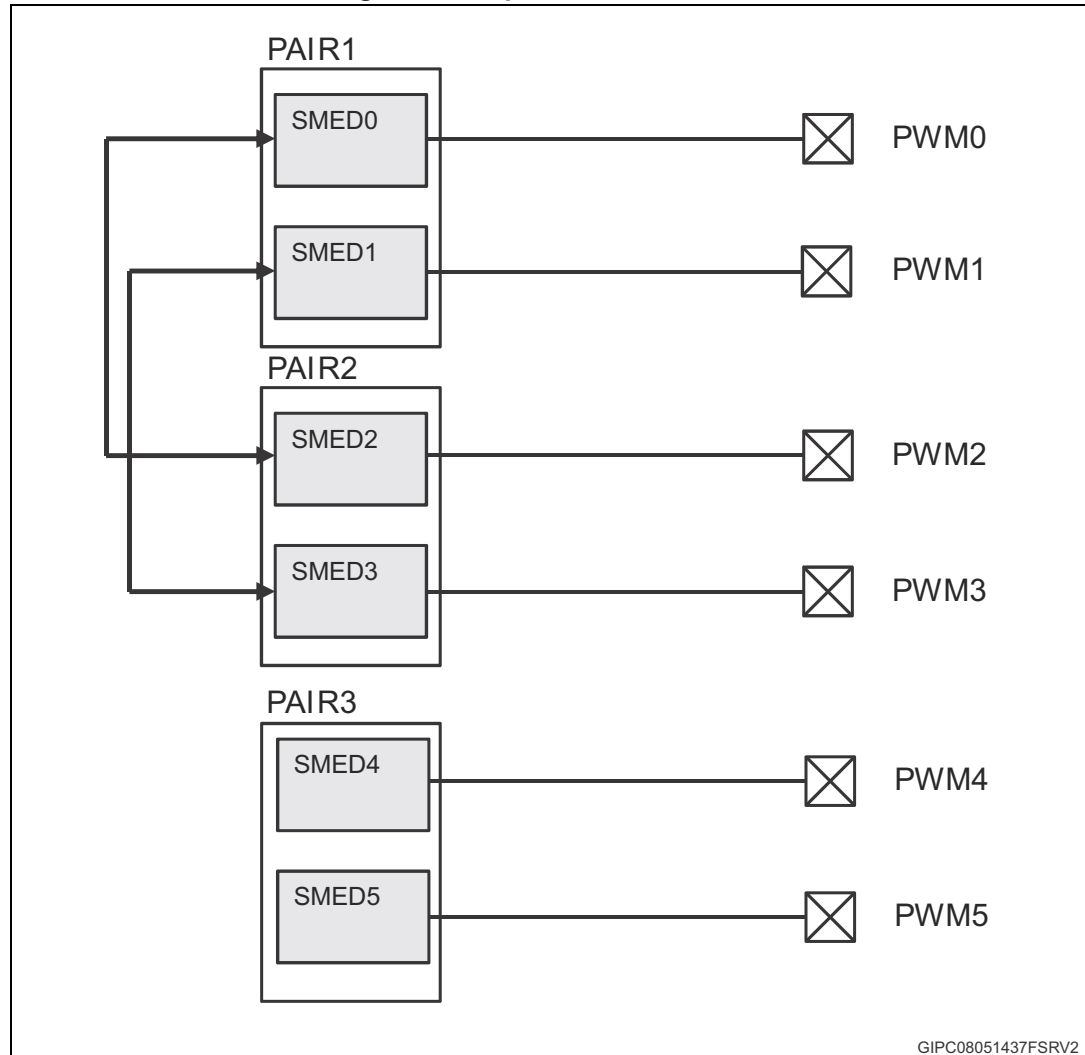
The SMED coupling extends the capability of the single SMED, preserving the independence of each FSM programmed state evolution. The coupling scheme allows the SMED pulse signals to be interleaved on their own PWM or on a merged single PWM output. The STLUX385A supports the following coupled configuration schemes:

- Single SMED configuration
- Synchronous coupled SMED
- Asynchronous coupled SMED
- Synchronous two coupled SMED
- Asynchronous two coupled SMED
- External controlled SMED

The SMED units may be configured in different coupled schemes through the SMDx\_GLBCONF and SMDx\_DRVOUT bit fields of MSC\_SMEDCFGxy registers.

An outline of SMED subsystem is shown in [Figure 3](#).

**Figure 3. Coupled SMED overview**



#### 4.1.2 Connection matrix

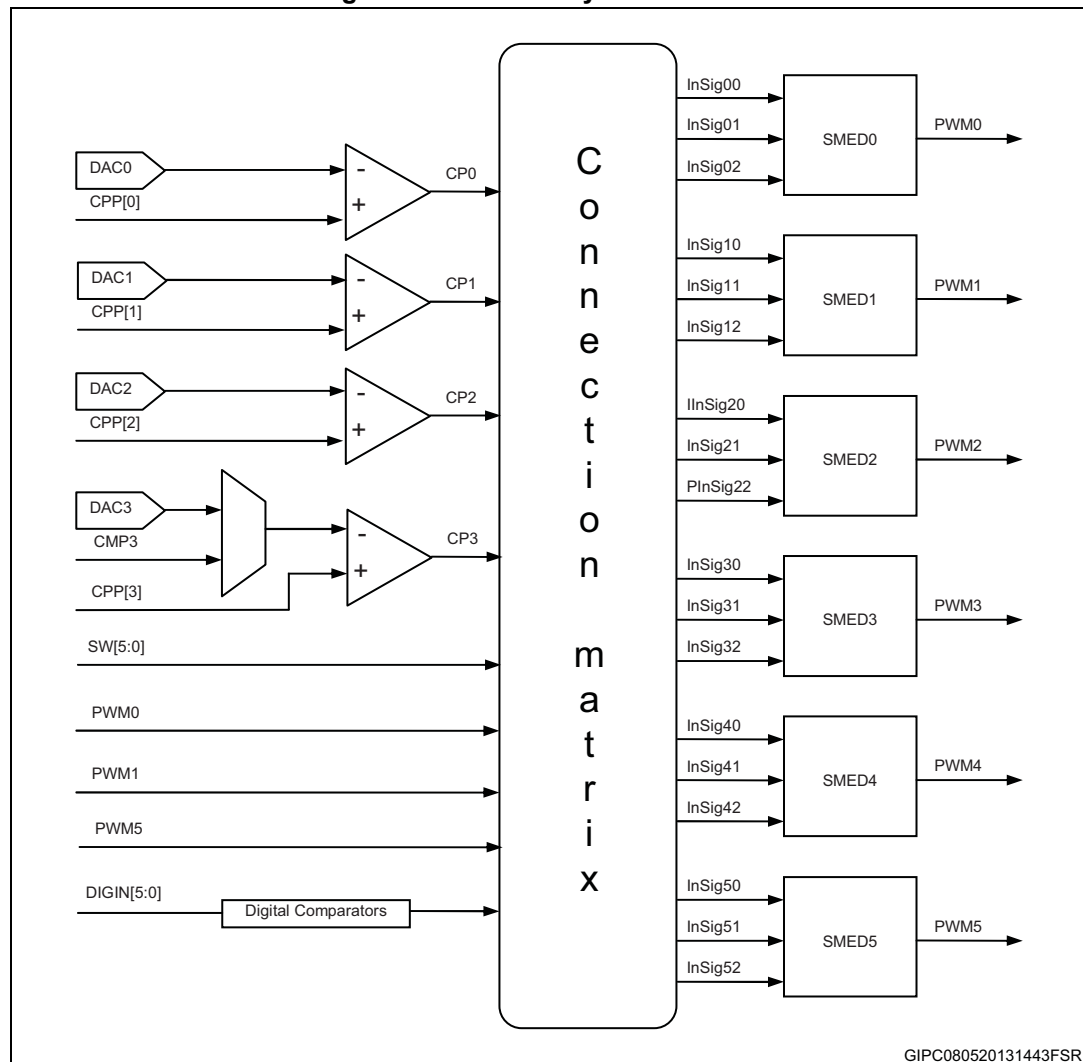
The connection matrix extends the input connectivity of each SMED unit so that a SMED can receive events from a wide range of sources. Through the matrix, it's possible to connect the SMED inputs to various signal families such as digital inputs, comparator output signals, SW events, and three PWM internal feedback signals as shown in [Figure 4](#).

The list of the available event sources is the following:

- DIGIN (5:0) digital input lines
- CMP (3:0) analog comparator outputs
- PWM (5:0) output signals of SMEDs (only PWM 0, 1 and 5 are accessible)
- SW (5:0) software events

Figure 4 shows the connection matrix and signal interconnections as they are implemented in the STLUX385A device.

**Figure 4. SMED subsystem overview**



### Connection matrix interconnection

Every SMED unit has three input selection lines, one for each In\_Sig input, configurable via the MSC\_CBOXS(5:0) register. The selection lines choose the interconnection between one of possible four connection matrix signals for each SMED input event In\_Sig (Y).

*Table 1* shows the layout of the connection matrix interconnection signals as implemented on the STLUX385A device.

**Table 1. Connection matrix interconnection**

| Conb_s(x)(y)(z) |            |                                 |      |      |      |
|-----------------|------------|---------------------------------|------|------|------|
| SMED number     | SMED input | SMED input signal selection (z) |      |      |      |
| (x)             | (y)        | 00                              | 01   | 10   | 11   |
| 0               | 0          | CP0                             | DIG0 | DIG2 | DIG5 |
|                 | 1          | CP1                             | DIG0 | DIG3 | CP3  |
|                 | 2          | CP2                             | DIG1 | DIG4 | SW0  |
| 1               | 0          | CP1                             | DIG1 | DIG3 | DIG0 |
|                 | 1          | CP2                             | DIG1 | DIG4 | CP3  |
|                 | 2          | CP0                             | DIG2 | DIG5 | SW1  |
| 2               | 0          | CP2                             | DIG2 | DIG4 | DIG1 |
|                 | 1          | CP0                             | DIG2 | DIG5 | PWM0 |
|                 | 2          | CP1                             | DIG3 | DIG0 | SW2  |
| 3               | 0          | CP0                             | DIG3 | DIG5 | DIG2 |
|                 | 1          | CP1                             | DIG3 | DIG0 | PWM1 |
|                 | 2          | CP2                             | DIG4 | DIG1 | SW3  |
| 4               | 0          | CP1                             | DIG4 | DIG0 | DIG3 |
|                 | 1          | CP2                             | DIG4 | DIG1 | PWM5 |
|                 | 2          | CP0                             | DIG5 | DIG2 | SW4  |
| 5               | 0          | CP2                             | DIG5 | DIG1 | DIG4 |
|                 | 1          | CP0                             | DIG5 | DIG2 | CP3  |
|                 | 2          | CP1                             | DIG0 | DIG3 | SW5  |

Connection matrix legend:

- X represents the SMED [5:0] number
- Y represents the SMED input signal number (In\_Sig [2:0])
- Z represents the In\_Sig (Y) selection signal

*Note:* Each SMED input has independent connection matrix selection signals.

## 4.2 Internal controller (CPU)

The STLUX385A device integrates a programmable STM8 controller acting as a device supervisor. The STM8 is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six of them directly addressable in each



execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

#### 4.2.1 Architecture and registers

- Harvard architecture with 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16 Mbyte linear memory space
- 16-bit stack pointer with access to a 64-Kbyte stack
- 8-bit condition code register with seven condition flags updated with the results of last executed instruction

#### 4.2.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located in the entire address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

#### 4.2.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

#### 4.2.4 Single wire interface module (SWIM)

The single wire interface module (SWIM), together with the integrated debug module (DM), permits non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging). The maximum data transmission speed is 145 byte/ms.

### 4.2.5 Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Besides memory and peripheral operation, the CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except for the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

## 4.3 Basic peripherals

[Section 4.3.1](#) and [Section 4.2.3](#) describe the basic peripherals accessed by the internal CPU controller.

### 4.3.1 Vectored interrupt controller

- Nested interrupts with three software priority levels
- 21 interrupt vectors with hardware priority
- Two vectors for 12 external maskable or un-maskable interrupt request lines
- Trap and reset interrupts

### 4.3.2 Timers

The STLUX385A device provides several timers which are used by software and do not interact directly with the SMED and the PWM generation.

#### System timers

The system timer consists of a 16-bit autoreload counter driven by a programmable prescaled clock and operating in one shoot or free running operating mode. The timer is used to provide the IC time base system clock, with an interrupt generation on timer overflow events.

#### Auxiliary timer

The auxiliary timer is a light timer with elementary functionality. The time base frequency is provided by the CCO clock logic (configurable with a different source clock and prescale division factors), while the interrupt functionality is supplied by an interrupt edge detection logic similarly to the solution adopted for the Port P0/P2.

The timer has the following main features:

- Free running mode
- Up counter
- Timer prescaler 8-bit
- Interrupt timer capability:
  - Vectored interrupt
  - Interrupt IRQ/NMI or Polling mode
- Timer pulse configurable as a clock output signal via the CCO primary pin

Thanks to the great configurability of the CCO frequency, the timer can cover a wide range of interval time to fit better the target application requirements.

### Auto-wakeup timer

The AWU timer is used to cyclically wake up the IC device from the active-halt state. The AWU frequency time base  $f_{AWU}$  can be selected between the following clock sources: LSI (153.6 kHz) and the external clock HSE scaled down to 128 kHz clock.

**By default the  $f_{AWU}$  clock is provided by the LSI internal source clock.**

### Watchdog timers

The watchdog system is based on two independent timers providing a high level of robustness to the applications. The watchdog timer activity is controlled by the application program or by suitable option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

#### Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which causes the application program to break the normal operating sequence.

The window function can be used to adjust the watchdog intervention period in order to match the application timing perfectly. The application software must refresh the counter before timeout and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

#### Independent watchdog timer

The independent watchdog peripheral can be used to resolve malfunctions due to hardware or software failures.

It is clocked by the 153.6 kHz LSI internal RC clock source. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of the count.

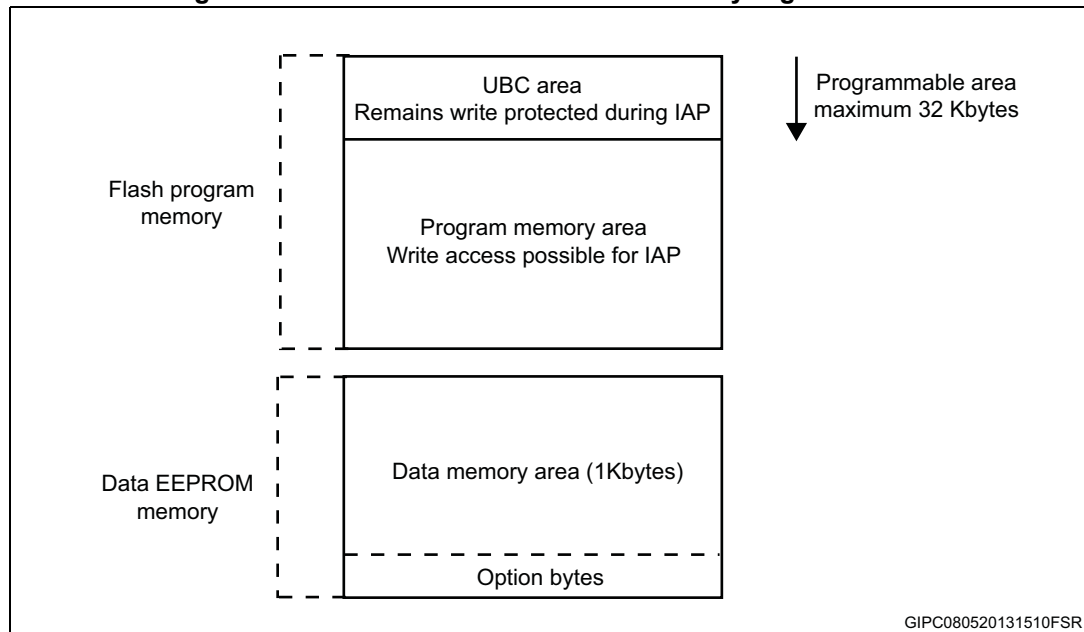
## 4.4 Flash program and data E<sup>2</sup>PROM

Embedded Flash and E<sup>2</sup>PROM with memory ECC code correction and protection mechanism preventing embedded program hacking.

- 32 Kbyte of single voltage program Flash memory
- 1 Kbyte true (not emulated) data E<sup>2</sup>PROM
- Read while write: writing in the data memory is possible while executing code program memory
- The device setup is stored in a user option area in the non-volatile memory.

### 4.4.1 Architecture

Figure 5. Flash and E<sup>2</sup>PROM internal memory organizations



- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

### 4.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

### 4.4.3 Protection of user boot code (UBC)

In the STLUX385A a memory area of 32 Kbyte can be protected from overwriting at a user option level. In addition to the standard write protection, the UBC protection can exclusively be modified via the debug interface, the user software cannot modify the UBC protection status.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and NUBC option bytes.

*Note: If users choose to update the boot code in the application programming (IAP), this has to be protected so to prevent unwanted modification.*

### 4.4.4 Read-out protection (ROP)

The STLUX385A device provides a read-out protection of the code and data memory which can be activated by an option byte setting.

The read-out protection prevents reading and writing program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. The temporary read access is protected by a user defined, 8-byte keyword stored in the option byte area. This keyword must be entered via the SWIM interface to temporarily unlock the device.

If desired, the temporary unlock mechanism can be permanently disabled by the user.

## 4.5 Clock controller

The clock controller distributes the system clock provided by different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

The main clock controller features are:

- Clock sources
- Internal 16 MHz and 153.6 kHz RC oscillators
- External source clock:
  - Crystal/resonator oscillator
  - External clock input
- Internal PLL at 96 MHz (not used as the  $f_{\text{MASTER}}$  source clock)
- Reset: after the reset the microcontroller restarts by default with an internal 2 MHz clock (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- Safe clock switching: clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- Clock management: to reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- Wakeup: In case the device wakes up from low-power modes, the internal RC oscillator (16 MHz/8) is used for a quick startup. After a stabilization time, the device switches to the clock source that was selected before Halt mode was entered.
- Clock security system (CSS): the CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- Configurable main clock output (CCO): this feature outputs the clock signal.

### 4.5.1 Internal 16 MHz RC oscillator (HSI)

The high speed internal (HSI) clock is the default master clock line, generated by an internal RC oscillator and with nominal frequency of 16 MHz. It has the following major features:

- RC architecture
- Glitch free oscillation
- 3-bit user calibration circuit.

#### 4.5.2 Internal 153.6 kHz RC oscillator (LSI)

The low speed internal (LSI) clock is a low speed clock line provided by an internal RC circuit. It drives both the independent watchdog (IWDG) circuit and the auto-wakeup unit (AWU). It can also be used as a low power clock line for the master clock  $f_{\text{MASTER}}$ .

#### 4.5.3 Internal 96 MHz PLL

The PLL provides a high frequency 96 MHz clock used to generate high frequency and accurate PWM waveforms. The input reference clock must be 16 MHz and may be sourced either by the internal HSI signal or by the external HSE auxiliary input crystal oscillator line.

The internal PLL prescaled clock cannot be selected as  $f_{\text{MASTER}}$ .

*Note: Should the end application require a PWM signal with a high degree of stability over long periods, an external clock source connected to the HSE auxiliary clock line as PLL input reference clock, should be used. In this case, the external clock source determines the PWM output stability.*

#### 4.5.4 External clock input/crystal oscillator (HSE)

The high speed external clock (HSE) allows the connection of an external clock generated, for example, by a highly accurate crystal oscillator. The HSE is interconnected with the  $f_{\text{MASTER}}$  clock line and to several peripherals. It allows users to provide a custom clock characterized by a high level of precision and stability to meet the application requirements. The HSE supports two possible external clock sources with a maximum of 24 MHz:

- Crystal/ceramic resonator interconnected with the HseOscin/HseOscout signals
- Direct drive clock interconnected with the HseOscin signal

The HseOscin and HseOscout signals are multifunction pins configurable through the I/O multiplex mechanism; for further information refer to [Section 6 on page 30](#).

*Note: When the HSE is configured as the  $f_{\text{MASTER}}$  source clock, the HSE input frequency cannot be higher than 16 MHz.*

*When the HSE is the PLL input reference clock, then the HSE input frequency must be equal to 16 MHz.*

*If the HSE is the reference for the SMED or the ADC logic, the input frequency can be configured up to 24 MHz.*

## 4.6 Power management

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between the lowest power consumption, the fastest startup time and available wakeup sources.

- **Wait mode:** in this mode, the CPU is stopped, but peripherals are kept running. The wakeup is performed by an internal or external interrupt or reset.
- **Active-halt mode with regulator on:** in this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto-wakeup unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in active-halt mode with the regulator off, but the wakeup time is faster. The wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active-halt mode with regulator off:** this mode is the same as active-halt with the regulator on, except that the main voltage regulator is powered off, so the wakeup time is slower.
- **Halt mode:** in this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, while the main voltage regulator is switched in power-off. Wakeup is triggered by an external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brownout reset circuit remains enabled.

## 4.7 Communication interfaces

### 4.7.1 Digital addressable lighting interface (DALI)

DALI (digital addressable lighting interface), standardized as IEC 929, is the new interface for lighting control solutions defined by the lighting industry.

The DALI protocol is generally implemented in a DALI communication module (DCM): a serial communication circuit designed for controllable electronic ballasts. “Ballast” is a device or circuit used to provide the required starting voltage and operating current for LED, fluorescent, mercury or other electronic-discharge lamps.

The STLUX385A DALI driver has the following characteristics:

- Improved DALI noise rejection filter (see [Section : DALI noise rejection filter](#))
- Speed line: 1.2, 2.4 and 4.8 kHz transmission rate  $\pm 10\%$
- Forward payload: 16, 17, 18 and 24-bit message length
- Backward payload: 8-bit message length.
- Bidirectional communications
- Monitor receiver line timeout 500 ms  $\pm 10\%$
- Polarity insensitive on DALI\_rx, DALI\_tx signal line
- Interoperability with different message length
- Configurable noise rejection filter on DALI\_rx input line
- Maskable interrupt request line
- DALI peripheral clock has slowed down to 153.6 kHz in low speed operating mode

### DALI noise rejection filter

The STLUX385A DALI interface includes a noise rejection filter interconnected on the RX channel capable to remove any bounce, glitch or spurious pulse from the RX line. The filter can be configured via three registers:

- MSC\_DALICKSEL: selects the source clock of filter timing
- MSC\_DALICKDIV: configures the clock prescaler value
- MSC\_DALICONF: configures the filter count and operating mode.

### 4.7.2 Universal asynchronous receiver/transmitter (UART)

UART is the asynchronous receiver/transmitter communication interface.

- SW flow control operating mode
- Full duplex, asynchronous communications
- High precision baud rate generator system
  - Common programmable transmit and receive baud rates up to  $f_{\text{MASTER}}/16$
- Programmable data word length (8 or 9-bit)
- Configurable stop bit - support for 1 or 2 stop bit
- Configurable parity control
- Separate enable bits for transmitter and receiver
- Interrupt sources:
  - Transmit events
  - Receive events
  - Error detection flags
- 2 interrupt vectors:
  - Transmitter interrupt
  - Receiver interrupt
- Reduced power consumption mode
- Wakeup from mute mode (by idle line detection or address mark detection)
- 2 receiver wakeup modes:
  - Address bit (MSB)
  - Idle line.



### 4.7.3 Inter-integrated circuit interface (I<sup>2</sup>C)

The I<sup>2</sup>C (inter-integrated circuit) bus interface serves as an interface between the microcontroller and the serial I<sup>2</sup>C bus. It provides a multi-master capability, and controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing. It supports standard and fast speed modes.

- Parallel-bus/I<sup>2</sup>C protocol converter
- Multi-master capability: the same interface can act as master or slave
- I<sup>2</sup>C master features:
  - Clock generation
  - Start and stop generation
- I<sup>2</sup>C slave features:
  - Programmable I<sup>2</sup>C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)
- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I<sup>2</sup>C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgment failure after address/ data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled
- Interrupt sources:
  - Communication interrupt
  - Error condition interrupt
  - Wakeup from Halt interrupt
- Wakeup capability:
  - MCU wakes up from low power mode on address detection in slave mode.

## 4.8 Analog-to-digital converter (ADC)

The STLUX385A device includes a 10-bit successive approximation ADC with 8 multiplexed input channels. The analog input signal can be amplified before conversion by a selectable gain of 1 or 4 times. The analog-to-digital converter can operate either in single or in continuous/circular modes. The ADC unit has the following main features:

- 8 ADC input channel
- 10-bit resolution
- Single and continuous conversion mode
- Independent channel gain value x 1 or x 4 to extend dynamic range and resolution to 12-bit equivalent
- Interrupt events:
  - EOC interrupt asserted on end of conversion cycle
  - EOS interrupt asserted on end of conversion sequences
  - SEQ\_FULL\_EN interrupt assert on sequencer buffer full
- ADC input voltage range dependent on selected gain value
- Selectable conversion data alignment
- Individual registers for up to 8 successive conversions.

## 4.9 Analog comparators

The STLUX385A includes four independent fast analog comparator units (COMP3-0). Each comparator has an internal reference voltage. The COMP3 can be also configured to use an external reference voltage connected to the CPM3 input pin.

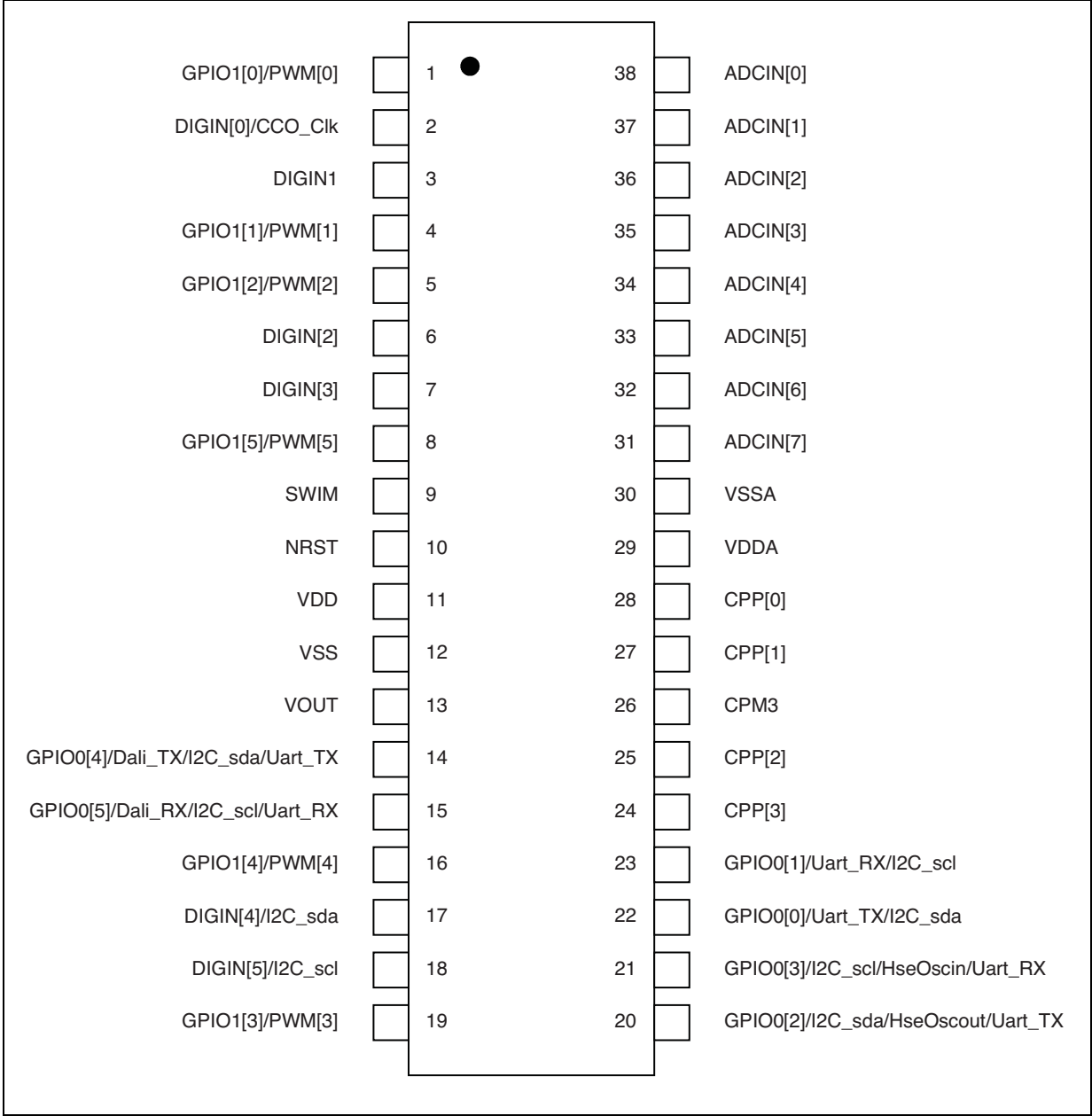
Each comparator reference voltage is generated by a dedicated internal-only 4-bit DAC unit. The main characteristics of the analog comparator unit (ACU) are the following:

- Each comparator has an internally configurable reference
- Internal reference voltages configurable in 16 steps with 83 mV voltage grain from 0 V (GND) to 1.24 V (voltage reference)
- Two stage comparator architecture is used to reach a high gain
- Comparator output stage value accessible from processor interface
- Continuous fast cycle comparison time.

5 Pinout and pin description

5.1 Pinout

Figure 6. TSSOP38 pinout



## 5.2 Pin description

Table 2. Pin description

| Pin number | Type | Pin name   | Main function                | Alternate function 1                   | Alternate function 2             | Alternate function 3 |
|------------|------|--|------------------------------|--|----------------------------------|----------------------|
| 1          | I/O  | GPIO1[0]/PWM[0]                                      | SMED PWM channel 0           | General purpose I/O 10                 | -                                | -                    |
| 2          | I/O  | DIGIN[0]/CCO_clk                                     | Digital input 0              | Configurable clock output signal (CCO) | -                                | -                    |
| 3          | I    | DIGIN[1]   | Digital input 1              | -                                      | -                                | -                    |
| 4          | I/O  | GPIO1[1]/PWM [1]                                     | SMED PWM channel 1           | General purpose I/O 11                 | -                                | -                    |
| 5          | I/O  | GPIO1 [2]/PWM [2]                                    | SMED PWM channel 2           | General purpose I/O 12                 | -                                | -                    |
| 6          | I    | DIGIN [2]  | Digital input 2              | -                                      | -                                | -                    |
| 7          | I    | DIGIN [3]  | Digital input 3              | -                                      | -                                | -                    |
| 8          | I/O  | GPIO1 [5]/PWM [5]                                    | SMED PWM channel 5           | General purpose I/O 15                 | -                                | -                    |
| 9          | I/O  | SWIM   | SWIM data interface          | -                                      | -                                | -                    |
| 10         | I/O  | NRST   | Reset                        | -                                      | -                                | -                    |
| 11         | PS   | VDD  | Digital and I/O power supply | -                                      | -                                | -                    |
| 12         | PS   | VSS  | Digital and I/O ground       | -                                      | -                                | -                    |
| 13         | PS   | VOUT   | 1.8 V regulator capacitor    | -                                      | -                                | -                    |
| 14         | I/O  | GPIO0 [4]/DALI_tx                                    | General purpose I/O 04       | DALI data transmit                     | -                                | -                    |
| 15         | I/O  | GPIO0 [5]/DALI_rx                                    | General purpose I/O 05       | DALI data receive                      | -                                | -                    |
| 16         | I/O  | GPIO1 [4]/PWM[4]                                     | SMED PWM channel 4           | General purpose I/O 14                 | -                                | -                    |
| 17         | I    | DIGIN [4]  | Digital input 4              | -                                      | -                                | -                    |
| 18         | I    | DIGIN [5]  | Digital input 5              | -                                      | -                                | -                    |
| 19         | I/O  | GPIO1[3]/PWM[3]                                      | SMED PWM channel 3           | General purpose I/O 13                 | -                                | -                    |
| 20         | I/O  | GPIO0 [2]/I <sup>2</sup> C_sda/<br>HseOscout/UART_tx | General purpose I/O 02       | I <sup>2</sup> C data                  | Output crystal oscillator signal | UART data transmit   |

Table 2. Pin description (continued)

| Pin number | Type | Pin name  | Main function                         | Alternate function 1   | Alternate function 2   | Alternate function 3 |
|------------|------|---|---------------------------------------|------------------------|--|----------------------|
| 21         | I/O  | GPIO0 [3]/I <sup>2</sup> C_scl/<br>HseOscin/UART_rx | General purpose<br>I/O 03             | I <sup>2</sup> C clock | Input crystal<br>oscillator<br>signal/input<br>frequency<br>signal | UART data<br>receive |
| 22         | I/O  | GPIO0 [0]<br>/UART_tx/I <sup>2</sup> C_scl          | General purpose<br>I/O 00             | UART data<br>transmit  | -  | -                    |
| 23         | I/O  | GPIO0 [1]<br>/UART_rx/I <sup>2</sup> C_scl          | General purpose<br>I/O 01             | UART data<br>receive   | -  | -                    |
| 24         | I    | CPP[3]  | Positive analog<br>comparator input 3 | -                      | -  | -                    |
| 25         | I    | CPP[2]  | Positive analog<br>comparator input 2 | -                      | -  | -                    |
| 26         | I    | CPM3  | Negative analog<br>comparator input 3 | -                      | -  | -                    |
| 27         | I    | CPP[1]  | Positive analog<br>comparator input 1 | -                      | -  | -                    |
| 28         | I    | CPP[0]  | Positive analog<br>comparator input 0 | -                      | -  | -                    |
| 29         | PS   | VDDA  | Analog power<br>supply                | -                      | -  | -                    |
| 30         | PS   | VSSA  | Analog ground                         | -                      | -  | -                    |
| 31         | I    | ADCIN [7]   | Analog input 7                        | -                      | -  | -                    |
| 32         | I    | ADCIN [6]   | Analog input 6                        | -                      | -  | -                    |
| 33         | I    | ADCIN [5]   | Analog input 5                        | -                      | -  | -                    |
| 34         | I    | ADCIN [4]   | Analog input 4                        | -                      | -  | -                    |
| 35         | I    | ADCIN [3]   | Analog input 3                        | -                      | -  | -                    |
| 36         | I    | ADCIN [2]   | Analog input 2                        | -                      | -  | -                    |
| 37         | I    | ADCIN [1]   | Analog input 1                        | -                      | -  | -                    |
| 38         | I    | ADCIN [0]   | Analog input 0                        | -                      | -  | -                    |

### 5.3 Input/output specifications

The STLUX385A device includes two different I/O types:

- Normal I/Os configurable either at 2 or 10 MHz (high sink)
- Fast I/O operating at 12 MHz.

The STLUX385A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA; further details are available in [Section 11 on page 68](#).

## 6 I/O multifunction signal configuration

Several I/Os have multiple functionalities selectable through the configuration mechanism described in [Section 6.1](#) and [Section 6.2](#). The STLUX385A I/Os are grouped into three different configurable ports: P0, P1 and P2.

### 6.1 Multifunction configuration policy

The STLUX385A supports either a cold or warm multifunction signal configuration policy according to the content of the EN\_COLD\_CFG bit field, a part of the GENCFG option byte register.

When EN\_COLD\_CFG bit is set, the cold configuration is selected and the multifunction signals are configured according to the values stored in the option bytes; otherwise when the EN\_COLD\_CFG bit is cleared (default case), the warm configuration mode is chosen and the multifunction pin functionality is configured through the miscellaneous registers.

The configuration options and the proper configuration registers are detailed in [Table 3](#):

**Table 3. Multifunction configuration registers**

| EN_COLD_CFG | Configuration policy | Multifunction configuration registers    |
|-------------|----------------------|--|
| 1           | Cold                 | AFR_IOMXP0, AFR_IOMXP1 and AFR_IOMXP2    |
| 0 (default) | Warm                 | MISC_IOMXP0, MISC_IOMXP1 and MISC_IOMXP2 |

The warm configuration is volatile, thus not maintained after a device reset.

### 6.2 Port P0 I/O multifunction configuration signal

The Port P0 multiplexes several input/output functionalities, increasing the device flexibility. The P0 port pins can be independently assigned to general purpose I/Os or to internal peripherals. All communication peripherals and the external oscillator are hosted by the Port P0 pins.

In order to avoid electrical conflicts on the user application board, the P0 signals are configured at reset as GPIO0 [5:0] inputs without pull-up resistors. Once reset is released, the firmware application must initialize the inputs with the proper configuration according to the application needs.

#### 6.2.1 Alternate function P0 configuration signals

The multifunction pins can be configured via one of the following two registers, depending on the overall configuration policy (warm/cold):

- Cold configuration: AFR\_IOMXP0 option byte registers (refer to [Section 9 on page 53](#)). After reset the P0 signals are configured in line with AFR\_IOMXP0 contents.
- Warm configuration: MISC\_IOMXP0 miscellaneous register (refer to [Section 6.5 on page 35](#)). After reset, the P0 signals are configured as GPIO input lines with pull-up disabled.

[Table 4](#) summarizes the Port P0 configuration scheme. Both registers MSC\_IOMXP0 and AFR\_IOMXP0 use the same register fields Sel\_p054, Sel\_p032 and Sel\_p010 which respectively control the bits [5, 4], [3, 2] and [1, 0] of the Port P0.

**Table 4. P0 internal multiplexing signals**

| Port P0 multifunction configuration signal |                       |                      |                  |                |
|--|-----------------------|----------------------|------------------|----------------|
| Port pins                                  | Multifunction signal  |                      | Mux sel          |                |
|  |                       |                      | Selection fields | Value (binary) |
| P0[1,0]                                    | GPIO0 [1]             | GPIO0 [0]            | Sel_p010         | 00             |
|  | UART_rx               | UART_tx              |                  | 01             |
|  | I <sup>2</sup> C_scl  | I <sup>2</sup> C_sda |                  | 10             |
|  | RFU Reserved encoding |                      |                  | 11             |
| P0[3,2]                                    | GPIO0 [3]             | GPIO0 [2]            | Sel_p032         | 00             |
|  | I <sup>2</sup> C_scl  | I <sup>2</sup> C_sda |                  | 01             |
|  | HseOscin              | HseOscout            |                  | 10             |
|  | UART_rx               | UART_tx              |                  | 11             |
| P0[5,4]                                    | GPIO0[5]              | GPIO0[4]             | Sel_p054         | 00             |
|  | DALI_rx               | DALI_tx              |                  | 01             |
|  | I <sup>2</sup> C_scl  | I <sup>2</sup> C_sda |                  | 10             |
|  | UART_rx               | UART_tx              |                  | 11             |

*Note:* Sel\_p054, Sel\_p032, Sel\_p010 are register fields for both registers MSC\_IOMXP0 and AFR\_IOMXP0.

*The peripheral conflict (same resources selected on different pins at the same time) has to be prevented by SW configuration.*

*When the I<sup>2</sup>C interface is selected either on GPIO0 [5:4] or on GPIO0 [3:2] signals the related I/O port speed has to be configured at 10 MHz by programming the GPIO0 internal peripheral.*

## 6.2.2 Port P0 diagnostic signals

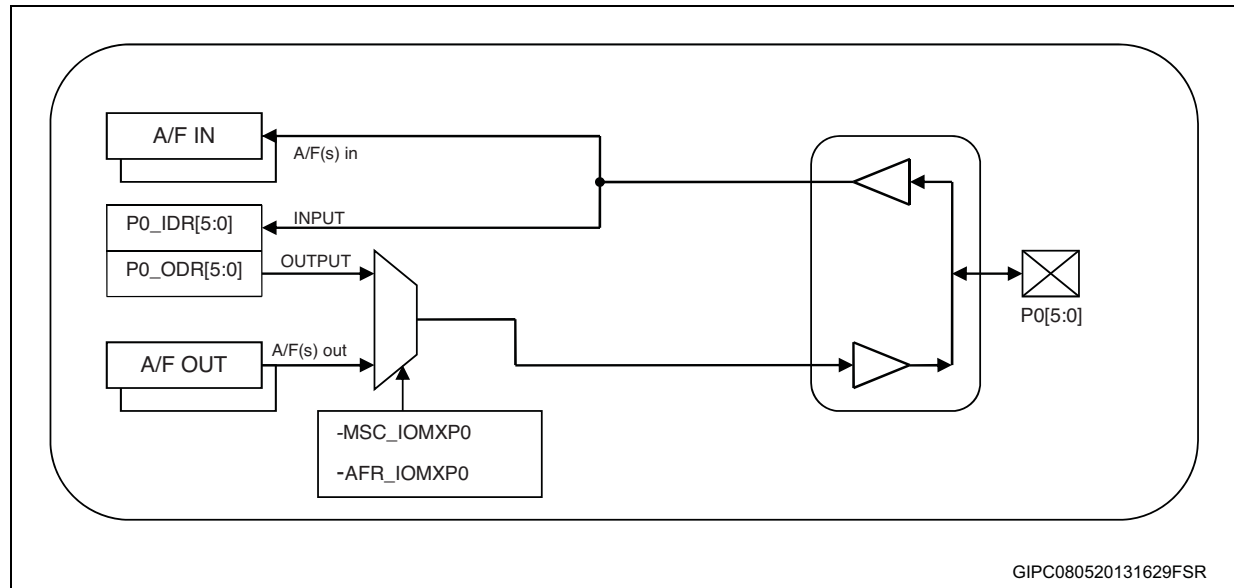
The primary I/Os can be used to trace the SMED's state evolution. This feature allows the debug of the complex SMED configurations. The trace selection can be enabled or disabled via register MSC\_IOMXSMD. The diagnostic signal selection through MSC\_IOMXSMD register overrides the functional configuration of MSC\_IOMXP0 register.

The Port P0 [5:3] or P0 [2:0] can be configured to output one or two different SMEDs' current state.

### 6.2.3 Port P0 I/O functional multiplexing signal

Figure 7 shows an outline view of the Port P0 multifunction multiplexing scheme.

Figure 7. Port P0 I/O functional multiplexing scheme



Note: Where “A/F(s) in” and “A/F(s) out” signals are defined in [Section 5.2 on page 28](#).

### 6.2.4 P0 programmable pull-up and speed feature

The I/O speed and pad pull-up resistance (47 kΩ) of the port P0 may be configured through the GPIO0 internal registers.

## 6.3 Port P1 I/O multifunction configuration signal

The Port1 I/O multifunction pins, similarly to the Port0, can be individually configured through the following set of registers based on the selected device configuration policy:

- Cold configuration: AFR\_IOMXP1 option byte register (refer to [Section 9 on page 53](#)). After reset the P1 signals are configured in line with AFR\_IOMXP1 contents.
- Warm configuration: MISC\_IOMXP1 miscellaneous register (refer to [Section 6.5 on page 35](#)). After reset the P1 signals are configured as PWM output lines.

Every Port1 I/O can be configured to operate as a PWM output pin or a GPIO. Differently from port P0s, the pins are configured as PWM output signals by default after reset.

[Table 5](#) summarizes the Port P1 configurations as selected by the register fields Sel\_p15 ... Sel\_p10 which respectively control the bits [5] ... [0] of the Port P1.



Table 5. Port P1 I/O multiplexing signal

| Port P1 multifunction configuration signal |                       |                |                |
|--|-----------------------|----------------|----------------|
| Output signal                              | Multi-function signal | Mux selection  |                |
|  |                       | Selection bits | Value (binary) |
| P1[0]                                      | PWM[0]                | Sel_p10        | 1              |
|  | GPIO1[0]              |                | 0              |
| P1[1]                                      | PWM[1]                | Sel_p11        | 1              |
|  | GPIO1[1]              |                | 0              |
| P1[2]                                      | PWM[2]                | Sel_p12        | 1              |
|  | GPIO1[2]              |                | 0              |
| P1[3]                                      | PWM[3]                | Sel_p13        | 1              |
|  | GPIO1[3]              |                | 0              |
| P1[4]                                      | PWM[4]                | Sel_p14        | 1              |
|  | GPIO1[4]              |                | 0              |
| P1[5]                                      | PWM[5]                | Sel_p15        | 1              |
|  | GPIO1[5]              |                | 0              |

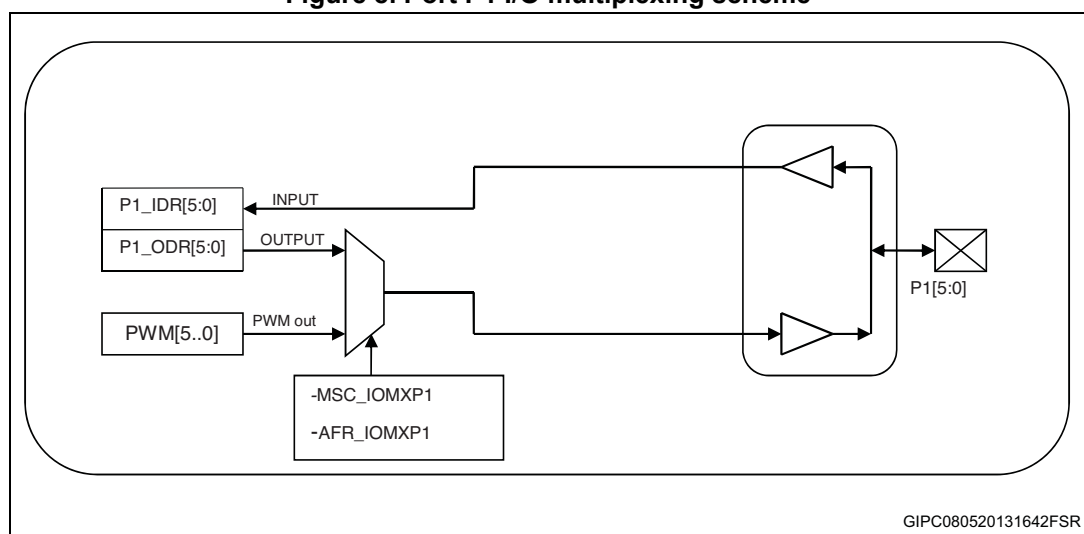
Note: Sel\_p15...Sel\_p10 are common register fields of both registers MISC\_IOMUXP1 and AFR\_IOMUXP1.

The PWM default polarity level is configured by the register option byte GENCFG.

### 6.3.1 Port P1 I/O multiplexing signal

Figure 8 shows an outline view of the port P1 signal multiplex scheme.

Figure 8. Port P1 I/O multiplexing scheme



**Note:** The P1[5:0] output signals may be read back from the P1\_IDR register only when the pins are configured as GPIO out or PWM signals.

The PWM internal signal is read-back also by the its own SMED through the SMD<n>\_FSM\_STS register

### 6.3.2 P1 programmable pull-up feature

The pad pull-up resistances (47 kΩ) of Port1 may be configured through the GPIO1 internal register.

## 6.4 Port P2 I/O multifunction configuration signal

The Port2 I/O multifunction pins, similarly to Port0 and Port2, can be individually configured through the following set of registers based on the selected device configuration policy:

- Cold configuration: AFR\_IOMXP2 option byte registers (refer to [Section 9 on page 53](#)). After reset the P2 signals are configured in line with AFR\_IOMXP2 contents.
- Warm configuration: MISC\_IOMXP2 miscellaneous register (refer to [Section 6.5](#)). After reset the P2 signals are configured as DIGIN input lines with pull-up enabled.

The following table summarizes the port P2 configurations selected by the register fields Sel\_p25...Sel\_p20 which respectively control the bits [5]...[0] of port P2.

**Table 6. Port P2 I/O multiplexing signal**

| Port P2 multifunction configuration signal |                       |                |                |
|--|-----------------------|----------------|----------------|
| Output signal                              | Multi-function signal | Mux sel        |                |
|  |                       | Selection bits | Value (binary) |
| P2[0]                                      | DIGIN[0]              | CCOEN          | 0              |
|  | CCO                   |                | 1              |
| P2[4]                                      | DIGIN[4]              | Sel_p254       | 1              |
|  | I <sup>2</sup> C_sda  |                | 0              |
| P2[5]                                      | DIGIN[5]              | Sel_p254       | 1              |
|  | I <sup>2</sup> C_scl  |                | 0              |

**Note:** Sel\_p254 is a common register field of both registers MSC\_IOMXP2 and AFR\_IOMXP2.

The peripheral conflict (same resources selected on different pins at the same time) has to be prevented by SW configuration.

The option byte AFR\_IOMXP2 before user configuration by default selects the I<sup>2</sup>C alternative functionality.

The signal ports P2[3:1] are exclusively interconnected with DIGIN[3:1] primary pins.

When the I<sup>2</sup>C i/f is selected on DIGIN[5:4] signals the I/O speed is auto-configured at 10 MHz and the internal pull-up functionality is controlled by the MSC\_INPP2AUX1 register.

The P2[0] signal for backward product compatibility is only controlled by field CCOEN of CKC\_CCOR register as shown in [Table 6](#).

### 6.4.1 P2 programmable pull-up feature

The pad pull-up resistances (47 kΩ) of Port2 signals are individually controllable by the MSC\_INPP2AUX1 register.

## 6.5 Multifunction Port configuration registers

### MSC\_IOMXP0 (Port P1 I/O mux control register)

Table 7. MSC\_IOMXP0 (Port P1 I/O mux control register)

|                     |   |                |   |                |   |                |   |
|---------------------|---|----------------|---|----------------|---|----------------|---|
| Offset: 0x2A        |   |                |   |                |   |                |   |
| Default value: 0x00 |   |                |   |                |   |                |   |
| 7                   | 6 | 5              | 4 | 3              | 2 | 1              | 0 |
| RFU                 |   | Sel_p054 [1:0] |   | Sel_p032 [1:0] |   | Sel_p010 [1:0] |   |
| r                   |   | r/w            |   | r/w            |   | r/w            |   |

The Port0 I/O multifunction signal configurations register (for functionality description refer to [Section 6.2 on page 30](#)).

Bit 1 - 0:

Sel\_p010 [1:0] Port0 [1:0] I/O multiplexing scheme:

00: Port0 [1:0] are interconnected to GPIO0 [1:0] signals

01: Port0 [1:0] are interconnected to UART\_rx and UART\_tx signals

10: Port0 [1:0] are interconnected to I<sup>2</sup>C\_scl and I<sup>2</sup>C\_sda signals

11: RFU

Bit 3 - 2:

Sel\_p032 [1:0] Port0 [3:2] I/O multiplexing scheme:

00: Port0 [3:2] are interconnected to GPIO0 [3:2] signals

01: Port0 [3:2] are interconnected to I<sup>2</sup>C\_scl and I<sup>2</sup>C\_sda signals

10: Port0 [3:2] are interconnected to HseOscin and HseOscout analog signals

11: Port0 [3:2] are interconnected to UART\_rx and UART\_tx signals

Bit 5 - 4:

Sel\_p054 [1:0] Port0 [5:4] I/O multiplexing scheme:

00: Port0 [5:4] are interconnected to GPIO0 [5:4] signals

01: Port0 [5:4] are interconnected to DALI\_rx and DALI\_tx signals

10: Port0 [5:4] are interconnected to I<sup>2</sup>C\_scl and I<sup>2</sup>C\_sda signals

11: Port0 [5:4] are interconnected to UART\_rx and UART\_tx signals

Bit 7 - 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

**MSC\_IOMUXP1 (Port P1 I/O mux control register)****Table 8. MSC\_IOMUXP1 (Port P1 I/O mux control register)**

|                            |   |         |         |         |         |         |         |
|----------------------------|---|---------|---------|---------|---------|---------|---------|
| <b>Offset: 0x2B</b>        |   |         |         |         |         |         |         |
| <b>Default value: 0x3F</b> |   |         |         |         |         |         |         |
| 7                          | 6 | 5       | 4       | 3       | 2       | 1       | 0       |
| RFU                        |   | Sel_p15 | Sel_p14 | Sel_p13 | Sel_p12 | Sel_p11 | Sel_p10 |
| r                          |   | r/w     |         |         |         |         |         |

The Port1 I/O multifunction signal configuration register (for functionality description refer to [Section 6.3 on page 32](#)).

Bit 0:

Sel\_p10 Port1 [0] I/O multiplexing scheme:

0: Port1 [0] is interconnected to GPIO1 [0] signal

1: Port1 [0] is interconnected to PWM [0] signal

Bit 1:

Sel\_p11 Port1 [1] I/O multiplexing scheme:

0: Port1 [1] is interconnected to GPIO1 [1] signal

1: Port1 [1] is interconnected to PWM [1] signal

Bit 2:

Sel\_p12 Port1 [2] I/O multiplexing scheme:

0: Port1 [2] is interconnected to GPIO1 [2] signal

1: Port1 [2] is interconnected to PWM [2] signal

Bit 3:

Sel\_p13 Port1 [3] I/O multiplexing scheme:

0: Port1 [3] is interconnected to GPIO1 [3] signal

1: Port1 [3] is interconnected to PWM [3] signal

Bit 4:

Sel\_p14 Port1 [4] I/O multiplexing scheme:

0: Port1 [4] is interconnected to GPIO1 [4] signal

1: Port1 [4] is interconnected to PWM [4] signal

Bit 5:

Sel\_p15 Port1 [5] I/O multiplexing scheme:

0: Port1[5] is interconnected to GPIO1 [5] signal

1: Port1 [5] is interconnected to PWM [5] signal

Bit 7 - 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

**MSC\_IOMUXP2 (Port P2 I/O mux control register)****Table 9. MSC\_IOMUXP2 (Port P2 I/O mux control register)**

|                                     |   |   |          |     |   |   |   |
|-------------------------------------|---|---|----------|-----|---|---|---|
| <b>Offset: 0x13 (indirect area)</b> |   |   |          |     |   |   |   |
| <b>Default value: 0xFF</b>          |   |   |          |     |   |   |   |
| 7                                   | 6 | 5 | 4        | 3   | 2 | 1 | 0 |
| RFU                                 |   |   | Sel_p254 | RFU |   |   |   |
| r                                   |   |   | r/w      | r   |   |   |   |

The Port1 I/O multifunction signal configurations register (for functionality description refer to [Section 6.4 on page 34](#)).

Bit 3 - 0:

RFU reserved; must be kept 0 during register writing for future compatibility

Bit 4:

Sel\_p254 Port2 [5:4] I/O multiplexing scheme:

0: Port2 [5:4] are interconnected to I<sup>2</sup>C\_scl and I<sup>2</sup>C\_sda signals

1: Port2 [5:4] are interconnected to DIGIN [5:4] signals

Bit 7 - 5:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

**MSC\_INPP2AUX1 (INPP aux register)****Table 10. MSC\_INPP2AUX1 (INPP aux register)**

|                            |   |                    |   |   |   |   |   |
|----------------------------|---|--------------------|---|---|---|---|---|
| <b>Offset: 0x08</b>        |   |                    |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |                    |   |   |   |   |   |
| 7                          | 6 | 5                  | 4 | 3 | 2 | 1 | 0 |
| RFU                        |   | INPP2_PULCTR [5:0] |   |   |   |   |   |
| r                          |   | r/w                |   |   |   |   |   |

Bit 5 - 0:

INPP2\_PULCTR [5:0] .This register configures respectively the INPP2 [5:0] pull-up functionality as follows:

0: enable pad pull-up features (enabled by default for compatibility with the STLUX385)

1: disable pad pull-up

Bit 7 - 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

**Note:** *MSC\_IOMUXP2 and MSC\_INPP2AUX1 are addressable in indirect mode.*

## 7 Memory and register map

### 7.1 Memory map overview

This section describes the register map implemented by the STLUX385A device. [Table 11](#) shows the main memory map organization. All registers and memory spaces are configured within the first 64 Kbytes of memory, the remaining address spaces are kept reserved for future use.

**Table 11. Internal memory map**

| Address              | Description                   |
|----------------------|-------------------------------|
| 00.0000h             | 2 kB RAM                      |
| 00.07FFh             | Stack                         |
| 00.0800h<br>00.3FFFh | Reserved                      |
| 00.4000h<br>00.43FFh | 1 kB data E <sup>2</sup> PROM |
| 00.4400h<br>00.47FFh | Reserved                      |
| 00.4800h<br>00.487Fh | 128 option bytes              |
| 00.4880h<br>00.4FFFh | Reserved                      |
| 00.5000h<br>00.57FFh | Peripheral register region    |
| 00.5800h<br>00.5FFFh | Reserved                      |
| 00.6000h<br>00.67FFh | 2 kB boot ROM                 |
| 00.6800h<br>00.7EFFh | Reserved                      |
| 00.7F00h<br>00.7FFFh | Core register region          |

Table 11. Internal memory map (continued)

| Address  | Description          |
|----------|----------------------|
| 00.8000h | 32 interrupt vectors |
| 00.8080h | 32 kB program Flash  |
| 00.FFFFh |                      |
| 01.0000h | Reserved             |
| FF.FFFFh |                      |

By default the stack address is initialized at 0x07FF and rolls over when it reaches the address value of 0x0400.

## 7.2 Register map

[Section 7.2.1](#) shows the STLUX385A memory map.

### 7.2.1 General purpose I/O GPIO0 register map

Table 12. General purpose I/O GPIO0 register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.5000 | GPIO0 | P0_ODR        | Output data          |
| 0x00.5001 |       | P0_IDR        | Input data           |
| 0x00.5002 |       | P0_DDR        | Data direction       |
| 0x00.5003 |       | P0_CR1        | Control register 1   |
| 0x00.5004 |       | P0_CR2        | Control register 2   |

### 7.2.2 General purpose I/O GPIO1 register map

Table 13. General purpose I/O GPIO0 register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.5005 | GPIO1 | P1_ODR        | Output data          |
| 0x00.5006 |       | P1_IDR        | Input data           |
| 0x00.5007 |       | P1_DDR        | Data direction       |
| 0x00.5008 |       | P1_CR1        | Control register 1   |
| 0x00.5009 |       | P1_CR2        | Control register 2   |

### 7.2.3 Miscellaneous registers

#### Direct register address mode

Table 14. Miscellaneous direct register address mode

| Address   | Block | Register name | Register description                   |
|-----------|-------|---------------|--|
| 0x00.5010 | MSC   | MSC_CFGP00    | P00 input line control                 |
| 0x00.5011 |       | MSC_CFGP01    | P01 input line control                 |
| 0x00.5012 |       | MSC_CFGP02    | P02 input line control                 |
| 0x00.5013 |       | MSC_CFGP03    | P03 input line control                 |
| 0x00.5014 |       | MSC_CFGP04    | P04 input line control                 |
| 0x00.5015 |       | MSC_CFGP05    | P05 input line control                 |
| 0x00.5016 |       | MSC_CFGP20    | P20 input line control                 |
| 0x00.5017 |       | MSC_CFGP21    | P21 input line control                 |
| 0x00.5018 |       | MSC_CFGP22    | P22 input line control                 |
| 0x00.5019 |       | MSC_CFGP23    | P23 input line control                 |
| 0x00.501A |       | MSC_CFGP24    | P24 input line control                 |
| 0x00.501B |       | MSC_CFGP25    | P25 input line control                 |
| 0x00.501C |       | MSC_STSP0     | Port0 status                           |
| 0x00.501D |       | MSC_STSP2     | Port2 status                           |
| 0x00.501E |       | MSC_INPP2     | Port2 read                             |
| 0x00.501F |       | RFU           | Reserved for future use                |
| 0x00.5020 |       | MSC_DACCTR    | Comparator4 and DAC4 configuration     |
| 0x00.5021 |       | MSC_DACIN0    | DAC0 input data                        |
| 0x00.5022 |       | MSC_DACIN1    | DAC1 input data                        |
| 0x00.5023 |       | MSC_DACIN2    | DAC2 input data                        |
| 0x00.5024 |       | MSC_DACIN3    | DAC3 input data                        |
| 0x00.5025 |       | MSC_SMDCFG01  | SMED 0 - 1 behavior                    |
| 0x00.5026 |       | MSC_SMDCFG23  | SMED 2 - 3 behavior                    |
| 0x00.5027 |       | MSC_SMDCFG45  | SMED 4 - 5 behavior                    |
| 0x00.5028 |       | MSC_SMSWEV    | SMED software events                   |
| 0x00.5029 |       | MSC_SMUNLOCK  | SMED unlock                            |
| 0x00.502A |       | MSC_CBOXS0    | Connection matrix selection for SMED 0 |



## Indirect register address mode

Table 15. Miscellaneous indirect register address mode

| Address (IDX) | Block | Register name | Register description                     |
|---------------|-------|---------------|--|
| 0x00 – 0x04   | MSC   | RFU           | Reserved for future use                  |
| 0x05          |       | MSC_DALICKSEL | DALI clock selection                     |
| 0x06          |       | MSC_DALICKDIV | DALI filter clock division factor        |
| 0x07          |       | MSC_DALICONF  | DALI filter mode configuration           |
| 0x08          |       | MSC_INPP2AUX1 | INPP2 auxiliary configuration register 1 |
| 0x09          |       | MSC_INPP2AUX2 | INPP2 auxiliary configuration register 2 |
| 0x0A – 0x12   |       | RFU           | Reserved for future use                  |
| 0x13          |       | MSC_IOMXP2    | Port2 alternate function mux register    |

7.2.4 Flash and E<sup>2</sup>PROM non-volatile memories

Table 16. Non-volatile memory register map

| Address   | Block | Register name | Register description                     |
|-----------|-------|---------------|--|
| 0x00.505A | MIF   | FLASH_CR1     | Control register 1                       |
| 0x00.505B |       | FLASH_CR2     | Control register 2                       |
| 0x00.505C |       | FLASH_nCR2    | Control register 2 (protection)          |
| 0x00.505D |       | FLASH_FPR     | Memory protection                        |
| 0x00.505E |       | FLASH_nFPR    | Memory protection (complemented reg.)    |
| 0x00.505F |       | FLASH_IAPSR   | Flash status                             |
| 0x00.5062 |       | FLASH_PUKR    | Write memory protection removal key reg. |
| 0x00.5063 |       | RFU           | Reserved for future use                  |
| 0x00.5064 |       | FLASH_DUKR    | Write memory protection removal data     |
| 0x00.5071 |       | FLASH_WAIT    | Time access wait-state reg.              |

## 7.2.5 Reset register

Table 17. RST\_SR register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.50B3 | RSTC  | RST_SR        | Reset control status |

## 7.2.6 Clock and clock controller

Table 18. Clock and clock controller register map

| Address   | Block | Register name | Register description       |
|-----------|-------|---------------|----------------------------|
| 0x00.50B4 | CKC   | CLK_SMD0      | SMED 0 clock configuration |
| 0x00.50B5 |       | CLK_SMD1      | SMED 1 clock configuration |
| 0x00.50B6 |       | CLK_SMD2      | SMED 2 clock configuration |
| 0x00.50B7 |       | CLK_SMD3      | SMED 3 clock configuration |
| 0x00.50B8 |       | CLK_SMD4      | SMED 4 clock configuration |
| 0x00.50B9 |       | CLK_SMD5      | SMED 5 clock configuration |
| 0x00.50BA |       | RFU           | Reserved for future use    |
| 0x00.50BB |       | RFU           | Reserved for future use    |
| 0x00.50BC |       | RFU           | Reserved for future use    |
| 0x00.50BD |       | RFU           | Reserved for future use    |
| 0x00.50BE |       | CLK_PLLDIV    | PLL clock divisor          |
| 0x00.50BF |       | CLK_AWUDIV    | AWU clock divisor          |
| 0x00.50C0 |       | CLK_ICKR      | Internal clock control     |
| 0x00.50C1 |       | CLK_ECKR      | External clock control     |
| 0x00.50C2 |       | CLK_PLLR      | PLL control                |
| 0x00.50C3 |       | CLK_CMSR      | Clock master               |
| 0x00.50C4 |       | CLK_SWR       | Clock switch               |
| 0x00.50C5 |       | CLK_SWCR      | Switch control             |
| 0x00.50C6 |       | CLK_CKDIVR    | Clock dividers             |
| 0x00.50C7 |       | CLK_PCKENR1   | Peripherals clock          |
| 0x00.50C8 |       | CLK_CSSR      | Clock security system      |
| 0x00.50C9 |       | CLK_CCOR      | Configurable clock output  |
| 0x00.50CA |       | CLK_PCKENR2   | Peripheral clock enable    |
| 0x00.50CB |       | RFU           | Reserved for future use    |
| 0x00.50CC |       | CLK_HSTRIMR   | HSI calibration trimmer    |
| 0x00.50CD |       | CLK_SWIMCCR   | SWIM clock division        |
| 0x00.50CE |       | CLK_CCODIVR   | CCO divider                |
| 0x00.50CF |       | CLK_ADCR      | ADC clock configuration    |

### 7.2.7 WWDG timers

Table 19. WWDG timer register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.50D1 | WWDG  | WWDG_CR       | Watchdog control     |
| 0x00.50D2 |       | WWDG_WR       | Watchdog window      |

### 7.2.8 IWDG timers

Table 20. IWDG timer register map

| Address   | Block | Register name | Register description                |
|-----------|-------|---------------|-------------------------------------|
| 0x00.50E0 | IWDG  | IWDG_KR       | Watchdog key                        |
| 0x00.50E1 |       | IWDG_PR       | Watchdog time base                  |
| 0x00.50E2 |       | IWDG_RLR      | Watchdog counter value after reload |

### 7.2.9 AWU timers

Table 21. AWU timer register map

| Address   | Block | Register name | Register description              |
|-----------|-------|---------------|-----------------------------------|
| 0x00.50F0 | AWU   | AWU_CSR       | AWU control status                |
| 0x00.50F1 |       | AWU_APR       | AWU asynchronous prescaler buffer |
| 0x00.50F2 |       | AWU_TBR       | AWU time base selection           |

### 7.2.10 Inter-integrated circuit interface (I<sup>2</sup>C)

Table 22. I<sup>2</sup>C register map

| Address   | Block            | Register name           | Register description                       |
|-----------|------------------|-------------------------|--|
| 0x00.5210 | I <sup>2</sup> C | I <sup>2</sup> C_CR1    | I <sup>2</sup> C control register 1        |
| 0x00.5211 |                  | I <sup>2</sup> C_CR2    | I <sup>2</sup> C control register 2        |
| 0x00.5212 |                  | I <sup>2</sup> C_FREQR  | I <sup>2</sup> C frequency register        |
| 0x00.5213 |                  | I <sup>2</sup> C_OARL   | I <sup>2</sup> C own add-low register      |
| 0x00.5214 |                  | I <sup>2</sup> C_OARH   | I <sup>2</sup> C own add-high register     |
| 0x00.5215 |                  | RFU                     | Reserved for future use                    |
| 0x00.5216 |                  | I <sup>2</sup> C_DR     | I <sup>2</sup> C data register             |
| 0x00.5217 |                  | I <sup>2</sup> C_SR1    | I <sup>2</sup> C status register 1         |
| 0x00.5218 |                  | I <sup>2</sup> C_SR2    | I <sup>2</sup> C status register 2         |
| 0x00.5219 |                  | I <sup>2</sup> C_SR3    | I <sup>2</sup> C status register 3         |
| 0x00.521A |                  | I <sup>2</sup> C_ITR    | I <sup>2</sup> C interrupt and DMA control |
| 0x00.521B |                  | I <sup>2</sup> C_CCRL   | I <sup>2</sup> C clock control             |
| 0x00.521C |                  | I <sup>2</sup> C_CCRH   | I <sup>2</sup> C clock control             |
| 0x00.521D |                  | I <sup>2</sup> C_TRISER | I <sup>2</sup> C rising edge               |

### 7.2.11 Universal asynchronous receiver/transmitter (UART)

Table 23. UART register map

| Address   | Block | Register name | Register description                                     |
|-----------|-------|---------------|--|
| 0x00.5230 | UART  | UART_SR       | UART status  |
| 0x00.5231 |       | UART_DR       | UART data  |
| 0x00.5232 |       | UART_BRR1     | UART baud rate div mantissa [7:0]                        |
| 0x00.5233 |       | UART_BRR2     | UART baud rate div mantissa [11:8]<br>SCIDIV FRACT [3:0] |
| 0x00.5234 |       | UART_CR1      | UART control register 1                                  |
| 0x00.5235 |       | UART_CR2      | UART control register 2                                  |
| 0x00.5236 |       | UART_CR3      | UART control register 3                                  |
| 0x00.5237 |       | UART_CR4      | UART control register 4                                  |
| 0x00.5238 |       | UART_CR5      | UART control register 5                                  |
| 0x00.5239 |       | UART_GTR      | UART guard time  |
| 0x00.523A |       | UART_PSCR     | SCI1 prescaler   |

### 7.2.12 System timer registers

Table 24. System timer register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.5340 | STMR  | STMR_CR1      | Control register 1   |
| 0x00.5341 |       | STMR_IER      | Interrupt enable     |
| 0x00.5342 |       | STMR_SR1      | Status register 1    |
| 0x00.5343 |       | STMR_EGR      | Event generation     |
| 0x00.5344 |       | STMR_CNTH     | Counter high         |
| 0x00.5345 |       | STMR_CNTL     | Counter low          |
| 0x00.5346 |       | STMR_PSCL     | Prescaler low        |
| 0x00.5347 |       | STMR_ARRH     | Autoreload high      |
| 0x00.5348 |       | STMR_ARRL     | Autoreload low       |

### 7.2.13 Digital addressable lighting interface (DALI)

**Table 25. DALI register map**

| Address   | Block | Register name | Register description          |
|-----------|-------|---------------|-------------------------------|
| 0x00.53C0 | DALI  | DALI_CLK_L    | Data rate control             |
| 0x00.53C1 |       | DALI_CLK_H    | Data rate control             |
| 0x00.53C2 |       | DALI_FB0      | Forward message               |
| 0x00.53C3 |       | DALI_FB1      | Forward message               |
| 0x00.53C4 |       | DALI_FB2      | Forward message               |
| 0x00.53C5 |       | DALI_BD       | Backward message              |
| 0x00.53C6 |       | DALI_CR       | Control                       |
| 0x00.53C7 |       | DALI_CSR      | Control and status register   |
| 0x00.53C8 |       | DALI_CSR1     | Control and status register 1 |
| 0x00.53C9 |       | DALI_REVLN    | Control reverse signal line   |

### 7.2.14 Analog-to-digital converter (ADC)

The ADC\_DATL/H register number <n> is 0 - 7.

Table 26. ADC register map and reset value

| Address   | Block | Register name | Register description       |
|-----------|-------|---------------|----------------------------|
| 0x00.5400 | ADC   | ADC_CFG       | Configuration              |
| 0x00.5401 |       | ADC_SOC       | Start of conversion        |
| 0x00.5402 |       | ADC_IER       | Interrupt enable           |
| 0x00.5403 |       | ADC_SEQ       | Sequencer                  |
| 0x00.5404 |       | ADC_DATL_0    | Low part data 0 converted  |
| 0x00.5405 |       | ADC_DATH_0    | High part data 0 converted |
| 0x00.5406 |       | ADC_DATL_1    | Low part data 1 converted  |
| 0x00.5407 |       | ADC_DATH_1    | High part data 1 converted |
| 0x00.5408 |       | ADC_DATL_2    | Low part data 2 converted  |
| 0x00.5409 |       | ADC_DATH_2    | High part data 2 converted |
| 0x00.540A |       | ADC_DATL_3    | Low part data 3 converted  |
| 0x00.540B |       | ADC_DATH_3    | High part data 3 converted |
| 0x00.540C |       | ADC_DATL_4    | Low part data 4 converted  |
| 0x00.540D |       | ADC_DATH_4    | High part data 4 converted |
| 0x00.540E |       | ADC_DATL_5    | Low part data 5 converted  |
| 0x00.540F |       | ADC_DATH_5    | High part data 5 converted |
| 0x00.5410 |       | ADC_DATL_6    | Low part data 6 converted  |
| 0x00.5411 |       | ADC_DATH_6    | High part data 6 converted |
| 0x00.5412 |       | ADC_DATL_7    | Low part data 7 converted  |
| 0x00.5413 |       | ADC_DATH_7    | High part data 7 converted |
| 0x00.5414 |       | ADC_SR        | Status                     |
| 0x00.5415 |       | ADC_DLYCNT    | SOC delay counter          |

### 7.2.15 State machine event driven (SMEDs)

The SMED<n> address register is:

$$\text{ADD\_REG} = (5500\text{h} + (40\text{h}) * n) + \text{offset}$$

where <n> is the SMED instance number 0 - 5.

Table 27. SMED register map

| Address (offset) | Block   | Register name  | Register description  |
|------------------|---------|----------------|-----------------------|
| 0x00             | SMED<n> | SMD<n>_CTR     | Control               |
| 0x01             |         | SMD<n>_CTR_TMR | Control time          |
| 0x02             |         | SMD<n>_CTR_INP | Control input         |
| 0x03             |         | SMD<n>_CTR_DTR | Dithering             |
| 0x04             |         | SMD<n>_TMR_T0L | Time T0 LSB           |
| 0x05             |         | SMD<n>_TMR_T0H | Time T0 MSB           |
| 0x06             |         | SMD<n>_TMR_T1L | Time T1 LSB           |
| 0x07             |         | SMD<n>_TMR_T1H | Time T1 MSB           |
| 0x08             |         | SMD<n>_TMR_T2L | Time T2 LSB           |
| 0x09             |         | SMD<n>_TMR_T2H | Time T2 MSB           |
| 0x0A             |         | SMD<n>_TMR_T3L | Time T3 LSB           |
| 0x0B             |         | SMD<n>_TMR_T3H | Time T3 MSB           |
| 0x0C             |         | SMD<n>_PRM_ID0 | IDLE state parameter0 |
| 0x0D             |         | SMD<n>_PRM_ID1 | IDLE state parameter1 |
| 0x0E             |         | SMD<n>_PRM_ID2 | IDLE state parameter2 |
| 0x0F             |         | SMD<n>_PRM_S00 | S0 state parameter0   |
| 0x10             |         | SMD<n>_PRM_S01 | S0 state parameter1   |
| 0x11             |         | SMD<n>_PRM_S02 | S0 state parameter2   |
| 0x12             |         | SMD<n>_PRM_S10 | S1 state parameter0   |
| 0x13             |         | SMD<n>_PRM_S11 | S1 state parameter1   |
| 0x14             |         | SMD<n>_PRM_S12 | S1 state parameter2   |
| 0x15             |         | SMD<n>_PRM_S20 | S2 state parameter0   |
| 0x16             |         | SMD<n>_PRM_S21 | S2 state parameter1   |
| 0x17             |         | SMD<n>_PRM_S22 | S2 state parameter2   |
| 0x18             |         | SMD<n>_PRM_S30 | S3 state parameter0   |
| 0x19             |         | SMD<n>_PRM_S31 | S3 state parameter1   |
| 0x1A             |         | SMD<n>_PRM_S32 | S3 state parameter2   |



Table 27. SMED register map (continued)

| Address (offset) | Block   | Register name  | Register description         |
|------------------|---------|----------------|------------------------------|
| 0x1B             | SMED<n> | SMD<n>_CFG     | Timer configuration register |
| 0x1C             |         | SMD<n>_DMP_L   | Counter dump LSB             |
| 0x1D             |         | SMD<n>_DMP_H   | Counter dump MSB             |
| 0x1E             |         | SMD<n>_GSTS    | General status               |
| 0x1F             |         | SMD<n>_IRQ     | Interrupt request register   |
| 0x20             |         | SMD<n>_IER     | Interrupt enable register    |
| 0x21             |         | SMD<n>_ISEL    | External event control       |
| 0x22             |         | SMD<n>_DMP     | Dump enable                  |
| 0x23             |         | SMD<n>_FSM_STS | FSM core status              |

### 7.2.16 CPU register

Table 28. CPU register map

| Address   | Block | Register name | Register description     |
|-----------|-------|---------------|--------------------------|
| 0x00.7F00 | CPU   | A             | Accumulator              |
| 0x00.7F01 |       | PCE           | Program counter extended |
| 0x00.7F02 |       | PCH           | Program counter high     |
| 0x00.7F03 |       | PCL           | Program counter low      |
| 0x00.7F04 |       | XH            | X-index high             |
| 0x00.7F05 |       | XL            | X-index low              |
| 0x00.7F06 |       | YH            | Y-index high             |
| 0x00.7F07 |       | YL            | Y-index low              |
| 0x00.7F08 |       | SPH           | Stack pointer high       |
| 0x00.7F09 |       | SPL           | Stack pointer low        |
| 0x00.7F0A |       | CC            | Code condition           |

*Note:* Register space accessible in debug mode only.

### 7.2.17 Global configuration register

Table 29. CFG\_GCR register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.7F60 | GCR   | CFG_GCR       | Global configuration |

### 7.2.18 Interrupt controller

Table 30. Interrupt software priority register map

| Address   | Block | Register name | Register description             |
|-----------|-------|---------------|----------------------------------|
| 0x00.7F70 | ITC   | ITC_SPR0      | Interrupt SW priority register 0 |
| 0x00.7F71 |       | ITC_SPR1      | Interrupt SW priority register 1 |
| 0x00.7F72 |       | ITC_SPR2      | Interrupt SW priority register 2 |
| 0x00.7F73 |       | ITC_SPR3      | Interrupt SW priority register 3 |
| 0x00.7F74 |       | ITC_SPR4      | Interrupt SW priority register 4 |
| 0x00.7F75 |       | ITC_SPR5      | Interrupt SW priority register 5 |
| 0x00.7F76 |       | ITC_SPR6      | Interrupt SW priority register 6 |
| 0x00.7F77 |       | ITC_SPR7      | Interrupt SW priority register 7 |

### 7.2.19 SWIM control register

Table 31. SWIM register map

| Address   | Block | Register name | Register description |
|-----------|-------|---------------|----------------------|
| 0x00.7F80 | SWIM  | SWIM_CSR      | SWIM control status  |

## 8 Interrupt table

[Table 32](#) shows the STLUX385A internal controller's interrupt.

**Table 32. Interrupt vector exception table**

| Priority | Source block     | Description                    | Wakeup from Halt        | Wakeup from active-halt | Interrupt vector address |
|----------|------------------|--------------------------------|-------------------------|-------------------------|--------------------------|
|          | RESET            | Reset                          | Yes                     | Yes                     | 8000h                    |
|          | TRAP             | Software interrupt             |                         |                         | 8004h                    |
| 0        | NMI              | NMI (not maskable interrupt)   | Yes <sup>(1)</sup>      | Yes <sup>(1)</sup>      | 8008h                    |
| 1        | AWU              | Auto-wakeup from Halt          |                         | Yes                     | 800Ch                    |
| 2        | CKC              | Clock controller               |                         |                         | 8010h                    |
| 3        | PO               | GPIO0[5:0]external interrupts  | Yes                     | Yes                     | 8014h                    |
| 4        | AUXTIM           | Auxiliary timer                |                         |                         | 8018h                    |
| 5        | P2               | DIGIN[5:0] external interrupts | Yes                     | Yes                     | 801Ch                    |
| 6        | SMED0            | SMED-0 control logic           |                         |                         | 8020h                    |
| 7        | SMED1            | SMED-1 control logic           |                         |                         | 8024h                    |
| 8        | RFU              | Reserved for future use        |                         |                         | 8028h                    |
| 9        | RFU              | Reserved for future use        |                         |                         | 802Ch                    |
| 10       | RFU              | Reserved for future use        |                         |                         | 8030h                    |
| 11       | RFU              | Reserved for future use        |                         |                         | 8034h                    |
| 12       | RFU              | Reserved for future use        |                         |                         | 8038h                    |
| 13       | RFU              | Reserved for future use        |                         |                         | 803Ch                    |
| 14       | RFU              | Reserved for future use        |                         |                         | 8040h                    |
| 15       | SMED2            | SMED-2 control logic           |                         |                         | 8044h                    |
| 16       | SMED3            | SMED-3 control logic           |                         |                         | 8048h                    |
| 17       | UART             | Tx complete                    |                         |                         | 804Ch                    |
| 18       | UART             | Receive register DATA FULL     | Indirect <sup>(2)</sup> | Indirect <sup>(2)</sup> | 8050h                    |
| 19       | I <sup>2</sup> C | I <sup>2</sup> C interrupt     | Indirect <sup>(2)</sup> | Yes                     | 8054h                    |
| 20       | RFU              | Reserved for future use        |                         |                         | 8058h                    |
| 21       | RFU              | Reserved for future use        |                         |                         | 805Ch                    |
| 22       | ADC              | End of conversion              |                         |                         | 8060h                    |
| 23       | SYS-TMR          | Update/overflow                |                         |                         | 8064h                    |
| 24       | FLASH            | EOP/WR_PG_DIS                  |                         |                         | 8068h                    |
| 25       | DALI             | DALI interrupt line            | Indirect <sup>(1)</sup> | Indirect <sup>(1)</sup> | 806Ch                    |
| 26       | SMED4            | SMED-4 control logic           |                         |                         | 8070h                    |
| 27       | SMED5            | SMED-5 control logic           |                         |                         | 8074h                    |

Table 32. Interrupt vector exception table (continued)

| Priority | Source block | Description         | Wakeup from Halt | Wakeup from active-halt | Interrupt vector address |
|----------|--------------|---------------------|------------------|-------------------------|--------------------------|
| 28       | RFU          | Reserved future use |                  |                         | 8078h                    |
| 29       | RFU          | Reserved future use |                  |                         | 807Ch                    |

1. P0[x] may be configured to generate an NMI request.
2. P0[x] may be configured to generate an IRQ request.

## 9 Option bytes

The user option byte is a memory E<sup>2</sup>PROM area allowing users to customize the IC device major functionalities:

- ROP: read-out protection control field
- UBC: user boot code protection
- PWM: configurable reset output value
- WDG: internal watchdog HW configuration
- AFR: alternate multifunction signals configuration
- CKC: clock controller functionalities (PLL, HSE enable, AWU clock selection, etc.)
- HSE: clock stabilization counter
- WAIT: Flash and E<sup>2</sup>PROM wait state access time has to be configured with value 0x00
- BOOT: configurable internal boot sources
- BL: bootloader control sequences

Except the ROP byte all the other option bytes are stored twice in a regular (OPT) and complemented format (NOPT) for redundancy. The option byte can be programmed in ICP mode through the SWIM interface or in IAP mode by the application with the exception of the ROP byte that can be only configured via the SWIM interface.

Refer to the the programming manual “How to program STM8S and STM8A Flash program memory and data EEPROM” (PM0051) for further information about Flash programming.

Refer to the STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

## 9.1 Option byte register overview

Table 33. Option byte register overview

| Address             | Option name | Option bits  |           |                |             |                |             |                |              | Default settings |
|---------------------|-------------|--------------|-----------|----------------|-------------|----------------|-------------|----------------|--------------|------------------|
|                     |             | 7            | 6         | 5              | 4           | 3              | 2           | 1              | 0            |                  |
| 4800h               | ROP         | ROP[7:0]     |           |                |             |                |             |                |              | 00h              |
| 4801h               | UCB         | UBC[7:0]     |           |                |             |                |             |                |              | 00h              |
| 4802h               | nUCB        | nUBC[7:0]    |           |                |             |                |             |                |              | FFh              |
| 4803h               | GENCFG      | Rst_PWM5     | Rst_PWM4  | Rst_PWM3       | Rst_PWM2    | Rst_PWM1       | Rst_PWM0    | COMP1_2        | EN_COLD_CFG  | 00h              |
| 4804h               | nGENCFG     | nRst_PWM5    | nRst_PWM4 | nRst_PWM3      | nRst_PWM2   | nRst_PWM1      | nRst_PWM0   | nCOMP1_2       | nEN_COLD_CFG | FFh              |
| 4805h               | MISCUOPT    | -            | -         | -              | -           | LSI_EN         | IWDG_HW     | WWDG_HW        | WWDG_HALT    | 28h              |
| 4806h               | nMISCUOPT   | -            | -         | -              | -           | nLSI_EN        | nIWDG_HW    | nWWDG_HW       | nWWDG_HALT   | D7h              |
| 4807h               | CLKCTL      | -            | -         | -              | CCKAWUSEL1  | EXTCLK         | CCKAWUSEL0  | PRSC[1:0]      |              | 09h              |
| 4808h               | nCLKCTL     | -            | -         | -              | nCCKAWUSEL1 | nEXTCLK        | nCCKAWUSEL0 | nP RSC[1:0]    |              | F6h              |
| 4809h               | HSESTAB     | HSECNT[7:0]  |           |                |             |                |             |                |              | 00h              |
| 480Ah               | nHSESTAB    | nHSECNT[7:0] |           |                |             |                |             |                |              | FFh              |
| 480Bh<br>-<br>480Ch | RESERVED    | -            |           |                |             |                |             |                |              | 00h<br>-<br>FFh  |
| 480Dh               | WAITSTATE   | -            | -         | -              | -           | -              | -           | WS[1:0]        |              | 00h              |
| 480Eh               | nWAITSTATE  | -            | -         | -              | -           | -              | -           | nWS[1:0]       |              | FFh              |
| 480Fh               | AFR_IOMXP0  | -            | -         | Sel_p054[1:0]  |             | Sel_p032[1:0]  |             | Sel_p010[1:0]  |              | 00h              |
| 4810h               | nAFR_IOMXP0 | -            | -         | nSel_p054[1:0] |             | nSel_p032[1:0] |             | nSel_p010[1:0] |              | FFh              |
| 4811h               | AFR_IOMXP1  | AUXTIM       | -         | Sel_p15        | Sel_p14     | Sel_p13        | Sel_p12     | Sel_p11        | Sel_p10      | 00h              |
| 4812h               | nAFR_IOMXP1 | nAUXTIM      | -         | nSel_p15       | nSel_p14    | nSel_p13       | nSel_p12    | nSel_p11       | nSel_p10     | FFh              |



Table 33. Option byte register overview (continued)

| Address | Option name | Option bits |   |                |           |   |              |   |   | Default settings |
|---------|-------------|-------------|---|----------------|-----------|---|--------------|---|---|------------------|
|         |             | 7           | 6 | 5              | 4         | 3 | 2            | 1 | 0 |                  |
| 4813h   | AFR_IOMXP2  | -           | - | -              | Sel_p254  | - | -            | - | - | 00h              |
| 4814h   | nAFR_IOMXP2 | -           | - | -              | nSel_p254 | - | -            | - | - | FFh              |
| 4815h   | MSC_OPT0    | -           | - | UARTLine(1:0)  |           | - | BOTSEL[2:0]  |   |   | 00h              |
| 4816h   | nMSC_OPT0   | -           | - | nUARTLine(1:0) |           | - | nBOTSEL[2:0] |   |   | FFh              |
| 487Dh   | RESERVED    | -           | - | -              | -         | - | -            | - | - | 00h              |
| 487Eh   | OPTBL       | BL(7:0)     |   |                |           |   |              |   |   | 00h              |
| 487Fh   | nOPTBL      | nBL(7:0)    |   |                |           |   |              |   |   | FFh              |

**Note:** *The default setting values refer to the factory configuration. The factory configuration can be overwritten by the user in accordance with the target application requirements.*

*This area of memory may be erased by the global Flash erase instruction generated by an unauthorized attempt to modify the ROP protection.*

## 9.2 Option byte register description

The option byte registers are mapped inside the E<sup>2</sup>PROM data region.

### ROP (memory read-out protection register)

**Table 34. ROP (memory read-out protection register)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x004800</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROP [7:0]                  |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

Bit 7 - 0:

ROP [7:0] memory read-out protection:

0xAA: enable read-out protection. When read-out protection is enabled, reading or modifying the Flash program memory and DATA area in ICP mode (using the SWIM interface) is forbidden, whatever the write protection settings are.

### UBC (UBC user boot code register)

**Table 35. UBC (UBC user boot code register)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x004801</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UBC [7:0]                  |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

Bit 7 - 0:

UBC [7:0] user boot code write protection memory size:

0x00: no UBC, no Flash memory write-protection

0x01: pages 0 to 1 defined as UBC; 1 Kbyte memory write-protected (0x00.8000-0x00.83FF)

0x02: pages 0 to 3 defined as UBC; 2 Kbyte memory write-protected (0x00.8000-0x00.87FF)

0x03: pages 0 to 4 defined as UBC; 2.5 Kbyte memory write-protected (0x00.8000-0x00.89FF)

...

0x3E: pages 0 to 63 defined as UBC; 32 Kbyte memory write-protected (0x00.8000-0x00.FFFF)

Other values: reserved.



**nUBC (UBC user boot code register protection)****Table 36. nUBC (UBC user boot code register protection)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x004802</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0xFF</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| nUBC [7:0]                 |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

nUBC: not (UBC) EMC byte protection.

**GENCFG (general configuration register)****Table 37. GENCFG (general configuration register)**

|                            |   |   |   |   |   |         |             |
|----------------------------|---|---|---|---|---|---------|-------------|
| <b>Offset: 0x004803</b>    |   |   |   |   |   |         |             |
| <b>Default value: 0xFF</b> |   |   |   |   |   |         |             |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1       | 0           |
| Rst_PWM [5:0]              |   |   |   |   |   | COMP1_2 | EN_COLD_CFG |
| r/w                        |   |   |   |   |   | r/w     | r/w         |

Bit 0:

EN\_COLD\_CFG enables IC cold configuration through the option byte register AFR\_IOMXP0,P1:

0: default case, the IC multifunction signal configuration is performed by the miscellaneous registers MSC\_IOMXP0 and MSC\_IOMXP1 (warm configuration).

1: enables the multifunction signal configuration through the option byte registers AFR\_IOMXP0 and AFR\_IOMXP1 (cold configuration).

Bit 1:

COMP1\_2 enables the complete backward compatibility with the previous device implementations. In detail, below features are inhibited:

Multiplexing of I<sup>2</sup>C interface on GPIO [5:4], GPIO [1:0], DIGIN [5:4]

Multiplexing of UART interface on GPIO [5:4]

Port0 and Port2 interrupt mask feature (polling)

DIGIN [5:0] pull-up disabling feature

DALI noise rejection filter.

**Note:** *This bit setting ensures the full device compatibility with the previous device model (STLUX385).*

Bit 7:2:

Rst\_PWM [5:0] configures the PWM [n] reset value after the NRST signal

0: PWM [n] output low level (native default value)

1: PWM [n] output high level.

*Note: The PWM signal programmed reset value is configured during the option byte loader phase, then before the NRST is released it assumes its proper initial values.*

### nGENCFG (general configuration register protection)

**Table 38. nGENCFG (general configuration register protection)**

|                            |   |   |   |   |   |          |              |
|----------------------------|---|---|---|---|---|----------|--------------|
| <b>Offset: 0x004804</b>    |   |   |   |   |   |          |              |
| <b>Default value: 0xFF</b> |   |   |   |   |   |          |              |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1        | 0            |
| Rst_PWM [5:0]              |   |   |   |   |   | nCOMP1_2 | nEN_COLD_CFG |
| r/w                        |   |   |   |   |   | r/w      | r/w          |

nGENCFG: not (GENCFG) EMC byte protection

### MISCUOPT (miscellaneous configuration register)

**Table 39. MISCUOPT (miscellaneous configuration register)**

|  |   |     |     |        |         |         |           |
|--|---|-----|-----|--------|---------|---------|-----------|
| <b>Offset: 0x004805</b>                            |   |     |     |        |         |         |           |
| <b>Default value: 0x28 (factory configuration)</b> |   |     |     |        |         |         |           |
| 7  | 6 | 5   | 4   | 3      | 2       | 1       | 0         |
| RFU  |   | RFU | RFU | LSI_EN | IWdg_hw | WWdg_hw | WWdg_HALT |
| r  |   | r   | r   | r/w    | r/w     | r/w     | r/w       |

Bit 0:

WWdg\_HALT window watchdog reset on Halt:

0: no reset generated on Halt if WWDG is active

1: reset generated on Halt if WWDG is active.

Bit 1:

WWdg\_hw window watchdog hardware enable:

0: window watchdog activation by SW

1: window watchdog activation by HW.

Bit 2:

IWdg\_hw independent watchdog hardware enable:

0: independent watchdog activation by SW

1: independent watchdog activation by HW.

Bit 3:

LSI\_EN low speed internal RCOSC clock enable:

0: LSI clock is not available to CPU

1: LSI clock is enabled for CPU.

Bit 4:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 5:

RFU reserved; must be kept 1 during register writing for future compatibility.

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

### nMISCUOPT (miscellaneous configuration register protection)

**Table 40. nMISCUOPT (miscellaneous configuration register protection)**

|                            |   |     |     |         |          |          |            |
|----------------------------|---|-----|-----|---------|----------|----------|------------|
| <b>Offset: 0x004806</b>    |   |     |     |         |          |          |            |
| <b>Default value: 0xD7</b> |   |     |     |         |          |          |            |
| 7                          | 6 | 5   | 4   | 3       | 2        | 1        | 0          |
| RFU                        |   | RFU | RFU | nLSI_EN | nIWdg_hw | nWWdg_hw | nWWdg_HALT |
| r                          |   | r   | r   | r/w     | r/w      | r/w      | r/w        |

nMISCUOPT: not (MISCUOPT) EMC byte protection

### CLKCTL (CKC configuration register)

**Table 41. CLKCTL (CKC configuration register)**

|  |   |   |           |        |           |            |   |
|--|---|---|-----------|--------|-----------|------------|---|
| <b>Offset: 0x004807</b>                            |   |   |           |        |           |            |   |
| <b>Default value: 0x09 (factory configuration)</b> |   |   |           |        |           |            |   |
| 7  | 6 | 5 | 4         | 3      | 2         | 1          | 0 |
| RFU  |   |   | CKAWUSEL1 | EXTCLK | CKAWUSEL0 | PRSC [1:0] |   |
| r  |   |   | r/w       | r/w    | r/w       | r/w        |   |

Bit 1 - 0:

PRSC [1:0] prescaler value for HSE to provide AWU unit with the low speed clock:

00: 24 MHz to 128 kHz prescaler

01: 16 MHz to 128 kHz prescaler

10: 8 MHz to 128 kHz prescaler

11: 4 MHz to 128 kHz prescaler.

Bit 3:

EXTCLK external clock selection:

0: external crystal oscillator clock connected to HseOscin and HseOscout signals

1: external direct drive clock connected to HseOscin.

Bit 4, 2:

CKAWUSEL[1:0] AWU clock selection:

00: low speed internal clock used for AWU module

01: HSE high speed external clock with prescaler used for AWU module

10: reserved encoding value

11: reserved encoding value.

Bit 7 - 5:

RFU reserved; must be kept 0 during register writing for future compatibility.

### nCLKCTL (CKC configuration register protection)

**Table 42. nCLKCTL (CKC configuration register protection)**

|  |   |   |            |         |            |             |   |
|--|---|---|------------|---------|------------|-------------|---|
| <b>Offset: 0x004808</b>                            |   |   |            |         |            |             |   |
| <b>Default value: 0xF6 (factory configuration)</b> |   |   |            |         |            |             |   |
| 7  | 6 | 5 | 4          | 3       | 2          | 1           | 0 |
| RFU  |   |   | nCKAWUSEL1 | nEXTCLK | nCKAWUSEL0 | nPRSC [1:0] |   |
| r  |   |   | r/w        | r/w     | r/w        | r/w         |   |

nCLKCTL: not (CLKCTL) EMC byte protection.

### HSESTAB (HSE clock stabilization register)

**Table 43. HSESTAB (HSE clock stabilization register)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x004809</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSECNT [7:0]               |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

Bit 7 - 0:

HSECNT [7:0] HSE crystal oscillator stabilization cycles:

0x00: 2048 clock cycles

0xB4: 128 clock cycles

0xD2: 8 clock cycles

0xE1: 0.5 clock cycles.

**nHSESTAB (HSE clock stabilization register protection)****Table 44. nHSESTAB (HSE clock stabilization register protection)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x00480A</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0xFF</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| nHSECNT [7:0]              |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

nHSESTAB: not (HSESTAB) EMC byte protection.

**WAITSTATE (Flash wait state register)****Table 45. WAITSTATE (Flash wait state register)**

|                            |   |   |   |   |   |                |   |
|----------------------------|---|---|---|---|---|----------------|---|
| <b>Offset: 0x00480D</b>    |   |   |   |   |   |                |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |                |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1              | 0 |
| RFU                        |   |   |   |   |   | Waitstat [1:0] |   |
| r                          |   |   |   |   |   | r/w            |   |

Bit 1 - 0:

Waitstat[ 1:0] configures the E<sup>2</sup>PROM and Flash programmable delay read access time:

00: 0 no delay cycle (default case  $f_{\text{MASTER}}$  at 16 MHz)

01: 1 delay cycles

10: 2 delay cycles

11: 3 delay cycles.

Bit 7 - 2:

RFU reserved; must be kept 0 during register writing for future compatibility.

**nWAITSTATE (Flash wait state register protection)****Table 46. nWAITSTATE (Flash wait state register)**

|                            |   |   |   |   |   |                 |   |
|----------------------------|---|---|---|---|---|-----------------|---|
| <b>Offset: 0x00480E</b>    |   |   |   |   |   |                 |   |
| <b>Default value: 0xFF</b> |   |   |   |   |   |                 |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1               | 0 |
| RFU                        |   |   |   |   |   | nWaitstat [1:0] |   |
| r                          |   |   |   |   |   | r/w             |   |

nWAITSTATE: not (WAITSTATE) EMC byte protection.

**AFR\_IOMXP0 (alternative Port0 configuration register)****Table 47. AFR\_IOMXP0 (alternative Port0 configuration register)**

|                            |   |                |   |                |   |                |   |
|----------------------------|---|----------------|---|----------------|---|----------------|---|
| <b>Offset: 0x00480F</b>    |   |                |   |                |   |                |   |
| <b>Default value: 0x00</b> |   |                |   |                |   |                |   |
| 7                          | 6 | 5              | 4 | 3              | 2 | 1              | 0 |
| RFU                        |   | Sel_p054 [1:0] |   | Sel_p032 [1:0] |   | Sel_p010 [1:0] |   |
| r                          |   | r/w            |   | r/w            |   | r/w            |   |

Bit 5 - 0:

Refer to MSC\_IOMXP0 miscellaneous register field description [Section 7.2 on page 39](#).

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

**nAFR\_IOMXP0 (alternative Port0 configuration register protection)****Table 48. nAFR\_IOMXP0 (alternative Port0 configuration register protection)**

|                            |   |                 |   |                 |   |                 |   |
|----------------------------|---|-----------------|---|-----------------|---|-----------------|---|
| <b>Offset: 0x004810</b>    |   |                 |   |                 |   |                 |   |
| <b>Default value: 0xFF</b> |   |                 |   |                 |   |                 |   |
| 7                          | 6 | 5               | 4 | 3               | 2 | 1               | 0 |
| RFU                        |   | nSel_p054 [1:0] |   | nSel_p032 [1:0] |   | nSel_p010 [1:0] |   |
| r                          |   | r/w             |   | r/w             |   | r/w             |   |

nAFR\_IOMXP0: not (AFR\_IOMXP0) EMC byte protection.

**AFR\_IOMXP1 (alternative Port1 configuration register)****Table 49. AFR\_IOMXP1 (alternative Port1 configuration register)**

|                            |     |         |         |         |         |         |         |
|----------------------------|-----|---------|---------|---------|---------|---------|---------|
| <b>Offset: 0x004811</b>    |     |         |         |         |         |         |         |
| <b>Default value: 0x00</b> |     |         |         |         |         |         |         |
| 7                          | 6   | 5       | 4       | 3       | 2       | 1       | 0       |
| AUXTIM                     | RFU | Sel_p15 | Sel_p14 | Sel_p13 | Sel_p12 | Sel_p11 | Sel_p10 |
| r                          | r   | r/w     | r/w     | r/w     | r/w     | r/w     | r/w     |

Bit 5 - 0:

Refer to MSC\_IOMXP1 miscellaneous register field description [Section 7.2.3 on page 40](#).

Bit 6:

RFU reserved; must be kept 0 during register writing for future product compatibility.

Bit 7:

AUXTIM CCO Aux timer compatibility features

0: CCO Aux timer enabled

1: CCO Aux timer disabled.

### nAFR\_IOMXP1 (alternative Port1 configuration register protection)

**Table 50. nAFR\_IOMXP1 (alternative Port1 configuration register protection)**

|                            |     |          |          |          |          |          |          |
|----------------------------|-----|----------|----------|----------|----------|----------|----------|
| <b>Offset: 0x004812</b>    |     |          |          |          |          |          |          |
| <b>Default value: 0xFF</b> |     |          |          |          |          |          |          |
| 7                          | 6   | 5        | 4        | 3        | 2        | 1        | 0        |
| nAUXTIM                    | RFU | nSel_p15 | nSel_p14 | nSel_p13 | nSel_p12 | nSel_p11 | nSel_p10 |
| r                          | r   | r/w      | r/w      | r/w      | r/w      | r/w      | r/w      |

nAFR\_IOMXP1: not (AFR\_IOMXP1) EMC byte protection.

### AFR\_IOMXP2 (alternative Port2 configuration register)

**Table 51. AFR\_IOMXP2 (alternative Port2 configuration register)**

|                            |   |   |          |     |     |     |     |
|----------------------------|---|---|----------|-----|-----|-----|-----|
| <b>Offset: 0x004811</b>    |   |   |          |     |     |     |     |
| <b>Default value: 0x00</b> |   |   |          |     |     |     |     |
| 7                          | 6 | 5 | 4        | 3   | 2   | 1   | 0   |
| RFU                        |   |   | Sel_p254 | RFU | RFU | RFU | RFU |
| r                          |   |   | r        | r   | r   | r   | r   |

Bit 3 - 0:

RFU reserved; must be kept 0 during register writing for future product compatibility

Bit 4:

Refer to MSC\_IOMXP2 Miscellaneous register field description [Section 7.2.3 on page 40](#).

Bit 7 - 5:

RFU reserved; must be kept 0 during register writing for future product compatibility.

### nAFR\_IOMXP2 (alternative Port2 configuration register protection)

**Table 52. nAFR\_IOMXP2 (alternative Port2 configuration register protection)**

|                            |   |   |           |     |     |     |     |
|----------------------------|---|---|-----------|-----|-----|-----|-----|
| <b>Offset: 0x004812</b>    |   |   |           |     |     |     |     |
| <b>Default value: 0xFF</b> |   |   |           |     |     |     |     |
| 7                          | 6 | 5 | 4         | 3   | 2   | 1   | 0   |
| RFU                        |   |   | nSel_p254 | RFU | RFU | RFU | RFU |
| r                          |   |   | r         | r   | r   | r   | r   |

nAFR\_IOMXP2: not (AFR\_IOMXP2) EMC byte protection.

### MSC\_OPT0 (miscellaneous configuration reg0)

**Table 53. MSC\_OPT0 (miscellaneous configuration reg0)**

|                            |   |                |   |     |               |   |   |
|----------------------------|---|----------------|---|-----|---------------|---|---|
| <b>Offset: 0x004815</b>    |   |                |   |     |               |   |   |
| <b>Default value: 0x00</b> |   |                |   |     |               |   |   |
| 7                          | 6 | 5              | 4 | 3   | 2             | 1 | 0 |
| RFU                        |   | UARTline [1:0] |   | RFU | Bootsel [2:0] |   |   |
| r                          |   | r/w            |   | r   | r/w           |   |   |

Bit 2 - 0:

Bootsel [2:0] boot-ROM peripheral enables:

000: automatic scan boot sources; this selection enables the automatic scan configuration sequence of all possible initializing peripheral devices: Periph0 (UART), Periph1 (RFU), Periph2 (RFU).

001: enable boot source: Periph0

010: enable boot source: Periph1

011: enable boot sources: Periph1, Periph0

100: enable boot source: Periph2

101: enable boot sources: Periph2, Periph0

110: enable boot sources: Periph2, Periph1

111: enable boot sources: Periph2, Periph1, Periph0.

Bit 3:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 5 - 4:

UARTline [1:0] selects the UART port configuration pins involved during the bootstrap sequence in warm configuration mode; in case of cold configuration, this field is ignored since the UART port is selected by the register AFR\_IOMP0.

00: boot sequence with UART i/f configured in all possible UART multiplexed signal schemes. This sequence is used when UART i/f position is not specified.

01: boot sequence with UART i/f configured on P0 (1, 0)

10: boot sequence with UART i/f configured on P0 (3, 2)

11: boot sequence with UART i/f configured on P0 (5, 4).

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.



**nMSC\_OPT0 (miscellaneous configuration reg0 protection)****Table 54. nMSC\_OPT0 (miscellaneous configuration reg0 protection)**

|                            |   |                |   |     |                |   |   |
|----------------------------|---|----------------|---|-----|----------------|---|---|
| <b>Offset: 0x004816</b>    |   |                |   |     |                |   |   |
| <b>Default value: 0xFF</b> |   |                |   |     |                |   |   |
| 7                          | 6 | 5              | 4 | 3   | 2              | 1 | 0 |
| RFU                        |   | UARTline [1:0] |   | RFU | nBootSel [2:0] |   |   |
| r                          |   | r/w            |   | r   | r/w            |   |   |

nMSC\_OPT0: not (MSC\_OPT0) EMC byte protection.

**OPTBL (option byte bootloader)****Table 55. OPTBL (option byte bootloader)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x00487E</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BL [7:0]                   |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

Bit 7 - 0:

BL [7:0] bootloader field checked by the internal BootROM code during the STLUX385A initialization phase. The content of register locations 0x00487E, 0x00487F and 0x008000 determine the bootloader SW flow execution sequence.

**nOPTBL (option byte boot loader protection)****Table 56. nOPTBL (option byte boot loader protection)**

|                            |   |   |   |   |   |   |   |
|----------------------------|---|---|---|---|---|---|---|
| <b>Offset: 0x00487F</b>    |   |   |   |   |   |   |   |
| <b>Default value: 0x00</b> |   |   |   |   |   |   |   |
| 7                          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| nBL [7:0]                  |   |   |   |   |   |   |   |
| r/w                        |   |   |   |   |   |   |   |

nOPTBL: not (OPTBL) EMC byte protection.

## 10 Device identification

### 10.1 Unique ID

The STLUX385A device provides a 56-bits unique identifier code usable as a device identification number which can be used to increase the device security. The unique ID code is a frozen signature not alterable by user.

The unique device identifier is ideally used by the application software and is suited for:

- Serial code
- Security keys in conjunction with cryptographic software to increase the embedded Flash code security
- Activating the secure boot sequence.

**Table 57. Unique ID register overview**

| Address | Option name | Unique ID bits |   |   |   |   |                |   |   |
|---------|-------------|----------------|---|---|---|---|----------------|---|---|
|         |             | 7              | 6 | 5 | 4 | 3 | 2              | 1 | 0 |
| 48E0h   | UID0        | LotNum [7:0]   |   |   |   |   |                |   |   |
| 48E1h   | UID1        | LotNum [15:8]  |   |   |   |   |                |   |   |
| 48E2h   | UID2        | LotNum [23:16] |   |   |   |   |                |   |   |
| 48E3h   | UID3        | WaferNum [4:0] |   |   |   |   | Xcoord [7:5]   |   |   |
| 48E4h   | UID4        | Xcoord [4:0]   |   |   |   |   | Ycoord [7:5]   |   |   |
| 48E5h   | UID5        | Ycoord [4:0]   |   |   |   |   | LotNum [42:40] |   |   |
| 48E6h   | UID6        | LotNum [31:24] |   |   |   |   |                |   |   |
| 48E7h   | UID7        | LotNum [39:32] |   |   |   |   |                |   |   |

### 10.2 Device ID

The STLUX385A device identification model is coded in the following register area and it cannot be altered by the user.

The register fields have the follow meaning:

Dev\_ID [7:0]:

Device identification model

0x00: STLUX385

Others: RFU reserved values.

Rev\_ID [4:0]:

Revision identification model

00000: STLUX385

00001: STLUX385A

Others: RFU reserved values.

Table 58. Dev ID register overview

| Address | Option name | Dev ID bits  |   |   |               |   |   |   |   | Default settings |
|---------|-------------|--------------|---|---|---------------|---|---|---|---|------------------|
|         |             | 7            | 6 | 5 | 4             | 3 | 2 | 1 | 0 |                  |
| 4896h   | DVD0        | DEV_ID[7:0]  |   |   |               |   |   |   |   | 00h              |
| 4897h   | nDVD0       | nDEV_ID[7:0] |   |   |               |   |   |   |   | FFh              |
| 4898h   | DVD1        | RFU          |   |   | Rev_ID [4:0]  |   |   |   |   | 01h              |
| 4899h   | nDVD1       | nRFU         |   |   | nRev_ID [4:0] |   |   |   |   | FEh              |

## 11 Electrical characteristics

### 11.1 Parameter conditions

Unless otherwise specified, all voltages are referred to  $V_{SS}$ .  $V_{DDA}$  and  $V_{DD}$  must be connected to the same voltage value.

#### 11.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25\text{ °C}$  and  $T_A = T_A \text{ max.}$  (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

#### 11.1.2 Typical values

Unless otherwise specified, typical data are based on  $T_A = 25\text{ °C}$ ,  $V_{DD}$  and  $V_{DDA} = 3.3\text{ V}$ . They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

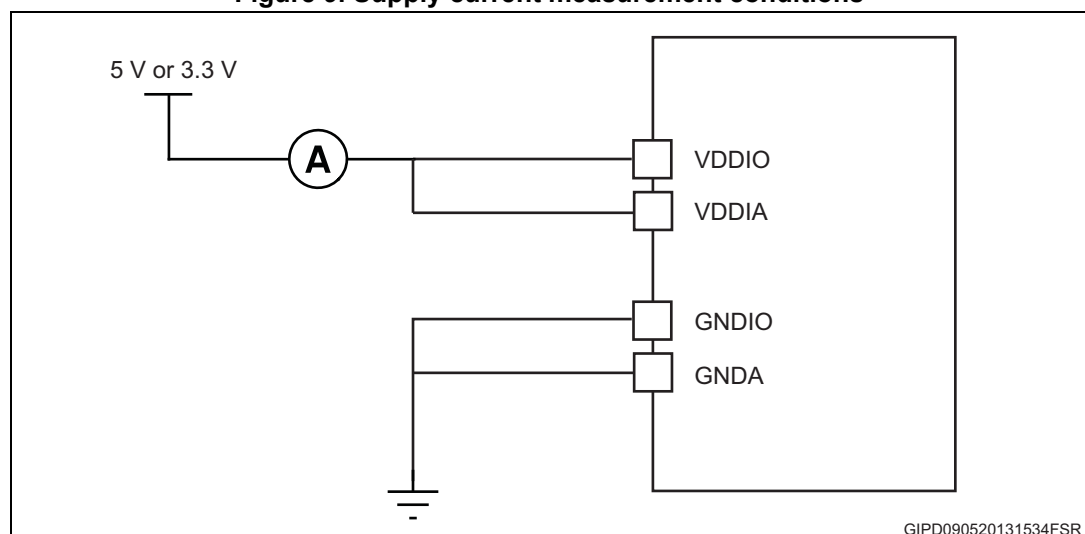
#### 11.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

#### 11.1.4 Typical current consumption

For typical current consumption measurements,  $V_{DD}$  and  $V_{DDA}$  are connected together as shown in [Figure 9](#).

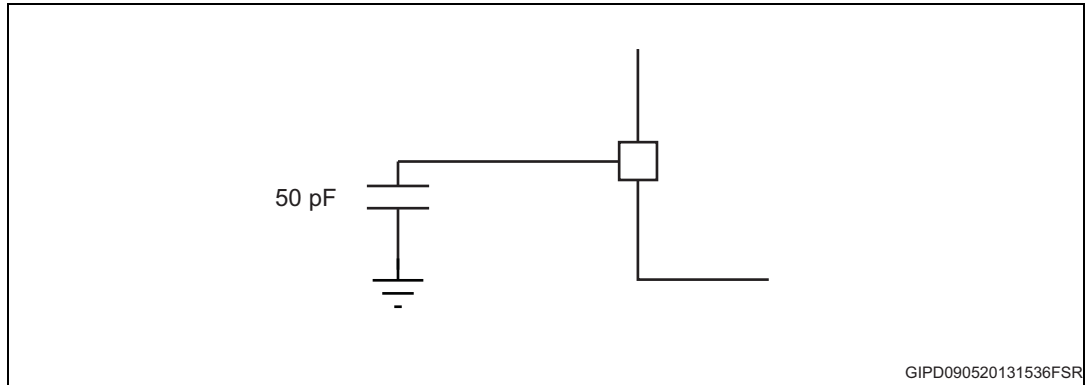
**Figure 9. Supply current measurement conditions**



### 11.1.5 Loading capacitors

The loading conditions used for pin parameter measurement are shown in [Figure 10](#):

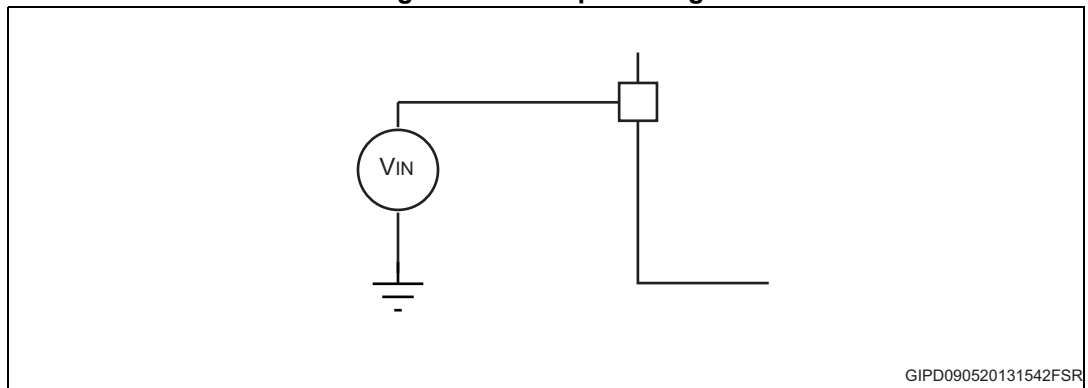
**Figure 10. Pin loading conditions**



### 11.1.6 Pin output voltage

The input voltage measurement on a pin is described in [Figure 11](#).

**Figure 11. Pin input voltage**



## 11.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

**Table 59. Voltage characteristics**

| Symbol              | Ratings  | Min.  | Max.           | Unit |
|---------------------|--|---|----------------|------|
| $V_{DDX} - V_{SSX}$ | Supply voltage <sup>(1)</sup>                                  | -0.3  | 6.5            | V    |
| $V_{IN}$            | Input voltage on any other pin <sup>(2)</sup>                  | $V_{SS} - 0.3$  | $V_{DD} + 0.3$ |      |
| $V_{DD} - V_{DDA}$  | Variation between different power pins                         |   | 50             | mV   |
| $V_{SS} - V_{SSA}$  | Variation between all the different ground pins <sup>(3)</sup> |   | 50             |      |
| $V_{ESD}$           | Electrostatic discharge voltage                                | Refer to absolute maximum ratings (electrical sensitivity) in <a href="#">Section 11.4.1 on page 93</a> |                |      |

1. All power  $V_{DDX}$  ( $V_{DD}$ ,  $V_{DDA}$ ) and ground  $V_{SSX}$  ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply.
2.  $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .
3.  $V_{SS}$  and  $V_{SSA}$  signals must be interconnected together with a short wire loop.

**Table 60. Current characteristics**

| Symbol   | Ratings  | Max. <sup>(1)</sup> | Unit |  |
|--|--|---------------------|------|--|
| I <sub>VDDX</sub>                              | Total current into V <sub>DDX</sub> power lines <sup>(2)</sup>   | 100                 | mA   |  |
| I <sub>VSSX</sub>                              | Total current out of V <sub>SSX</sub> power lines <sup>(2)</sup> | 100                 |      |  |
| I <sub>IO</sub>                                | Output current sunk by any I/Os and control pin                  | Ref.                |      |  |
|  | Output current source by any I/Os and control pin                |                     |      |  |
| I <sub>INJ(PIN)</sub> <sup>(3), (4)</sup>      | Injected current on any pin                                      | ±4                  |      |  |
| I <sub>INJ(TOT)</sub> <sup>(3), (4), (5)</sup> | Sum of injected currents   | ±20                 |      |  |

1. Data based on characterization results, not tested in production.
2. All power  $V_{DDX}$  ( $V_{DD}$ ,  $V_{DDA}$ ) and ground  $V_{SSX}$  ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply.
3.  $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ .
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

Table 61. Thermal characteristics

| Symbol           | Ratings                      | Max.       | Unit |
|------------------|------------------------------|------------|------|
| T <sub>STG</sub> | Storage temperature range    | -65 to 150 | °C   |
| T <sub>J</sub>   | Maximum junction temperature | 150        |      |

## 11.3 Operating conditions

The device must be used in operating conditions that respect the parameters in [Table 62](#). In addition, full account must be taken for all physical capacitor characteristics and tolerances.

Table 62. General operating conditions

| Symbol                                  | Parameter  | Conditions                    | Min.               | Typ.               | Max.               | Unit |
|---|--|-------------------------------|--------------------|--------------------|--------------------|------|
| f <sub>CPU</sub>                        | Internal CPU clock frequency   | -40 ≤ T <sub>A</sub> ≤ 105 °C | 0                  |                    | 16                 | MHz  |
| V <sub>DD1</sub> ,<br>V <sub>DDA1</sub> | Operating voltages   |                               | 3 <sup>(1)</sup>   |                    | 5.5 <sup>(1)</sup> | V    |
| V <sub>DD</sub> , V <sub>DDA</sub>      | Nominal operating voltages   |                               | 3.3 <sup>(1)</sup> |                    | 5 <sup>(1)</sup>   |      |
| V <sub>OUT</sub>                        | Core digital power supply  |                               |                    | 1.8 <sup>(2)</sup> |                    |      |
|   | C <sub>VOUT</sub> : capacitance of external capacitor <sup>(3)</sup> | at 1 MHz                      | 470                |                    | 3300               | nF   |
|   | ESR of external capacitor <sup>(2)</sup>                             |                               | 0.05               |                    | 0.2                | Ω    |
|   | ESL of external capacitor <sup>(2)</sup>                             |                               |                    |                    | 15                 | nH   |
| Θ <sub>JA</sub> <sup>(4)</sup>          | FR4 multilayer PCB   |                               |                    | 80                 |                    | °C/W |
| T <sub>A</sub>                          | Ambient temperature  | P <sub>d</sub> = 100 mW       | -40                |                    | 105                | °C   |

1. The external power supply can be within range from 3 V up to 5.5 V although IC performances are optimized for power supply equal to 3.3 V.
2. Internal core power supply voltage.
3. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
4. To calculate P<sub>Dmax</sub> (T<sub>A</sub>), use the formula P<sub>Dmax</sub> = (T<sub>Jmax</sub> - T<sub>A</sub>)/Θ<sub>JA</sub>.

Table 63. Operating conditions at power-up/power-down

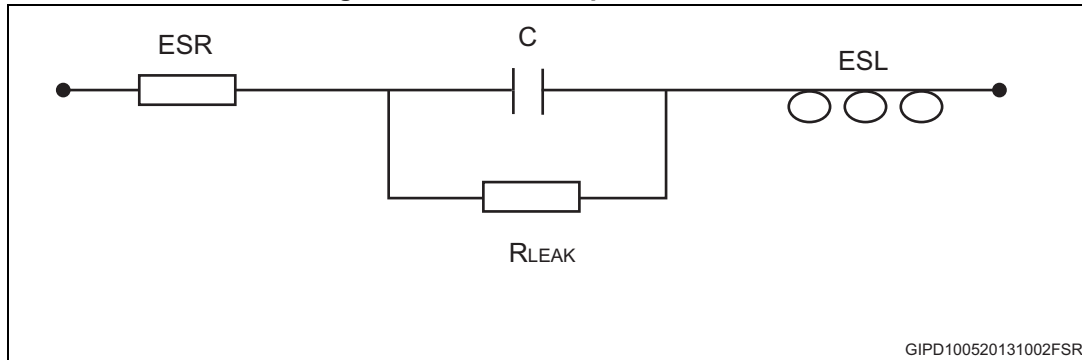
| Symbol                | Parameter                      | Conditions             | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup>     | Unit |
|-----------------------|--------------------------------|------------------------|---------------------|------|-------------------------|------|
| t <sub>VDD</sub>      | V <sub>DD</sub> rise time rate |                        | 2 μs/V              |      | 1 sec./V <sup>(2)</sup> |      |
|                       | V <sub>DD</sub> fall time rate |                        | 2 μs/V              |      | 1 sec./V <sup>(2)</sup> |      |
| t <sub>TEMP</sub>     | Reset release delay            | V <sub>DD</sub> rising |                     | 3    |                         | ms   |
| V <sub>IT+</sub>      | Power-on reset threshold       |                        | 2.65                | 2.8  | 2.98                    | V    |
| V <sub>IT-</sub>      | Brownout reset threshold       |                        | 2.58                | 2.73 | 2.88                    |      |
| V <sub>HYS(BOR)</sub> | Brownout reset hysteresis      |                        |                     | 70   |                         | mV   |

1. Guaranteed by design, not tested in production.
2. Power supply ramp must be monotone.

### 11.3.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor CVOUT<sup>(a)</sup> to the VOUT pin. The CVOUT is specified in [Section 11.3: Operating conditions](#). Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor CVOUT



### 11.3.2 Supply current characteristics

The STLUX385A supply current is calculated by summing the supply base current in the desired operating mode as per [Table 64](#), with the peripheral supply current value reported in [Table 66](#) and [Table 67 on page 77](#).

For example, considering an application where:

- $f_{\text{MASTER}} = f_{\text{CPU}} = 16 \text{ MHz}$  provided by HSI internal RC oscillator
- CPU code execution in Flash
- All base peripheral actives: I<sup>2</sup>C, UART, DALI, ITC, GPIO0, SysTimr, WWDG and IWDG
- ADC conversion frequency  $f_{\text{ADC}} = 5.3 \text{ MHz}$
- ACU (comparator and DAC units) actives
- 6 PWM toggling at  $f_{\text{PWM}} = 0.5 \text{ MHz}$  provided by 6 SMEDs running at  $f_{\text{SMED}} = 12 \text{ MHz}$  ( $N_{\text{PWM}} = 6$ ).

The total current consumption is given by [Equation 1](#):

#### Equation 1

$$I_{\text{DD}} = I_{\text{DD(Run2)}} + I_{\text{DD(ADC2)}} + I_{\text{DD(ACU)}} + I_{\text{DD(PLL)}} + I_{\text{DD(PWM)}}$$

where  $I_{\text{DD(PWM)}} = I_{\text{DD(PWM1)}} * N_{\text{PWM}}$

More generally, the PWM current consumption has to be individually evaluated for each  $f_{\text{SMED}}$  clock grouping, using [Equation 2](#).

a. ESR is the equivalent series resistance and ESL is the equivalent inductance.



**Equation 2**

$$I_{DD(PWM)} = \sum_{i=1}^{N_{fSMED}} [I_{DD(PWM[i1])} \cdot N_i]$$

where  $i = f_{SMED}$  clock group index;  $N_i = PWM$  number of the  $i$ \_th clock group;  
 $N_{fSMED} = f_{SMED}$  clock group number.

**IC supply base current consumption**

*Table 64* summarizes the current consumption measured on  $V_{DD}/V_{DDA}$  supply pins in relevant operative conditions.

**Table 64. Supply base current consumption at  $V_{DD}/V_{DDA} = 3.3/5\text{ V}$** 

| Symbol                        | Code      | Clock              |                     |                  | Peripheral                 | Consumption <sup>(1)</sup> |                     | Note  |
|-------------------------------|-----------|--------------------|---------------------|------------------|----------------------------|----------------------------|---------------------|---|
| Op. mode                      | Code area | SRC <sup>(2)</sup> | $f_{\text{MASTER}}$ | $f_{\text{CPU}}$ | Periph <sup>(3), (4)</sup> | Typ. <sup>(5)</sup>        | Max. <sup>(5)</sup> | Description                                   |
|                               |           | Clock              | MHz                 | MHz              | Enable                     | mA                         | mA                  |   |
| $I_{\text{DD}}(\text{Run1})$  | Flash     | HSI                | 2                   | 2                | All                        | 2.3                        | 2.77                | Reset exit condition                          |
| $I_{\text{DD}}(\text{Run2})$  | Flash     | HSI                | 16                  | 16               | All                        | 9.4                        | 11.3                |   |
| $I_{\text{DD}}(\text{Run3})$  | RAM       | HSI                | 16                  | 16               | All                        | 4.2                        | 5.1                 |   |
| $I_{\text{DD}}(\text{Run4})$  | Flash     | HSE <sup>(6)</sup> | 16                  | 16               | All                        | 10.0                       | 12.1                | $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$ |
|                               |           |                    |                     |                  |                            | 10.6                       | 12.74               | $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$   |
| $I_{\text{DD}}(\text{Run5})$  | RAM       | HSE <sup>(6)</sup> | 16                  | 16               | All                        | 4.6                        | 5.53                | $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$ |
|                               |           |                    |                     |                  |                            | 5.2                        | 6.63                | $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$   |
| $I_{\text{DD}}(\text{SLOW1})$ | Flash     | HSI                | 16                  | 2                | All                        | 3.6                        | 4.33                |   |
| $I_{\text{DD}}(\text{SLOW2})$ | RAM       | HSI                | 16                  | 2                | All                        | 2.9                        | 3.5                 |   |
| $I_{\text{DD}}(\text{SLOW3})$ | Flash     | HSE <sup>(6)</sup> | 16                  | 2                | All                        | 3.9                        | 4.7                 | $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$ |
|                               |           |                    |                     |                  |                            | 4.5                        | 5.5                 | $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$   |
| $I_{\text{DD}}(\text{SLOW4})$ | Flash     | HSI                | 16                  | 0.125            | All                        | 2.7                        | 3.3                 |   |
| $I_{\text{DD}}(\text{SLOW5})$ | Flash     | HSE <sup>(6)</sup> | 16                  | 0.125            | All                        | 3.0                        | 3.7                 | $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$ |
|                               |           |                    |                     |                  |                            | 3.6                        | 4.4                 | $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$   |
| $I_{\text{DD}}(\text{SLOW6})$ | Flash     | LSI                | 0,153               | 0.153            | All                        | 1.5                        | 1.9                 |   |
| $I_{\text{DD}}(\text{WF11})$  | Flash     | HSI                | 16                  | 16               | All                        | 2.6                        | 3.2                 |   |
| $I_{\text{DD}}(\text{WF12})$  | Flash     | HSE <sup>(6)</sup> | 16                  | 16               | All                        | 3.1                        | 3.8                 | $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$ |
|                               |           |                    |                     |                  |                            | 3.8                        | 5.6                 | $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$   |

1. Data based on characterization results not tested in production.
2.  $f_{\text{MASTER}}$  clock source.
3. "All" means: I<sup>2</sup>C, UART, DALI, ITC, GPIO0, SysTmr, WWDG and IWDG peripherals active.
4. The peripheral current consumption is supplied by the VCORE voltage (1.8 V).
5. Temperature operating:  $T_A = 25\text{ °C}$ .
6. HSE frequency provided by external quartz.

### IC low power current consumption

**Table 65** summarizes the current consumption measured on  $V_{DD}/V_{DDA}$  supply pins in power saving conditions.

**Table 65. Supply low power consumption at  $V_{DD}/V_{DDA} = 3.3/5$  V**

| Symbol                       | Code      | Clock                   |   | Peripheral                         |                        | Consumption <sup>(11)</sup> |                           | Note                                      |
|------------------------------|-----------|-------------------------|---|------------------------------------|------------------------|-----------------------------|---------------------------|---|
| Op. mode <sup>(1), (2)</sup> | Code area | SRC <sup>(3)</sup>      | f <sub>MASTER</sub><br>f <sub>CPU</sub> | E <sup>2</sup> PROM <sup>(6)</sup> | MVRreg. <sup>(5)</sup> | Typ. <sup>(8), (10)</sup>   | Max. <sup>(9), (10)</sup> | Description                               |
|                              |           | Clock                   | MHz                                     | Enable                             | Enable                 | mA                          | mA                        |   |
| I <sub>DD</sub> (AHLT1)      | Flash     | HSI                     | 16                                      | Enable                             | Enable                 | 0.23                        | 0.32                      | AWU clocked by LSI                        |
| I <sub>DD</sub> (AHLT2)      | Flash     | HSI                     | 16                                      | Enable                             | Disable                | 0.085                       | 0.12                      | AWU clocked by LSI                        |
| I <sub>DD</sub> (AHLT3)      | Flash     | HSE <sup>(4), (7)</sup> | 16                                      | Enable                             | Enable                 | 0.73                        | 0.90                      | V <sub>DD</sub> /V <sub>DDA</sub> = 3.3 V |
|                              |           |                         |   |                                    |                        | 1.4                         | 1.7                       | V <sub>DD</sub> /V <sub>DDA</sub> = 5 V   |
| I <sub>DD</sub> (AHLT4)      | Flash     | HSE <sup>(4), (7)</sup> | 16                                      | Enable                             | Disable                | 0.65                        | 0.95                      | V <sub>DD</sub> /V <sub>DDA</sub> = 3.3 V |
|                              |           |                         |   |                                    |                        | 1.2                         | 1.45                      | V <sub>DD</sub> /V <sub>DDA</sub> = 5 V   |
|                              |           |                         |   |                                    |                        |                             |                           |   |
| I <sub>DD</sub> (HLT1)       | Flash     | HSI                     | 16                                      | Enable                             | Disable                | 0.087                       | 0.13                      |   |
| I <sub>DD</sub> (HLT2)       | Flash     | HSE <sup>(4), (7)</sup> | 16                                      | Enable                             | Disable                | 0.075                       | 0.11                      | V <sub>DD</sub> /V <sub>DDA</sub> = 3.3 V |
|                              |           |                         |   |                                    |                        | 0.090                       | 0.15                      | V <sub>DD</sub> /V <sub>DDA</sub> = 5 V   |

1. Active-halt op. mode: all peripherals except AWU and IWDG are disabled (clock gated).
2. HALT op. mode: all peripherals are disabled (clock gated).
3.  $f_{MASTER}$  clock source.
4. HSE frequency provided by external quartz.
5.  $V_{CORE}$  Main DC voltage regulator.
6. E<sup>2</sup>PROM is considered always enabled.
7. AWU clocked by HSE source clock.
8. Temperature operating:  $T_A = 25$  °C.
9. Temperature operating:  $T_A = 105$  °C.
10. All the analog input signals are connected to GND; the signals of the port P0, P1 and P2 are configured as input with pull-up enabled.
11. Data based on characterization results not tested in production.

**IC peripheral current consumption (3.3 V)**

*Table 66* summarizes the peripheral current consumption measured on  $V_{DD}/V_{DDA}$  supply pins.

**Table 66. Peripheral supply current consumption at  $V_{DD}/V_{DDA} = 3.3\text{ V}$** 

| Symbol              | Clock   |                  |                 |                 | Peripherals        |                        |                    | Consumption <sup>(9)</sup> |                    |
|---------------------|---------|------------------|-----------------|-----------------|--------------------|------------------------|--------------------|----------------------------|--------------------|
| Op.mode             |         | $f_{SMED}^{(1)}$ | $f_{PWM}^{(2)}$ | $f_{ADC}^{(3)}$ | ADC <sup>(7)</sup> | PWM <sup>(4),(5)</sup> | ACU <sup>(6)</sup> | Typ <sup>(8)</sup>         | Max <sup>(8)</sup> |
|                     | Enb/Dis | MHz              | MHz             | MHz             | Enb/Dis            | Num                    | Enb/Dis            | mA                         | mA                 |
| $I_{DD}(PLL)$       | Enab    | 0                | 0               | 0               | Disab              | 0                      | Disab              | 2.26                       | 2.7                |
| $I_{DD}(ACU)$       | Disab   | 0                | 0               | 0               | Disab              | 0                      | Enab               | 1.89                       | 2.27               |
| $I_{DD}(PWM1PLL96)$ | Enab    | 96               | 0.5             | 0               | Disab              | 1                      | Disab              | 1.75                       | 2.1                |
| $I_{DD}(PWM6PLL96)$ |         |                  |                 |                 |                    | 6                      |                    | 10.12                      | 12.2               |
| $I_{DD}(PWM1PLL48)$ | Enab    | 48               | 0.5             | 0               | Disab              | 1                      | Disab              | 1.12                       | 1.33               |
| $I_{DD}(PWM6PLL48)$ |         |                  |                 |                 |                    | 6                      |                    | 6.54                       | 7.85               |
| $I_{DD}(PWM1PLL24)$ | Enab    | 24               | 0.5             | 0               | Disab              | 1                      | Disab              | 0.71                       | 0.86               |
| $I_{DD}(PWM6PLL24)$ |         |                  |                 |                 |                    | 6                      |                    | 4.39                       | 5.27               |
| $I_{DD}(PWM1PLL12)$ | Enab    | 12               | 0.5             | 0               | Disab              | 1                      | Disab              | 0.54                       | 0.65               |
| $I_{DD}(PWM6PLL12)$ |         |                  |                 |                 |                    | 6                      |                    | 3.33                       | 4                  |
| $I_{DD}(PWM1PLL6)$  | Enab    | 6                | 0.5             | 0               | Disab              | 1                      | Disab              | 0.44                       | 0.53               |
| $I_{DD}(PWM6PLL6)$  |         |                  |                 |                 |                    | 6                      |                    | 2.81                       | 3.4                |
| $I_{DD}(PWM1HSI16)$ | Enab    | 16               | 0.5             | 0               | Disab              | 1                      | Disab              | 0.46                       | 0.56               |
| $I_{DD}(PWM6HSI16)$ |         |                  |                 |                 |                    | 6                      |                    | 2.63                       | 3.3                |
| $I_{DD}(PWM1HSI8)$  | Enab    | 8                | 0.5             | 0               | Disab              | 1                      | Disab              | 0.34                       | 0.41               |
| $I_{DD}(PWM6HSI8)$  |         |                  |                 |                 |                    | 6                      |                    | 2.12                       | 2.55               |
| $I_{DD}(PWM1HSI4)$  | Enab    | 4                | 0.5             | 0               | Disab              | 1                      | Disab              | 0.29                       | 0.35               |
| $I_{DD}(PWM6HSI4)$  |         |                  |                 |                 |                    | 6                      |                    | 1.78                       | 2.2                |
| $I_{DD}(PWM1HSI2)$  | Enab    | 2                | 0.5             | 0               | Disab              | 1                      | Disab              | 0.25                       | 0.3                |
| $I_{DD}(PWM6HSI2)$  |         |                  |                 |                 |                    | 6                      |                    | 1.60                       | 1.93               |

**Table 66. Peripheral supply current consumption at  $V_{DD}/V_{DDA} = 3.3\text{ V}$  (continued)**

| Symbol         | Clock |   |   |     | Peripherals |   |       | Consumption <sup>(9)</sup> |      |
|----------------|-------|---|---|-----|-------------|---|-------|----------------------------|------|
| $I_{DD}(ADC1)$ | Disab | 0 | 0 | 1   | Enab        | 0 | Disab | 1.55                       | 1.87 |
| $I_{DD}(ADC2)$ | Disab | 0 | 0 | 5.3 | Enab        | 0 | Disab | 1.59                       | 1.91 |
| $I_{DD}(ADC3)$ | Enab  | 0 | 0 | 6   | Enab        | 0 | Disab | 1.56                       | 1.88 |

- SMED frequency:
  - 96 MHz and 6 MHz frequencies require the PLL enabled.
  - Current table shows only a subset value of possible SMED frequencies.
- PWM frequency:
  - PWM toggle frequency is considered fixed to 500 kHz, close to the maximum applicative value.
- ADC frequency:
  - 6 MHz frequency requires the PLL enabled.
  - Current table shows only a subset value of possible ADC frequencies
- Number of active PWMs.
- PWM pins are loaded with a CL (load capacitance) of 50 pF.
- If enabled all DACs and comparator units are active.
- ADC configured in circular mode.
- Temperature operating:  $T_A = 25\text{ }^{\circ}\text{C}$ .
- Data based on characterization results not tested in production.

### IC peripheral current consumption (5 V)

**Table 67** summarizes the peripheral current consumption measured on  $V_{DD}/V_{DDA}$  supply pins.

**Table 67. Peripheral supply current consumption at  $V_{DD}/V_{DDA} = 5\text{ V}$** 

| Symbol              | Clock   |                  |                 |                 | Peripherals        |                      |                    | Consumption        |                    |
|---------------------|---------|------------------|-----------------|-----------------|--------------------|----------------------|--------------------|--------------------|--------------------|
| Op.<br>Mode         | PLL     | $f_{SMED}^{(1)}$ | $f_{PWM}^{(2)}$ | $f_{ADC}^{(3)}$ | ADC <sup>(7)</sup> | PWM <sup>(4,5)</sup> | ACU <sup>(6)</sup> | Typ <sup>(8)</sup> | Max <sup>(8)</sup> |
|                     | Enb/Dis | MHz              | MHz             | MHz             | Enb/Dis            | Num                  | Enb/Dis            | mA                 | mA                 |
| $I_{DD}(PLL)$       | Enab    | 0                | 0               | 0               | Disab              | 0                    | Disab              | 2.32               | 2.78               |
| $I_{DD}(ACU)$       | Disab   | 0                | 0               | 0               | Disab              | 0                    | Enab               | 2.22               | 2.66               |
| $I_{DD}(PWM1PLL96)$ | Enab    | 96               | 0.5             | 0               | Disab              | 1                    | Disab              | 1.81               | 2.17               |
| $I_{DD}(PWM6PLL96)$ |         |                  |                 |                 |                    | 6                    |                    | 10.49              | 12.59              |
| $I_{DD}(PWM1PLL48)$ | Enab    | 48               | 0.5             | 0               | Disab              | 1                    | Disab              | 1.18               | 1.42               |
| $I_{DD}(PWM6PLL48)$ |         |                  |                 |                 |                    | 6                    |                    | 6.88               | 8.26               |
| $I_{DD}(PWM1PLL24)$ | Enab    | 24               | 0.5             | 0               | Disab              | 1                    | Disab              | 0.79               | 0.95               |
| $I_{DD}(PWM6PLL24)$ |         |                  |                 |                 |                    | 6                    |                    | 4.73               | 5.68               |
| $I_{DD}(PWM1PLL12)$ | Enab    | 12               | 0.5             | 0               | Disab              | 1                    | Disab              | 0.58               | 0.7                |
| $I_{DD}(PWM6PLL12)$ |         |                  |                 |                 |                    | 6                    |                    | 3.66               | 4.4                |
| $I_{DD}(PWM1PLL6)$  | Enab    | 6                | 0.5             | 0               | Disab              | 1                    | Disab              | 0.49               | 0.6                |
| $I_{DD}(PWM6PLL6)$  |         |                  |                 |                 |                    | 6                    |                    | 3.11               | 3.75               |

Table 67. Peripheral supply current consumption at  $V_{DD}/V_{DDA} = 5\text{ V}$  (continued)

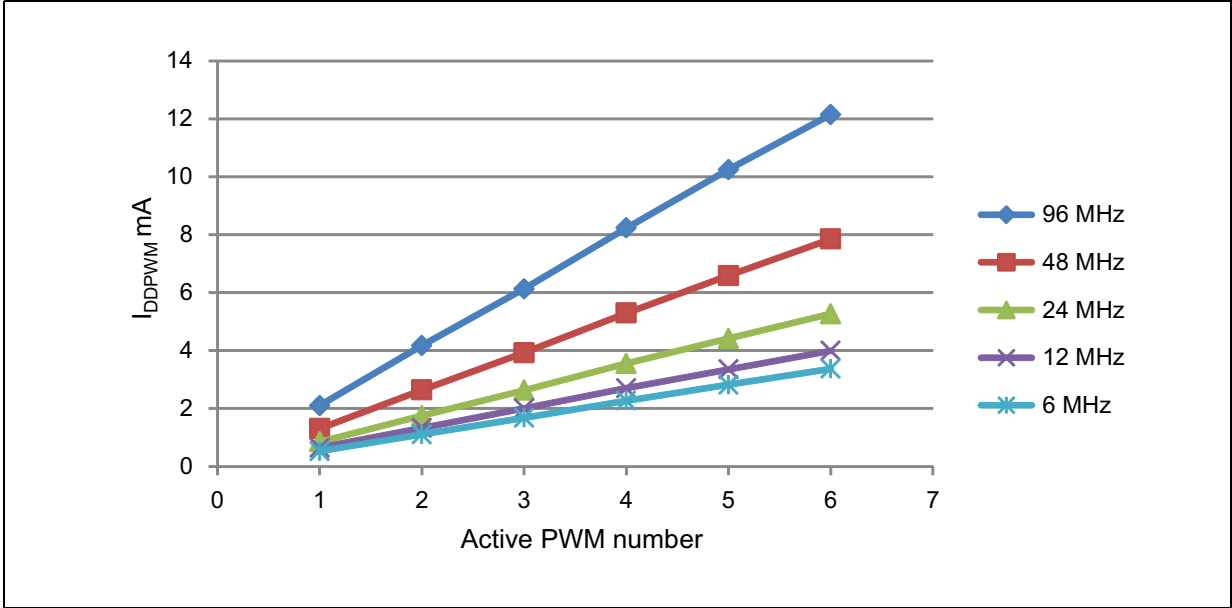
| Symbol              | Clock |    |     |     | Peripherals |   |       | Consumption |      |
|---------------------|-------|----|-----|-----|-------------|---|-------|-------------|------|
| $I_{DD}(PWM1HSI16)$ | Enab  | 16 | 0.5 | 0   | Disab       | 1 | Disab | 0.56        | 0.67 |
| $I_{DD}(PWM6HSI16)$ |       |    |     |     |             | 6 |       | 3.13        | 3.78 |
| $I_{DD}(PWM1HSI8)$  | Enab  | 8  | 0.5 | 0   | Disab       | 1 | Disab | 0.49        | 0.58 |
| $I_{DD}(PWM6HSI8)$  |       |    |     |     |             | 6 |       | 2.56        | 3.1  |
| $I_{DD}(PWM1HSI4)$  | Enab  | 4  | 0.5 | 0   | Disab       | 1 | Disab | 0.39        | 0.47 |
| $I_{DD}(PWM6HSI4)$  |       |    |     |     |             | 6 |       | 2.33        | 2.78 |
| $I_{DD}(PWM1HSI2)$  | Enab  | 2  | 0.5 | 0   | Disab       | 1 | Disab | 0.47        | 0.54 |
| $I_{DD}(PWM6HSI2)$  |       |    |     |     |             | 6 |       | 2.1         | 2.49 |
| $I_{DD}(ADC1)$      | Disab | 0  | 0   | 1   | Enab        | 0 | Disab | 2.11        | 2.54 |
| $I_{DD}(ADC2)$      | Disab | 0  | 0   | 5.3 | Enab        | 0 | Disab | 2.16        | 2.6  |
| $I_{DD}(ADC3)$      | Enab  | 0  | 0   | 6   | Enab        | 0 | Disab | 2.17        | 2.61 |

- SMED frequency:
  - 96 MHz and 6 MHz frequencies require the PLL enabled.
  - Current table shows only a subset value of possible SMED frequencies.
- PWM frequency:
  - PWM toggle frequency is considered fixed to 500 kHz, close to the maximum applicative value.
- ADC frequency:
  - 6 MHz frequency requires the PLL enabled.
  - Current table shows only a subset value of possible ADC frequencies.
- Number of active PWMs.
- PWM pins are loaded with a CL (load capacitance) of 50 pF.
- If enabled all DACs and comparator units are active.
- ADC configured in circular mode.
- Temperature operating:  $T_A = 25\text{ }^{\circ}\text{C}$ .
- Data based on characterization results not tested in production.

### PWM current consumption overview

From [Figure 13](#) to [Figure 16](#) provide an outline view of PWM current consumption results. The consumptions are evaluated considering the maximum current at  $T_A = 25\text{ }^{\circ}\text{C}$  with different SMED operating frequencies. The charts summarize the measurements carried out from [Table 66](#) and [Table 67](#) allowing users to derive the PWM current consumption values.

**Figure 13. PWM current consumption with  $f_{\text{SMED}} = \text{PLL}$   $f_{\text{PWM}} = 0.5\text{ MHz}$  at  $V_{\text{DD}}/V_{\text{DDA}} = 3.3\text{ V}$**



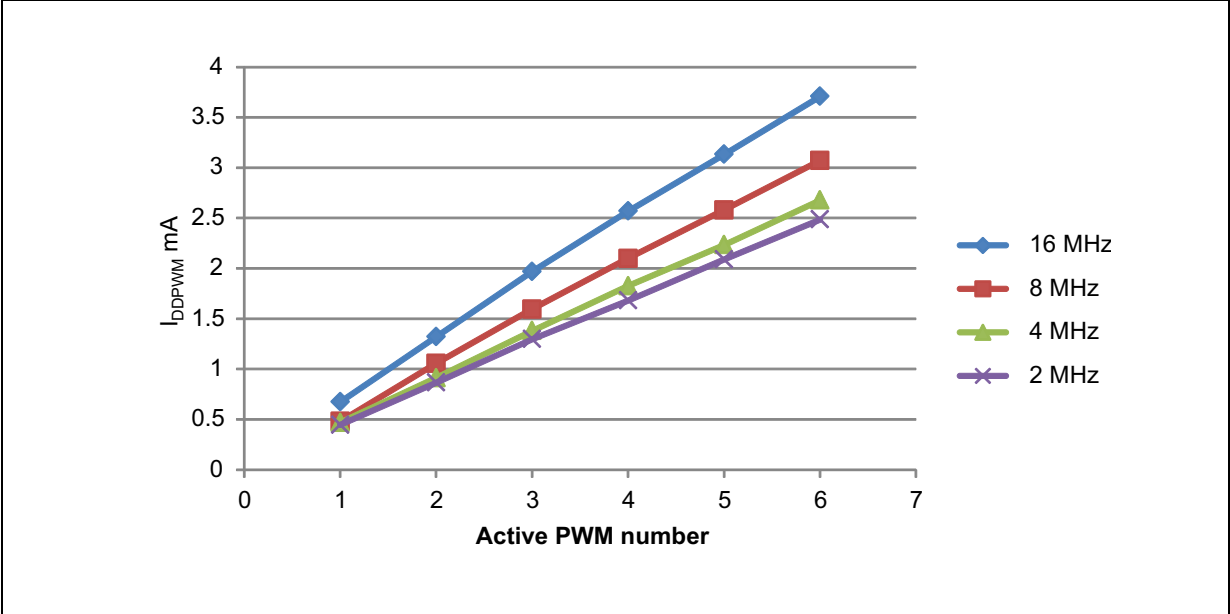
**Figure 14. PWM current consumption with  $f_{\text{SMED}} = \text{PLL}$   $f_{\text{PWM}} = 0.5\text{ MHz}$  at  $V_{\text{DD}}/V_{\text{DDA}} = 5\text{ V}$**



Figure 15. PWM current consumption with  $f_{SMED} = HSI$   $f_{PWM} = 0.5$  MHz at  $V_{DD}/V_{DDA} = 3.3$  V



Figure 16. PWM current consumption with  $f_{SMED} = HSI$   $f_{PWM} = 0.5$  MHz at  $V_{DD}/V_{DDA} = 5$  V





### 11.3.3 External clock sources and timing characteristics

#### HSE user external clock

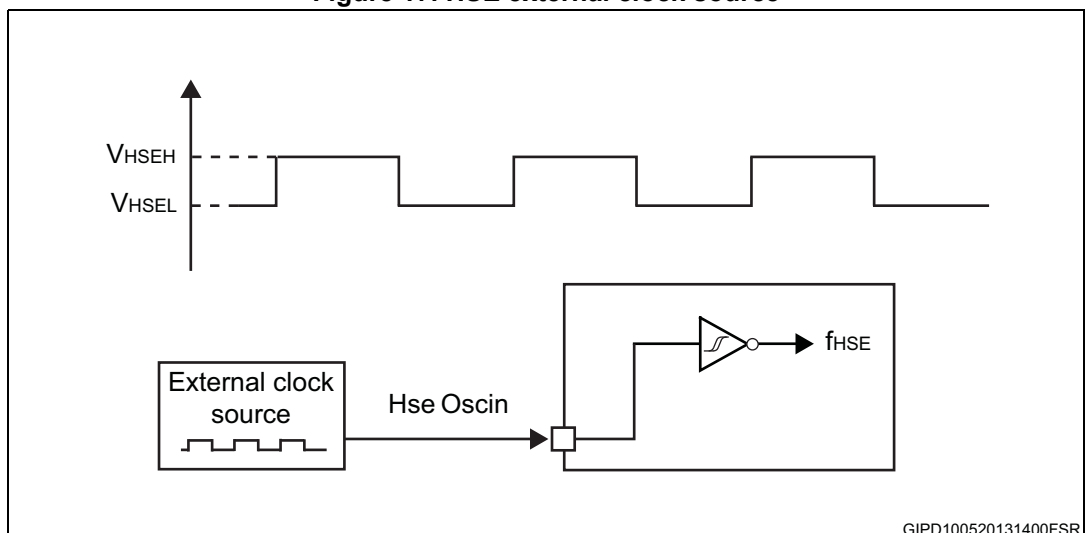
Subject to general operating conditions for  $V_{DD}$  and  $T_A$ .

**Table 68. HSE user external clock characteristics**

| Symbol              | Parameter                             | Conditions  | Min.                | Max.                | Unit          |
|---------------------|---------------------------------------|---|---------------------|---------------------|---------------|
| $f_{HSE\_ext}$      | User external clock source frequency  | $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ | 0                   | 16 <sup>(1)</sup>   | MHz           |
| $V_{HSEH}^{(2)}$    | HSEOSCIN input pin high level voltage |   | $0.7 \times V_{DD}$ | $V_{DD}$            | V             |
| $V_{HSEL}^{(2)}$    | HSEOSCIN input pin low level voltage  |   | $V_{SS}$            | $0.3 \times V_{DD}$ |               |
| $I_{LEAKHSE}^{(2)}$ | HSEOSCIN input pin leakage            | $V_{SS} \leq V_{IN} \leq V_{DD}$  | -1                  | +1                  | $\mu\text{A}$ |

1. In case  $f_{HSE}$  is configured as a direct clock for the SMED logics the maximum frequency can be 24 MHz.
2. Data based on characterization results, not tested in production.

**Figure 17. HSE external clock source**



#### HSE crystal/ceramic resonator oscillator

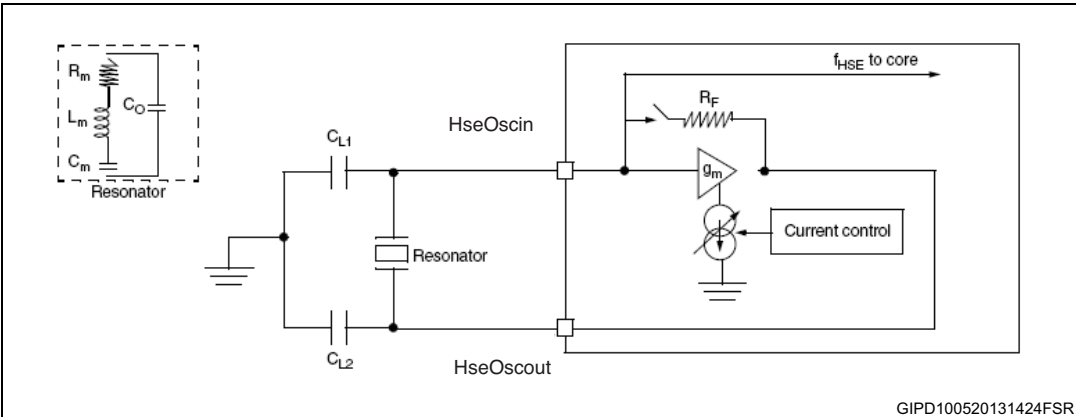
The HSE clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy, etc.).

Table 69. HSE crystal/ceramic resonator oscillator

| Symbol                          | Parameter                                   | Conditions             | Min. | Typ. | Max.                          | Unit |
|---------------------------------|---|------------------------|------|------|-------------------------------|------|
| $f_{HSE}$                       | External high speed oscillator frequency    |                        | 1    |      | 16 <sup>(1)</sup>             | MHz  |
| $R_F$                           | Feedback resistor                           |                        |      | 220  |                               | kΩ   |
| $C_{L1}, C_{L2}$ <sup>(2)</sup> | Recommended load capacitance <sup>(3)</sup> |                        |      |      | 20                            | pF   |
| $I_{DD(HSE)}$                   | HSE oscillator power consumption            |                        |      |      | 6 (startup)<br>2 (stabilized) | mA   |
| $g_m$                           | Oscillator transconductance                 |                        | 5    |      |                               | mA/V |
| $t_{SU(HSE)}$ <sup>(4)</sup>    | Startup time                                | $V_{DD}$ is stabilized |      | 2.8  |                               | ms   |

1. In case  $f_{HSE}$  is configured as a direct clock for the SMED logic the maximum frequency can be 24 MHz.
2. The oscillator needs two load capacitors, CL1 and CL2, to act as load for the crystal. The total load capacitance (Cload) is  $(CL1 * CL2)/(CL1 + CL2)$ . If  $CL1 = CL2$ , Cload =  $CL1 / 2$ . Some oscillators have built-in load capacitors, CL1 and CL2.
3. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small  $R_m$  value.
4.  $t_{SU(HSE)}$  is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



The crystal characteristics have to be checked with [Equation 3](#):

**Equation 3**

$$g_m \gg g_{mCritic}$$

where  $g_{mCritic}$  is calculated with the crystal parameters as follows:

**Equation 4**

$$g_{mCritic} = (2 \cdot \pi \cdot f_{HSE})^2 \cdot R_m (2C_O + C)$$

and where:

- $R_m$ : motional resistance<sup>(b)</sup>
- $L_m$ : motional inductance<sup>(b)</sup>
- $C_m$ : motional capacitance<sup>(b)</sup>
- $CO$ : shunt capacitance<sup>(b)</sup>
- $CL1 = CL2 = C$ : grounded external capacitance

### 11.3.4 Internal clock sources and timing characteristics

#### HSI RC oscillator

Subject to general operating conditions for  $V_{DD}$  and  $T_A$ .

**Table 70. HSI RC oscillator**

| Symbol        | Parameter   | Conditions   | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup> | Unit          |
|---------------|---|--|---------------------|------|---------------------|---------------|
| $f_{HSI}$     | Frequency   |  |                     | 16   |                     | MHz           |
| $ACC_{HSI}$   | Accuracy of HSI oscillator (factory calibrated) <sup>(1), (2)</sup> | $V_{DD} = 3.3\text{ V}$<br>$T_A = 25\text{ °C}$                        | -1%                 |      | +1%                 | %             |
|               |   | $V_{DD} = 3.3\text{ V}$<br>$-40\text{ °C} \leq T_A \leq 105\text{ °C}$ | -4%                 |      | +4%                 |               |
|               |   | $V_{DD} = 5\text{ V}$<br>$-40\text{ °C} \leq T_A \leq 105\text{ °C}$   | -4%                 |      | +4%                 |               |
| $t_{SU(HSI)}$ | HSI oscillator wakeup time including calibration                    |  |                     | 1    |                     | $\mu\text{s}$ |

1. Data based on characterization results, not tested in production.

2. Variation referred to  $f_{HSI}$  nominal value.

#### LSI RC oscillator

Subject to general operating conditions for  $V_{DD}$  and  $T_A$ .

**Table 71. LSI RC oscillator**

| Symbol        | Parameter                  | Conditions  | Min. <sup>(1)</sup> | Typ.  | Max. <sup>(1)</sup> | Unit          |
|---------------|----------------------------|---|---------------------|-------|---------------------|---------------|
| $f_{LSI}$     | Frequency                  |   |                     | 153.6 |                     | kHz           |
| $ACC_{LSI}$   | Accuracy of LSI oscillator | $3.3\text{ V} \leq V_{DD} \leq 5\text{ V}$<br>$-40\text{ °C} \leq T_A \leq 105\text{ °C}$ | -10%                |       | 10%                 | %             |
| $t_{SU(LSI)}$ | LSI oscillator wakeup time |   |                     | 7     |                     | $\mu\text{s}$ |

1. Guaranteed by design, not tested in production.

b. Refer to application crystal specification.

**PLL internal source clock****Table 72. PLL internal source clock**

| Symbol     | Parameter                      | Conditions  | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup> | Unit |
|------------|--------------------------------|---|---------------------|------|---------------------|------|
| $f_{IN}$   | Input frequency <sup>(2)</sup> | $3.3\text{ V} \leq V_{DD} \leq 5\text{ V}$<br>$-40\text{ °C} \leq T_A \leq 105\text{ °C}$ |                     | 16   |                     | MHz  |
| $f_{OUT}$  | Output frequency               |   |                     | 96   |                     |      |
| $t_{lock}$ | PLL lock time                  |   |                     |      | 200                 | μs   |

1. Data based on characterization results, not tested in production.

2. PLL maximum input frequency 16 MHz.

**11.3.5 Memory characteristics****Flash program and memory/data E<sup>2</sup>PROM memory**

General conditions:  $T_A = -40\text{ °C}$  to  $105\text{ °C}$ .

**Table 73. Flash program memory/data E<sup>2</sup>PROM memory**

| Symbol      | Parameter   | Conditions                | Min. <sup>(1)</sup> | Typ. | Max. | Unit   |
|-------------|---|---------------------------|---------------------|------|------|--------|
| $t_{PROG}$  | Standard programming time   |                           |                     | 6    | 6.6  | ms     |
|             | (including erase) for byte/word/block   |                           |                     |      |      |        |
|             | (1 byte/4 bytes/128 bytes)  |                           |                     |      |      |        |
|             | Fast programming time for 1 block (128 bytes)   |                           |                     | 3    | 3.3  |        |
| $t_{ERASE}$ | Erase time for 1 block (128 bytes)  |                           |                     | 3    | 3.3  | ms     |
| $N_{WE}$    | Erase/write cycles <sup>(2)</sup> (program memory)                                    | $T_A = 25\text{ °C}$      | 10 K                |      |      | Cycles |
|             | Erase/write cycles <sup>(2)</sup> (data memory)                                       | $T_A = 85\text{ °C}$      | 100 K               |      |      |        |
|             |   | $T_A = 105\text{ °C}$     | 35 K                |      |      |        |
| $t_{RET}$   | Data retention (program memory) after 10 K erase/write cycles at $T_A = 25\text{ °C}$ | $T_{RET} = 85\text{ °C}$  | 15                  |      |      | Years  |
|             | Data retention (program memory) after 10 K erase/write cycles at $T_A = 25\text{ °C}$ | $T_{RET} = 105\text{ °C}$ | 11                  |      |      |        |
|             | Data retention (data memory) after 100 K erase/write cycles at $T_A = 85\text{ °C}$   | $T_{RET} = 85\text{ °C}$  | 15                  |      |      |        |
|             | Data retention (data memory) after 35 K erase/write cycles at $T_A = 105\text{ °C}$   | $T_{RET} = 105\text{ °C}$ | 6                   |      |      |        |

1. Data based on characterization results, not tested in production.

2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

### 11.3.6 I/O port pin characteristics

Subject to general operating conditions for  $V_{DD}$  and  $T_A$  unless otherwise specified. Unused input pins should not be left floating.

**Table 74. Voltage DC characteristics**

| Symbol    | Description   | Min.                  | Typ. | Max.           | Unit |
|-----------|---|-----------------------|------|----------------|------|
| $V_{IL}$  | Input low voltage   | -0.3                  |      | $0.3 * V_{DD}$ | V    |
| $V_{IH}$  | Input high voltage <sup>(1)</sup>                                     | $0.7 * V_{DD}$        |      | $V_{DD}$       |      |
| $V_{OL1}$ | Output low voltage at 3.3 V <sup>(2), (3)</sup>                       |                       |      | $0.4^{(13)}$   |      |
| $V_{OL2}$ | Output low voltage at 5 V <sup>(2), (3)</sup>                         |                       |      | 0.5            |      |
| $V_{OL3}$ | Output low voltage high sink at 3.3 V / 5 V <sup>(1), (4), (5)</sup>  |                       |      | $0.6^{(13)}$   |      |
| $V_{OH1}$ | Output high voltage at 3.3 V <sup>(2), (3)</sup>                      | $V_{DD} - 0.4^{(13)}$ |      |                |      |
| $V_{OH2}$ | Output high voltage at 5 V <sup>(2), (3)</sup>                        | $V_{DD} - 0.5$        |      |                |      |
| $V_{OH3}$ | Output high voltage high sink at 3.3 V / 5 V <sup>(1), (4), (5)</sup> | $V_{DD} - 0.6^{(13)}$ |      |                |      |
| $H_{VS}$  | Hysteresis input voltage <sup>(6)</sup>                               | $0.1 * V_{DD}$        |      |                |      |
| $R_{PU}$  | Pull-up resistor  | 30                    | 45   | 60             | kΩ   |

1. All signals are not 5 V tolerant (input signals can't be exceeded  $V_{DDX}$  ( $V_{DDX} = V_{DD}, V_{DDA}$ )).
2. Parameter applicable to signals: GPIO0 [5:0] (high sink selectable by high speed config.).
3. Parameter applicable to signals: GPIO1 [5:0]/PWM [5:0].
4. Parameter applicable to signal: SWIM.
5. Parameter applicable to signal: DIGIN [0]/CCO\_clk.
6. Applicable to any digital inputs.

Table 75. Current DC characteristics

| Symbol           | Description   | Min. | Typ. | Max.     | Unit    |
|------------------|---|------|------|----------|---------|
| $I_{OL1}$        | Standard output low level current at 3.3 V and $V_{OL1}^{(1), (2)}$           |      |      | 1.5      | mA      |
| $I_{OL2}$        | Standard output low level current at 5 V and $V_{OL2}^{(1), (2)}$             |      |      | 3        |         |
| $I_{OLhs1}$      | High sink output low level current at 3.3 V and $V_{OL3}^{(1), (3), (4)}$     |      |      | 5        |         |
| $I_{OLhs2}$      | High sink output low level current at 5 V and $V_{OL3}^{(1), (3), (4)}$       |      |      | 7.75     |         |
| $I_{OH1}$        | Standard output high level current at 3.3 V and $V_{OH1}^{(1), (2)}$          |      |      | 1.5      |         |
| $I_{OH2}$        | Standard output high level current at 5 V and $V_{OH2}^{(1), (2)}$            |      |      | 3        |         |
| $I_{OHhs1}$      | High sink output high level current at 3.3 V and $V_{OH3}^{(1), (3), (4)}$    |      |      | 5        |         |
| $I_{OHhs2}$      | High sink output high level current at 5 V and $V_{OH3}^{(1), (3), (4)}$      |      |      | 7.75     |         |
| $I_{LKg}$        | Input leakage current digital - analog $V_{SS} \leq V_{IN} \leq V_{DD}^{(5)}$ |      |      | $\pm 1$  | $\mu A$ |
| $I_{Inj}$        | Injection current <sup>(6), (7)</sup>   |      |      | $\pm 4$  | mA      |
| $\Sigma I_{Inj}$ | Total injection current (sum of all I/O and control pins) <sup>(6)</sup>      |      |      | $\pm 20$ |         |

1. Parameter applicable to signals: GPIO0 [5:0] (high sink selectable by high speed config.).
2. Parameter applicable to signals: GPIO1 [5:0]/PWM [5:0].
3. Parameter applicable to signal: SWIM.
4. Parameter applicable to signal: DIGIN [0]/CCO\_clk.
5. Applicable to any digital inputs.
6. Maximum value must never be exceeded.
7. Negative injection current on the ADCIN [7:0] signals have to avoid since impact the ADC conversion accuracy.

Table 76. Operating frequency characteristics

| Symbol    | Description  | Min. | Typ. | Max. | Unit |
|-----------|--|------|------|------|------|
| $f_{IL1}$ | Digital input signal operating frequency <sup>(1), (2), (3)</sup>                    |      |      | 12   | MHz  |
| $f_{IH1}$ | Analog input signal operating frequency <sup>(4), (5)</sup>                          |      |      | 24   |      |
| $f_{IH2}$ | High speed input signal operating frequency <sup>(6), (7)</sup>                      |      |      | 128  |      |
| $f_{OL1}$ | Standard output signal operating frequency with 50 pF max. load <sup>(1)</sup>       |      |      | 2    |      |
| $f_{OL2}$ | High sink output signal operating frequency with 50 pF max. load <sup>(1), (2)</sup> |      |      | 10   |      |
| $f_{OH1}$ | High speed output signal operating frequency with 50 pF max. load <sup>(6)</sup>     |      |      | 12   |      |
| $f_{OH2}$ | High speed output signal operating frequency with 50 pF max. load <sup>(7)</sup>     |      |      | 32   |      |

1. Parameter applicable to signals: GPIO0 [5:0] (high sink selectable by high speed config.).
2. Parameter applicable to signal: SWIM.
3. Parameter applicable to signals: DIGIN [5:1].
4. Parameter applicable to signals: GPIO0 [3:2] when configured as HSE\_Oscin/Oscout.
5. Parameter applicable to any analog signals: ADCIN [7:0], CPP [3:0] and CPM3.
6. Parameter applicable to signals: GPIO1 [5:0]/PWM [5:0].
7. Parameter applicable to signal: DIGIN [0]/CCO\_clk.

### 11.3.7 Reset pin characteristics

Subject to general operating conditions for  $V_{DD}$  and  $T_A$  unless otherwise specified.

**Table 77. NRST pin characteristics**

| Symbol           | Parameter                                    | Conditions              | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup> | Unit          |
|------------------|--|-------------------------|---------------------|------|---------------------|---------------|
| $V_{IL(NRST)}$   | NRST input low level voltage <sup>(1)</sup>  |                         | -0.3                |      | $0.3 \times V_{DD}$ | V             |
| $V_{IH(NRST)}$   | NRST input high level voltage <sup>(1)</sup> |                         | $0.7 \times V_{DD}$ |      | $V_{DD} + 0.3$      |               |
| $V_{OL(NRST)}$   | NRST output low level voltage <sup>(1)</sup> | $I_{OL} = 2 \text{ mA}$ |                     |      | 0.5                 |               |
| $R_{PU(NRST)}$   | NRST pull-up resistor <sup>(2)</sup>         |                         | 30                  | 40   | 60                  | k $\Omega$    |
| $t_{IFP(NRST)}$  | NRST input filtered pulse <sup>(3)</sup>     |                         |                     |      | 75                  | ns            |
| $t_{INFP(NRST)}$ | NRST not input filtered pulse <sup>(3)</sup> |                         | 500                 |      |                     |               |
| $t_{OP(NRST)}$   | NRST output filtered pulse <sup>(3)</sup>    |                         | 15                  |      |                     | $\mu\text{s}$ |

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

### 11.3.8 I<sup>2</sup>C interface characteristics

Table 78. I<sup>2</sup>C interface characteristics

| Symbol                | Parameter   | Standard mode       |                     | Fast mode <sup>(1)</sup> |                     | Unit    |
|-----------------------|---|---------------------|---------------------|--------------------------|---------------------|---------|
|                       |   | Min. <sup>(2)</sup> | Max. <sup>(2)</sup> | Min. <sup>(2)</sup>      | Max. <sup>(2)</sup> |         |
| $t_{w(SCLL)}$         | SCL clock low time  | 4.7                 |                     | 1.3                      |                     | $\mu s$ |
| $t_{w(SCLH)}$         | SCL clock high time   | 4.0                 |                     | 0.6                      |                     |         |
| $t_{su(SDA)}$         | SDA setup time  | 250                 |                     | 100                      |                     | ns      |
| $t_h(SDA)$            | SDA data hold time  | 0 <sup>(3)</sup>    |                     | 0 <sup>(3)</sup>         | 900 <sup>(3)</sup>  |         |
| $t_r(SDA) \ t_r(SCL)$ | SDA and SCL rise time ( $V_{DD} = 3.3$ to $5\text{ V}$ ) <sup>(4)</sup> |                     | 1000                |                          | 300                 |         |
| $t_f(SDA) \ t_f(SCL)$ | SDA and SCL fall time ( $V_{DD} = 3.3$ to $5\text{ V}$ ) <sup>(4)</sup> |                     | 300                 |                          | 300                 |         |
| $t_h(STA)$            | START condition hold time   | 4.0                 |                     | 0.6                      |                     | $\mu s$ |
| $t_{su(STA)}$         | Repeated START condition setup time                                     | 4.7                 |                     | 0.6                      |                     |         |
| $t_{su(STO)}$         | STOP condition setup time   | 4.0                 |                     | 0.6                      |                     | $\mu s$ |
|                       |   |                     |                     |                          |                     |         |
|                       |   |                     |                     |                          |                     |         |
| $t_{w(STO:STA)}$      | STOP to START condition time (bus free)                                 | 4.7                 |                     | 1.3                      |                     | $\mu s$ |
| $C_b$                 | Capacitive load for each bus line <sup>(5)</sup>                        |                     | 50                  |                          | 50                  | pF      |

1.  $f_{MASTER}$  must be at least 8 MHz to achieve maximum fast I<sup>2</sup>C speed (400 kHz).
2. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time.
4. I<sup>2</sup>C multifunction signals require the high sink pad configuration and the interconnection of 1 K $\Omega$  pull-up resistances.
5. 50 pF is the maximum load capacitance value to meet the I<sup>2</sup>C std timing specifications.



### 11.3.9 10-bit Sar ADC characteristics

Subject to general operating conditions for  $V_{DDA}$ ,  $f_{MASTER}$ , and  $T_A$  unless otherwise specified.

**Table 79. ADC characteristics**

| Symbol      | Parameter  | Conditions        | Min. | Typ.  | Max.                       | Unit       |
|-------------|--|-------------------|------|-------|----------------------------|------------|
| N           | Resolution   |                   |      | 10    |                            | bit        |
| $R_{ADCIN}$ | ADC input impedance                                |                   | 1    |       |                            | M $\Omega$ |
| $f_{ADC}$   | ADC Clock frequency                                |                   | 1    |       | 6 <sup>(1)</sup>           | MHz        |
| $V_{IN1}$   | Conversion voltage range for gain x1               |                   | 0    |       | 1.25 <sup>(2), (3)</sup>   |            |
| $V_{IN2}$   | Conversion voltage range for gain x4               |                   | 0    |       | 0.3125 <sup>(2), (3)</sup> |            |
| $V_{ref}$   | ADC main reference voltage <sup>(4)</sup>          |                   |      | 1.250 |                            | V          |
| $t_S$       | Sampling time                                      | $f_{ADC} = 6$ MHz |      | 0.50  |                            | $\mu s$    |
| $t_{STAB}$  | Wakeup time from ADC standby                       |                   |      | 30    |                            |            |
| $t_{CONV1}$ | Single conversion time including sampling time     | $f_{ADC} = 6$ MHz |      | 2.42  |                            |            |
| $t_{CONV2}$ | Continuous conversion time including sampling time | $f_{ADC} = 6$ MHz |      | 3     |                            |            |

1. Frequency generated selecting the PLL source clock.
2. Maximum input analog voltage cannot exceed  $V_{DDA}$ .
3. Exceeding the maximum voltage on the ADCIN [7:0] signals for the related conversion scale must be avoided since the ADC conversion accuracy can be impacted.
4. ADC reference voltage at  $T_A = 25$  °C.

ADC accuracy characteristics at  $V_{DD}/V_{DDA}$  3.3 VTable 80. ADC accuracy characteristics at  $V_{DD}/V_{DDA}$  3.3 V

| Symbol    | Parameter   | Conditions <sup>(1)</sup>           | Typ. <sup>(2)</sup> | Min. <sup>(3)</sup> | Max. <sup>(3)</sup> | Unit |
|-----------|---|-------------------------------------|---------------------|---------------------|---------------------|------|
| $ E_T $   | Total unadjusted error <sup>(4), (5), (6)</sup>       | $f_{ADC} = 6 \text{ MHz}$<br>gain 1 | 2.8                 |                     |                     | LSB  |
| $ E_O $   | Offset error <sup>(4), (5), (6)</sup>                 |                                     | 0.3                 |                     |                     |      |
| $ E_G $   | Gain error <sup>(4), (5), (6), (7)</sup>              |                                     | 0.4                 |                     |                     |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (8)</sup>               |                                     |                     | -8.5                | 9.3                 |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (9)</sup>               |                                     |                     | -11                 | 11                  |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (10)</sup>              |                                     |                     | -14.3               | 11.3                |      |
| $ E_D $   | Differential linearity error <sup>(2), (3), (4)</sup> |                                     |                     |                     | 0.5                 |      |
| $ E_L $   | Integral linearity error <sup>(4), (5), (6)</sup>     |                                     |                     |                     | 1.4                 |      |
| $ E_T $   | Total unadjusted error <sup>(4), (5), (6)</sup>       | $f_{ADC} = 6 \text{ MHz}$<br>gain 4 | 2.8                 |                     |                     |      |
| $ E_O $   | Offset error <sup>(4), (5), (6)</sup>                 |                                     | 0.3                 |                     |                     |      |
| $ E_G $   | Gain error <sup>(4), (5), (6), (7)</sup>              |                                     | 0.4                 |                     |                     |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (8)</sup>               |                                     |                     | -12.7               | 15.5                |      |
| $E_{O+G}$ | Offset + gain error <sup>(5), (9)</sup>               |                                     |                     | -16.7               | 18.8                |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (10)</sup>              |                                     |                     | -19.2               | 18.8                |      |
| $ E_D $   | Differential linearity error <sup>(4), (5), (6)</sup> |                                     |                     |                     | 0.5                 |      |
| $ E_L $   | Integral linearity error <sup>(4), (5), (6)</sup>     |                                     |                     |                     | 1.4                 |      |

1. Measured with  $R_{AIN} < 10 \text{ k}\Omega$  ( $R_{AIN}$  external series resistance interconnected between the AC signal generator and the ADC input pin).
2. Temperature operating:  $T_A = 25^\circ\text{C}$ .
3. Data based on characterization results, not tested in production.
4. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject the negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage  $V_{IN1}$  or  $V_{IN2}$ .
5. Results in manufacturing test mode.
6. Data aligned with trimming voltage parameters.
7. Gain error evaluation with two point method.
8. Temperature operating range:  $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ .
9. Temperature operating range:  $-25^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ .
10. Temperature operating range:  $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ .

ADC accuracy characteristics at  $V_{DD}/V_{DDA}$  5 VTable 81. ADC accuracy characteristics at  $V_{DD}/V_{DDA}$  5 V

| Symbol    | Parameter   | Conditions <sup>(1)</sup>           | Typ. <sup>(2)</sup> | Min. <sup>(3)</sup> | Max. <sup>(3)</sup> | Unit |
|-----------|---|-------------------------------------|---------------------|---------------------|---------------------|------|
| $ E_T $   | Total unadjusted error <sup>(4), (5), (6)</sup>       | $f_{ADC} = 6 \text{ MHz}$<br>gain 1 | TBD                 |                     |                     | LSB  |
| $ E_O $   | Offset error <sup>(4), (5), (6)</sup>                 |                                     | 0.5                 |                     |                     |      |
| $ E_G $   | Gain error <sup>(4), (5), (6), (7)</sup>              |                                     | 0.4                 |                     |                     |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (8)</sup>               |                                     |                     | -8.3                | 8.9                 |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (9)</sup>               |                                     |                     | -10.9               | 10.9                |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (10)</sup>              |                                     |                     | -13.8               | 10.9                |      |
| $ E_D $   | Differential linearity error <sup>(2), (3), (4)</sup> |                                     | 0.8                 |                     |                     |      |
| $ E_L $   | Integral linearity error <sup>(4), (5), (6)</sup>     |                                     | 2.0                 |                     |                     |      |
| $ E_T $   | Total unadjusted error <sup>(4), (5), (6)</sup>       | $f_{ADC} = 6 \text{ MHz}$<br>gain 4 | TBD                 |                     |                     |      |
| $ E_O $   | Offset error <sup>(4), (5), (6)</sup>                 |                                     | 1.2                 |                     |                     |      |
| $ E_G $   | Gain error <sup>(4), (5), (6), (7)</sup>              |                                     | 0.2                 |                     |                     |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (8)</sup>               |                                     |                     | -12.2               | 15.3                |      |
| $E_{O+G}$ | Offset + gain error <sup>(5), (9)</sup>               |                                     |                     | -16.4               | 18.5                |      |
| $E_{O+G}$ | Offset + gain error <sup>(7), (10)</sup>              |                                     |                     | -18.8               | 18.5                |      |
| $ E_D $   | Differential linearity error <sup>(4), (5), (6)</sup> |                                     | 0.8                 |                     |                     |      |
| $ E_L $   | Integral linearity error <sup>(4), (5), (6)</sup>     |                                     | 2.0                 |                     |                     |      |

1. Measured with  $R_{AIN} < 10 \text{ k}\Omega$  ( $R_{AIN}$  external series resistance interconnected between the AC signal generator and the ADC input pin).
2. Temperature operating:  $T_A = 25 \text{ }^\circ\text{C}$ .
3. Data based on characterization results, not tested in production.
4. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for  $I_{INJ(PIN)}$  and  $\Sigma I_{INJ(PIN)}$  in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage  $V_{IN1}$  or  $V_{IN2}$ .
5. Results in manufacturing test mode.
6. Data aligned with trimming voltage parameters.
7. Gain error evaluation with two point method.
8. Temperature operating range:  $0 \text{ }^\circ\text{C} \leq T_A \leq 85 \text{ }^\circ\text{C}$ .
9. Temperature operating range:  $-25 \text{ }^\circ\text{C} \leq T_A \leq 105 \text{ }^\circ\text{C}$ .
10. Temperature operating range:  $-40 \text{ }^\circ\text{C} \leq T_A \leq 105 \text{ }^\circ\text{C}$ .

### 11.3.10 Analog comparator characteristics

Table 82. Analog comparator characteristics

| Symbol              | Parameter                                 | Conditions                       | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup>    | Unit |
|---------------------|---|----------------------------------|---------------------|------|------------------------|------|
| V <sub>IN</sub>     | Comparator input voltage range            | -40 °C ≤ T <sub>A</sub> ≤ 105 °C | 0                   |      | 1.23 <sup>(2)</sup>    | V    |
| V <sub>ICPM3</sub>  | Comparator 3 external input voltage range |                                  | 0                   |      | 1.23 <sup>(2)(3)</sup> | V    |
| V <sub>offset</sub> | Comparator offset error                   |                                  |                     |      | 15                     | mV   |
| t <sub>COMP</sub>   | Comparison delay time                     |                                  |                     |      | 50                     | ns   |

1. Data based on characterization results, not tested in production.
2. Maximum analog input voltage cannot exceed V<sub>DDA</sub>.
3. The comparator 3 can be configured with the external reference voltage signal CPM3.

### 11.3.11 DAC characteristics

Table 83. DAC characteristics

| Symbol                  | Parameter              | Conditions                       | Min. <sup>(1)</sup> | Typ. | Max. <sup>(1)</sup>     | Unit |
|-------------------------|------------------------|----------------------------------|---------------------|------|-------------------------|------|
| V <sub>full scale</sub> | DAC full scale         | -40 °C ≤ T <sub>A</sub> ≤ 105 °C | 1.2                 |      | 1.26                    | V    |
| V <sub>offset</sub>     | DAC offset             |                                  |                     |      | 4                       | mV   |
| V <sub>dac</sub>        | DAC out voltage        |                                  | V <sub>offset</sub> |      | V <sub>full scale</sub> | mV   |
| LSB                     |                        |                                  |                     | 82   |                         | mV   |
| INL                     | Integral non linearity |                                  |                     |      | 0.12                    | LSB  |

1. Data based on characterization results, not tested in production.

#### Equation 5

$$n[0,15]:V_{dac}(n) = \frac{(V_{fullscale} - V_{offset})}{15} \times (n) + V_{offset}$$

#### Equation 6

$$n[1-14]:V_{dac}(n) = \frac{(V_{fullscale} - V_{offset})}{15} \times (n + INL) + V_{offset}$$

where:

- V<sub>fullscale</sub> = V<sub>fullscale</sub> (sample, T)
- V<sub>offset</sub> = V<sub>offset</sub> (sample, T)
- INL = INL (sample, n)

## 11.4 EMC characteristics

### 11.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \* (n + 1) supply pin).

**Table 84. ESD absolute maximum ratings**

| Symbol                | Ratings   | Conditions   | Maximum value | Unit |
|-----------------------|---|--|---------------|------|
| $V_{\text{ESD(HBM)}}$ | Electrostatic discharge voltage (human body model)    | $T_A = 25\text{ }^{\circ}\text{C}$ , conforming to JEDEC/JESD22-A114E      | 2000          | V    |
| $V_{\text{ESD(CDM)}}$ | Electrostatic discharge voltage (charge device model) | $T_A = 25\text{ }^{\circ}\text{C}$ , conforming to ANSI/ESD STM 5.3.1 ESDA | 500           |      |
| $V_{\text{ESD(MM)}}$  | Electrostatic discharge voltage (machine model)       | $T_A = 25\text{ }^{\circ}\text{C}$ , conforming to JEDEC/JESD-A115-A       | 200           |      |

### 11.4.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.

**Table 85. Electrical sensitivity**

| Symbol | Parameter             | Conditions                          | Level |
|--------|-----------------------|-------------------------------------|-------|
| LU     | Static latch-up class | $T_A = 105\text{ }^{\circ}\text{C}$ | A     |

## 12 Thermal characteristics

The STLUX385A functionality cannot be guaranteed when the device is operating under the maximum chip junction temperature ( $T_{Jmax}$ ).

$T_{Jmax}$ , in degrees Celsius, may be calculated using [Equation 7](#):

### Equation 7

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

$T_{Amax}$  is the maximum ambient temperature in °C

$\Theta_{JA}$  is the package junction to ambient thermal resistance in °C/W

$P_{Dmax}$  is the sum of  $P_{INTmax}$  and  $P_{I/Omax}$  ( $P_{Dmax} = P_{INTmax} + P_{I/Omax}$ )

$P_{INTmax}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in watts. This is the maximum chip internal power.

$P_{I/Omax}$  represents the maximum power dissipation on output pins where:

$$P_{I/Omax} = \Sigma (V_{OL} * I_{OL}) + \Sigma ((V_{DD} - V_{OH}) * I_{OH}),$$

taking into account the actual  $V_{OL}/I_{OL}$  and  $V_{OH}/I_{OH}$  of the I/Os at low and high level.

**Table 86. Package thermal characteristics**

| Symbol        | Parameter   | Value | Unit |
|---------------|---|-------|------|
| $\Theta_{JA}$ | Thermal resistance junction to ambient <sup>(1)</sup> | 80    | °C/W |

1. Thermal resistance is based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

## 13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 19. TSSOP8 package outline

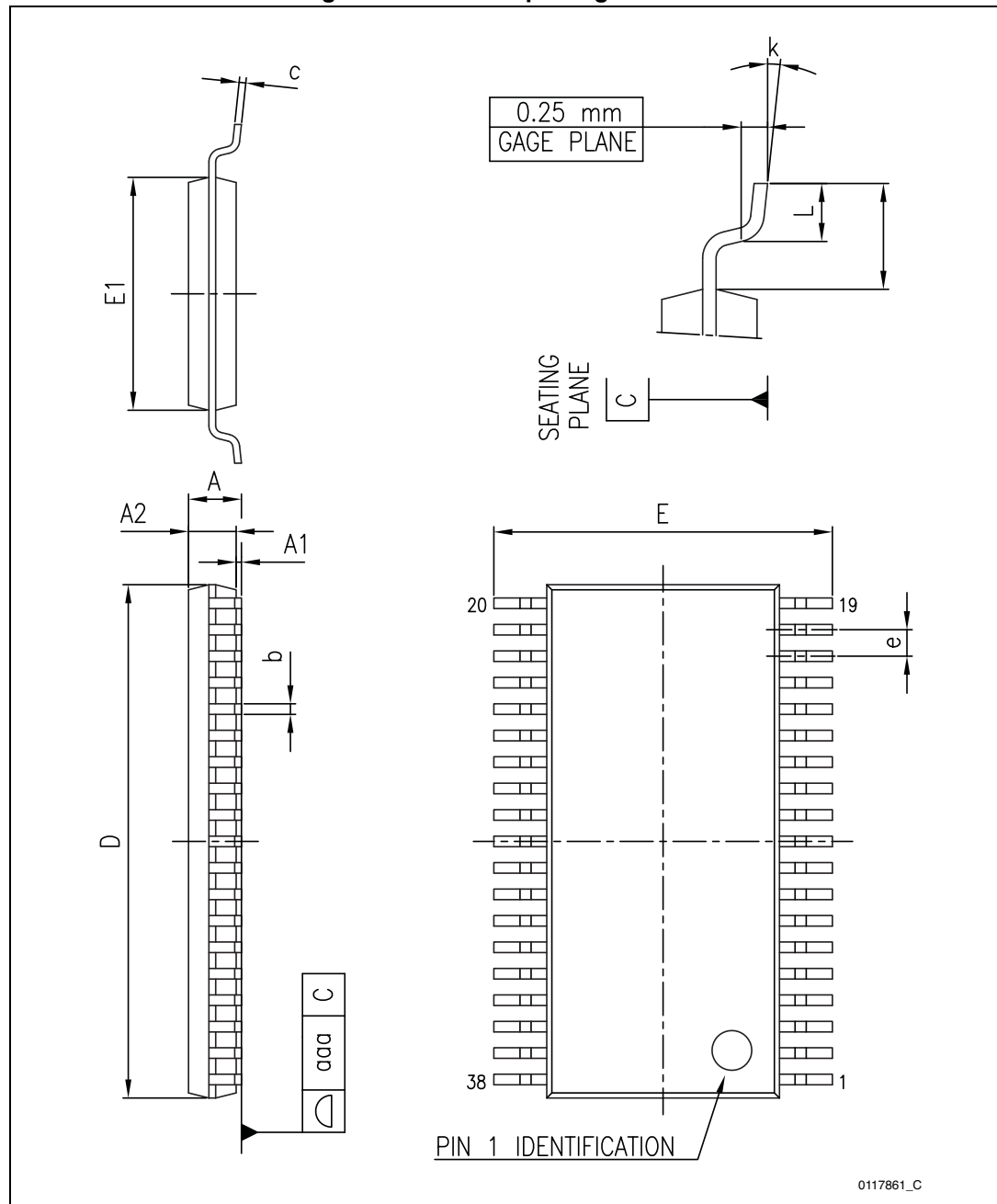


Table 87. TSSOP38 mechanical data

| Symbol | Dimensions (mm) |      |      |
|--------|-----------------|------|------|
|        | Min.            | Typ. | Max. |
| A      |                 |      | 1.20 |
| A1     | 0.05            |      | 0.15 |
| A2     | 0.80            | 1.00 | 1.05 |
| b      | 0.17            |      | 0.27 |
| c      | 0.09            |      | 0.20 |
| D      | 9.60            | 9.70 | 9.80 |
| E      | 6.20            | 6.40 | 6.60 |
| E1     | 4.30            | 4.40 | 4.50 |
| e      |                 | 0.50 |      |
| L      | 0.45            | 0.60 | 0.75 |
| L1     |                 | 1.00 |      |
| k      | 0               |      | 8    |
| aaa    |                 |      | 0.10 |



## 14 STLUX385A development tools

The development tool for the STLUX385A microcontroller is provided by Raisonance with the C compiler and the integrated development environment (IIDE 7), which provides start-to-finish control of application development including code editing, compilation, optimization and debugging.

The hardware tool includes the RLink in-circuit debugger/programmer (USB/JTAG).

## 15 Order codes

Table 88. Ordering information

| Order code  | Package | Packaging     |
|-------------|---------|---------------|
| STLUX385A   | TSSOP38 | Tube          |
| STLUX385ATR |         | Tape and reel |

## 16 Revision history

**Table 89. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 04-Apr-2013 | 1        | Initial release.   |
| 06-Jun-2013 | 2        | Document status promoted from preliminary to production data.  |
| 09-Jan-2014 | 3        | <p>Updated <a href="#">Section 1: Description on page 9</a> (replaced MASTERLUX™ by STLUX™, minor modifications).</p> <p>Updated <a href="#">Section : Documentation on page 10</a> (replaced PM0047 programming manual by PM0051 programming manual).</p> <p>Minor modifications in <a href="#">Figure 1 on page 11</a>.</p> <p>Updated <a href="#">Section 6.5 on page 35</a> (added titles from <a href="#">Table 7</a> to <a href="#">Table 10</a>).</p> <p>Updated <a href="#">Section 7.1: Memory map overview on page 38</a> (added cross-reference to <a href="#">Table 11</a>).</p> <p>Updated <a href="#">Section 9.2 on page 56</a> (added titles from <a href="#">Table 34</a> to <a href="#">Table 56</a>, added title of <a href="#">Section : nAFR_IOMXP2 (alternative Port2 configuration register protection) on page 63</a>, minor modifications in register titles).</p> <p>Updated <a href="#">Table 64 on page 74</a> (updated/renumbered notes and references to notes below <a href="#">Table 64</a>).</p> <p>Updated <a href="#">Section : IC low power current consumption on page 75</a> (removed superfluous note).</p> <p>Removed Section 11.3.7 Typical output curves from page 87.</p> <p>Updated <a href="#">Table 79: ADC characteristics on page 89</a> (updated note 4. - replaced the original note by: "ADC reference voltage at T<sub>A</sub> = 25 °C.").</p> <p>Updated <a href="#">Section 13: Package information on page 95</a> (updated titles, header of <a href="#">Table 87</a>, reversed order of <a href="#">Figure 19</a> and <a href="#">Table 87</a>).</p> <p>Minor modifications throughout document.</p> |

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