

## FDS7296N3

### 30V N-Channel PowerTrench® MOSFET

#### General Description

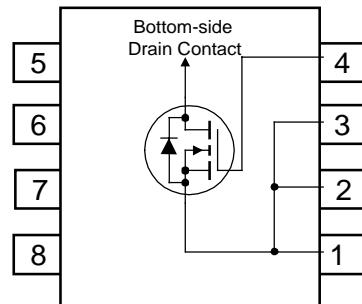
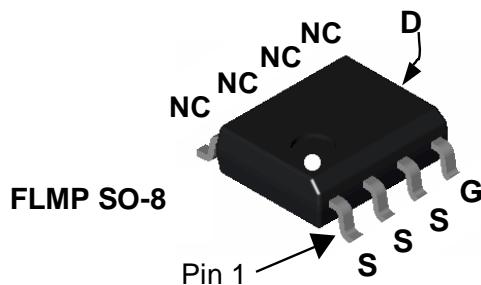
This N-Channel MOSFET in the thermally enhanced SO8 FLMP package has been designed specifically to improve the overall efficiency of DC/DC converters. Providing a balance of low  $R_{DS(ON)}$  and  $Q_g$  it is ideal for synchronous rectifier applications in both isolated and non-isolated topologies. It is also well suited for high and low side switch applications in Point of Load converters.

#### Applications

- Secondary side Synchronous rectifier
- Synchronous Buck VRM and POL Converters

#### Features

- 15 A, 30 V  $R_{DS(ON)} = 8 \text{ m}\Omega$  @  $V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 11 \text{ m}\Omega$  @  $V_{GS} = 4.5 \text{ V}$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Optimized for low  $Q_{gd}$  to enable fast switching and reduced  $CdV/dt$  gate coupling.
- SO-8 FLMP for enhanced thermal performance in an industry-standard package outline.



#### Absolute Maximum Ratings

$T_A=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a)	15	A
	– Pulsed	60	
$P_D$	Power Dissipation for Single Operation (Note 1a)	3.0	W
	(Note 1b)	1.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.5	°C/W

#### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS7296N3	FDS7296N3	13"	12mm	2500 units

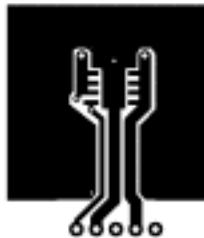
## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain-Source Avalanche Ratings</b>						
$W_{DSS}$	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 27\text{ V}$ , $I_D = 15\text{ A}$			189	$\text{mJ}$
$I_{AR}$	Drain-Source Avalanche Current				15	$\text{A}$
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			$\text{V}$
$\Delta BV_{DSS}$ $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		28		$\text{mV/}^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	$\text{nA}$
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.8	3	$\text{V}$
$\Delta V_{GS(th)}$ $\Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.5		$\text{mV/}^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 13\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$ , $T_J = 125^\circ\text{C}$		6.5 8.2 9.7	8 11 13	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 15\text{ A}$		58		$\text{S}$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		1540		$\text{pF}$
$C_{oss}$	Output Capacitance			430		$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance			140		$\text{pF}$
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}$ , $f = 1.0\text{ MHz}$		1.0		$\Omega$
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\Omega$		10	20	$\text{ns}$
$t_r$	Turn-On Rise Time			4	9	$\text{ns}$
$t_{d(off)}$	Turn-Off Delay Time			27	44	$\text{ns}$
$t_f$	Turn-Off Fall Time			14	25	$\text{ns}$
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}$ , $I_D = 15\text{ A}$ , $V_{GS} = 5\text{ V}$		12.7	18	$\text{nC}$
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}$ , $I_D = 15\text{ A}$ , $V_{GS} = 10\text{ V}$		23	32	$\text{nC}$
$Q_{gs}$	Gate-Source Charge			4.2		$\text{nC}$
$Q_{gd}$	Gate-Drain Charge			3.5		$\text{nC}$
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				2.5	$\text{A}$
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.5\text{ A}$ (Note 2)		0.7	1.2	$\text{V}$
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 15\text{ A}$ , $d_I/dt = 100\text{ A}/\mu\text{s}$		27		$\text{nS}$
$Q_{rr}$	Diode Reverse Recovery Charge			19		$\text{nC}$

**Notes:**

1.  $R_{\text{thJA}}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\text{thJC}}$  is guaranteed by design while  $R_{\text{thCA}}$  is determined by the user's board design.



a) 40°C/W when  
mounted on a 1in<sup>2</sup> pad  
of 2 oz copper



b) 85°C/W when mounted on  
a minimum pad of 2 oz  
copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics

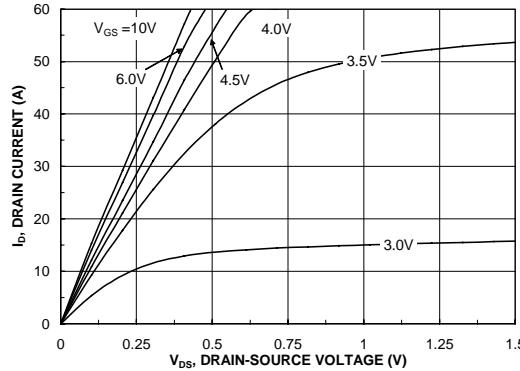


Figure 1. On-Region Characteristics.

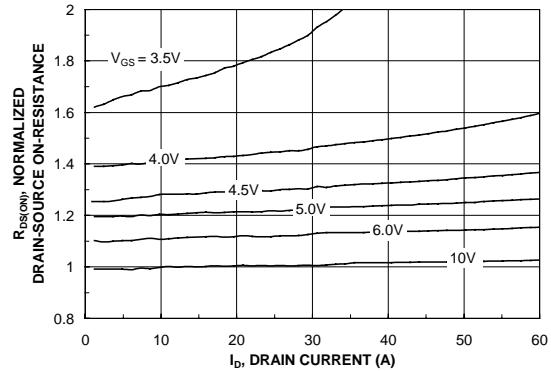


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

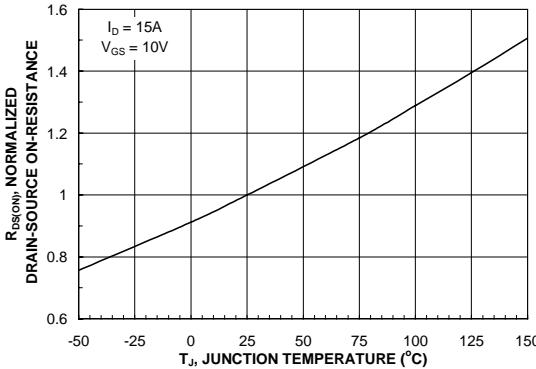


Figure 3. On-Resistance Variation with Temperature.

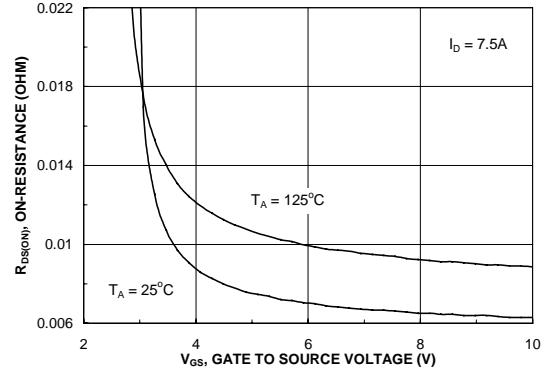


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

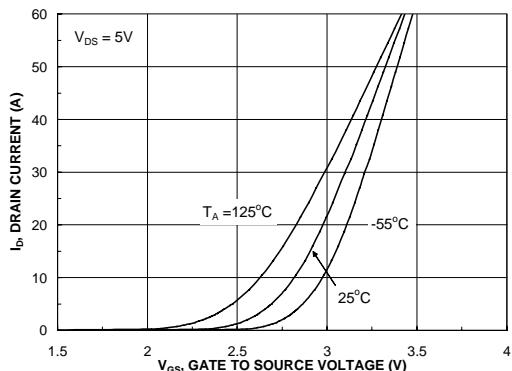


Figure 5. Transfer Characteristics.

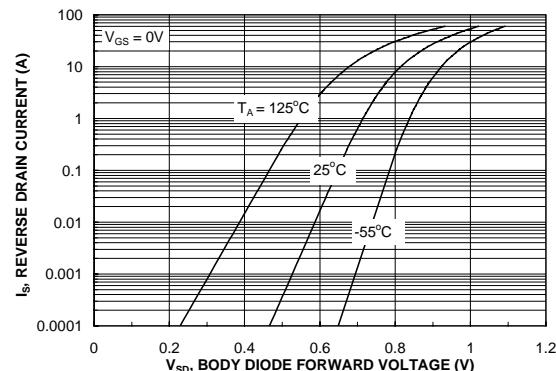


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

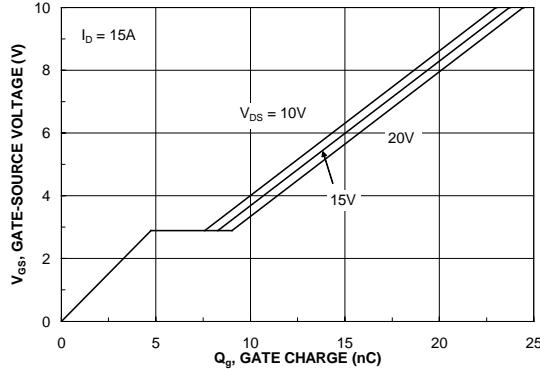


Figure 7. Gate Charge Characteristics.

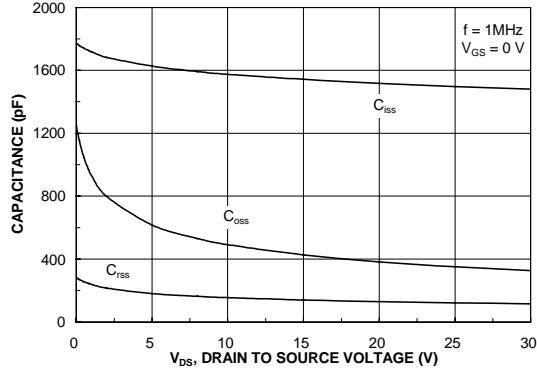


Figure 8. Capacitance Characteristics.

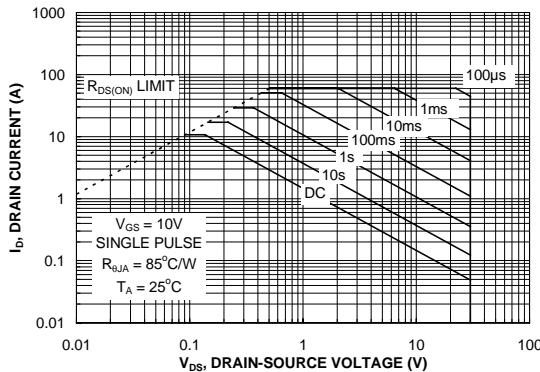


Figure 9. Maximum Safe Operating Area.

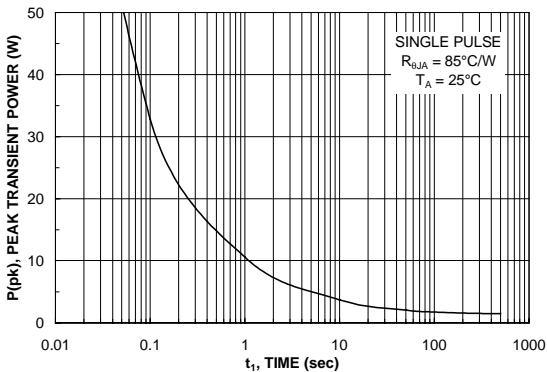


Figure 10. Single Pulse Maximum Power Dissipation.

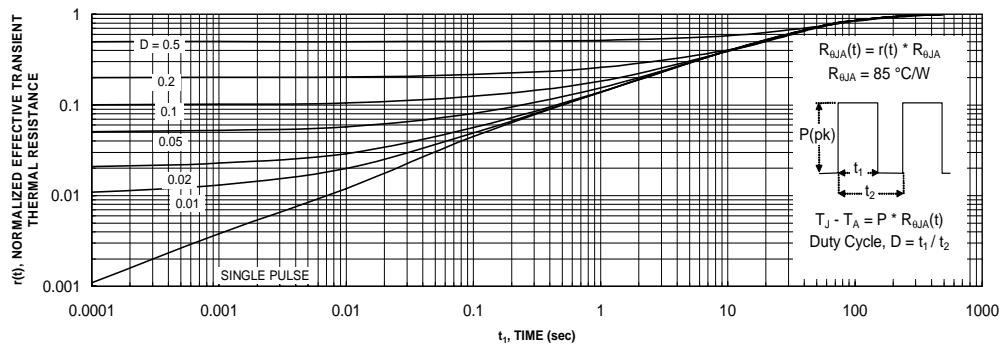
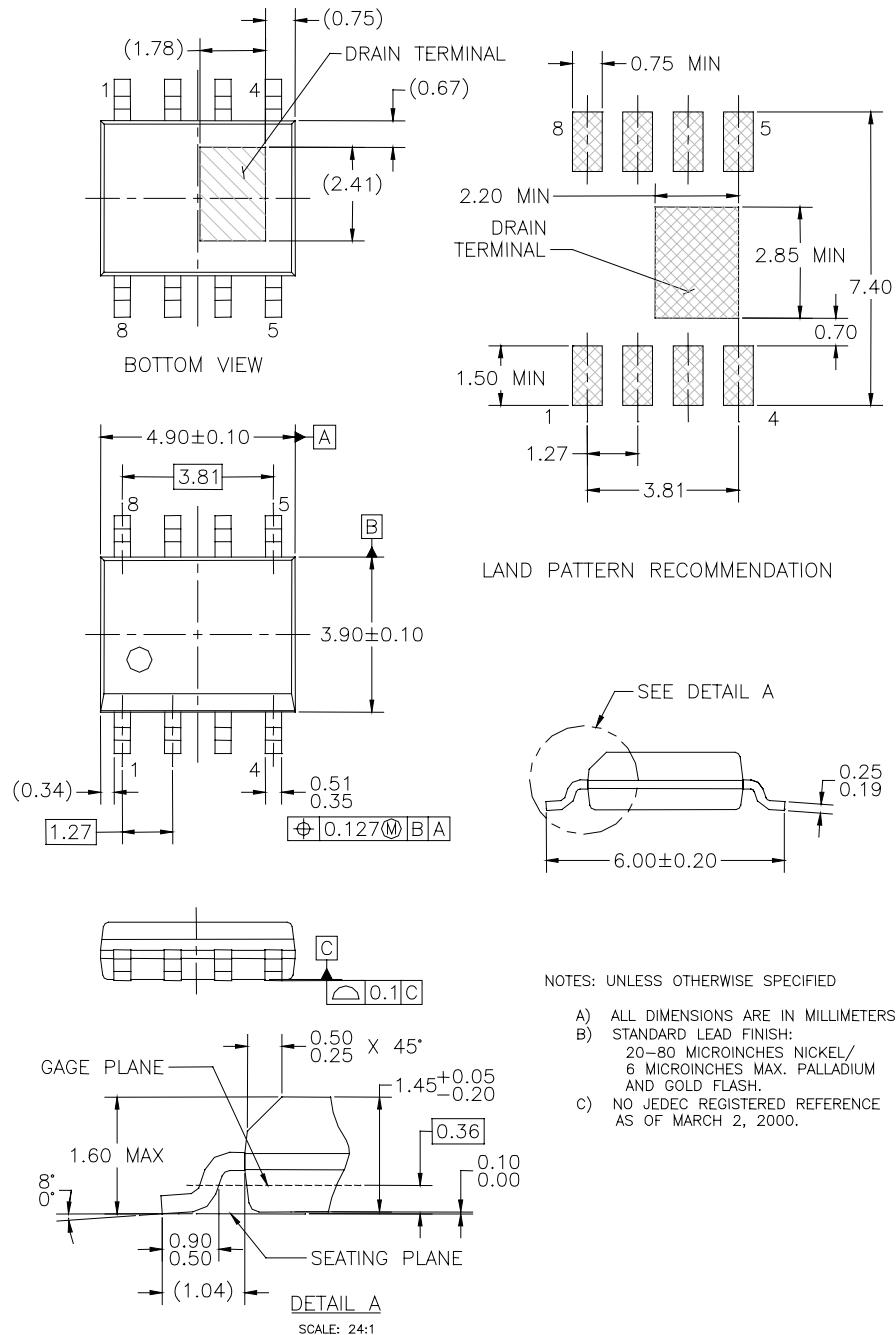


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

## Dimensional Outline and Pad Layout



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