



M74HCT00

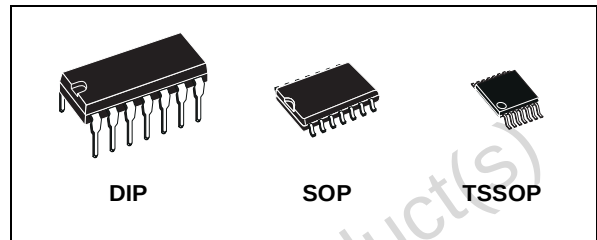
QUAD 2-INPUT NAND GATE

- HIGH SPEED:
 $t_{PD} = 12\text{ns}$ (TYP.) at $V_{CC} = 4.5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 1\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS :
 $V_{IH} = 2\text{V}$ (MIN.) $V_{IL} = 0.8\text{V}$ (MAX)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \equiv t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 00

DESCRIPTION

The M74HCT00 is an high speed CMOS QUAD 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.



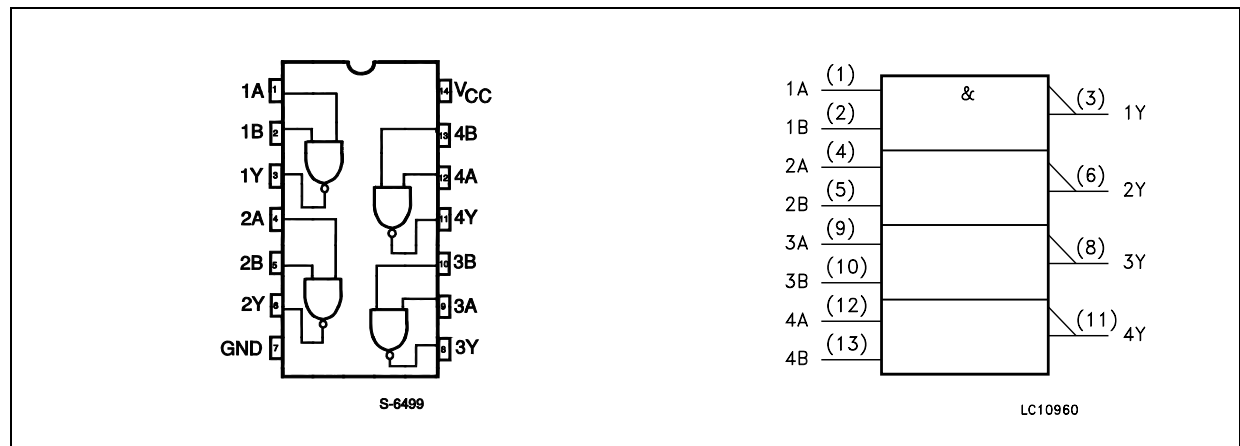
ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HCT00B1R	
SOP	M74HCT00M1R	M74HCT00RM13TR
TSSOP		M74HCT00TTR

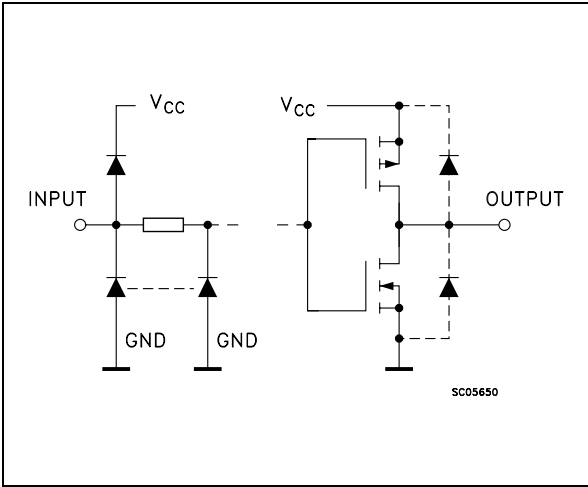
The M74HCT00 is designed to directly interface HSC²MOS systems with TTL and NMOS components.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
t_r, t_f	Input Rise and Fall Time ($V_{CC} = 4.5$ to $5.5V$)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		V
			I _O =-4.0 mA	4.18	4.31		4.13		4.10		
V _{OL}	Low Level Output Voltage	4.5	I _O =20 μA		0.0	0.1		0.1		0.1	V
			I _O =4.0 mA		0.17	0.26		0.33		0.40	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			1		10		20	μA
Δ I _{CC}	Additional Worst Case Supply Current	5.5	Per Input pin V _I = 0.5V or V _I = 2.4V Other Inputs at V _{CC} or GND I _O = 0			2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

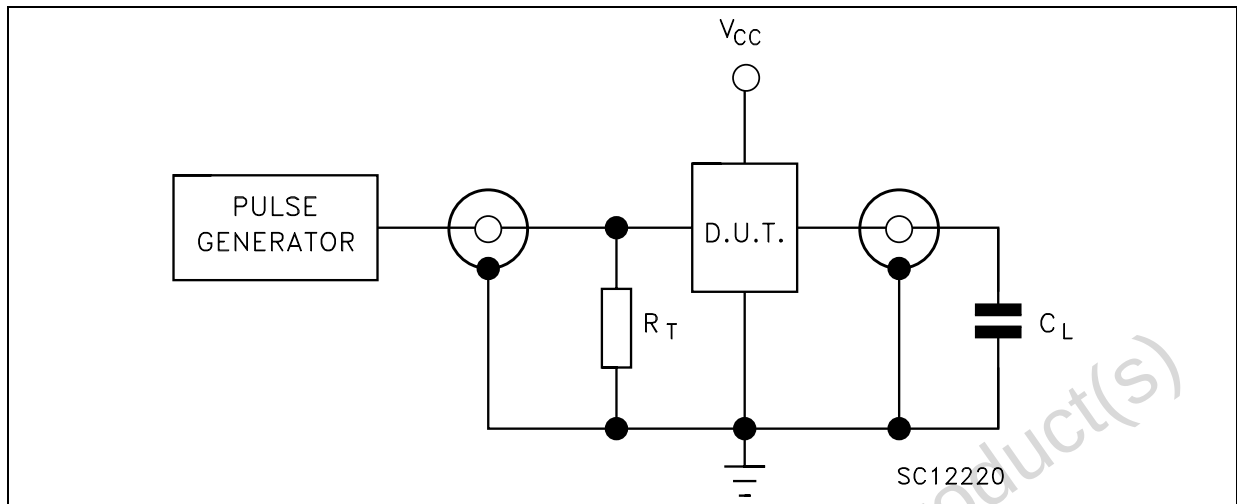
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	4.5			8	15		19		22	ns
t _{PLH} t _{PHL}	Propagation Delay Time	4.5			12	19		24		29	ns

CAPACITIVE CHARACTERISTICS

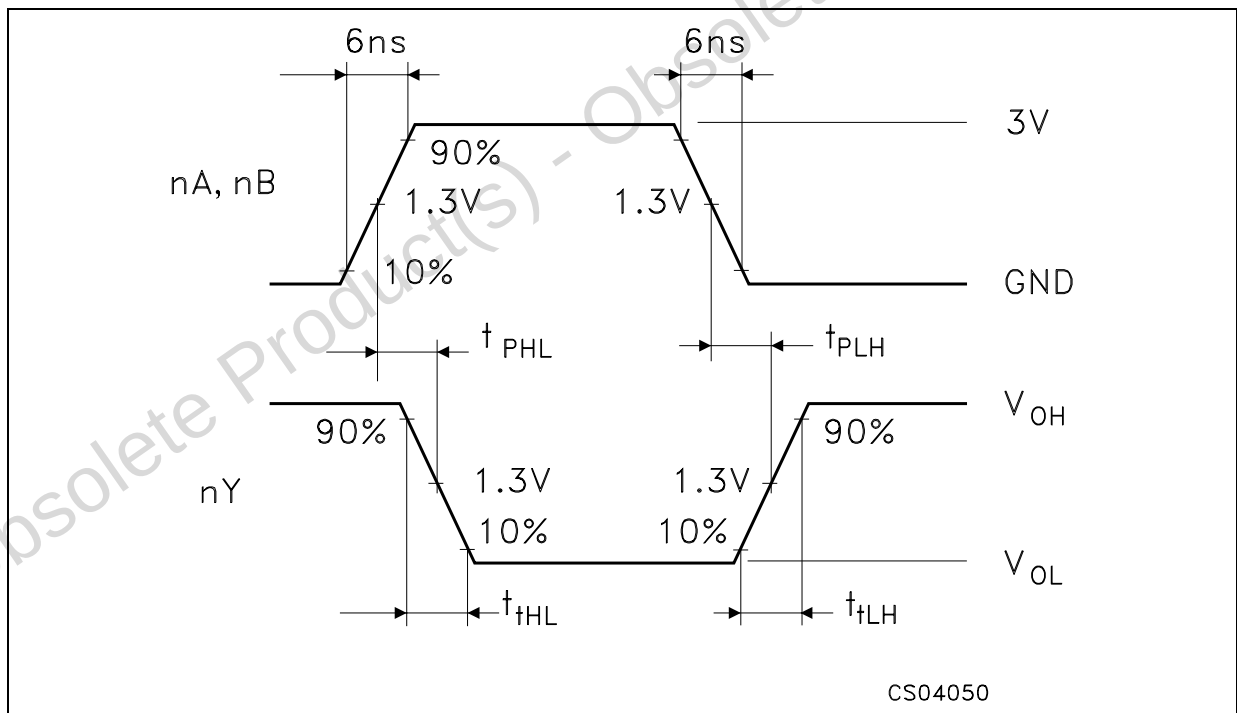
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance				5	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)				40						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/4 (per gate)

TEST CIRCUIT

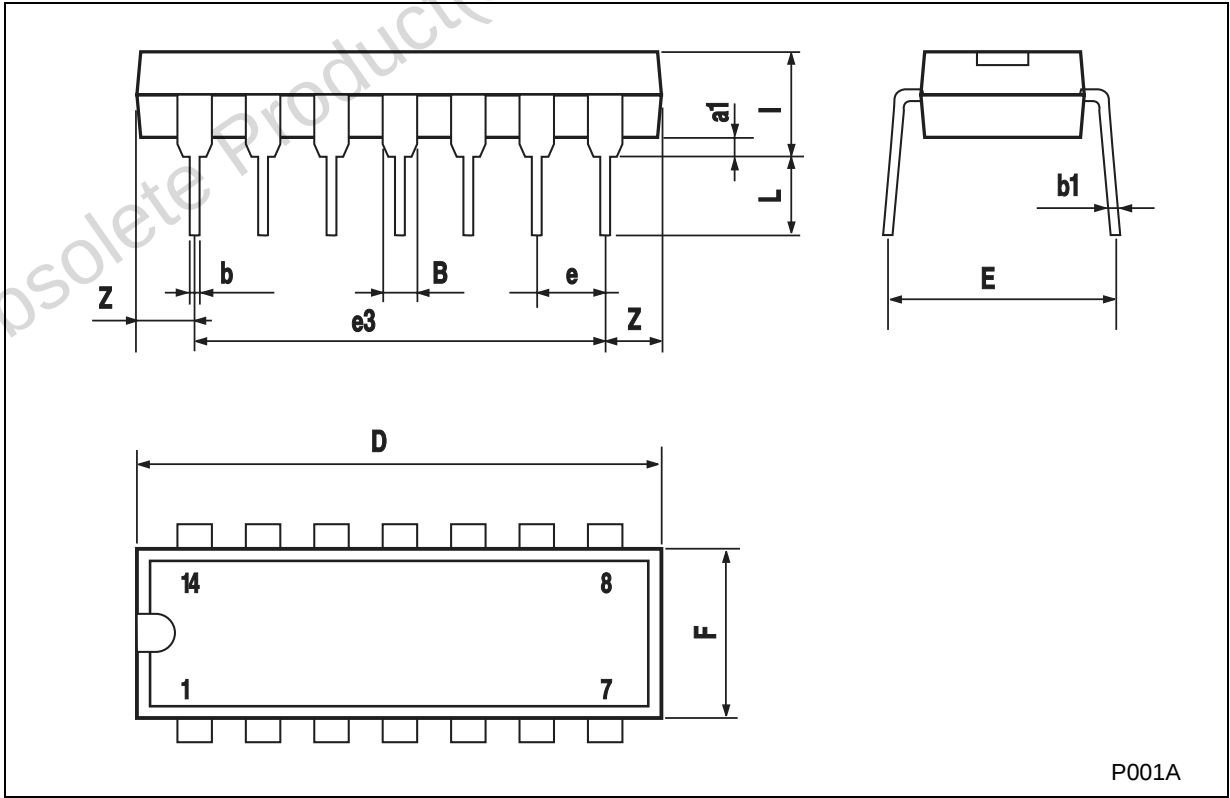


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)

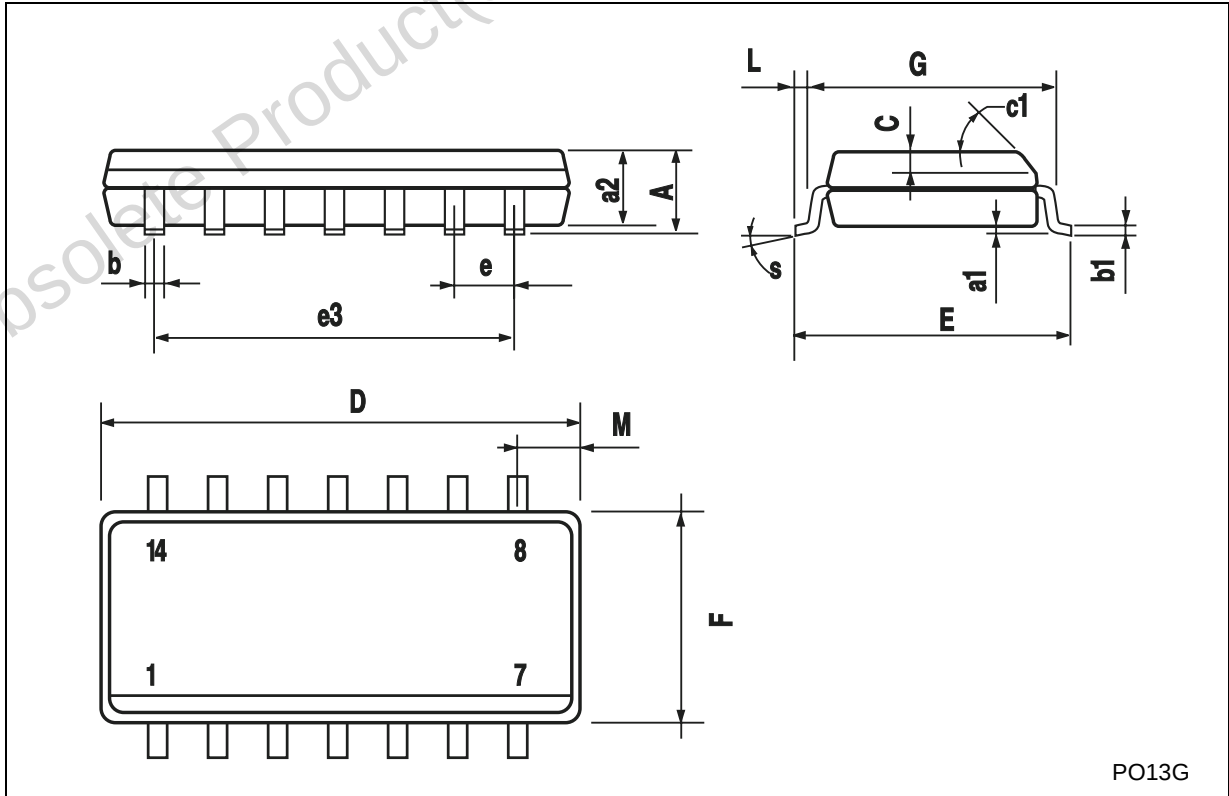
Plastic DIP-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

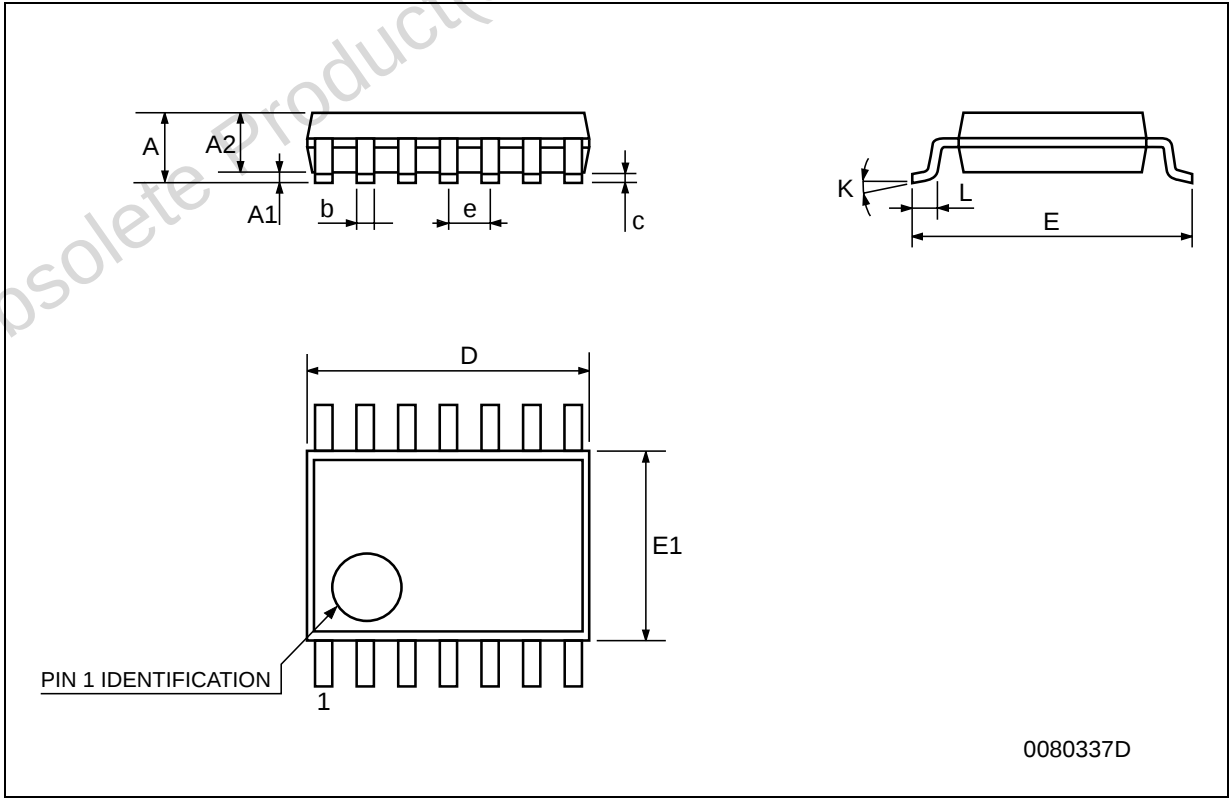


PO13G



TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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