

QP82S100 – PLS100 Field Programmable Logic Array (16 x 48 x 8)

General Description

The QP82S100 – PLS100 PLA is a tri-state output bi-polar programmable logic array with field programmable metal fuse technology (NiChrome). The device utilizes the standard AND/OR/NOT (invert) architecture to directly implement custom sum of product logic equations.

Each Device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs can be ANDed together to comprise one P-Term. All 48 P-Terms can be selectively Ored to each output.

The device is fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. The device features Tri-State outputs for ease of expansion terms and application in bus-organized systems.

The QP82S100 – PLS100 features:

- Field-Programmable (Ni-Cr link)
- Output Functions: 8
- I/O propagation delay: 50ns
- Input loading: -100uA
- Tri-State Output
- Input Variables: 16
- Product Terms: 48
- Power Dissipation: 600mW (typ.)
- Chip Enable Input
- Output Disable Function: High-Z

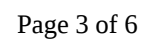
Applications:

- CRT Display Systems
- Code Conversion
- Peripheral Controllers
- Function Generators
- Look-up and Decision Tables
- Microprogramming
- Address Mapping
- Character Generators
- Data Security Encoders
- Fault Detectors
- Frequency Synthesizers
- 16-bit to 8-bit Bus Interface
- Random Logic Replacement

The device/family is constructed using Bipolar/NiChrome processing.

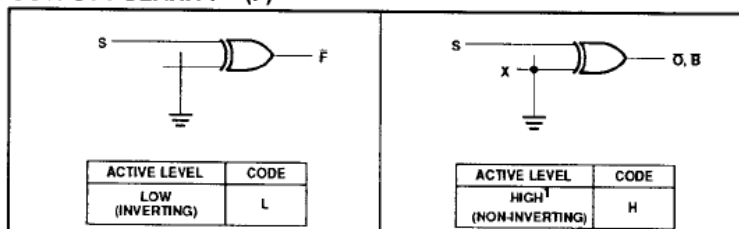
Programming supported by Data I/O under QP Semi/Qualified Parts Lab 82S100

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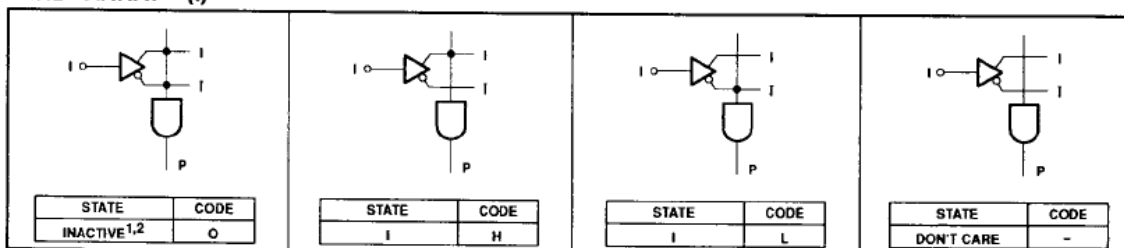


Fuse Function

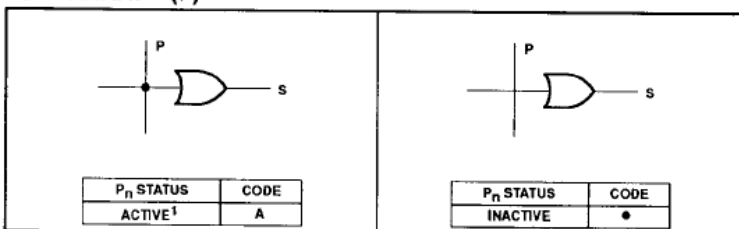
OUTPUT POLARITY – (F)



“AND” ARRAY – (I)



“OR” ARRAY – (F)



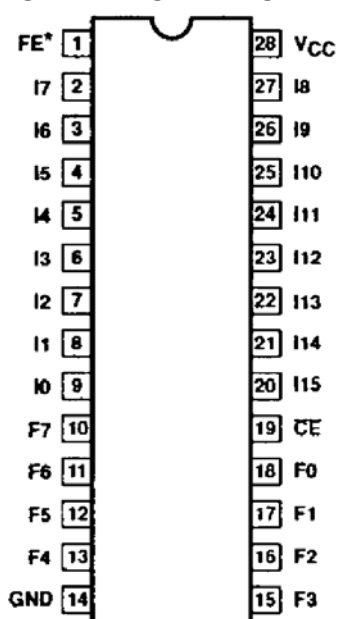
NOTES:

1. This is the initial unprogrammed state of all links. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

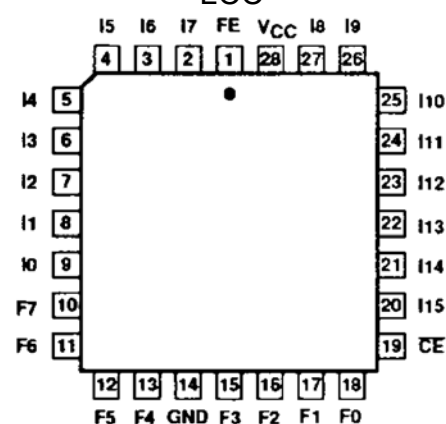
Connection Diagrams

QP82S100 – PLS100

CERDIP/CERPACK



LCC



* Fuse Enable Pin: It is recommended that this pin be left open or connected to ground during normal operation.

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage; extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Power Supply and Input Voltage	-0.5 to +7.0	Volts DC	
Output Current	+100	mA	
Input Clamp Current	-30 to +30	mA	
No Terminal may exceed VCC	>0.5	Volts	/1
Storage Temperature Range	-65 to +150	°C	
Lead Temperature (soldering, 10 seconds)	+300	°C	
Junction Temperature (T _J)	+150	°C	

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range (V _{CC})	4.5 to 5.5	Volts DC	
Input or Output Voltage Range	0.0 to V _{CC}	Volts DC	/1
Minimum High-Level Input Voltage (V _{IH})	2.0	Volts DC	
Maximum Low-Level Input Voltage (V _{IL})	0.8	Volts DC	
Case Operating Range (T _c)	-55°C to +125	°C	/2

/1 – For V_{CC} ≥ 6.5V, the upper limit on the range is limited to 7.0V
/2 – Maximum PD, Maximum T_J Are Not to Be Exceeded

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C Unless Otherwise Specified	Min	Max	Unit
Input High Voltage	V _{IH}	V _{CC} = 5.5V	2.0		V
Input Low Voltage	V _{IL}	V _{CC} = 4.5V		0.8	V
Input High Current	I _{IH}	V _{CC} = 5.5V, V _{IN} = 5.5V		50	µA
Input Low Current	I _{IL}	V _{CC} = 5.5V, V _{IN} = 0.45V	-1.0	-250	µA
Input Clamp	V _{ic}	V _{CC} = 4.5V, I _{IN} = -18mA		1.2	V
Output High Voltage	V _{OH}	V _{CC} = 4.5V, I _{OH} = -2mA	2.4		V
Output Low Voltage	V _{OL}	V _{CC} = 5.5V, I _{OH} = 9.6mA		0.5	V
Tri-State Output Current	I _{OZL}	V _{CC} = 5.5V, V _{OUT} = 0.45V, CE _{BAR} = High	-60.0		µA
(High Impedance State)	I _{OZH}	V _{CC} = 5.5V, V _{OUT} = 5.5V, CE _{BAR} = High		+100.0	µA
Short Circuit Current	I _{OS}	V _{CC} = 5.5V, V _{OUT} = 0V, CE _{BAR} = Low Duration not to exceed 1 second, one output at a time	-15	-85	mA
Power Supply Current	I _{CC}	V _{CC} = 5.5V		180	mA

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions -55°C ≤ TA ≤ +125°C Unless Otherwise Specified	Min	Max	Unit
Input to Output Propagation Delay	t _{PD}	V _{CC} = 4.5 - 5.5V		80	ns
Chip Enable Delay ENABLE to OUTPUT	t _{CE}	V _{CC} = 4.5 - 5.5V		50	ns
Chip Disable Delay ENABLE to OUTPUT	t _{CD}	V _{CC} = 4.5 - 5.5V		50	ns

Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
QP82S100/B3A-MIL	CQCC1-N28 (LCC)	82S100 – PLS100
QP82S100/BXA-MIL	GDIP1-T28 CDIP2-T28 (DIP)	82S100 – PLS100
QP82S100/BYA-MIL	GDFP2-F28 CDFP3-F28 (FLATPACK)	82S100 – PLS100

QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

“-MIL” products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at <http://www.dscc.dla.mil/>

Additional information is available at our website <http://www.qpsemi.com>