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October 2014

FDMS86310

N-Channel PowerTrench® MOSFET

80 V, 50 A, 4.8 mΩ

Features

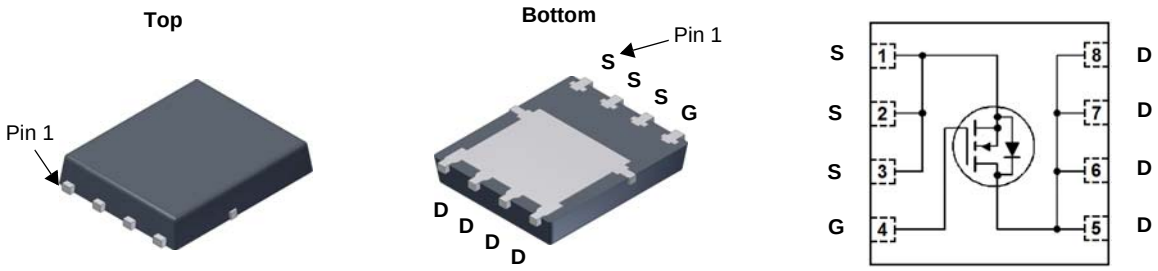
- Max $r_{DS(on)}$ = 4.8 mΩ at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 6.7 mΩ at V_{GS} = 8 V, I_D = 14 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers.It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Applications

- Primary Switch
- Synchronous Rectifier
- Motor Switch



Power 56

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		50	A
	-Continuous (Silicon limited)	T_C = 25 °C		105	
	-Continuous	T_A = 25 °C	(Note 1a)	17	
	-Pulsed			100	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	183	mJ
P_D	Power Dissipation	T_C = 25 °C		96	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86310	FDMS86310	Power 56	13 ”	12 mm	3000 units

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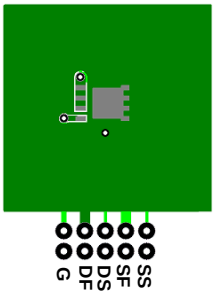
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Electrical Characteristics T_J = 25 °C unless otherwise noted

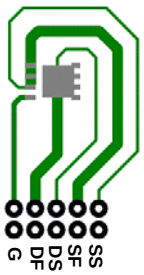
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		45		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.4	3.3	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17 A		3.8	4.8	mΩ
		V_{GS} = 8 V, I_D = 14 A		4.5	6.7	
		V_{GS} = 10 V, I_D = 17 A, T_J = 125 °C		5.7	7.2	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 17 A		49		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		4730	6290	pF
C_{oss}	Output Capacitance			693	925	pF
C_{rss}	Reverse Transfer Capacitance			19	45	pF
R_g	Gate Resistance			1.3		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 17 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		28	45	ns
t_r	Rise Time			23	37	ns
$t_{d(off)}$	Turn-Off Delay Time			35	56	ns
t_f	Fall Time			9	18	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 40 V, I_D = 17 A		66	95	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 8 V; V_{DD} = 40 V, I_D = 17 A		55	78	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 17 A		24		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40 V, I_D = 17 A		14		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.72	1.2	V
		V_{GS} = 0 V, I_S = 17 A (Note 2)		0.81	1.3	
t_{rr}	Reverse Recovery Time	I_F = 17 A, di/dt = 100 A/μs		51	80	ns
Q_{rr}	Reverse Recovery Charge			41	65	nC
t_{rr}	Reverse Recovery Time	I_F = 17 A, di/dt = 300 A/μs		43	69	ns
Q_{rr}	Reverse Recovery Charge			87	140	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 35 A, V_{DD} = 72 V, V_{GS} = 10 V.

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Typical Characteristics T_J = 25 °C unless otherwise noted

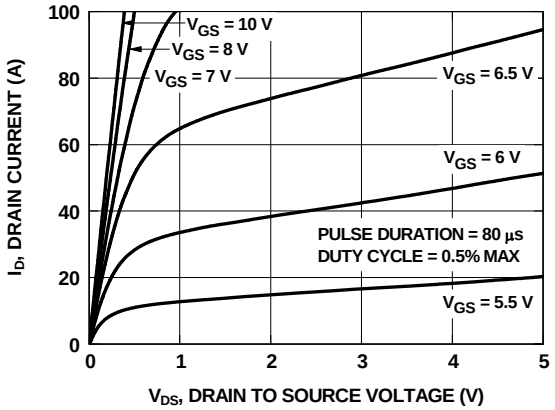


Figure 1. On-Region Characteristics

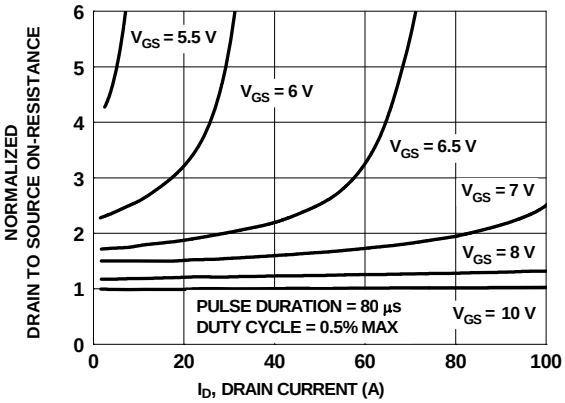


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

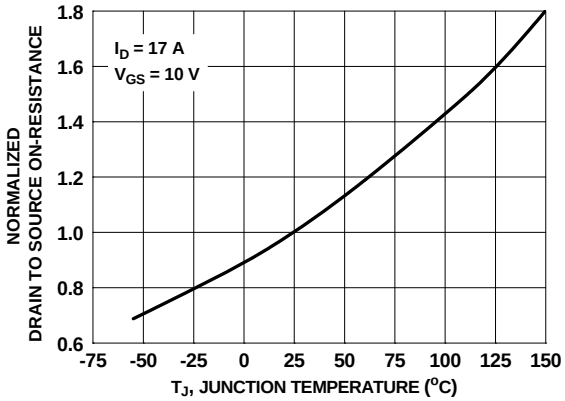


Figure 3. Normalized On-Resistance vs Junction Temperature

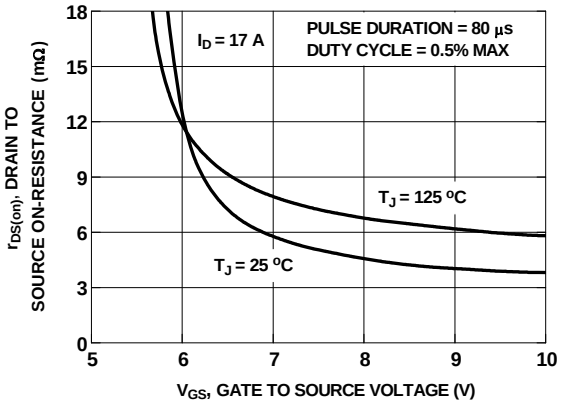


Figure 4. On-Resistance vs Gate to Source Voltage

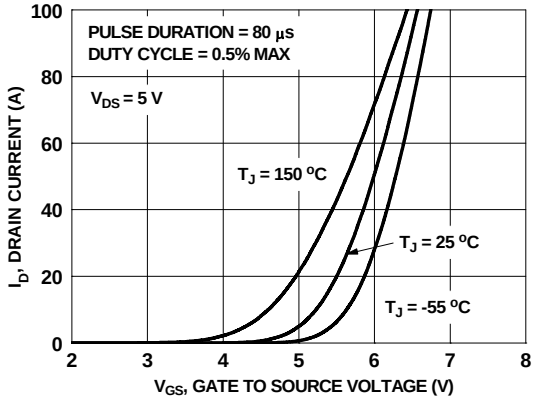


Figure 5. Transfer Characteristics

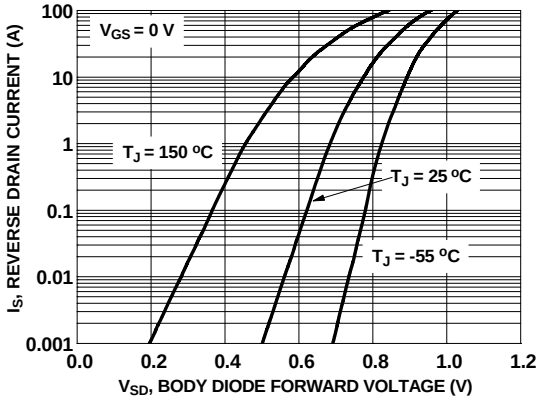


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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Typical Characteristics T_J = 25 °C unless otherwise noted

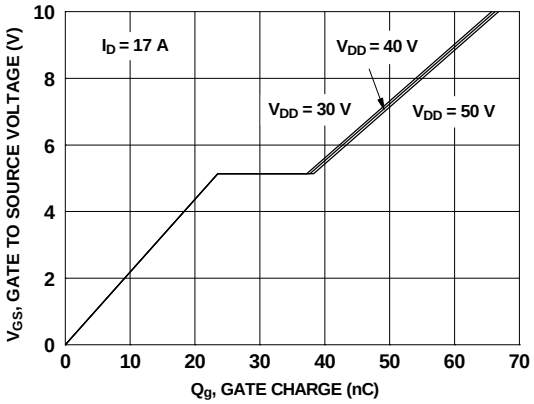


Figure 7. Gate Charge Characteristics

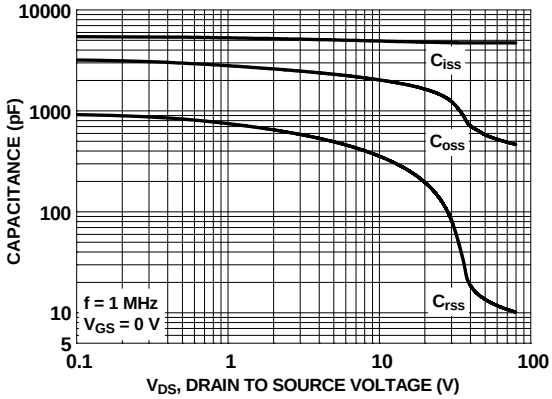


Figure 8. Capacitance vs Drain to Source Voltage

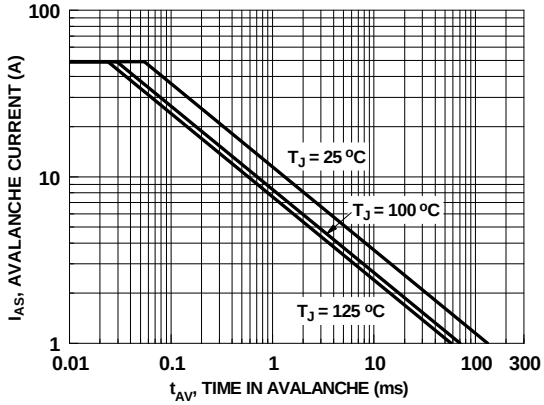


Figure 9. Unclamped Inductive Switching Capability

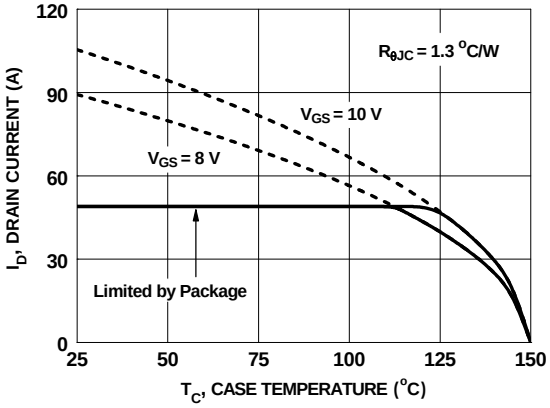


Figure 10. Maximum Continuous Drain Current vs Case Temperature

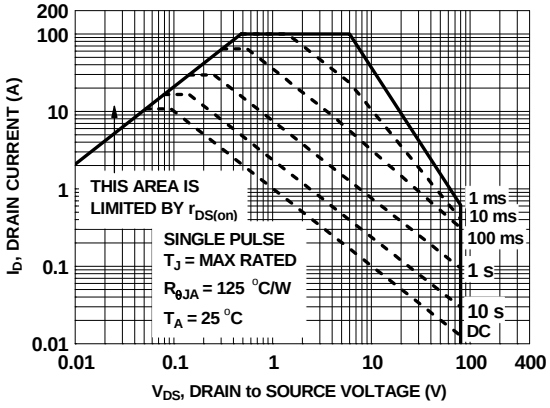


Figure 11. Forward Bias Safe Operating Area

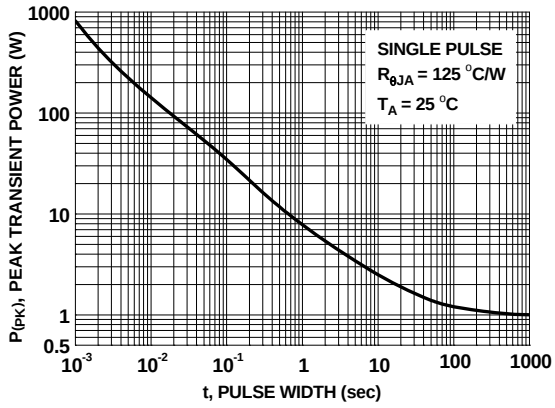


Figure 12. Single Pulse Maximum Power Dissipation

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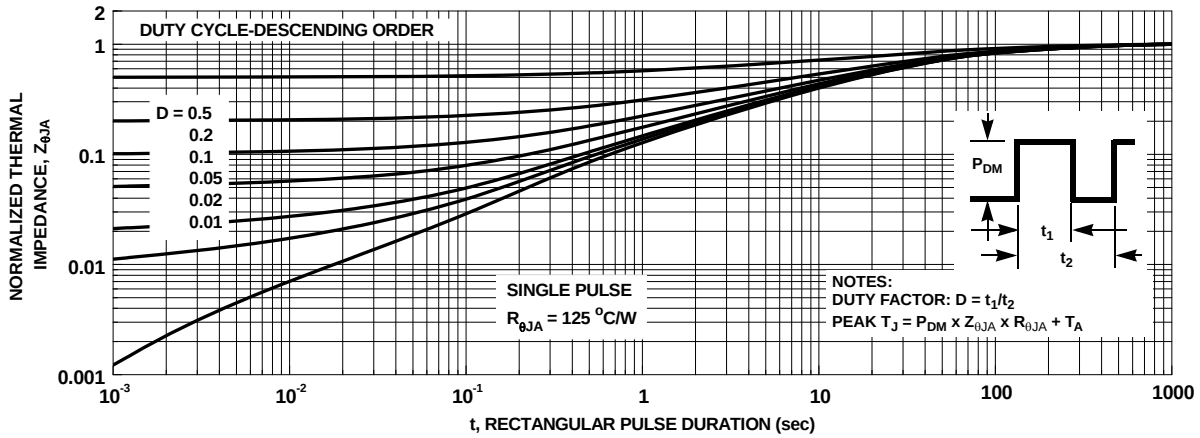
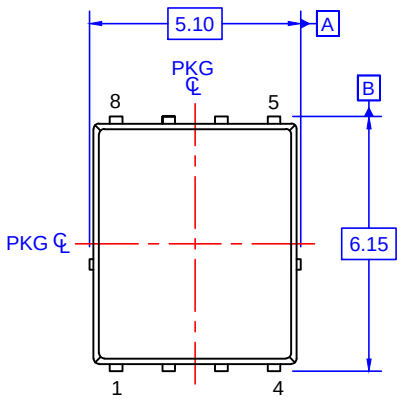


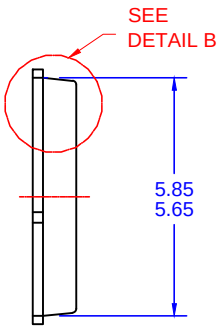
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

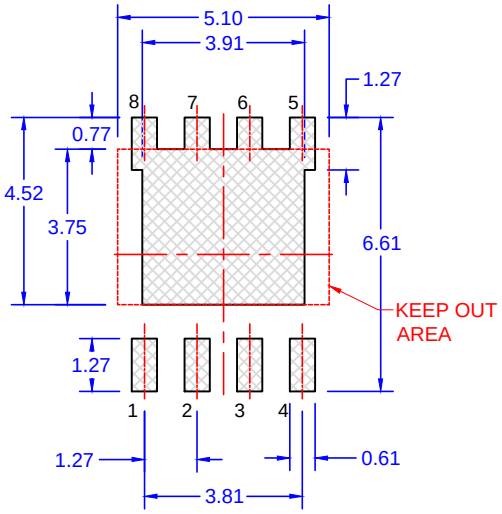
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PQFN8 5X6, 1.27P
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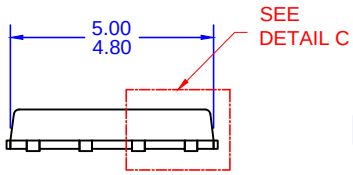


TOP VIEW

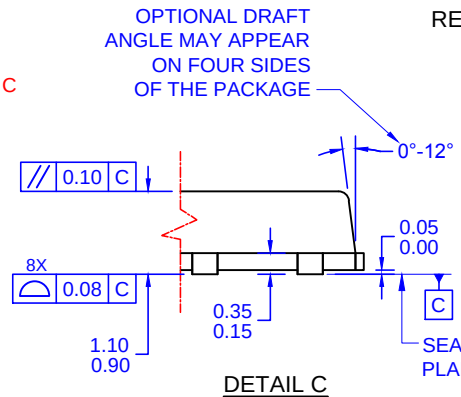




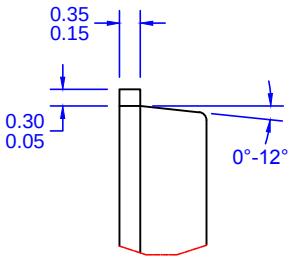
LAND PATTERN
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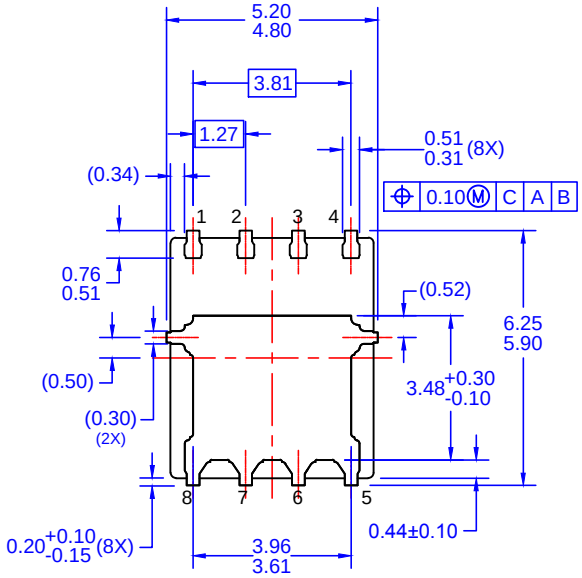
SIDE VIEW



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

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D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
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