STM32WBA6xxx

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M33 with TrustZone®, FPU, Bluetooth® IEEE802.15.4 radio solution

Data brief

Features

Includes ST state-of-the-art patented technology

Ultra-low power radio

- 2.4 GHz radio
- RF transceiver supporting Bluetooth® Low Energy 5.4 specification, IEEE 802.15.4-2015 PHY and MAC, supporting Thread, Matter, and Zigbee®
- Proprietary protocols
- RX sensitivity: -96 dBm (Bluetooth® Low Energy at 1 Mbps), -100 dBm (IEEE 802.15.4 at 250 kbps)
- Programmable output power up to +10 dBm, with 1 dB steps
- Support for external PA
- Isochronous channel (Auracast/Unicast), AOA/AOD, long range
- Packet traffic arbitration
- Integrated balun to reduce BOM
- Single crystal operation
- Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66

Ultra-low power with FlexPowerControl

- 1.71 to 3.6 V power supply
- -40 to 85/105 °C ambient temperature range
- Autonomous peripherals with DMA, functional down to Stop 1 mode
- TBD nA Standby mode (16 wake-up pins)
- TBD nA Standby mode with RTC
- TBD µA Standby mode with 64 KB SRAM
- TBD µA Stop 2 mode with 64 KB SRAM

UFQFPN48
7 x 7 mm solder pad

VFQFPN68
8 x 8 mm solder pad

Thin WLCSP88
3.78 x 3.46 mm

UFBGA121
6 x 6mm

- TBD µA/MHz Run mode
- Radio: Rx TBD mA / Tx at 0 dBm TBD mA

Core

- Arm® 32-bit Cortex®-M33 CPU with TrustZone®, MPU, DSP, and FPU

ART Accelerator

- 8-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 100 MHz, 150 DMIPS)

Benchmarks

- 1.5 DMIPS/MHz (Drystone 2.1)
- 410 CoreMark® (4.10 CoreMark/MHz)

Memories

- Up to 2-Mbyte dual bank flash memory with ECC, including 512 Kbytes with 100 K cycles
- Up to 512-Kbyte SRAM, including 64 Kbytes with parity check
- 512-byte (32 rows) OTP

Power management

- Embedded regulator LDO and SMPS step-down converter, supporting switch on-the-fly and voltage scaling

Clock management

- 32 MHz crystal oscillator
- 32 kHz crystal oscillator (LSE)
- Internal low power 32 kHz (±5%) RC
- Internal low frequency 32 kHz RC (500 ppm/°C)
- Internal 16 MHz factory trimmed RC (±1%)
- PLL for system clock, audio, and ADC

General-purpose input/output

- Up to 86 I/Os (most of them 5 V-tolerant) with interrupt capability, and up to 14 I/Os with independent supply down to 1.08 V

Analog peripherals (independent supply)

- 12-bit ADC 2.5 Msps, up to 16-bit with hardware oversampling
- Two ultra-low power comparators

Communication peripherals

- One USB OTG high-speed with embedded PHY
- One SAI (serial audio interface)
- Four UARTs (ISO 7816, IrDA, modem)
- Three SPIs
- Four I2Cs FM+ (1 Mbit/s), SMBus/PMBus®

System peripherals

- Touch sensing controller, up to 24 sensors, supporting touch key, linear, and rotary touch sensors
- One 16-bit, advanced motor control timer
- Three 16-bit timers and two 32-bit timers
- Two low power 16-bit timers (available in Stop mode)
- Two Systick timers
- RTC with hardware calendar and calibration
- Two watchdogs
- 8-channel DMA controller, functional in Stop mode

Security and cryptography

- Arm® TrustZone® and securable I/Os, memories, and peripherals
- Flexible life cycle scheme with read-out protection (RDP) and password protected debug
- Root of trust thanks to unique boot entry and secure hide protection area (HDP)
- Secure firmware installation (SFI), thanks to embedded root secure services (RSS)
- Secure data storage with hardware unique key (HUK)
- Secure firmware upgrade support with TF-M
- Two AES coprocessors, including one with DPA resistance
- Public key accelerator, DPA resistant
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Active tampers
- CRC calculation unit

Development support

- Serial wire debug (SWD), JTAG
- Embedded trace (ETM)

ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32WBA62xx	STM32WBA62CG, STM32WBA62CI, STM32WBA62MG, STM32WBA62MI, STM32WBA62PG, STM32WBA62PI
STM32WBA63xx	STM32WBA63CG, STM32WBA63CI
STM32WBA64xx	STM32WBA64CG, STM32WBA64CI
STM32WBA65xx	STM32WBA65CG, STM32WBA65CI, STM32WBA65MG, STM32WBA65MI, STM32WBA65PG, STM32WBA65PI, STM32WBA65RG, STM32WBA65RI

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1 Introduction

This document provides information on the STM32WBA6xxx microcontrollers, based on Arm® cores[a].

Throughout the whole document TBD indicates a value to be defined.

For information on the device errata with respect to the datasheet and reference manual refer to the STM32WBA6xxx errata sheet (ES0644).

For information on the Arm® Cortex®-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available on the www.arm.com website.

For information on 802.15.4, refer to the IEEE website (www.ieee.org).

For information on Bluetooth®, refer to www.bluetooth.com.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32WBA6xxx multiprotocol wireless and ultra-low power devices embed a powerful and ultra-low power radio compliant with the Bluetooth® SIG Low Energy specification 5.4 and with IEEE 802.15.4-2015. They contain a high-performance Arm® Cortex®-M33 32-bit RISC core, and operate at a frequency of up to 100 MHz.

The devices integrate a 2.4 GHz RADIO supporting Bluetooth Low Energy, Matter, Thread, and Zigbee®, and make possible to use proprietary protocols and concurrent operation modes. They provide support for an array of up to eight antennas, and an external power amplifier. PTA (packet traffic arbitration) interface is supported as well.

The Cortex-M33 core features a single-precision floating-point unit (FPU), supporting all the Arm single-precision data-processing instructions and all the data types. This core implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 2-Mbyte flash, up to 512-Kbyte SRAM), an extensive range of enhanced I/Os, and peripherals connected to AHB and APB buses on the 32-bit multi-AHB bus matrix.

The security foundation is compliant with the TBSA (trusted-based security architecture) requirements from Arm. It embeds the features needed to implement secure boot, secure data storage, and secure firmware update. Besides these capabilities, the devices incorporate a secure firmware installation feature that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels readout protection and debug unlock with password.

Firmware hardware isolation is supported thanks to securable peripherals, memories and I/Os, and privilege configuration of peripherals and memories.

The devices feature protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

Dedicated peripherals reinforce security: a fast AES coprocessor, a secure AES coprocessor with DPA resistance and hardware unique key that can be shared by hardware with fast AES, a PKA (public key accelerator) with DPA resistance, a HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient perturbation attacks, thanks to several internal monitoring generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

Hardware semaphores allow synchronization between software processes.

The devices offer one 12-bit ADC (2.5 Msps), up to two comparators, a low-power RTC, up to two 32-bit general-purpose timer, one 16-bit PWM timer for motor control, three 16-bit general-purpose timers, and two 16-bit low-power timers. They also feature standard and advanced communication interfaces, namely up to four I2Cs, up to three SPIs, one SAI, up to three USARTs, one low-power UART, and one USB OTG high-speed.

The devices operate in the -40 to 85 °C (105 °C junction) and -40 to 105 °C (125 °C junction) temperature ranges from a 1.71 to 3.6 V power supply.

The design of low-power applications is enabled by a comprehensive set of power-saving modes.

Many peripherals (including radio, communication, analog, and timer peripherals) can be functional and autonomous in Stop mode with direct memory access thanks to background autonomous mode (BAM) support.

Some independent power supplies are supported, like an analog independent supply input for ADC and comparators, USB OTG high-speed, and dedicated supply inputs for the 2.4 GHz RADIO.

The devices offer four packages, from 48 to 121 pins, with or without SMPS.

Table 2. Device features and peripheral counts

Feature		STM32WBA62CI	STM32WBA62CG	STM32WBA63CI	STM32WBA63CG	STM32WBA64CI	STM32WBA64CG	STM32WBA65CI	STM32WBA65CG	STM32WBA65RI	STM32WBA65RG	STM32WBA62PI	STM32WBA62PG	STM32WBA65PI	STM32WBA65PG	STM32WBA62MI	STM32WBA62MG	STM32WBA65MI	STM32WBA65MG
Flash memory density (Mbytes)		2	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1
SRAM density	SRAM1 (Kbytes)	448	192	448	192	448	192	448	192	448	192	448	192	448	192	448	192	448	192
	SRAM2 (Kbytes)	64																	
Bluetooth Low Energy		Yes																	
IEEE802.15.4		No		Yes								No		Yes		No		Yes	
SMPS		No		Yes		No		Yes				No		Yes		No		Yes	
PTA		Yes																	
External PA support		No		Yes								No		Yes		No		Yes	
BLE AoA, AoD support		No		Yes								No		Yes		No		Yes	
Timers	Advanced control (16-bit)	1																	
	General purpose (32-bit)	2		1		2													
	General purpose (16-bit)	3																	
	Low power (16-bit)	2																	
	SysTick	2																	
Communication interfaces	SPI	2								3									
	I2C	4		2		4		2		4									
	USART	3		2		3													
	LPUART	1																	
	SAI	1																	
	USB OTG high-speed	Yes		No		Yes													
	IRTIM	No		Yes		No				Yes									
RTC		Yes																	
Tamper pins (active tampers)(1)		4 (3)		5 (4)		4 (3)						6 (5)							
Wake-up pins		11		14		11		10		14		16							
GPIOs		34		31		34		30		46		86				54			
TSC (capacitive sensing channels)		10		12		10		7		16		24				19			
12-bit ADC4 (channels)		7		8		7		6		10									
Comparators		1		2		1				2									
VREF		No								Yes									

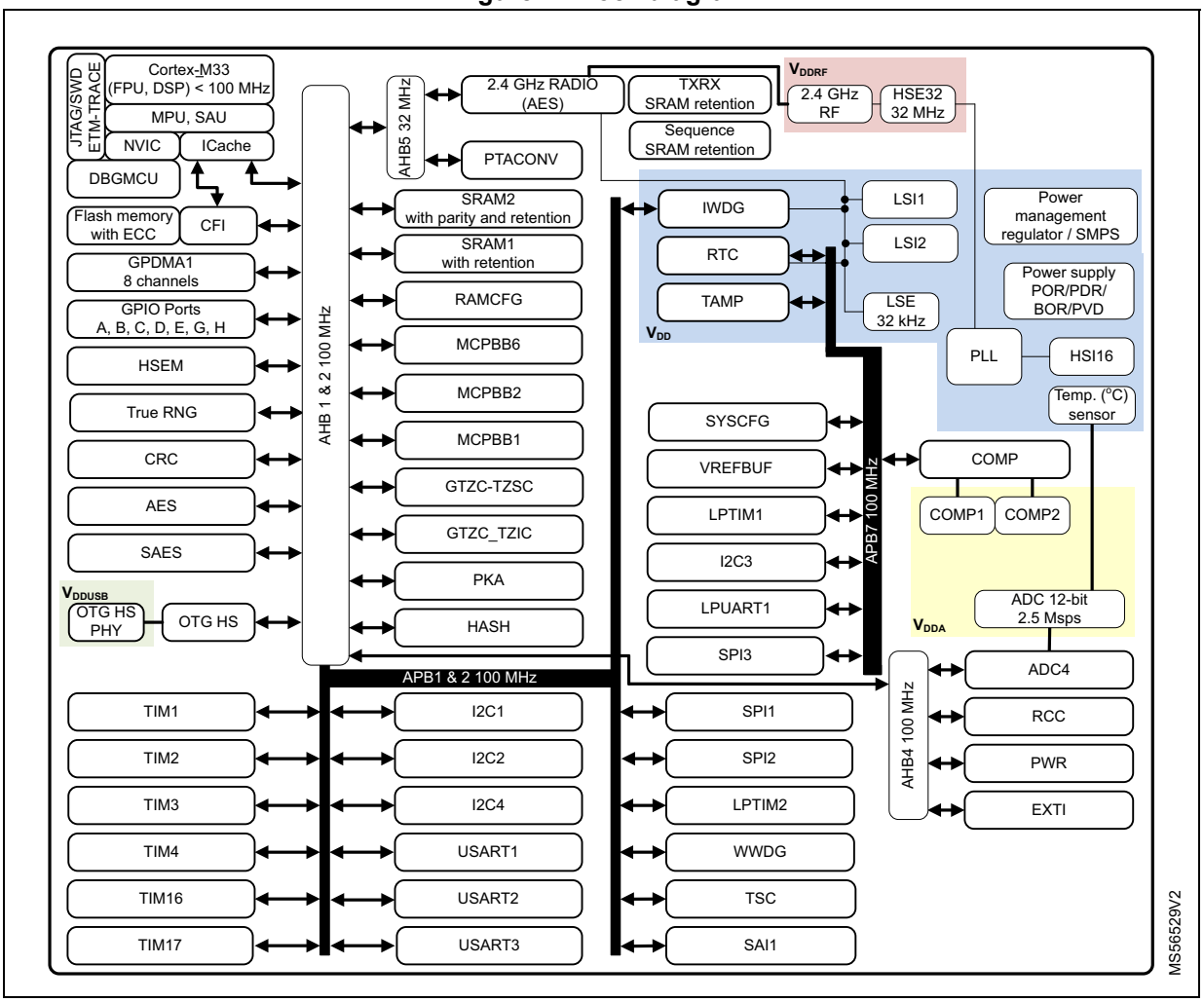
Table 2. Device features and peripheral counts (continued)

Feature	STM32WBA62CI	STM32WBA62CG	STM32WBA63CI	STM32WBA63CG	STM32WBA64CI	STM32WBA64CG	STM32WBA65CI	STM32WBA65CG	STM32WBA65RI	STM32WBA65RG	STM32WBA62PI	STM32WBA62PG	STM32WBA65PI	STM32WBA65PG	STM32WBA62MI	STM32WBA62MG	STM32WBA65MI	STM32WBA65MG
True random number generator	Yes																	
SAES, AES	Yes																	
Public key accelerator (PKA)	Yes																	
HASH	Yes																	
Debug ETM	No								Yes									
Maximum CPU frequency	100 MHz																	
Operating temperature	Ambient: -40 to 85 °C / -40 to 105 °C Junction: -40 to 105 °C / -40 to 125 °C																	
Operating voltage	1.71 to 3.6 V																	
Package	UFQFPN48								VFQ FPN68		UFBGA121				Thin WLCSP88			

1. Active tampers in output sharing mode (one output shared by all inputs).

Figure 1 shows the general block diagram of the devices.

Figure 1. Block diagram



3 Functional overview

3.1 Arm Cortex-M33 core with TrustZone, MPU, DSP, and FPU

The Cortex-M33 with TrustZone, MPU, DSP and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and nonsecure states
- MPUs (memory protection units), supporting up to 16 regions for secure and nonsecure applications
- Configurable SAU (secure attribute unit) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB (S-AHB) bus: used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, and Vendor_SYS regions of the Armv8-M memory map.
- Code AHB (C-AHB) bus: used for any instruction fetch and data access to the code region of the Armv8-M memory map.

3.2 ART Accelerator (ICACHE)

The ICACHE (instruction cache) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from internal memories.

ICACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal flash memory
  - Master2 port performing refill requests to internal SRAM memories
  - Second slave port dedicated to ICACHE registers access

- Close to 0 wait-states instructions/data access performance:
  - 0 wait-states on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports to decouple internal flash memory and SRAM traffic, on fast and slow buses, respectively; also minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic enabling the definition of four cacheable regions
- Power consumption reduced intrinsically (more accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default two-ways set-associative mode)
- TrustZone security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The MPU is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 16 protected areas. The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1, USB OTG) and the slaves (flash memory, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several peripherals work simultaneously.

3.5 Embedded flash memory

The devices feature an up to 2-Mbyte embedded flash memory, available to store programs and data. This memory supports 10000 cycles, and up to 100000 cycles on 64 pages (512 Kbytes).

A 128-bit instruction prefetch is implemented and can optionally be enabled.

The flash memory interface features dual-bank operation modes and read-while-write (RWW), hence a read operation to be performed from one bank while an erase or program operation is performed on the other bank. The dual-bank boot is also supported. Each bank contains up to 128 pages of 8 Kbytes. The flash memory also embeds a 512-byte one-time programmable (OTP) memory for user data.

The whole nonvolatile memory embeds the error correction code (ECC) feature supporting:

- single-error detection and correction
- double-error detection
- ECC fail address report

3.5.1 Flash memory protections

The user options allow the configuration of flexible protections:

- write protection (WRP) to protect areas against erasing and programming. Two areas per bank can be selected with 8-Kbyte granularity
- readout protection (RDP) to protect the whole memory, has four levels of protection available (see *Table 3* and *Table 4*):
  - Level 0: no readout protection
  - Level 0.5: available only when TrustZone is enabled

    All read/write operations (if no write protection is set) from/to the nonsecure flash memory are possible. The debug access to secure area is prohibited. Debug access to nonsecure area remains possible.
  - Level 1: memory readout protection

    The flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected. If TrustZone is enabled, the nonsecure debug is possible and the boot in SRAM is not possible. Regressions from Level 1 to lower levels can be protected by password authentication.
  - Level 2: chip readout protection

    The debug features, the boot in RAM and the bootloader selection are disabled. A secure secret key can be configured in the secure options to allow the regression capability from Level 2 to Level 1. By default (key not configured), this Level 2 selection is irreversible and JTAG/SWD interfaces are disabled. If the secret key was previously configured in lower RDP levels, the device enables the RDP regression from Level 2 to Level 1 after password authentication through JTAG/SWD interface.

Note: To reach the best protection level, it is recommended to activate TrustZone and to set RDP level 2 with password authentication regression enabled.

Table 3. Access status versus protection level and execution modes when TZEN = 0

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/ bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(4)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory(2)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(3)	1	Yes	Yes(4)	N/A	Yes	Yes(4)	N/A
	2	Yes	No(5)	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	2	Yes	Yes(6)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port, the boot from RAM, and the boot from system memory are disabled.
2. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
3. Option bytes are accessible only through the flash memory interface registers and OPSTRT bit.
4. The flash main memory is erased when the RDP option byte changes from level 1 to level 0.
5. SWAP_BANK user option can be modified.
6. OTP can be written only once.
7. The backup registers are erased when RDP changes from level 1 to level 0.
8. All SRAMs are erased when RDP changes from level 1 to level 0.

Table 4. Access status versus protection level and execution modes when TZEN = 1

Area	RDP level	User execution (boot from flash memory)			Debug/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	0.5	Yes	Yes	Yes	Yes(2)	Yes(2)	Yes(2)
	1	Yes	Yes	Yes	No	No	No(5)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory(3)	0.5	Yes	No	No	Yes	No	No
	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(4)	0.5	Yes	Yes(5)	N/A	Yes	Yes (5)	N/A
	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	No(6)	N/A	N/A	N/A	N/A

Table 4. Access status versus protection level and execution modes when TZEN = 1 (continued)

Area	RDP level	User execution (boot from flash memory)			Debug/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
OTP	0.5	Yes	Yes(7)	N/A	Yes	Yes(7)	N/A
	1	Yes	Yes(7)	N/A	Yes	Yes(7)	N/A
	2	Yes	Yes(7)	N/A	N/A	N/A	N/A
Backup registers	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(8)
	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(9)
	1	Yes	Yes	N/A	No	No	N/A(9)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port and the bootloader mode are disabled.
2. Depends on TrustZone security access rights.
3. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
4. Option bytes are only accessible through the flash registers interface and OPSTRT bit.
5. The flash main memory is erased when the RDP option byte regresses from level 1 to level 0.
6. SWAP_BANK user option can be modified.
7. OTP can be written only once.
8. The backup registers are erased when RDP changes from level 1 to level 0.
9. All SRAMs are erased when RDP changes from level 1 to level 0.

3.5.2 Additional flash memory protections when TrustZone is activated

When the TrustZone security is enabled through option bytes, the whole flash memory is secure after reset and the following protections are available:

- Non volatile watermark-based secure flash memory area

  The secure area can be accessed only in Secure mode. One area can be selected with a page granularity.
- Secure hide protection area (HDP)

  It is part of the flash memory secure area and can be protected to deny access to this area by any data read, write, and instruction fetch. For example, a software code in the secure flash memory hide protection area can be executed only once and deny any further access to this area until the next system reset. One area can be selected at the beginning of the secure area.
- Volatile block-based secure flash memory area

  Each page can be programmed on-the-fly as secure or nonsecure.

3.5.3 FLASH privilege protection

Each flash memory page can be programmed on-the-fly as privileged or unprivileged.

3.6 Embedded SRAMs

SRAM1 and SRAM2 are the main embedded SRAMs, each with specific features. These memories can be used for peripherals background autonomous mode (BAM).

The SRAMs can be powered down in Stop mode to reduce consumption:

- SRAM1: up to seven 64-Kbyte blocks (up to 448 Kbytes), can be retained in Standby mode
- SRAM2: one 64-Kbyte block with parity, can be retained in Standby mode.

3.6.1 SRAMs TrustZone security

When TrustZone security is enabled, SRAMs are secure after reset. SRAM1 and SRAM2 can be programmed as secure or nonsecure by blocks, using the block-based memory protection controller (MPCBB).

The granularity of SRAM secure block based is a page of 512 bytes.

3.6.2 SRAMs privilege protection

The SRAM1 and SRAM2 can be programmed as privileged or non-privileged by blocks, using the MPCBB. The granularity of SRAM block-based privilege is a page of 512 bytes.

3.7 TrustZone security architecture

The security architecture is based on Arm TrustZone with the Armv8-M main extension.

The TZEN option bit in the FLASH_OPTR register activates the TrustZone security.

When TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAM and peripheral memory space is aliased twice for secure and nonsecure states.

Table 5 shows an example of typical SAU regions configuration based on IDAU regions.

Table 5. Example of memory map security attribution versus SAU configuration regions

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
ICACHE Re-mappable (Reserved)	0x0000 0000 0x07FF FFFF	Nonsecure	Secure or nonsecure or nonsecure callable	
Code flash memory and SRAM	0x0800 0000 0x0BFF FFFF	Nonsecure		
	0x0C00 0000 0x0FFF FFFF	Nonsecure callable	Secure or NSC	

Table 5. Example of memory map security attribution versus SAU configuration regions (contin-

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
ICACHE Re-mappable (Reserved)	0x1000 0000 0x17FF FFFF	Nonsecure	Nonsecure	
	0x1800 0000 0x1FFF FFFF			
SRAM	0x2000 0000 0x2FFF FFFF	Nonsecure		
	0x3000_0000 0x3FFF FFFF	Nonsecure callable	Secure or nonsecure callable	
Peripherals	0x4000 0000 0x4FFF FFFF	Nonsecure		
	0x5000 0000 0x5FFF FFFF	Nonsecure callable	Secure or nonsecure callable	
Reserved	0x6000 0000 0xDFFF FFFF	Nonsecure	Secure or nonsecure or nonsecure callable	

3.7.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable or TrustZone-aware type as follows:

- Securable: peripheral protected by an AHB/APB firewall gate that is controlled from TZSC to define security properties
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior such as a subset of registers being secure

3.7.2 Default TrustZone security state

The default system security state is detailed below:

- CPU: Cortex-M33 is in secure state after reset. The boot address must be in secure area.
- Memory map: SAU is fully secure after reset, hence all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermark user options.
  - Flash memory block based area is nonsecure after reset.
- SRAMs:
  - All are secure after reset, MPCBB is secure.
- Peripherals:
  - Securable peripherals are nonsecure after reset.
  - TrustZone-aware peripherals are nonsecure after reset.
- All GPIOs are secure after reset.

- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and nonsecure state.
  - TZIC: All illegal access interrupts are disabled after reset.

3.8 Boot modes

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx[24:0] (x = 0, 1), and SECBOOTADD0[24:0] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory bootloader
- Boot from any address in embedded SRAM
- Boot from RSS (root security services)

The BOOT0 value comes from the PH3-BOOT0 pin or from an option bit, depending upon the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory, programmed by ST during production. It is used to program the flash memory by using USART, I^2C, SPI or USB OTG in device mode.

The bootloader is available on all devices. Refer to AN2606 *STM32 microcontroller system memory boot mode*, available on *www.st.com*, for more details.

The RSS are embedded in the flash memory area named secure information block, programmed during ST production. For example, the RSS enables the SFI (secure firmware installation), thanks to the RSSe (RSS extension firmware). This feature allows the customers to produce the confidentiality of the firmware to be provisioned into the STM32, when production is subcontracted to untrusted third party.

The RSS is available on all devices, after enabling the TrustZone through the TZEN option bit. Refer to AN4992 *STM32 MCUs secure firmware install (SFI) overview*, available on *www.st.com*, for more details.

Refer to *Table 6* and *Table 7*, respectively, for boot modes with TrustZone disabled and enabled.

Table 6. Boot modes when TrustZone is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x08000 000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

Table 6. Boot modes when TrustZone is disabled (TZEN = 0) (continued)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

Table 7. Boot modes when TrustZone is enabled (TZEN = 1)

BOOT_LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF8 0000
	-	-	-	≠0	N/A	RSS	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in the secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the address selected by SECBOOTADD0[24:0] option bytes. All other boot options are ignored.

The boot address option bytes allow to program any boot memory address, but the allowed address space depends on the flash memory RDP level. If the programmed boot memory address is out of the allowed memory mapped area when RDP level is 0.5 or higher, the default boot address is forced either in secure or nonsecure flash memory, depending on TrustZone security option, as detailed in *Table 8*.

Table 8. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address
0.5	Boot address only in RSS or secure flash memory: 0x0C00 0000 - 0x0C1F FFFF. Otherwise, forced boot address is 0x0FF8 0000	N/A
1		Any boot address
2		Boot address only in flash memory: 0x0800 0000 - 0x081F FFFF. Otherwise, forced boot address is: 0x0800 0000

3.9 Global TrustZone controller (GTZC)

GTZC is used to configure TrustZone and privileged attributes within the full system.

The GTZC includes different sub-blocks:

- **TZSC**: TrustZone security controller

  Defines the secure/privilege state of slave/master peripherals. The TZSC block informs some peripherals (such as RCC or GPIO) about the secure status of each securable peripheral.
- **TZIC**: TrustZone illegal access controller

  Gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- **MPCBB**: block-based memory protection controller

  Controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral configures the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB
- Secure and nonsecure access supported for privileged/unprivileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable memories
  - Illegal access interrupt notification

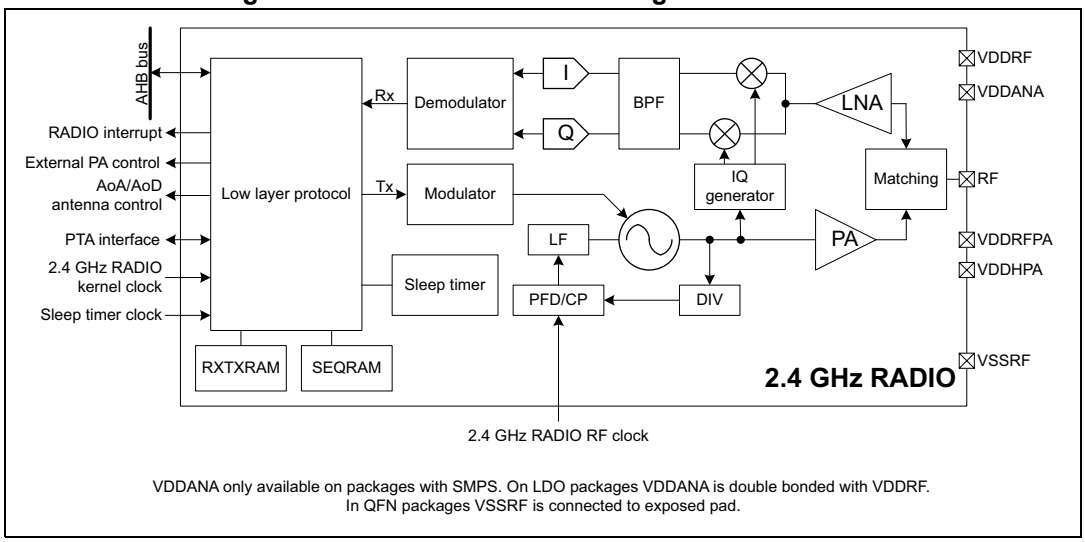
3.10 2.4 GHz RADIO

The 2.4 GHz RADIO is ultra-low power, operating in the 2.4 GHz ISM band. It provides Bluetooth LE 1 Mbps coded, 1 Mbps, and 2 Mbps non-coded GFSK, and IEEE802.15.4 chip rate 2 Mchip/s, spreading mode DSSS, data rate 125 kbps and 250 kbps, O-QPSK-C modulation. It is compliant with the Bluetooth 5.4, Matter, Thread, and Zigbee specifications, and with radio regulations including ETSI EN 300 328, EN 300 440, EN 301 489-17, ARIB STD-T66, FCC CFR47 part 15 section 15.205, 15.209, 15.247 and 15.249, IC RSS-139 and RSS-210.

The 2.4 GHz RADIO supports the following features:

- Radio protocol:
  - Bluetooth Low Energy
  - IEEE802.15.4
  - Proprietary protocols
  - Concurrent mode
- Bluetooth LE
  - Data rate 1 Mpbs, 2 Mbps, 500 kbps, and 125 kbps.
  - Device privacy and network privacy modes
  - Anonymous device address types
  - Advertising extension PDUs
  - Advertising channel index
  - Periodic advertising synchronous transfer
  - High duty cycle, nonconnectable advertising
  - Channel selection algorithm #2
  - Angle of arrival (AoA), angle of departure (AoD)
  - Up to 20 connections in any role in addition to advertiser and scanner roles
  - Audio connected isochronous streams
  - Audio broadcast isochronous streams
- IEEE 802.15.4 features:
  - Beacon management
  - 16-bit short and 64-bit IEEE addressing modes
  - PAN formation along with association and disassociation
  - Full handshake protocol for transfer reliability, frame validation, and acknowledgment frame delivery
  - IEEE802.15.4 2020 MAC for non-beaconed PANs
- Matter
- Thread
- Zigbee
- External PA support
- Packet traffic arbitration

Figure 2. 2.4 GHz RADIO block diagram



3.11 PTA interface

The PTA interface enables packet traffic arbitration with other connectivity devices, as WiFi

PTA main features:

- based on IEEE802.15.2 standard
- supports both grant and deny signaling
- supports from 1- up to 4-wire protocols
- programmable transmit receive PTA_STATUS polarity
- programmable priority polarity
- programmable grant polarity
- programmable active polarity
- programmable PTA_ACTIVE timing
- programmable PTA_STATUS time multiplexed priority timing
- programmable transmit packet abort

3.12 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} and backup domain
  - Analog domain (V_{DDA})
  - SMPS power stage (V_{DDSMPS}, available only on SMPS packages)
  - V_{DDUSB} domain USB OTG (available only on USB packages)
  - V_{DDRF} for 2.4 GHz RADIO
- System supply voltage regulation
  - SMPS step-down converter

  - Voltage regulator (LDO)
- Power supply supervision
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- TrustZone security and privilege protection

3.12.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 to 3.6 V (functionality guaranteed down to V_{BORx} minimum value)
  External power supply for the I/Os, the internal regulator, the system analog such as reset, power management, and internal clocks, and the backup domain. It is provided externally through the VDD pins. VDDRF must be connected to the same supply used for VDD.
- V_{DDIO2} = 1.08 to 3.6 V
  External power supply for 14 I/Os (GPIOG[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage and must be connected to VDD (preferably) or to VSS pin when these I/Os are not used.
- V_{DDA} = 1.58 (COMP) / 1.62 (ADC) to 3.6 V
  External analog power supply for ADC and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and must be connected to VDD (preferably) or to VSS pin when these peripherals are not used.
- V_{REF+}
  Reference voltage for the ADC. It is also the output of the internal voltage reference buffer (VREFBUF) when enabled. The V_{REF+} can be connected to VSS pin when ADC and VREFBUF are not used. The VREF+ pin is not available on all packages, when not available, it is bonded to VDDA.
- V_{DDUSB} = 3.0 to 3.6 V
  External power supply for the USB OTG transceiver. It is provided externally through the VDDUSB pin. The V_{DDUSB} voltage level is independent from the V_{DD} voltage and must be connected to VDD (preferably) or to VSS pin when the USB OTG is not used.
- V_{DDSMPS} = 1.71 to 3.6 V
  External power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin, and must be connected to the same supply as V_{DD}.
- V_{LXSMPS} is the switched SMPS step down converter output.
  The SMPS power supply pins are available only on a specific package with SMPS step-down converter option.
- V_{DDRF} = 1.71 to 3.6 V
  External power supply for the 2.4 GHz RADIO, it must be connected to the same supply used for VDD.
- V_{DDANA} = 0 to 3.6 V (must be ≥ 1.2 V for 2.4 GHz RADIO operation)

An external power supply for the 2.4 GHz RADIO, can be connected to V_{DD11}.

- V_{DDRFPA} = 0 to 3.6 V (must be ≥ 1.2 V for 2.4 GHz RADIO operation)
  An external power supply for the 2.4 GHz RADIO and power amplifier regulator, can be connected to V_{DD11}. The maximum reachable transmit output power is determined by V_{DDRFPA} supply level.

The devices embed two regulators: one LDO and one SMPS in parallel to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, 2.4 GHz RADIO and embedded flash memory. The LDO generates this voltage on VCAP pin connected to a 4.7 µF (typical) external capacitor. The SMPS generates this voltage on VDD11 pin, with a total a 4.7 µF (typical) external capacitor. The SMPS requires an external 2.2 µH (typical) coil.

Both regulators can provide two different voltages (voltage scaling), and can operate in Stop modes.

It is possible to switch from SMPS to LDO and from LDO to SMPS on-the-fly.

Figure 3. Power supply overview (with SMPS)

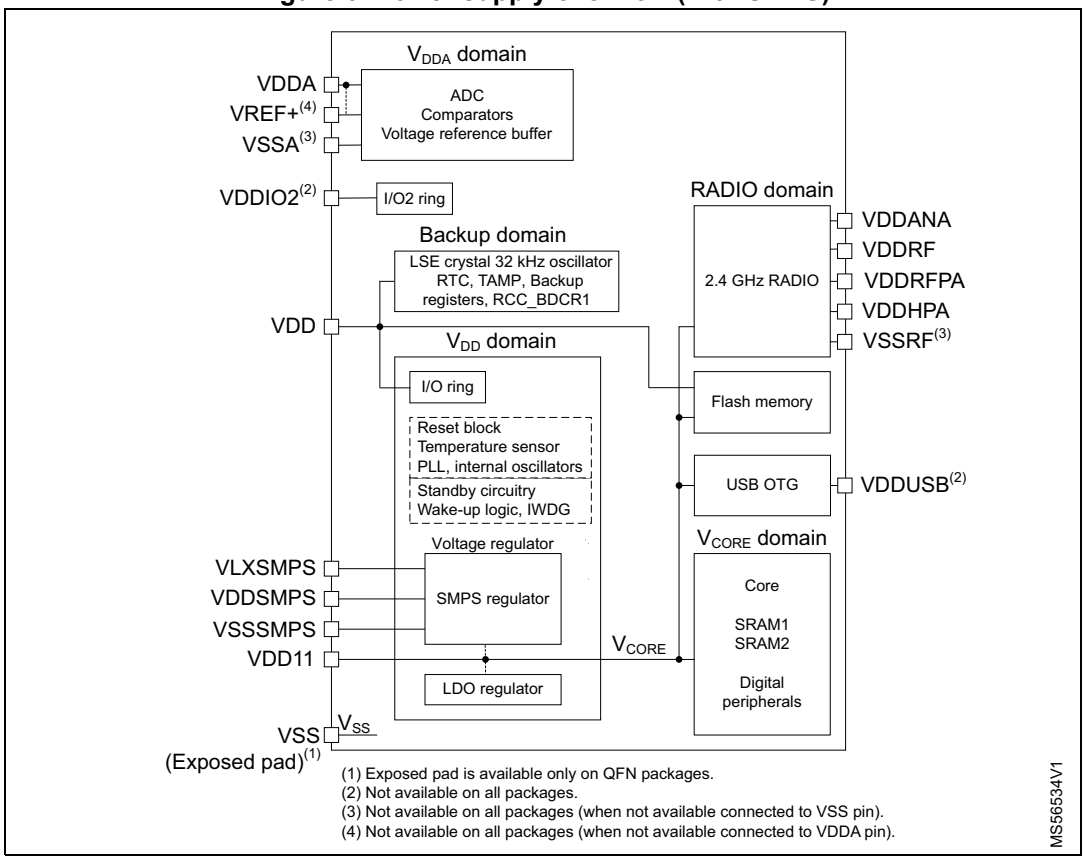
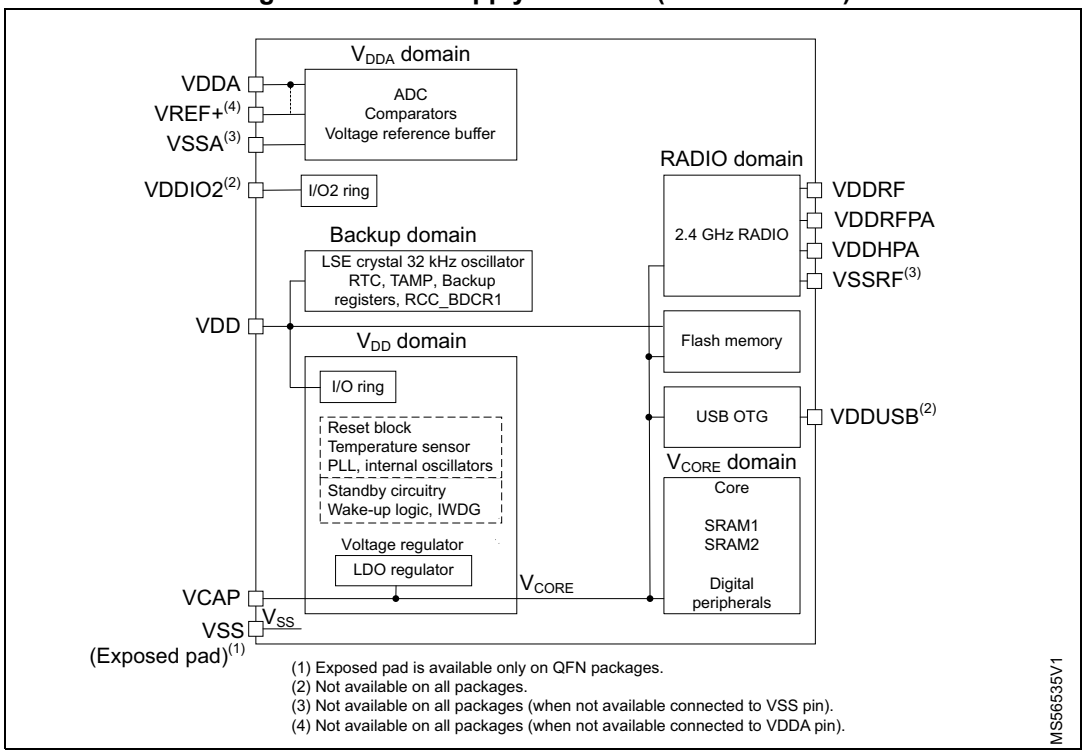


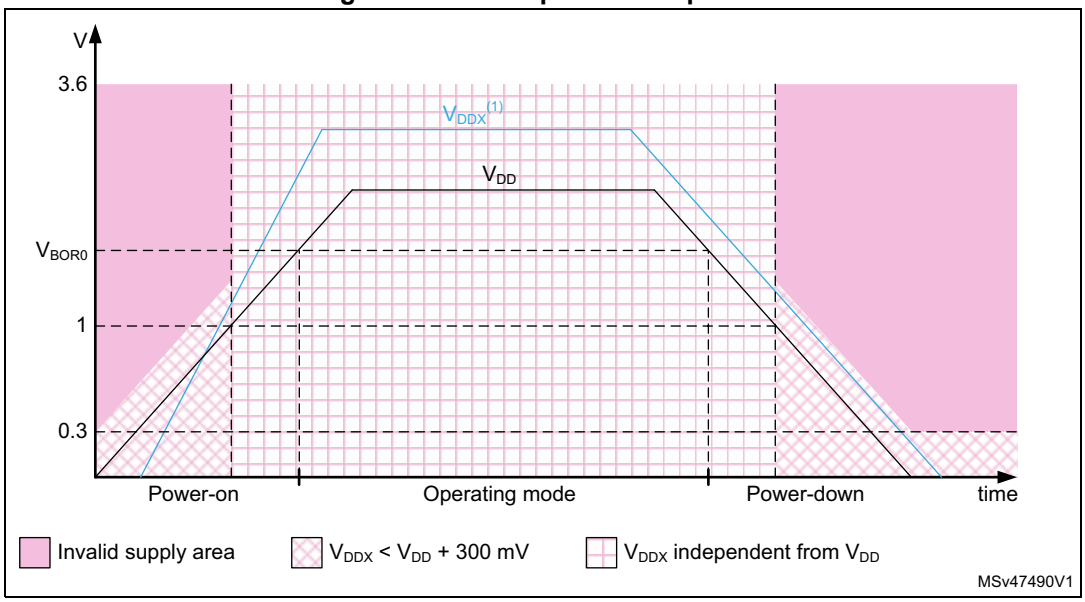
Figure 4. Power supply overview (without SMPS)



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (namely V_{DDA}, V_{DDIO2}, V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is equal to or above 1 V, other power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up /down sequence



1. V_{DDX} refers to power supplies V_{DDA},V_{DDIO2}, and V_{DDUSB}.

3.12.2 Power supply supervisor

The devices have an integrated ultra-low power BOR (brownout reset) active in all modes. The BOR ensures proper operation after power on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes. The devices feature an embedded PVD (programmable voltage detector) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below and/or rises above the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The devices support dynamic voltage scaling to optimize power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 (V_{CORE} = 1.2 V) with CPU and peripherals running at up to 100 MHz
- Range 2 (V_{CORE} = 0.9 V) with CPU and peripherals running at up to 16 MHz

Low-power modes

The devices support different low-power modes to achieve the best compromise between low-power consumption, startup time, available peripherals, and available wake-up sources.

Table 9. Operating modes overview

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range 2					All except USB OTG and 2.4 GHz RADIO	
Sleep	Range 1	No	ON	ON[4]	Any	All	Any interrupt or event
	Range 2					All except USB OTG and 2.4 GHz RADIO	
Stop 0	Range 1	No	OFF	ON[5]	LSE LSI[6]	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4[7] (temperature sensor), COMPx (x = 1, 2), USARTx (x = 1..3)[8], LPUART1, SPIx (x = 1..3)[9], I2Cx (x = 1..4)[10], LPTIMx (x = 1, 2)[11], GPIO, GPDMA1[12], 2.4 GHz RADIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), COMPx (x = 1, 2), USARTx (x = 1..3), LPUART1, SPIx (x = 1..3), I2Cx (x = 1..4), LPTIMx (x = 1, 2), GPDMA1, 2.4 GHz RADIO
	Range 2					All from Stop 0 Range 1 except USB OTG and 2.4 GHz RADIO	
Stop 1[13]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), COMPx (x = 1, 2), USARTx (x = 1..3), LPUART1, SPIx (x = 1..3), I2Cx (x = 1..4), LPTIMx (x = 1, 2), GPIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), COMPx (x = 1, 2), USARTx (x = 1..3), LPUART1, SPIx (x = 1..3), I2Cx (x = 1..4), LPTIMx (x = 1, 2)

Table 9. Operating modes overview (continued)

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Stop 2[14]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, LPUART1, SPI3, I2C3, LPTIM1, GPIO All other peripherals are powered off.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, LPUART1, SPI3, I2C3, LPTIM1
Standby retention	LPR	Powered off	OFF	ON[5]	LSE LSI	BOR, RTC, TAMP, IWDG, SLEEP_TIMER All other peripherals are powered off. I/O configuration can be retained, floating, pull-up or pull-down.	Reset pin, WKUPx (x = 1...8), BOR, RTC, TAMP, IWDG, SLEEP_TIMER
Standby	OFF			Powered off		All from mode Standby retention, except SLEEP_TIMER	

1. LPR means that the main regulator is OFF and the low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. The SRAM can be individually powered off to save power consumption.
6. HSI16 can be temporary enabled upon peripheral request, for autonomous functions with DMA or wake-up from Stop event detections.
7. The ADC conversion is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on conversion events.
8. UART and LPUART transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
9. SPI transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
10. I2C transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
11. LPTIM is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on all events.
12. GPDMA is functional and autonomous in Stop 0 mode, and can generate a wake-up interrupt on events.
13. Active peripherals ADC, COMP, USART, LPUART, SPI, I2C and LPTIM, can generate bus clock request and/or a wake-up interrupt on event.
14. Active peripherals LPUART1, SPI3, I2C3 and LPTIM1, can generate bus clock request and/or a wake-up interrupt on event.

By default, the microcontroller is in Run mode after a system or a power on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt or event occurs.

- **Stop 0 and Stop 1** modes

  Stop modes achieve the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the HSI16, and the HSE32 crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC, TAMP, IWDG and SLEEP_TIMER can remain active.

  Some peripherals are autonomous and can operate in Stop modes by requesting their kernel clock and their bus clock when needed, to transfer data with DMA Stop 0 modes will be entered. Refer to *PWR background autonomous mode (BAM)* for more details. In Stop modes the bus clocks when requested use HSI16.

  Stop 0 offer the largest number of active peripherals, with or without DMA, and wake-up sources, a smaller wake-up time but a higher consumption than Stop 1.

  In Stop 0 mode, the main regulator remains ON, allowing a very fast wake-up time, but with higher power consumption.

  Stop 1 is the lowest power mode with full retention, but the functional peripherals and sources of wake-up are reduced.

  The BOR can be configured in ultra-low power mode to further reduce consumption during Stop 1 mode.

  The system clock when exiting from Stop 0 or Stop 1 modes is HSI16.

- **Stop 2** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and some registers. All clocks in the V_{CORE} domain are stopped, the PLL, the HSI16, and the HSE32 crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC, TAMP, IWDG and SLEEP_TIMER can remain active.

  A reduced set of peripherals are autonomous and can operate in Stop 2 mode by requesting their kernel clock and their bus clock when needed. Refer to *PWR background autonomous mode (BAM)* for more details.

  Stop 2 is the lowest power mode with partial retention, but the functional peripherals and sources of wake-up are reduced.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Stop 2 mode.

  The system clock when exiting from Stop 2 modes is HSI16.

- **Standby retention and Standby** modes

  The Standby mode is used to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16 and the HSE32 crystal oscillators are also switched off. The LSE or LSI is still running.

  The RTC and IWDG can remain active.

  The BOR always remains active in Standby mode.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Standby mode.

  The state of each I/O during Standby mode can be retained with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAMs and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM1 and/or SRAM2 can be retained in Standby mode, supplied by the low-power regulator (Standby with RAM retention mode). Also optionally the 2.4 GHz RADIO can be retained in Standby mode, supplied by the low-power regulator (Standby with 2.4 GHz RADIO retention mode).

  The device exits Standby modes when an external reset (NRST pin), an IWDG event or reset, WKUP pin event (configurable rising or falling edge), an RTC event occurs (alarm, periodic wake-up, timestamp), or a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  When in Standby with 2.4 GHz RADIO retention mode also the SLEEP_TIMER can exit the device from Standby mode.

  The system clock after wake-up is HSI16.

PWR background autonomous mode (BAM)

The devices support BAM (background autonomous mode), that allows peripherals to be functional and autonomous in Stop mode (Stop 0, Stop 1 and Stop 2 modes), so without any software running.

In Stop 0 modes, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), USARTx (x = 1..3), LPUART1, SPIx (x = 1..3), I2Cx (x = 1..4), 2.4 GHz RADIO and GPDMA1. In this mode the GPDMA1 can be used to transfer data or control peripherals and access SRAM1 and SRAM2. The ADC4 can also be used to measure temperature. The 2.4 GHz RADIO is only autonomous in Stop 0 range 1.

In Stop 1 mode, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), USARTx (x = 1..3), LPUART1, SPIx (x = 1..3), I2Cx (x = 1..4). These peripherals can request a transition to Stop 0 mode allowing then data transfers with GPDMA1.

In Stop 2 mode, the autonomous peripherals are the following: LPTIM1, LPUART1, SPI3, I2C3. These peripherals can request a transition to Run mode allowing then data transfers.

Those peripherals support the features detailed below:

- Functionality in Stop mode thanks to its own independent clock (named kernel clock) request capability: the peripheral kernel clock is automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it.
- DMA transfers supported in Stop 0 mode thanks to system clock request capability: the system clock (HSI16) automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it. When the system clock is requested by an autonomous peripheral, Stop 0 mode is automatically entered and the

system clock is woken up and distributed to all peripherals enabled in the RCC. This allows the DMA to access the enabled SRAM, and any enabled peripheral register (for instance GPIO registers). When no peripheral requests its bus clock Stop 1 mode is automatically re-entered when Stop 1 mode selected as low-power mode.

- Automatic start of the peripheral thanks to hardware synchronous or asynchronous triggers (such as I/Os edge detection and low-power timer event).
- Wake-up from Stop mode with peripheral interrupt.

The GPDMA is fully functional and the linked-list is updated in Stop 0 mode, allowing the different DMA transfers to be linked without any CPU wake-up. This can be used to chain different peripherals transfers, or to write peripherals registers in order to change their configuration while remaining in Stop 0 mode.

The DMA transfers from memory to memory can be started by hardware synchronous or asynchronous triggers, and the DMA transfers between peripherals and memories can also be gated by those triggers.

Here below some use-cases that can be done while remaining in Stop mode:

- A/D conversion triggered by a low-power timer (or any other trigger)
  - wake-up from Stop mode on analog watchdog if the A/D conversion result is out of programmed thresholds
  - wake-up from Stop mode on DMA buffer event
- I^2C slave reception or transmission, SPI reception, UART/LPUART reception
  - wake-up at the end of peripheral transfer or on DMA buffer event
- I^2C master transfer, SPI transmission, UART/LPUART transmission, triggered by a low-power timer (or any other trigger):
  - example: sensor periodic read
  - wake-up at the end of peripheral transfer or on DMA buffer event
- Bridges between peripherals
  - example: ADC converted data transferred by communication peripherals
- Data transfer from/to GPIO to/from SRAM for:
  - controlling external components
  - implementing data transmission and reception protocols

Table 10. Functionalities depending on the working mode(1)

Peripheral	Run		Sleep		Stop 0			Stop 1		Stop 2		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
CPU	Y		R		R		-	R	-	R	-	-	-	-	-
Flash memory	O(2)		O(2)		R		-	R	-	R	-	R	-	R	-
Flash interface	O		R		R		-	R	-	R	-	-	-	-	-
SRAM1	O		O		O(3)		-	O(3)	-	O(3)	-	O(3)	-	-	-
SRAM2	O		O		O(3)		O(4)	O(3)		O(3)		O(3)	-	-	-

Table 10. Functionalities depending on the working mode[1] (continued)

Peripheral	Run		Sleep		Stop 0			Stop 1		Stop 2		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
RAMCFG	O		R		R		-	R	-	R	-	-	-	-	-
Backup registers	O		O		O		-	R	-	R	-	R	-	R	-
PWR	O		O		R		-	R[5]	-	R[5]	-	-	-	-	-
RCC	O		O		R[6]		-	R[6]	-	R[6]	-	-	-	-	-
EXTI	O		R		R		-	R	-	R	-	-	-	-	-
SYSCFG	O		R		R		-	R	-	R	-	-	-	-	-
ICACHE	O		R		R		-	R	-	R	-	-	-	-	-
2.4 GHz RADIO	O	R	O	R	O	R	O	R	-	-	-	-	-	-	-
2.4 GHz RADIO SRAM	O	R	O	R	O	R	-	R	-	R	-	R	-	-	-
PTACONV	O		O		O	R	-	R	-	-[7]	-	-	-	-	-
SLEEP_TIMER	O		O		O		O	O	O	O	O	O	O	-	-
BOR	Y		Y		Y		Y	Y	Y	Y	Y	Y	Y	Y	Y
PVD	O		O		O		O	O	O	O	O	-	-	-	-
HSI16	O		O		O[8]		-	O[8]	-	O[8]	-	-	-	-	-
HSE32	O		O		O[9]	-	-	-	-	-	-	-	-	-	-
LSI	O		O		O		-	O	-	O	-	O	-	O	-
LSE	O		O		O		-	O	-	O	-	O	-	O	-
HSECSS	O		O		O	-	O	-	-	-	-	-	-	-	-
LSECSS	O		O		O		O	O	O	O	O	O	O	O	O
IWDG	O		O		O		O	O	O	O	O	O	O	O	O
RTC	O		O		O		O	O	O	O	O	O	O	O	O
TAMP tamper pins	Up to 6		Up to 6		Up to 6		O	Up to 6	O	Up to 6	O	Up to 6	O	Up to 6	O
GPIO pins	O		O		O		O	O	O	O	O	O/R (10)	O (11)	O/R (10)	O (11)
USARTx (x = 1..3)	O		O		O		O[12]	O	O[12]	-	-	-	-	-	-
LPUART1	O		O		O		O[12]	O	O[12]	O	O[12]	-	-	-	-
I2Cx (x = 1, 2, 4)	O		O		O		O[13]	O	O[13]	-	-	-	-	-	-
I2C3	O		O		O		O[13]	O	O[13]	O	O[13]	-	-	-	-
SPIx (x = 1, 2)	O		O		O		O[14]	O	O[14]	-	-	-	-	-	-

Table 10. Functionalities depending on the working mode(1) (continued)

Peripheral	Run		Sleep		Stop 0			Stop 1		Stop 2		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
SPI3	O		O		O		O(14)	O	O(14)	O	O(14)	-	-	-	-
ADC4	O		O		O		O(15)	O	O(15)	-	-	-	-	-	-
COMPx (x = 1, 2)	O		O		O		O	O	O	-	-	-	-	-	-
LPTIM1	O		O		O		O(16)	O	O(16)	O	O(16)	-	-	-	-
LPTIM2	O		O		O		O(16)	O	O(16)	-	-	-	-	-	-
GPDMA1	O		O		O		O(17)	R	-	-	-	-	-	-	-
USB OTG	O	-	O	-	R	-	O	-	-	-	-	-	-	-	-
TIMx (x = 1, 2, 3, 4, 16, 17)	O		O		R		-	R	-	-	-	-	-	-	-
SAI1	O		O		R		-	R	-	-	-	-	-	-	-
TSC	O		O		R		-	R	-	-	-	-	-	-	-
RNG	O		O		R		-	R	-	-	-	-	-	-	-
AES and SAES	O		O		R		-	R	-	-	-	-	-	-	-
PKA	O		O		R		-	R	-	-	-	-	-	-	-
HASH	O		O		R		-	R	-	-	-	-	-	-	-
CRC	O		O		R		-	R	-	-	-	-	-	-	-
HSEM	O		R		R		-	R	-	-	-	-	-	-	-
GTZC_TZSC	O		R		R		-	R	-	R	-	-	-	-	-
GTZC_TZIC	O		R		R		-	R	-	R	-	-	-	-	-
GTZC_MPCBB1	O		R		R		-	R	-	R	-	-	-	-	-
GTZC_MPCBB2	O		R		R		-	R	-	R	-	-	-	-	-
GTZC_MPCBB6	O		R		R		-	R	-	R	-	-	-	-	-
WWDG	O		O		R		-	R	-	R	-	-	-	-	-
SysTick timer	O		O		R		-	R	-	R	-	-	-	-	-
DBGMCU	O		O		O(18)		-	O (18)	-	O (18)	-	O (19)	-	O (19)	-

1. Legend: Y = yes (enabled). O = optional (disabled by default, can be enabled by software).R = retained, - = not available.
   Gray cells highlight the wake-up capability in each mode.
2. The flash memory can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAMs can be powered on or off independently.
4. Parity error interrupt or NMI wake-up from Stop mode.
5. PWR voltage scaling is reset to range 2.
6. RCC sysclk source is reset to HSI16.

7. PTACONV interface signal levels can be retained on GPIOs.
8. Some peripherals with autonomous mode and wake-up from Stop capability can request HSI16 to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically put off when no peripheral needs it.
9. The 2.4 GHz RADIO peripheral in autonomous mode request HSE32 to be enabled. In this case, the oscillator is kept active by the peripheral, and is automatically put off when it no longer needs it.
10. I/O levels can be retained with pull-up, pull-down, or floating.
11. There are 16 wake-up pins available.
12. UART and LPUART reception and transmission are functional and autonomous in Stop mode in asynchronous and in SPI master modes, and generate a wake-up interrupt on transfer events.
13. I2C reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
14. SPI reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
15. A/D conversion is functional and autonomous in Stop mode, and generates a wake-up interrupt on conversion events.
16. LPTIM is functional and autonomous in Stop mode, and generates a wake-up interrupt on events.
17. GPDMA transfers are functional and autonomous in Stop 0 mode, and generates a wake-up interrupt on transfer events.
18. DBGMCU remains accessible trough AP0.
19. DBGMCU remains accessible through AP0 when CDBGPWRUPREQ is set.

3.12.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.12.4 PWR TrustZone security

When TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security secures the following configuration:

- Low-power mode
- WKUP (wake-up) pins
- Voltage detection
- Backup domain control

Some of the PWR configuration bits security is defined by the security of other peripherals:

- The VOS (voltage scaling) configuration is secure when the system clock selection is secure in RCC.
- The I/O Standby mode retention configuration is secure when the corresponding GPIO is secure.

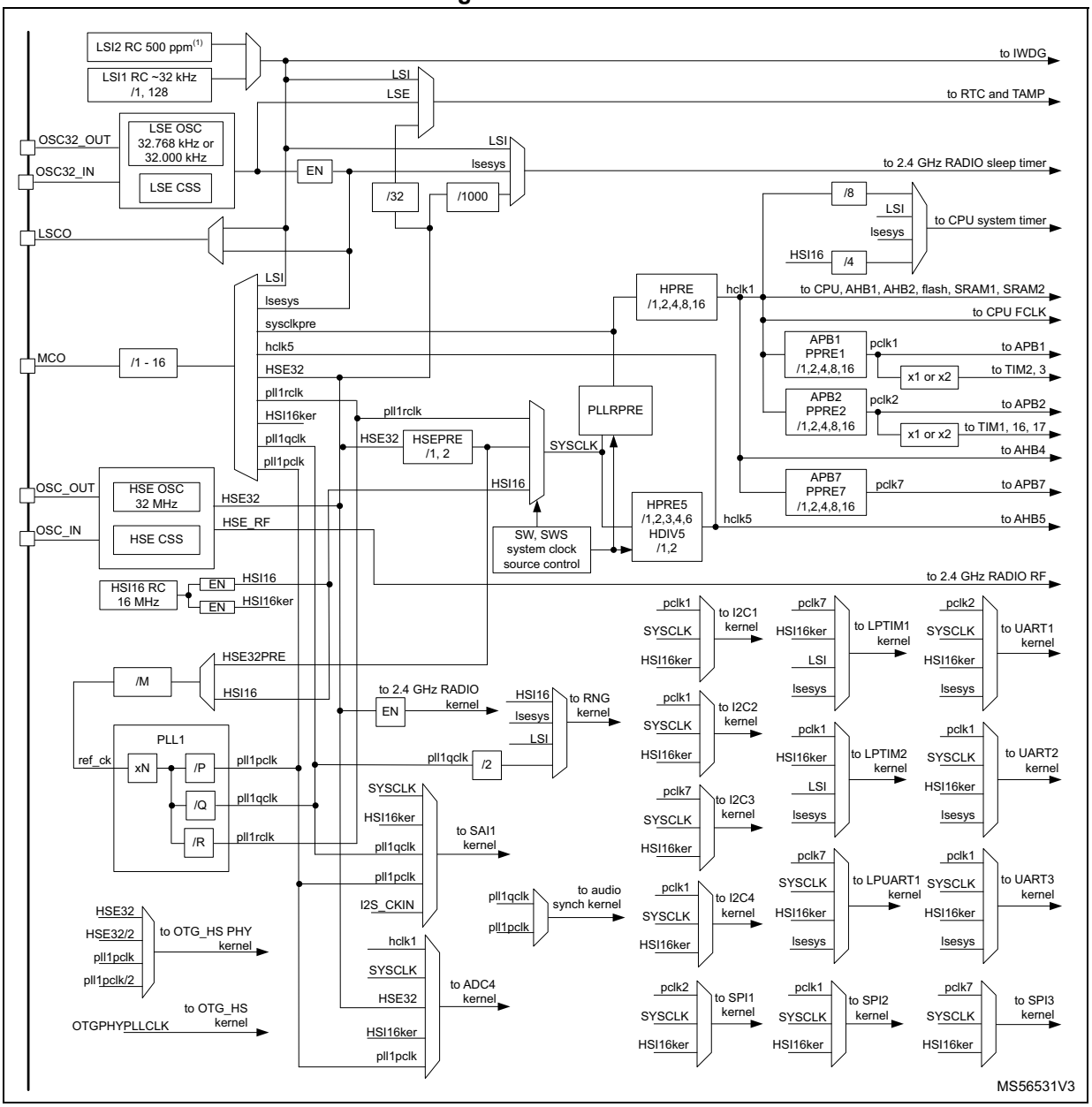
3.13 Reset and clock controller (RCC)

The RCC (reset and clock controller) manages device and peripheral reset and distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- Device reset source monitoring.
- Individual peripheral reset control.
- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- Clock selection system: clock sources can be changed safely on-the-fly in Run mode through a configuration register.
- Clock management: in order to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- System clock source: different clock sources can be used to drive the system clock SYSCLK:
  - HSE32 (32 MHz high-speed external crystal oscillator), trimmable by software. The HSE32 can also be used with an external clock.
  - HSI16 (16 MHz high-speed internal RC oscillator), trimmable by software.
  - System PLL, can be fed by HSE32 or HSI16 with a maximum output frequency at 100 MHz.
- Auxiliary clock source: two ultra-low power clock sources that can be used to drive e.g. the real-time clock:
  - LSE (32.000 kHz or 32.768 kHz low-speed external crystal oscillator), supporting programmable drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - LSI (~32 kHz low-speed internal RC oscillators), also used to drive the independent watchdog.
    The LSI1 clock absolute accuracy is ±5%, it can be divided by 128 to output a 250 Hz source clock.
    The LSI2 clock has a high stability, ±500 ppm. It can be used to drive the 2.4 GHz RADIO sleep timer.
- Peripheral clock sources: several peripherals have their own independent kernel clock whatever the system clock. The PLL has three independent outputs allowing the highest flexibility and can generate clocks for the ADC, SAI, USB OTG and the RNG.
- Startup clock: after reset, the microcontroller restarts by default with the HSI16. The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- CSS (Clock security systems): these features can be enabled by software.
  - If a HSE32 clock failure occurs, the system clock automatically switches to HSI16 and a software interrupt is generated if enabled.
  - LSE failure can also be detected and generates an interrupt, in this case the clock switches to LSI.
- Clock-out capability:
  - MCO (microcontroller clock output): outputs one of the internal clocks for external use by the application. (only available in Run, Sleep and Stop mode)
  - LSCO (low-speed clock output): outputs LSI or LSE in all operating modes.

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 100 MHz, except for AHB5 domain, which is limited to maximum 32 MHz.

Figure 6. Clock tree



3.13.1 RCC TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security secures some RCC system configuration and peripheral configuration from being read or modified by nonsecure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- For securable peripherals, when the corresponding SEC security bit is set in the TZSC (TrustZone security controller).
- For TrustZone-aware peripherals, when a security feature of the peripheral is enabled through dedicated peripheral bits.

3.14 General-purpose input/output (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence, to avoid spurious writing to the I/Os registers.

The GPIO allows dynamic I/O control in Stop 0 mode thanks to GPDMA1. All I/Os can be configured and controlled as input or output (open-drain or push-pull depending on GPIO configuration).

When enabled in the PWR, latest I/Os output level can be retained by pulling the I/Os high or low before entering Standby mode. I/O levels are retained after exit from Standby mode, until they are reconfigured by software.

3.14.1 GPIO TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a nonsecure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.15 System configuration controller (SYSCFG)

The main purpose of the SYSCFG (system configuration controller) are the following:

- Managing robustness features
- Configuring FPU interrupts
- Enabling/disabling the I^2C fast-mode plus (FMP) high-drive mode of some I/Os and booster for I/Os analog switches
- Managing the I/O compensation
- Provides memory erase status
- Communication channel with the RSS

3.15.1 SYSCFG TrustZone security

When TrustZone security is activated by the TZEN option bit, the SYSCFG is switched in TrustZone security mode.

The SYSCFG TrustZone security secures the following configuration:

- FPU interrupt configuration
- Robustness features
- I/O compensation and memory erase status

Some of the SYSCFG configuration bits security is defined by the security of other peripherals:

- The FMP high-drive mode of some I/Os configuration is secure when the corresponding GPIO is secure.
- The booster for I/Os analog switches configuration is secure when the ADC4 is secure.

3.16 Peripheral interconnect matrix

Several peripherals have direct connections between them, enabling autonomous communication between them, and saving CPU resources (and power consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep and Stop modes.

3.17 General purpose direct memory access controller (GPDMA)

The general purpose direct memory access (GPDMA) controller is a bus master and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Run, Sleep and Stop 0 modes
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers

  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone support:
  - Support for secure and nonsecure DMA transfers, independently at a first channel level, and independently at a source/destination and link sub-levels
  - Secure and nonsecure interrupts reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone-aware AHB slave port, protecting any DMA secure resource (register, register field) from a nonsecure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

Table 11. GPDMA1 channels implementation and usage

Channel x	Hardware parameters		Features
	dma_fifo_size[x]	dma_addressing[x]	
x = 0 to 5	2	0	Channel x is implemented with: – a FIFO of 8 bytes, 2 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between an APB or AHB peripheral and SRAM.
x = 6 to 7	4	0	Channel x is implemented with: – a FIFO of 32 bytes, 8 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between a demanding AHB or APB peripheral and SRAM.

Table 12. GPDMA1 autonomous mode and wake-up in low-power modes

Feature	Low-power modes
Autonomous mode and wake-up	Sleep, Stop 0 modes

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller (NVIC) that is able to manage 16 priority levels and to handle up to 70 maskable interrupt vectors plus the 16 interrupt vectors of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support: NVIC registers banked across secure and nonsecure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The extended interrupts and event controller (EXTI) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the

power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run and Sleep modes. The EXTI also includes the peripheral interconnect EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure
- EXTI I/O port selection for peripheral interconnect use.

3.19 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, that can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.20 Analog-to-digital converter (ADC4)

The devices embed one 12-bit successive approximation analog-to-digital converter.

Table 13. ADC features

ADC modes/features(1)	ADC4
Resolution	12 bits
Maximum sampling speed for 12-bit resolution	2.5 Msps
Hardware offset calibration	X
Hardware linearity calibration	-
Single-ended inputs	X
Differential inputs	-

Table 13. ADC features (continued)

ADC modes/features[1]	ADC4
Injected channel conversion	-
Oversampling	Up to x256
Data register	16 bits
DMA support	X
Autonomous mode	X
Offset compensation	-
Gain compensation	-
Number of analog watchdogs	3
Wake-up from Stop mode	X

1. X = supported.

ADC4 has up to 19 multiplexed channels, allowing it to measure signals from up to 10 external and 3 internal sources (the other channels are reserved). The conversion of the various channels can be performed in Single, Continuous, Scan or Discontinuous mode. The result of is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency. The ADC4 is autonomous in low-power modes down to Stop modes.

A built-in hardware oversampler allows analog performances to be improved while off-loading the related computational burden from the CPU.

The ADC4 main features are:

- High performance
  - 12-, 10-, 8- or 6-bit configurable resolution
  - ADC conversion time: 0.4 µs for 12-bit resolution (2.5 MHz), faster conversion times obtained by lowering resolution
  - Self-calibration
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low-power
  - PCLK frequency reduced for low-power operation while still keeping optimum ADC performance
  - Wait mode: ADC overrun prevented in applications with low frequency PCLK
  - Auto-off mode: ADC automatically powered off except during the active conversion phase, dramatically reducing the ADC power consumption
  - Autonomous mode: in low-power modes (down to Stop 1), the ADC4 automatically switches on when a trigger occurs to start conversion, and it automatically switches off after conversion. Data are transfered to SRAM with DMA.
  - ADC4 interrupts wake up the device down to Stop 1 mode.

- Analog input channels
  - Up to 10 external analog inputs
  - One channel for the internal temperature sensor (V_{SENSE})
  - One channel for the internal reference voltage (V_{REFINT})
  - One channel for the internal digital core voltage (V_{CORE})
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity (timer events or GPIO input events)
- Conversion modes
  - Conversion of a single channel or scan of a sequence of channels
  - Selected inputs converted once per trigger in Single mode
  - Selected inputs converted continuously in Continuous mode
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events, with wake-up from Stop capability
- Three analog watchdogs
- ADC supply requirements: 1.62 to 3.6 V
- ADC input range: $V_{SSA} < V_{IN} < V_{DDA}$

Note: The ADC4 analog block clock frequency after the ADC4 prescaler must be between 140 kHz and 55 MHz.

Note: V_{SSA} is connected to package pin VSS.

3.20.1 Temperature sensor (V_{SENSE})

The temperature sensor generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to ADC4 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

Table 14. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor ADC4 12-bit raw data acquired at (30 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BFA 0710 - 0x0BFA 0711
TS_CAL2	Temperature sensor ADC4 12-bit raw data acquired at (130 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BFA 0742 - 0x0BFA 0743

3.20.2 Internal voltage reference (V_{REFINT})

The internal voltage reference voltage V_{REFINT} provides a stable (bandgap) voltage for the ADC and comparators. The V_{REFINT} is internally connected to ADC4 input channel that is used to convert the voltage into a digital value.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

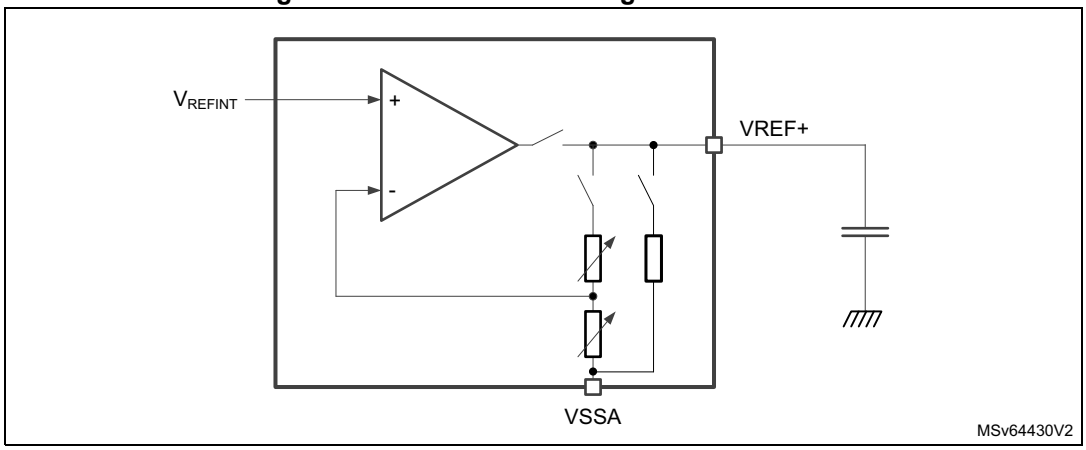
Table 15. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Internal voltage reference ADC4 12-bit raw data acquired at (30 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BFA 07A5 - 0x0BFA 07A6

3.21 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer (VREFBUF) that can be used as voltage reference for the ADC and external components through the VREF+ pin.

Figure 7. VREFBUF block diagram



The internal VREFBUF supports four voltages between 1.5 and 2.5 V, for more information see VREFBUF characteristics.

When the VREFBUF is disabled, an external voltage reference can be provided through the VREF+ pin.

3.22 Comparators (COMP)

The devices embed two rail-to-rail comparators, COMP1 and COMP2, with programmable reference voltage (internal or external), hysteresis and speed (low-speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- internal reference voltage or sub-multiple (1/4, 1/2, 3/4).
- external reference voltage on GPIO in function COMPx_INM.

All comparators can wake up from Stop 0 and Stop 1 modes, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.23 Touch sensing controller (TSC)

The TSC (touch sensing controller) provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The TSC is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The TSC main features are the following:

- Proven and robust surface charge transfer acquisition principle
- Support of up to 24 capacitive sensing channels
- Up to eight capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the packages and subject to I/O availability.

3.24 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- Produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz (256 RNG clock cycles otherwise)
- Embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- Has an AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

3.25 Secure advanced encryption standard hardware accelerator (SAES) and encryption standard hardware accelerator (AES)

The devices embed two AES accelerators: SAES and AES. The SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. The SAES can share its current key register information with the faster AES using a dedicated hardware bus.

The SAES and the AES can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM and GMAC chaining is supported by both SAES and AES.

SAES and AES support DMA single transfers for incoming and outgoing data (two DMA channels required).

The SAES supports the selection of all the following key sources, while the AES support only the first:

- 256-bit software key, written by the application in the key registers (write only)
- 256-bit DHUK (derived hardware unique key), computed inside the SAES engine from a non-volatile OTP based RHUK (root hardware unique key)
- 256-bit BHK (boot hardware key), stored in tamper-resistant secure backup registers, written by a secure code during boot. Once written, this key cannot be read or write by any application until the next product reset.
- XOR of DHUK (provisioned chip secret) and BHK (software secret)

DHUK, BHK and their XOR are not visible by any software (even secure).

Note: 128-bit key size can also be selected.

BHK key is cleared in case of tamper or RDP regression.

When the SAES is secure (respectively nonsecure), DHUK secure (respectively nonsecure) is used.

The SAES peripheral is connected by hardware to the true random number generator RNG (for side-channel resistance).

The SAES and AES peripherals support:

- Compliant implementation of standard NIST *Special Publication 197, Advanced Encryption Standard (AES)* and *Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for cipher keys length of 128- and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 528 or 743 clock cycle latency in ECB encryption mode for SAES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit input buffer and one 32-bit output buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- Possibility for software to suspend a message if the SAES/AES needs to process another message with a higher priority (suspend/resume operation)
- SAES additional features:
  - Security context enforcement for keys
  - Hardware secret key encryption/ decryption (wrapped key mode) and sharing with faster AES peripheral (Shared key mode)
  - Protection against DPA (differential power analysis) and related side-channel attacks
  - Optional hardware loading of two hardware secret keys (BHK, DHUK) that can be XORed together

On top of standard AES encryption and decryption with a key loaded by software, SAES peripheral makes possible the following advanced use cases:

- Allow or deny the sharing of a key between a secure and a nonsecure application, enforced by hardware
- Encrypt once a key using side-channel resistant AES, then share it to a faster AES engine by decrypting it (Shared key mode)
- On-chip encrypted storage using secret DHUK

- Transport key generation by encrypting the device public unique ID with the application secret BHK
- Binding of device secure storage keys, using the secret derived hardware unique key (DHUK) XORed with the secret boot hardware key (BHK). If BHK is lost, the whole device secure storage is lost.

Note: Encrypted storage or derived keys that are using DHUK or BHK, cannot be used anymore when a security breach is detected.

Table 16. AES/SAES features

AES/SAES modes/features(1)	AES	SAES
ECB, CBC chaining	X	X
CTR, CCM, GCM chaining	X	X
AES 128-bit ECB encryption in cycles	51	528
DHUK and BHK key selection	-	X
Side-channel attacks resistance	-	X
Shared key between SAES and AES	X	

1. X = supported.

3.26 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA2-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the keyed-hash message authentication code (HMAC) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes Federal information processing standards (FIPS) approved digests of length of 160, 224, 256 bits, for messages of up to (2^{64} – 1) bits. It also computes 128 bits digests for the MD5 algorithm.

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital* Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 1321, *MD5* Message-Digest Algorithm
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message* Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA-256, and MD5
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - 66 clock cycles for processing one 512-bit block of data using MD5 algorithm

- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest
- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.27 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, DU (Diffie-Hellmann) or (ECC) elliptic curve cryptography over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA CRT (Chinese remainder theorem) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- Protection against DPA (differential power analysis) and related side-channel attacks.

3.28 Timers and watchdogs

The devices include one advanced control timer, up to five general-purpose timers, two low-power timers, two watchdog timers and two SysTick timers.

Table 17 compares the features of the advanced control, general-purpose and basic timers.

Table 17. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1	16 bits	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM4	32 bits	Up, down, Up/down			4	No
	TIM3,	16 bits				4	No
	TIM16, TIM17		Up			1	1

3.28.1 Advanced-control timers (TIM1)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.28.2 General-purpose timers (TIM2, TIM3, TIM4, TIM16, TIM17)

There are up to five synchronizable general-purpose timers embedded in the device (see *Table 17* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3 and TIM4
  - They are full-featured general-purpose timers with TIM2 and TIM4 32-bit auto-reload up/downcounter, TIM3 16-bit auto-reload up/downcounter, all with 16-bit prescaler.
  - These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
  - The counters can be frozen in Debug mode.
  - All have independent DMA request generation and support quadrature encoders.
- TIM16 and 17
  - They are general-purpose timers with mid-range features.
  - They have 16-bit auto-reload upcounters and 16-bit prescalers. and have one channel and one complementary channel.
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The timers can work together via the *Timer Link* feature for synchronization or event chaining. The timers have independent DMA request generation.
  - The counters can be frozen in Debug mode.
  - All have independent DMA request generation.

3.28.3 Low-power timers (LPTIM1, LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by HSI16, LSE, LSI or an external clock. They are able to wake up the system from Stop mode.

LPTIM1, LPTIM2 are active in Stop modes. Only LPTIM1 is active in Stop 2 mode.

The low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with following possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity

- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.28.4 Infrared interface (IRTIM)

An infrared interface (IRTIM) for remote control is available on the device. It can be used with an infrared LED to perform remote control functions. It uses internal connections with TIM16 and TIM17.

3.28.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and a 10-bit prescaler. It is clocked from the independent LSI and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software enabled through the option bytes. The counter can be frozen in low-power and Debug mode.

3.28.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.28.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone is disabled, only one SysTick timer is available.

This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.29 Real-time clock (RTC)

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

As long as the VDD supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in binary-coded decimal (BCD) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a reference clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied from the V_{DD} supply.

The RTC clock sources can be one of the following:

- LSE, used as 32.768 kHz external crystal oscillator
- LSE, with external resonator or oscillator
- LSI, internal low-power RC oscillator (with typical frequency of 32 kHz)
- HSE32, high-speed external clock divided by a prescaler in the RCC.

The RTC is functional in all low-power modes when it is clocked by the LSE or LSI.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.30 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained in all low-power modes. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with six tamper pins and nine internal tampers. The external tamper pins can be configured for level

detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, SRAM2, ICACHE and cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the Backup domain that remains powered-on by V_{DD} power.
- Up to six tamper pins for six external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from three meshes (each input associated to its own exclusive output) to five meshes (single output shared for up to five tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Nine internal tamper events to protect against transient or environmental perturbation attacks:
  - LSE monitoring
  - RTC calendar overflow
  - JTAG/SWD access if RDP different from 0
  - Monotonic counter overflow
  - Cryptographic peripherals fault (RNG, SAES, AES, PKA)
  - Independent watchdog reset when tamper flag is already set
  - Three ADC4 watchdogs
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate a RTC time stamp event.
- TrustZone support:
  - Tamper secure or nonsecure configuration.
  - Backup registers configuration in three configurable-size areas:
    - a read/write secure area
    - a write secure/read nonsecure area
    - a read/write nonsecure area
  - Secret boot hardware key (BHK) only usable by secure SAES peripheral, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.31 Inter-integrated circuit interface (I2C)

The device embeds up to four I2C, refer to *Table 18* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multi-master capability
  - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware packet error checking (PEC) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Autonomous functionality in Stop modes with wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 18. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 Kbit/s)	X	X	X	X
Fast-mode (up to 400 Kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Autonomous in Stop 0, 1 modes with wake-up capability	X	X	X	X
Wake-up capability in Stop 2 mode	-	-	X	-

1. X: supported

3.32 Universal synchronous/asynchronous receiver transmitter (USART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have up to three embedded universal synchronous receiver transmitters (USART1, USART2, USART3) and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 19. USART and LPUART features

USART modes/features(1)	USART1	USART2	USART3	LPUART1
Hardware flow control for modem	X	X	X	X
Continuous communication using DMA	X	X	X	X
Multiprocessor communication	X	X	X	X
Synchronous mode (master/slave)	X	X	X	-
Smartcard mode	X	X	X	-
Single-wire half-duplex communication	X	X	X	X
IrDA SIR ENDEC block	X	X	X	-
LIN mode	X	X	X	-
Dual-clock domain, wake-up from Stop modes	X	X	X	X
Dual-clock domain, wake-up from Stop 2 modes	-	-	-	X
Receiver timeout interrupt	X	X	X	-
Modbus communication	X	X	X	-
Auto-baud rate detection	X	X	X	-
Driver enable	X	X	X	X
USART data length	7, 8, and 9 bits			
Tx/Rx FIFO	X	X	X	X
Tx/Rx FIFO size	8 bytes			
Autonomous in Stop 0, 1 modes with wake-up capability	X	X	X	X
Wake-up capability in Stop 2 mode	-	-	-	X

1. X = supported.

3.32.1 USART

The USART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the direct memory access (DMA) for multibuffer configuration.

The USART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data
  Each FIFO can be enabled/disabled by software and come with a status flag.
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.32.2 LPUART

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data (each FIFO can be enabled/disabled by software and come with status flags for FIFOs states)
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags

- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop modes with wake-up.

3.33 Serial peripheral interface (SPI)

The devices embed up to three serial peripheral interfaces (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO and MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16 x or 8 x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)

- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

Table 20. SPI features

Feature[1]	SPI1, SPI2 (full feature set instances)	SPI3 (limited feature set instance)
Data size	Configurable from 4- to 32-bit	8- and 16-bit
CRC computation	CRC polynomial length, configurable from 5- to 33-bit	CRC polynomial length, configurable from 9- to 17-bit
Size of FIFOs	16 x 8-bit	8 x 8-bit
Number of transfered data	Unlimited, expandable	Up to 1024, no data counter
Autonomous in Stop 0, 1 modes with wake-up capability	X	X
Wake-up capability in Stop 2 mode	-	X

1. X: supported

3.34 Serial audio interfaces (SAI)

The devices embed one SAI, see *Table 21* for its features. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks that can be transmitters or receivers with their respective FIFOs
- 8-word integrated FIFOs for each audio sub-block
- Synchronous or Asynchronous mode between the audio sub-blocks
- Master or slave configuration independent for both audio sub-blocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24- and 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I^2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in Slave mode
  - Late frame synchronization signal detection in Slave mode
  - Codec not ready for the AC'97 mode in reception
- Interruption sources when enabled:
  - Errors
  - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block

Table 21. SAI implementation

Features	SAI1
I^2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/mono audio frame capability	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, and 32-bit	X

Table 21. SAI implementation (continued)

Features	SAI1
FIFO size	X (8 words)
SPDIF	X
PDM	X

3.35 USB on-the-go high-speed (USB OTG)

The devices embed an USB OTG high-speed device/host peripheral with integrated transceivers. This peripheral is compliant with the USB 2.0 specification. It has software-configurable endpoint setting, and supports suspend/resume.

This interface requires a precise 60 MHz clock that is generated from the internal USB OTG HS PHY PLL (the clock source must use the HSE crystal oscillator).

The USB OTG HS features are:

- USB-IF certified to the Universal Serial Bus Specification Rev 2.0
- On-chip high-speed PHY
- Full support (PHY)
  - Integrated support for A-B device identification (ID line)
  - Supports monitoring of V_{BUS} levels with internal comparators
- Software-configurable to operate as USB high-speed device/host role device
- Supports HS/FS SOF and LS keep-alives with
  - SOF pulse PAD connectivity
  - SOF pulse internal connection to timer (TIMx)
  - Configurable framing period
  - Configurable end of frame interrupt
- Internal DMA with thresholding support and software selectable AHB burst type in DMA mode
- Power saving features, such as system stop during USB OTG suspend, switch-off of clock domains internal to the digital core, PHY and DFIFO power management
- Dedicated RAM of 4 Kbytes with advanced FIFO control:
  - Configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM
  - Each FIFO able to hold multiple packets
  - Dynamic memory allocation
  - Configurable FIFO sizes that are not powers of two to allow the use of contiguous memory locations
- Max guaranteed USB bandwidth for up to one frame (1 ms) without system intervention

Host-mode features:

- External charge pump for V_{BUS} voltage generation
- Up to 16 host channels (pipes): each channel is dynamically reconfigurable to allocate any type of USB transfer
- Built-in hardware scheduler holding:

  - Up to 16 interrupt plus isochronous transfer requests in the periodic hardware queue
  - Up to 16 control plus bulk transfer requests in the non-periodic hardware queue
- Management of a shared Rx FIFO, a periodic Tx FIFO and a non periodic Tx FIFO for efficient usage of the USB data RAM

Peripheral-mode features:

- 1 bidirectional control endpoint0
- 8 IN endpoints (EPs) configurable to support bulk, interrupt or isochronous transfers
- 8 OUT endpoints configurable to support bulk, interrupt or isochronous transfers
- Management of a shared Rx FIFO and a Tx-OUT FIFO for efficient usage of the USB data RAM
- Management of up to 9 dedicated Tx-IN FIFOs (one for each active IN EP) to put less load on the application
- Support for the soft disconnect feature

3.36 Development support

3.36.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.36.2 Embedded Trace Macrocell (ETM)

The Arm embedded trace macrocell (ETM) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

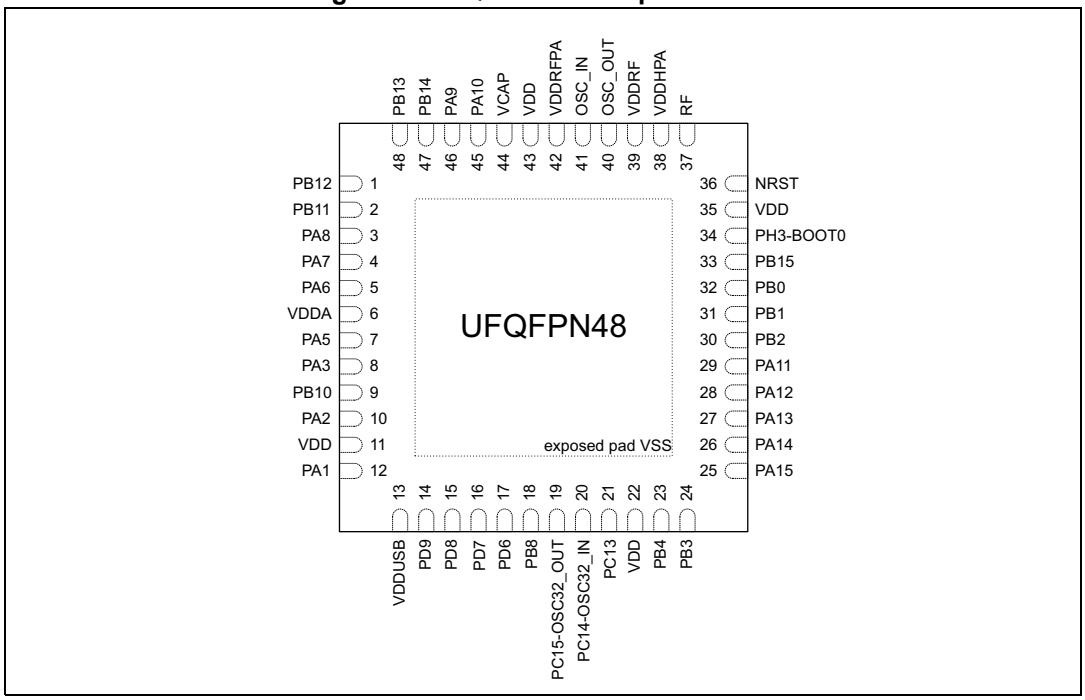
Real-time instruction and data flow activity is recorded and then formatted for display on the host computer that runs the debugger software. PTA hardware is commercially available from common development tools vendors.

The ETM operates with third party debugger software tools.

4 Pinout, pin description and alternate functions

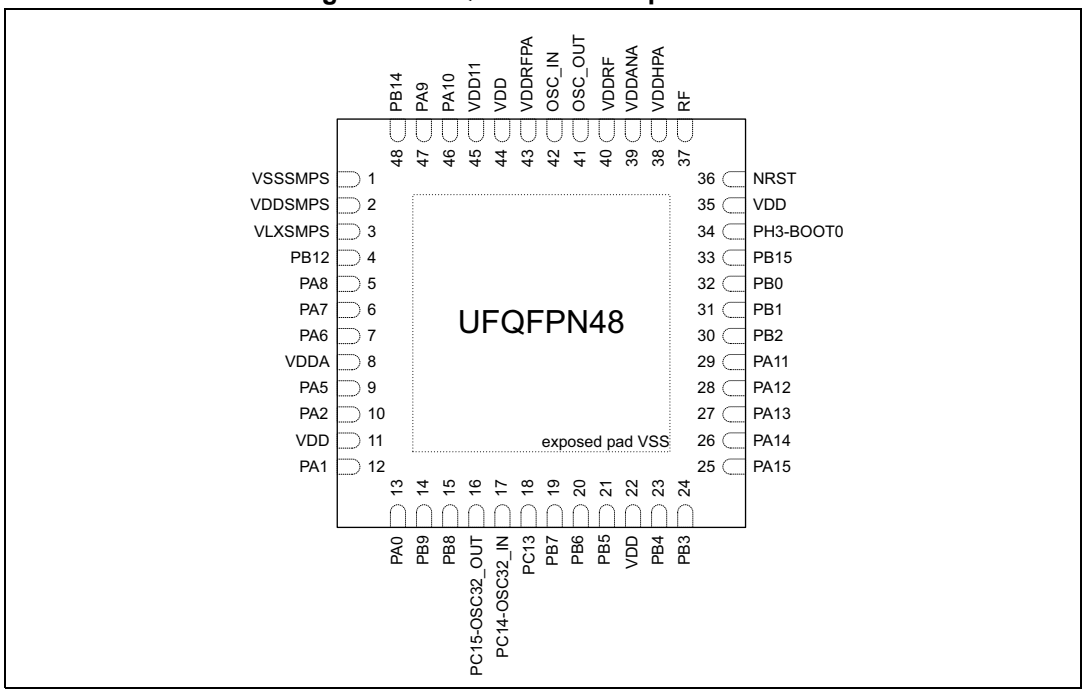
4.1 Pinout/ballout schematics

Figure 8. UFQFPN48-USB pinout(1) (2)



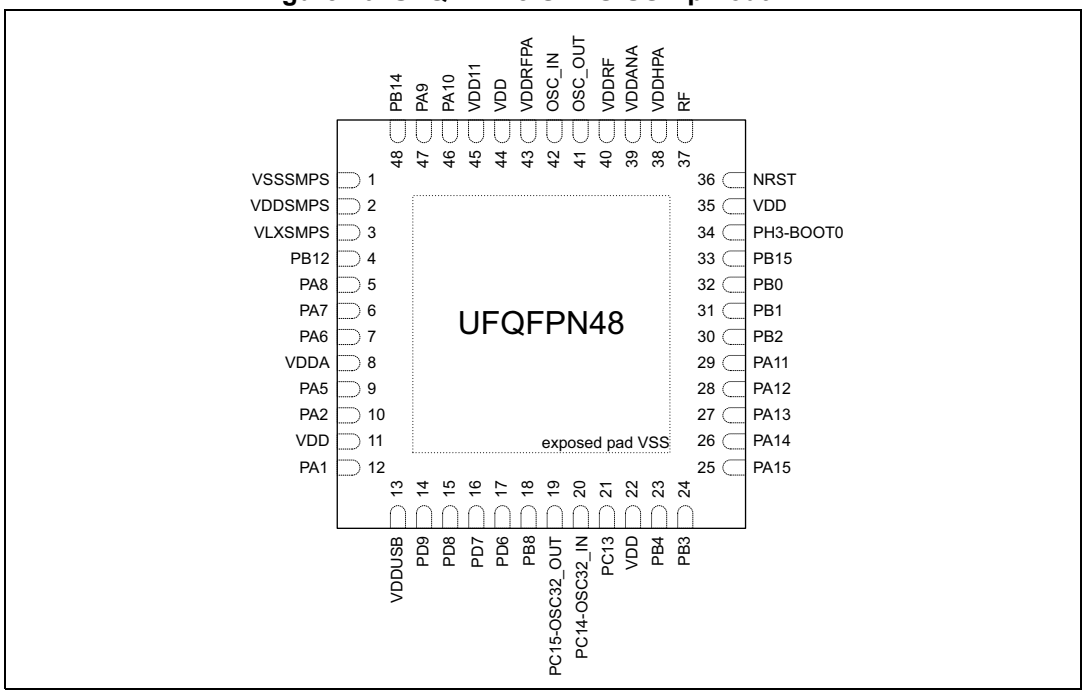
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 9. UFQFPN48-SMPS pinout(1) (2)



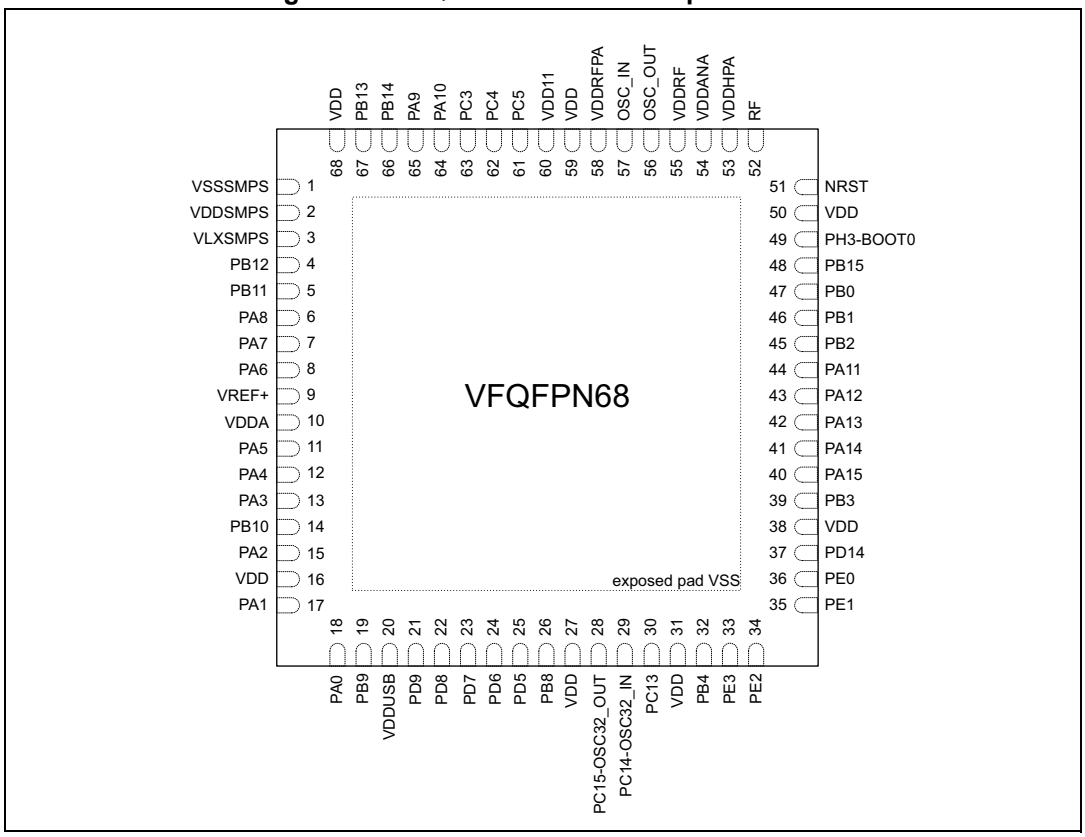
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 10. UFQFPN48-SMPS-USB pinout(1) (2)



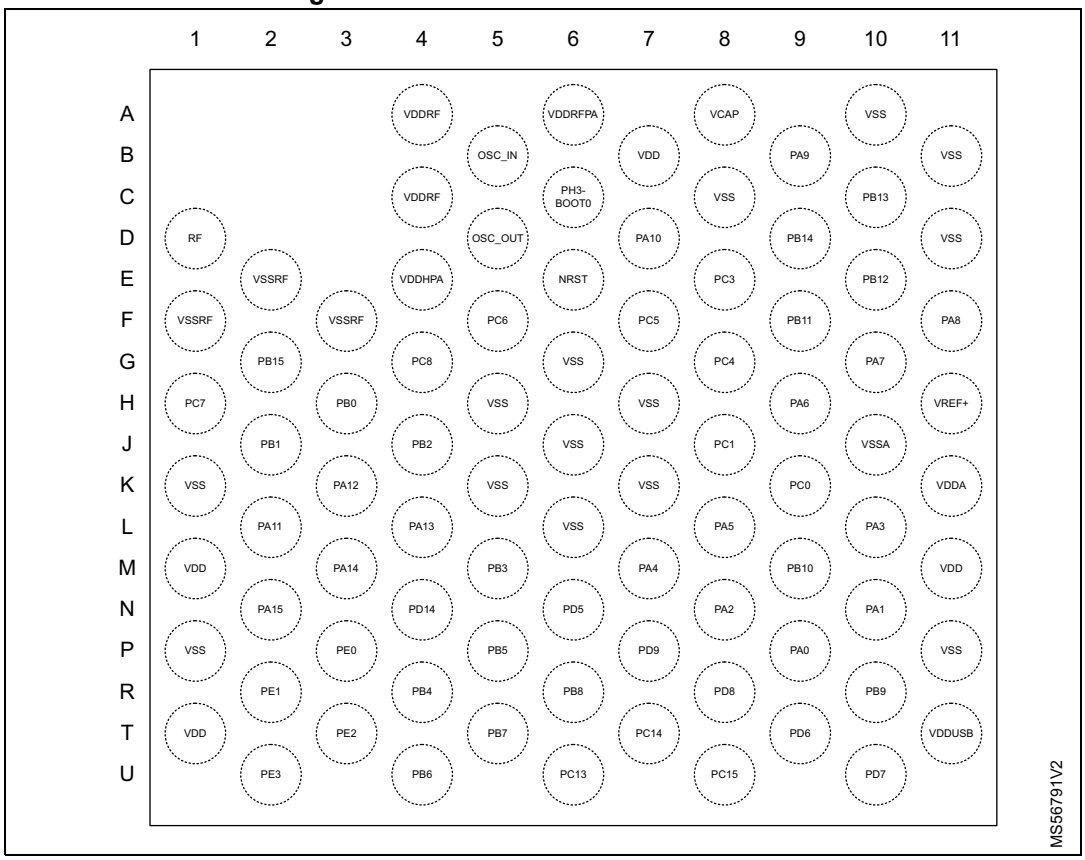
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 11. VFQFPN68-SMPS-USB pinout(1) (2)



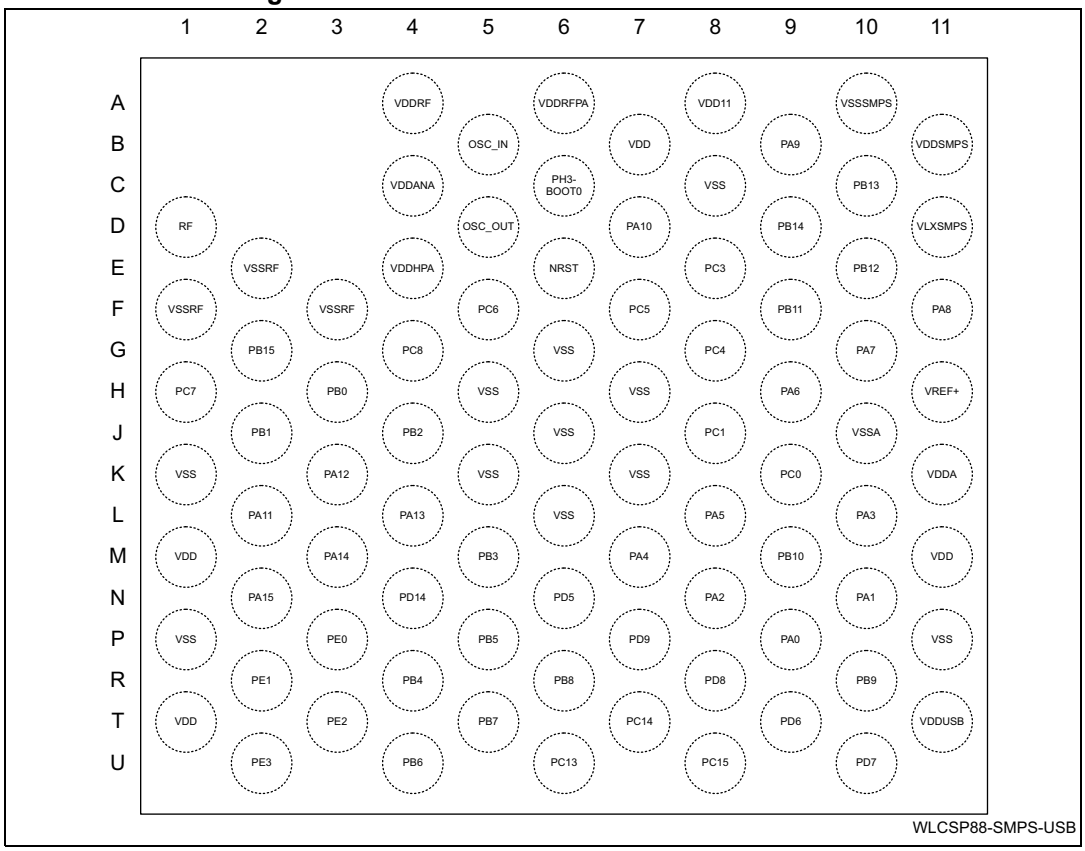
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 12. Thin WLCSP88-USB ballout (1)



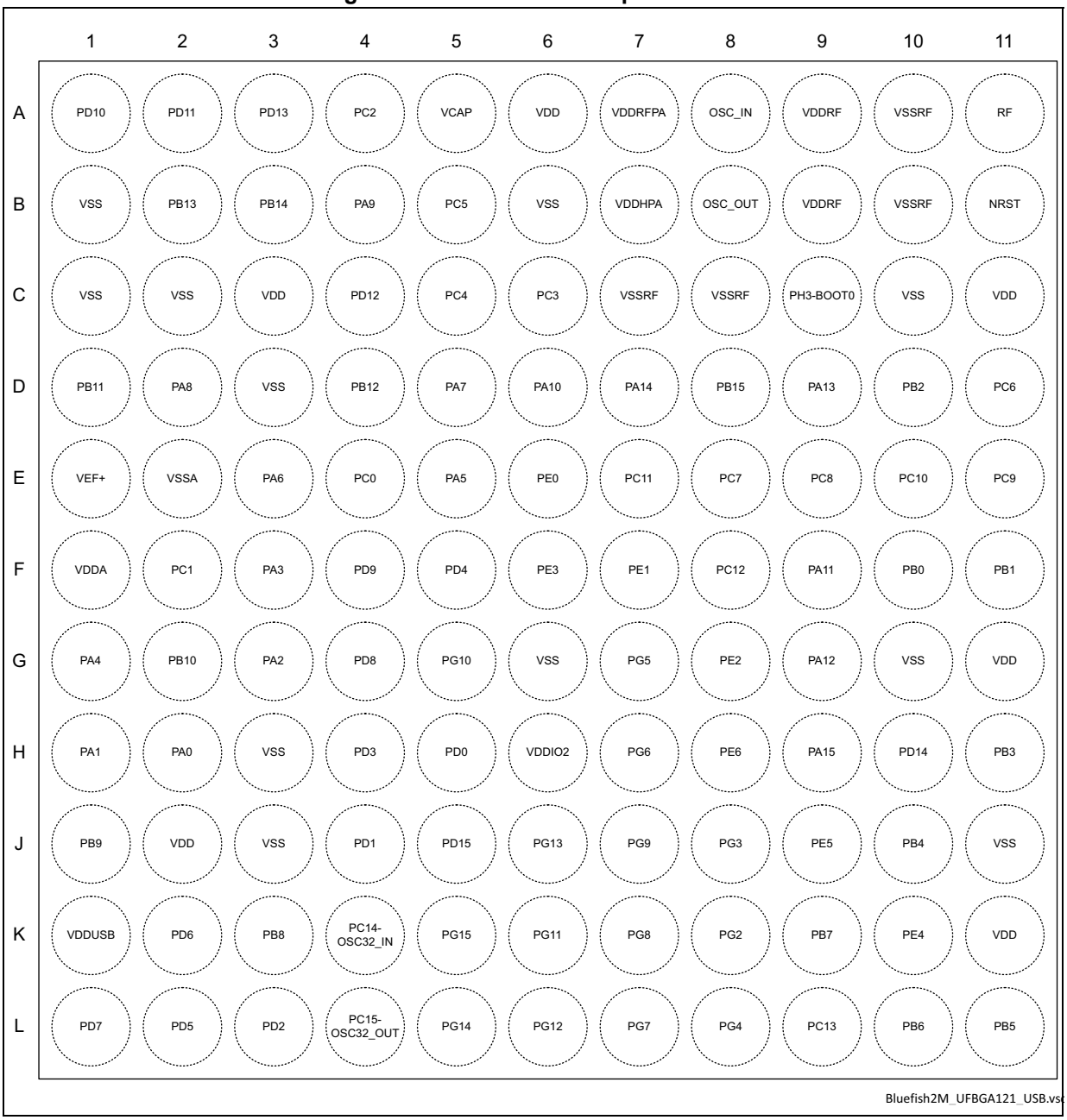
1. The above figure shows the package top view.

Figure 13. Thin WLCSP88-SMPS-USB ballout (1)



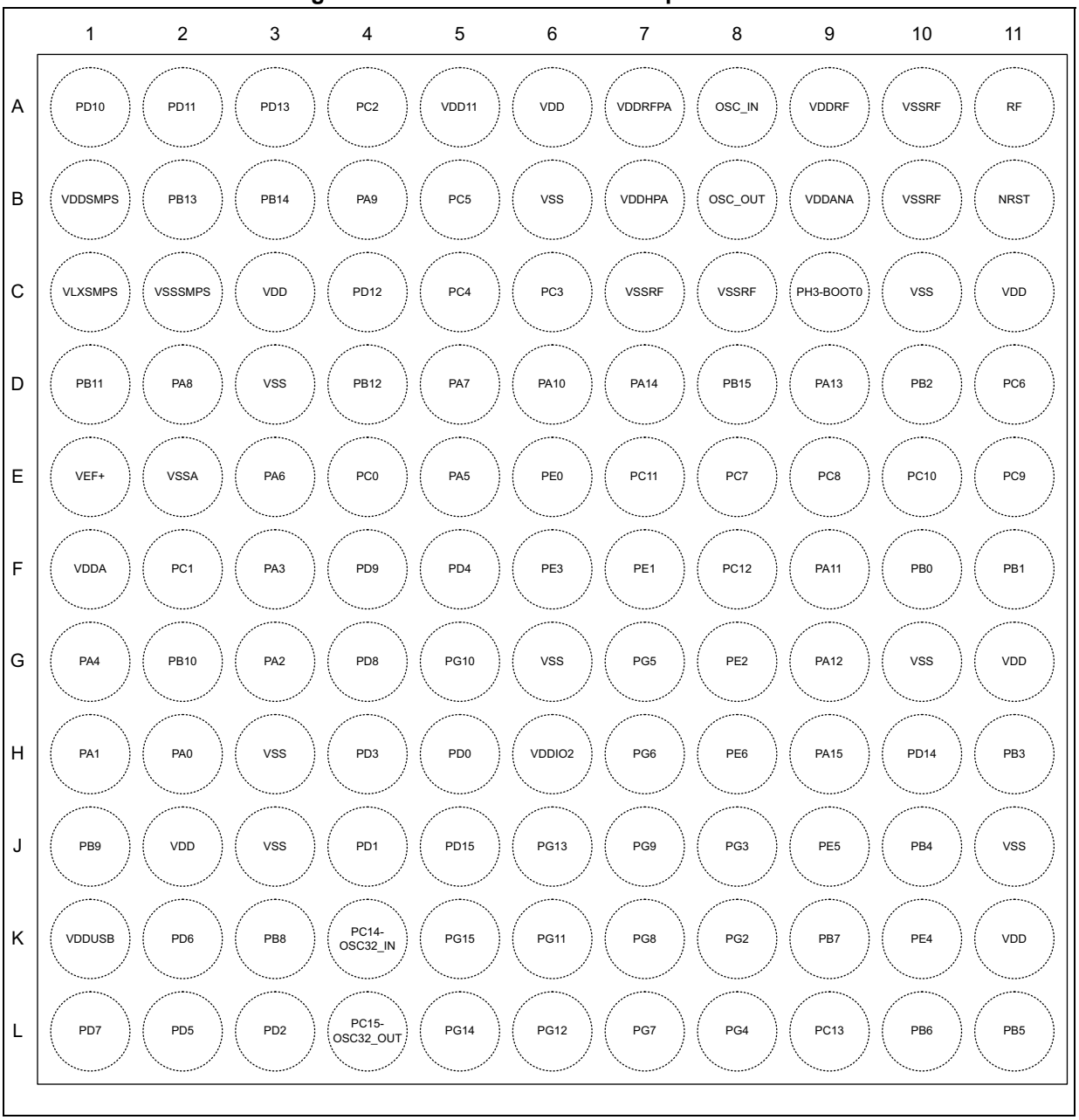
1. The above figure shows the package top view.

Figure 14. UFBGA121-USB pinout(1) (2)



1. The above figure shows the package top view.

Figure 15. UFBGA121-SMPS-USB pinout(1) (2)



1. The above figure shows the package top view.

Table 22. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_a	I/O with analog switch function supplied by V_{DDA}
		_f	I/O Fm+ capable
		_h	I/O with high-speed low voltage mode
		_s	I/O, supplied only by V_{DDIO2}
		_u	I/O, with USB function supplied by V_{DDUSB}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 23* are a concatenation of various options. Examples: FT_a, FT_fa, FT_f.

Table 23. Device pin definitions

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	A10	-	-	-	-	C2	-	VSS	S	-	-	-	-
-	-	1	1	1	A10	-	C2	VSSSMPS	S	-	-	-	-
-	B11	-	-	-	-	B1	-	VSS	S	-	-	-	-
-	-	2	2	2	B11	-	B1	VDDSMPS	S	-	-	-	-
-	D11	-	-	-	-	C1	-	VSS	S	-	-	-	-
-	-	3	3	3	D11	-	C1	VLXSMPS	S	-	-	-	-
1	E10	4	4	4	E10	D4	D4	PB12	I/O	FT	-	TIM2_CH1, TIM2_ETR, I2C2_SMBA, SPI1_RDY, SPI2_NSS, USART1_TX, USART3_CK, TSC_SYNC, SAI1_SD_A, TIM3_ETR, EVENTOUT	-
2	F9	-	-	5	F9	D1	D1	PB11	I/O	FT_f	-	LPTIM1_CH1, LPTIM1_ETR, I2C4_SDA, I2C2_SDA, SPI2_RDY, USART3_RX, LPUART1_TX, EVENTOUT	-
3	F11	5	5	6	F11	D2	D2	PA8	I/O	FT_a	-	MCO, TIM2_CH2, LPTIM1_CH2, SPI3_RDY, USART1_RX, TSC_G1_IO1, OTG_SOF, SAI1_FS_A, EVENTOUT	ADC4_IN1
4	G10	6	6	7	G10	D5	D5	PA7	I/O	FT_fa	-	TIM2_CH3, I2C3_SDA, SPI3_SCK, USART1_CTS, USART3_TX, TSC_G1_IO2, COMP1_OUT, SAI1_SCK_A, EVENTOUT	ADC4_IN2, WKUP8, TAMP_IN1/TAMP_OUT2
5	H9	7	7	8	H9	E3	E3	PA6	I/O	FT_fa	-	CSTOP, TIM2_CH4, SAI1_CK2, I2C3_SCL, SPI3_RDY, USART1_RTS_DE, USART3_CTS, TSC_G1_IO3, SAI1_MCLK_A, EVENTOUT	ADC4_IN3, WKUP7
-	J10	-	-	-	J10	E2	E2	VSSA	S	-	-	-	

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	H11	-	-	9	H11	E1	E1	VREF+	S	-	-	-	-
6	K11	8	8	10	K11	F1	F1	VDDA	S	-	-	-	-
-	J8	-	-	-	J8	F2	F2	PC1	I/O	FT_f	-	LPTIM1_CH1, SPI2_MOSI, I2C3_SDA, LPUART1_TX, SAI1_SD_A, EVENTOUT	-
-	K9	-	-	-	K9	E4	E4	PC0	I/O	FT_f		LPTIM1_IN1, I2C3_SCL, SPI2_RDY, LPUART1_RX, LPTIM2_IN1, EVENTOUT	-
7	L8	9	9	11	L8	E5	E5	PA5	I/O	FT_a	-	CSLEEP, TIM2_CH1, TIM2_ETR, SAI1_D2, SPI3_NSS, USART1_CK, USART3_RX, TSC_G1_IO4, AUDIOCLK, LPTIM2_ETR, EVENTOUT	ADC4_IN4, WKUP6
-	M7	-	-	12	M7	G1	G1	PA4	I/O	FT_a	-	USART1_CTS, TSC_G4_IO1, AUDIOCLK, TIM16_CH1, EVENTOUT	ADC4_IN5, WKUP2, TAMP_IN6/TAMP_OUT3
8	L10	-	-	13	L10	F3	F3	PA3	I/O	FT_a	-	USART1_RTS_DE, TSC_G4_IO2, TIM16_CH1N, EVENTOUT	ADC4_IN6, WKUP5
9	M9	-	-	14	M9	G2	G2	PB10	I/O	FT_a	-	I2C4_SCL, I2C2_SCL, SPI2_SCK, USART1_CK, USART3_TX, TSC_G4_IO3, TIM16_BKIN, EVENTOUT	-
10	N8	10	10	15	N8	G3	G3	PA2	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, SAI1_D1, USART1_RTS_DE, LPUART1_TX, TSC_G4_IO4, TIM16_CH1, EVENTOUT	COMP1_INP1, ADC4_IN7, WKUP4, LSCO
-	P11	-	-	-	P11	H3	H3	VSS	S	-	-	-	-
11	M11	11	11	16	M11	J2	J2	VDD	S	-	-	-	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
12	N10	12	12	17	N10	H1	H1	PA1	I/O	FT_a	-	TIM1_CH1N, TIM3_CH2, SAI1_CK1, SPI1_RDY, SPI3_MISO, USART1_CK, LPUART1_RX, TSC_G2_IO1, LPTIM2_CH2, TIM17_CH1, EVENTOUT	COMP1_INM1, ADC4_IN8, WKUP3
-	P9	13	-	18	P9	H2	H2	PA0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH2N, TIM3_CH3, SPI3_SCK, LPUART1_CTS, TSC_G2_IO2, TIM3_ETR, EVENTOUT	COMP2_INP1, ADC4_IN9, WKUP1
-	R10	14	-	19	R10	J1	J1	PB9	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, IR_OUT, SPI2_NSS, SPI3_MISO, LPUART1_RTS_DE, TSC_G2_IO3, TIM4_CH4, LPTIM2_IN1, TIM16_CH1, EVENTOUT	COMP2_INM1, ADC4_IN10, WKUP8
13	T11	-	13	20	T11	K1	K1	VDDUSB	S	-	-	-	-
14	P7	-	14	21	P7	F4	F4	PD9	I/O	FT_u	-	USART2_TX, USART3_TX, EVENTOUT	OTG_VBUS
15	R8	-	15	22	R8	G4	G4	PD8	I/O	FT_u	-	USART2_CK, OTG_ID, EVENTOUT	-
16	U10	-	16	23	U10	L1	L1	PD7	I/O	TT	-	-	OTG_HSDM
17	T9	-	17	24	T9	K2	K2	PD6	I/O	TT	-	-	OTG_HSDP
-	N6	-	-	25	N6	L2	L2	PD5	I/O	FT	-	SAI1_D1, SPI3_MOSI, USART2_RX, SAI1_SD_A, EVENTOUT	-
18	R6	15	18	26	R6	K3	K3	PB8	I/O	FT_a	-	LPTIM1_ETR, TIM1_CH1, TIM3_ETR, USART2_RX, SPI3_MOSI, TSC_G2_IO4, COMP1_OUT, TIM4_CH3, TIM16_CH1N, EVENTOUT	PVD_IN
-	-	-	-	-	-	F5	F5	PD4	I/O	FT	-	LPTIM2_IN2, USART3_RX, EVENTOUT	-
-	-	-	-	-	-	H4	H4	PD3	I/O	FT_a	-	SPI2_SCK, SPI2_MISO, USART2_CTS, TSC_G8_IO1, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	-	-	-	-	-	L3	L3	PD2	I/O	FT	-	TIM3_ETR, USART3_RTS_DE, TSC_SYNC, EVENTOUT	-
-	-	-	-	27	-	-	-	VDD	S	-	-	-	-
19	U8	16	19	28	U8	L4	L4	PC15-OSC32_OUT	I/O	FT	-	EVENTOUT	OSC32_OUT
20	T7	17	20	29	T7	K4	K4	PC14-OSC32_IN	I/O	FT	-	EVENTOUT	OSC32_IN
-	-	-	-	-	-	J4	J4	PD1	I/O	FT_a	-	SPI2_SCK, TSC_G8_IO2, EVENTOUT	-
-	-	-	-	-	-	H5	H5	PD0	I/O	FT_a	-	SPI2_NSS, TSC_G8_IO3, EVENTOUT	-
-	-	-	-	-	-	J5	J5	PD15	I/O	FT_a	-	TSC_G8_IO4, TIM4_CH4, EVENTOUT	-
-	-	-	-	-	-	K5	K5	PG15	I/O	FT_hs	-	LPTIM1_CH1, I2C1_SMBA, EVENTOUT	-
-	-	-	-	-	-	L5	L5	PG14	I/O	FT_hfs	-	LPTIM1_CH2, I2C1_SCL, EVENTOUT	-
-	-	-	-	-	-	H6	H6	VDDIO2	S	-	-	-	-
-	K7	-	-	-	K7	G6	G6	VSS	S	-	-	-	-
-	-	-	-	-	-	J6	J6	PG13	I/O	FT_hfs	-	I2C1_SDA, SPI3_RDY, USART1_CK, EVENTOUT	-
-	-	-	-	-	-	L6	L6	PG12	I/O	FT_hs	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS_DE, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	-	K6	K6	PG11	I/O	FT_hs	-	LPTIM1_IN2, SPI3_MOSI, USART1_CTS, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	G5	G5	PG10	I/O	FT_hs	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	-	J7	J7	PG9	I/O	FT_hs	-	SPI3_SCK, USART1_TX, SAI1_SCK_A, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	-	-	-	-	-	K7	K7	PG8	I/O	FT_hfs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	L7	L7	PG7	I/O	FT_hfs	-	SAI1_CK1, I2C3_SCL, LPUART1_TX, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	H7	H7	PG6	I/O	FT_hs	-	I2C3_SMBA, SPI1_RDY, LPUART1_RTS_DE, EVENTOUT	-
-	-	-	-	-	-	G7	G7	PG5	I/O	FT_hs	-	SPI1_NSS, LPUART1_CTS, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	L8	L8	PG4	I/O	FT_hs	-	SPI1_MOSI, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	J8	J8	PG3	I/O	FT_hs	-	SPI1_MISO, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	K8	K8	PG2	I/O	FT_hs	-	SPI1_SCK, SAI1_SCK_B, EVENTOUT	-
-	L6	-	-	-	L6	J3	J3	VSS	S	-	-	-	-
21	U6	18	21	30	U6	L9	L9	PC13	I/O	FT_a	-	TIM1_BKIN2, TSC_G5_IO1, EVENTOUT	WKUP2, RTC_TS/ RTC_OUT1, TAMP_IN4/TAMP_OUT5
-	T5	19	-	-	T5	K9	K9	PB7	I/O	FT_a	-	TIM1_CH4N, TSC_G5_IO2, TIM4_CH2, SAI1_SD_B, EVENTOUT	WKUP5, TAMP_IN5/TAMP_OUT4
-	-	-	-	-	-	H8	H8	PE6	I/O	FT	-	TIM3_CH4, SAI1_D1, SAI1_SD_A, EVENTOUT	-
-	U4	20	-	-	U4	L10	L10	PB6	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, TSC_G5_IO3, TIM4_CH1, SAI1_SCK_B, EVENTOUT	WKUP3
-	-	-	-	-	-	J9	J9	PE5	I/O	FT	-	TIM3_CH3, SAI1_CK2, SAI1_SCK_A, EVENTOUT	-
-	P5	21	-	-	P5	L11	L11	PB5	I/O	FT_a	-	TIM3_CH1, SAI1_D2, LPUART1_TX, TSC_G5_IO4, SAI1_FS_B, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	-	-	-	-	-	K10	K10	PE4	I/O	FT	-	TIM3_CH2, SAI1_D2, SAI1_FS_A, EVENTOUT	-
22	-	22	22	31	-	K11	K11	VDD	S	-	-	-	-
-	K5	-	-	-	K5	J11	J11	VSS	S	-	-	-	-
23	R4	23	23	32	R4	J10	J10	PB4(NJRST)	I/O	FT_a	(1)	NJTRST, TIM1_CH3, LPTIM2_IN2, USART2_RX, SPI1_SCK, TSC_G3_IO1, PTA_PRIORITY, PTA_ACTIVE, SAI1_MCLK_B, TIM17_CH1, EVENTOUT	-
-	U2	-	-	33	U2	F6	F6	PE3	I/O	FT_ha	-	TRACED2, TIM3_CH1, TSC_G7_IO1, SAI1_SD_B, EVENTOUT	-
-	T3	-	-	34	T3	G8	G8	PE2	I/O	FT_ha	-	TRACED1, TIM3_ETR, SAI1_CK1, TSC_G7_IO2, SAI1_MCLK_A, EVENTOUT	-
-	R2	-	-	35	R2	F7	F7	PE1	I/O	FT_ha	-	TRACED0, TSC_G7_IO3, TIM17_CH1, EVENTOUT	-
-	P3	-	-	36	P3	E6	E6	PE0	I/O	FT_ha	-	TRACECLK, TSC_G7_IO4, TIM4_ETR, TIM16_CH1, EVENTOUT	-
-	N4	-	-	37	N4	H10	H10	PD14	I/O	FT_h	-	TRACED3, TIM4_CH3, EVENTOUT	-
-	P1	-	-	-	P1	G10	G10	VSS	S	-	-	-	-
-	T1	-	-	38	T1	G11	G11	VDD	S	-	-	-	-
24	M5	24	24	39	M5	H11	H11	PB3 (JTDO/TRACESWO)	I/O	FT_fa	-	JTDO/TRACESWO, TIM1_CH4, LPTIM1_IN2, USART2_CK, I2C1_SDA, SPI1_MISO, TSC_G3_IO2, PTA_ACTIVE, TIM17_CH1N, EVENTOUT	-
25	N2	25	25	40	N2	H9	H9	PA15 (JTDI)	I/O	FT_fa	(1)	JTDI, TIM1_ETR, LPTIM1_CH2, USART2_RTS_DE, I2C1_SCL, SPI1_MOSI, USART3_RTS_DE, TSC_G3_IO3, PTA_STATUS, TIM17_BKIN, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
26	M3	26	26	41	M3	D7	D7	PA14 (JTCK/SWCLK)	I/O	FT	(1)	JTCK/SWCLK, USART2_TX, I2C4_SMBA, OTG_SOF/PTA_STATUS, COMP2_OUT, EVENTOUT	TAMP_IN3/TAMP_OUT6
27	L4	27	27	42	L4	D9	D9	PA13 (JTMS/SWDIO)	I/O	FT	(1)	JTMS/SWDIO, IR_OUT, PTA_PRIORITY, EVENTOUT	-
28	K3	28	28	43	K3	G9	G9	PA12	I/O	FT_a	-	TIM1_CH2, USART2_TX, SPI1_NSS, TSC_G3_IO4, PTA_STATUS, RF_ANTSW0, COMP2_OUT, EVENTOUT	WKUP6
29	L2	29	29	44	L2	F9	F9	PA11.	I/O	FT	-	TIM1_CH1, USART2_RX, RF_ANTSW1, LPTIM2_CH1, EVENTOUT	-
-	M1	-	-	-	M1	C11	C11	VDD	S	-	-	-	-
-	K1	-	-	-	K1	-	-	VSS	S	-	-	-	-
30	J4	30	30	45	J4	D10	D10	PB2	I/O	FT_f	-	TIM1_CH1N, USART2_CTS, I2C1_SCL, I2C3_SCL, RF_ANTSW2, EVENTOUT	WKUP1, RTC_OUT2
31	J2	31	31	46	J2	F11	F11	PB1	I/O	FT_f	-	TIM1_CH2N, USART2_RTS_DE, I2C1_SDA, I2C3_SDA, USART3_RTS_DE, EVENTOUT	WKUP4
32	H3	32	32	47	H3	F10	F10	PB0	I/O	FT	-	-TIM1_CH3N, LPTIM2_IN2, USART2_TX, SPI2_MOSI, USART3_CK, EVENTOUT	-
-	-	-	-	-	-	F8	F8	PC12	I/O	FT	-	SPI3_MOSI, USART3_CK, EVENTOUT	-
-	-	-	-	-	-	E7	E7	PC11	I/O	FT	-	SPI3_MISO, USART3_RX, EVENTOUT	-
-	-	-	-	-	-	E10	E10	PC10	I/O	FT	-	SPI3_SCK, USART3_TX, EVENTOUT	-
-	-	-	-	-	-	E11	E11	PC9	I/O	FT	-	TIM3_CH4, USART2_TX, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	G4	-	-	-	G4	E9	E9	PC8	I/O	FT	-	TIM3_CH3, USART2_RX, EVENTOUT	-
-	H1	-	-	-	H1	E8	E8	PC7	I/O	FT	-	CSTOP, TIM3_CH2, USART2_RTS_DE, LPTIM2_CH2, EVENTOUT	-
-	J6	-	-	-	J6	-	-	VSS	S	-	-	-	-
-	F5	-	-	-	F5	D11	D11	PC6	I/O	FT	-	CSLEEP, TIM3_CH1, EVENTOUT	-
33	G2	33	33	48	G2	D8	D8	PB15	I/O	TT	-	TIM1_BKIN2, USART2_CTS, I2C1_SMBA, I2C3_SMBA, LPUART1_CTS, PTA_GRANT, RF_EXTPABYP, TIM16_BKIN, EVENTOUT	-
34	C6	34	34	49	C6	C9	C9	PH3-BOOT0	I/O	TT	-	PTA_GRANT, RF_EXTPABYP, EVENTOUT	TAMP_IN2/TAMP_OUT1
35	-	35	35	50	-	-	-	VDD	S	-	-	-	-
-	H5	-	-	-	H5	C10	C10	VSS	S	-	-	-	-
36	E6	36	36	51	E6	B11	B11	NRST	I/O	RST	-	-	-
-	G6	-	-	-	G6	-	-	VSS	S	-	-	-	-
-	F1	-	-	-	F1	B10	B10	VSSRF	S	-	-	-	-
37	D1	37	37	52	D1	A11	A11	RF	I/O	RF	-	-	-
-	E2	-	-	-	E2	A10	A10	VSSRF	S	-	-	-	-
38	E4	38	38	53	E4	B7	B7	VDDHPA	S	-	-	-	-
-	-	39	39	54	C4	-	B9	VDDANA	S	-	-	-	-
-	C4	-	-	-	-	B9	-	VDDRF	S	-	-	-	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
39	A4	40	40	55	A4	A9	A9	VDDRF	S	-	-	-	-
-	F3	-	-	-	F3	C7	C7	VSSRF	S	-	-	-	-
40	D5	41	41	56	D5	B8	B8	OSC_OUT	O	RF	-	-	-
41	B5	42	42	57	B5	A8	A8	OSC_IN	I	RF	-	-	-
42	A6	43	43	58	A6	A7	A7	VDDRFPA	S	-	-	-	-
43	B7	44	44	59	B7	A6	A6	VDD	S	-	-	-	-
-	C8	-	-	-	C8	B6	B6	VSS	S	-	-	-	-
-	-	45	45	60	A8	-	A5	VDD11	S	-	-	-	-
44	A8	-	-	-	-	A5	-	VCAP	S	-	-	-	-
-	F7	-	-	61	F7	B5	B5	PC5	I/O	FT	-	TIM1_CH4N, SAI1_D3, USART3_RX, SAI1_SD_B, EVENTOUT	-
-	G8	-	-	62	G8	C5	C5	PC4	I/O	FT	-	TIM3_CH2, SAI1_D2, SPI3_MISO, USART3_TX, SAI1_FS_A, LPTIM2_CH2, EVENTOUT	-
-	E8	-	-	63	E8	C6	C6	PC3	I/O	FT	-	LPTIM1_ETR, TIM3_CH1, SAI1_D1, SPI2_MOSI, SPI3_MOSI, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	-
45	D7	46	46	64	D7	D6	D6	PA10	I/O	FT	-	TIM3_CH1, SAI1_D1, SPI2_NSS, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	A4	A4	PC2	I/O	FT	-	LPTIM1_IN2, SPI2_MISO, EVENTOUT	-
46	B9	47	47	65	B9	B4	B4	PA9	I/O	FT	-	TIM3_CH2, SAI1_CK1, SPI2_MISO, SPI2_SCK, LPUART1_RTS_DE, EVENTOUT	-

Table 23. Device pin definitions (continued)

Pin								Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN48-USB	Thin WLCSP88-USB	UFQFPN48-SMPS	UFQFPN48-SMPS-USB	VFQFPN68-SMPS-USB	Thin WLCSP88-SMPS-USB	UFBGA121-USB	UFBGA121-SMPS-USB						
-	-	-	-	-	-	A13	A13	PD13	I/O	FT_fa	-	I2C4_SDA, TSC_G6_IO4, TIM4_CH2, LPTIM2_CH1, EVENTOUT	-
-	-	-	-	-	-	C4	C4	PD12	I/O	FT_fa	-	I2C4_SCL, USART3_RTS_DE, TSC_G6_IO3, TIM4_CH1, LPTIM2_IN1, EVENTOUT	-
47	D9	48	48	66	D9	B3	B3	PB14	I/O	FT_a	-	RTC_REFIN, TIM3_CH3, I2C2_SDA, SPI2_MISO, USART1_TX, USART3_RTS_DE, TSC_G6_IO1, SAI1_SD_A, EVENTOUT	WKUP7
-	-	-	-	-	-	A2	A2	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	-	-	A1	A1	PD10	I/O	FT	-	LPTIM2_CH2, USART3_CK, EVENTOUT	-
48	C10	-	-	67	C10	B2	B2	PB13	I/O	FT_a	-	TIM3_CH4, I2C2_SCL, SPI2_SCK, USART3_CTS, TSC_G6_IO2, EVENTOUT	-
-	H7	-	-	-	H7	D3	D3	VSS	S	-	-	-	-
-	-	-	-	68	-	C3	C3	VDD	S	-	-	-	-
49	-	49	49	69	-	-	-	VSS (exposed pad)	S	-	-	-	-

1. After reset, this pin is configured as JTAG/SWD alternate functions. The internal pull-up on PA15, PA13, and PB4 pins, and the internal pull-down on PA14 pin are activated.

4.2 Alternate functions

Table 24. Alternate functions (AF0 to AF7)(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS	LPTIM1/ TIM1/2	LPTIM1/2/ TIM1/2/3	I2C4/SAI1/SPI2 /USART2	I2C1/2/3/4/ OTG	I2C4/ SPI1/2/3	I2C3/ SPI2/3	USART1/2/3
A	PA0	LPTIM1_IN1	TIM1_CH2N	TIM3_CH3	-	-	-	SPI3_SCK	-
	PA1	-	TIM1_CH1N	TIM3_CH2	SAI1_CK1	-	SPI1_RDY	SPI3_MISO	USART1_CK
	PA2	-	TIM1_BKIN	TIM3_CH1	SAI1_D1	-	-	-	USART1_RTS_DE
	PA3	-	-	-	-	-	-	-	USART1_RTS_DE
	PA4	-	-	-	-	-	-	-	USART1_CTS
	PA5	CSLEEP	TIM2_CH1	TIM2_ETR	SAI1_D2	-	-	SPI3_NSS	USART1_CK
	PA6	CSTOP	TIM2_CH4	-	SAI1_CK2	I2C3_SCL	-	SPI3_RDY	USART1_RTS_DE
	PA7	-	TIM2_CH3	-	-	I2C3_SDA	-	SPI3_SCK	USART1_CTS
	PA8	MCO	TIM2_CH2	LPTIM1_CH2	-	-	-	SPI3_RDY	USART1_RX
	PA9	-	-	TIM3_CH2	SAI1_CK1	-	SPI2_MISO	SPI2_SCK	-
	PA10	-	-	TIM3_CH1	SAI1_D1	-	-	SPI2_NSS	-
	PA11	-	TIM1_CH1	-	USART2_RX	-	-	-	-
	PA12	-	TIM1_CH2	-	USART2_TX	-	SPI1_NSS	-	-
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	-	-	USART2_TX	OTG_SOF	I2C4_SMBA	-	-
	PA15	JTDI	TIM1_ETR	LPTIM1_CH2	USART2_RTS_DE	I2C1_SCL	SPI1_MOSI	-	USART3_RTS_DE

Table 24. Alternate functions (AF0 to AF7)[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS	LPTIM1/ TIM1/2	LPTIM1/2/ TIM1/2/3	I2C4/SAI1/SPI2 /USART2	I2C1/2/3/4/ OTG	I2C4/ SPI1/2/3	I2C3/ SPI2/3	USART1/2/3
B	PB0	-	TIM1_CH3N	LPTIM2_IN2	USART2_TX	-	SPI2_MOSI	-	USART3_CK
	PB1	-	TIM1_CH2N	-	USART2_RTS_DE	I2C1_SDA	-	I2C3_SDA	USART3_RTS_DE
	PB2	-	TIM1_CH1N	-	USART2_CTS	I2C1_SCL	-	I2C3_SCL	-
	PB3	JTDO/ TRACESWO	TIM1_CH4	LPTIM1_IN2	USART2_CK	I2C1_SDA	SPI1_MISO	-	-
	PB4	NJTRST	TIM1_CH3	LPTIM2_IN2	USART2_RX	-	SPI1_SCK	-	-
	PB5	-	-	TIM3_CH1	SAI1_D2	-	-	-	-
	PB6	-	TIM2_CH1	TIM2_ETR	-	-	-	-	-
	PB7	-	TIM1_CH4N	-	-	-	-		-
	PB8	LPTIM1_ETR	TIM1_CH1	TIM3_ETR	USART2_RX	-	-	SPI3_MOSI	-
	PB9	-	TIM1_CH3N	TIM3_CH4	IR_OUT	-	SPI2_NSS	SPI3_MISO	-
	PB10	-	-	-	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART1_CK
	PB11	LPTIM1_CH1	-	LPTIM1_ETR	I2C4_SDA	I2C2_SDA	SPI2_RDY	-	USART3_RX
	PB12	-	TIM2_CH1	TIM2_ETR	-	I2C2_SMBA	SPI1_RDY	SPI2_NSS	USART1_TX
	PB13	-	-	TIM3_CH4	-	I2C2_SCL	SPI2_SCK	-	USART3_CTS
	PB14	RTC_REFIN	-	TIM3_CH3	-	I2C2_SDA	SPI2_MISO	-	USART1_TX
	PB15	-	TIM1_BKIN2	-	USART2_CTS	I2C1_SMBA	-	I2C3_SMBA	-

Table 24. Alternate functions (AF0 to AF7)(1) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS	LPTIM1/ TIM1/2	LPTIM1/2/ TIM1/2/3	I2C4/SAI1/SPI2 /USART2	I2C1/2/3/4/ OTG	I2C4/ SPI1/2/3	I2C3/ SPI2/3	USART1/2/3
C	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	SPI2_RDY	-	-
	PC1	-	LPTIM1_CH1	-	SPI2_MOSI	I2C3_SDA	-	-	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-
	PC3	-	LPTIM1_ETR	TIM3_CH1	SAI1_D1	-	SPI2_MOSI	SPI3_MOSI	-
	PC4	-	-	TIM3_CH2	SAI1_D2	-	-	SPI3_MISO	USART3_TX
	PC5	-	TIM1_CH4N	-	SAI1_D3	-	-	-	USART3_RX
	PC6	CSLEEP	-	TIM3_CH1	-	-	-	-	-
	PC7	CSTOP	-	TIM3_CH2	-	-	-	-	USART2_RTS_DE
	PC8	-	-	TIM3_CH3	-	-	-	-	USART2_RX
	PC9	-	-	TIM3_CH4	-	-	-	-	USART2_TX
	PC10	-	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX
	PC12	-	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	TIM1_BKIN2	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 24. Alternate functions (AF0 to AF7)[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS	LPTIM1/ TIM1/2	LPTIM1/2/ TIM1/2/3	I2C4/SAI1/SPI2 /USART2	I2C1/2/3/4/ OTG	I2C4/ SPI1/2/3	I2C3/ SPI2/3	USART1/2/3
D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	-	-	TIM3_ETR	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO	-	USART2_CTS
	PD4	-	-	LPTIM2_IN2	-	-	-	-	USART3_RX
	PD5	-	-	-	SAI1_D1	-	SPI3_MOSI	-	USART2_RX
	PD6	-	-	-	-	-	-	-	-
	PD7	-	-	-	-	-	-	-	-
	PD8	-	-	-	-	-	-	-	USART2_CK
	PD9	-	-	-	USART2_TX	-	-	-	USART3_TX
	PD10	-	-	LPTIM2_CH2	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS
	PD12	-	-	-	-	I2C4_SCL	-	-	USART3_RTS_DE
	PD13	-	-	-	-	I2C4_SDA	-	-	-
	PD14	TRACED3	-	-	-	-	-	-	-
	PD15	-	-	-	-	-	-	-	-
E	PE0	TRACECLK	-	-	-	-	-	-	-
	PE1	TRACED0	-	-	-	-	-	-	-
	PE2	TRACED1	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED2	-	TIM3_CH1	-	-	-	-	-
	PE4	-	-	TIM3_CH2	SAI1_D2	-	-	-	-
	PE5	-	-	TIM3_CH3	SAI1_CK2	-	-	-	-
	PE6	-	-	TIM3_CH4	SAI1_D1	-	-	-	-

Table 24. Alternate functions (AF0 to AF7)[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS	LPTIM1/ TIM1/2	LPTIM1/2/ TIM1/2/3	I2C4/SAI1/SPI2 /USART2	I2C1/2/3/4/ OTG	I2C4/ SPI1/2/3	I2C3/ SPI2/3	USART1/2/3
G	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	-	I2C3_SMBA	SPI1_RDY	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	-	-	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	-	-	-	SPI3_MOSI	USART1_CTS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	SPI3_RDY	USART1_CK
	PG14	-	LPTIM1_CH2	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_CH1	-	-	I2C1_SMBA	-	-	-
H	PH3	-	-	-	-	-	-	-	-

1. For AF8 to AF15 refer to *Table 25*.

Table 25. Alternate functions (AF8 to AF15)(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1 /USART3	TSC	OTG/PTA	RF	COMP1/2 /PTA/TIM4	LPTIM2/SAI1 /TIM4	LPTIM2/ TIM3/16/17	EVENTOUT
A	PA0	LPUART1_CTS	TSC_G2_IO2	-	-	-	-	TIM3_ETR	EVENTOUT
	PA1	LPUART1_RX	TSC_G2_IO1	-	-	-	LPTIM2_CH2	TIM17_CH1	EVENTOUT
	PA2	LPUART1_TX	TSC_G4_IO4	-	-	-	-	TIM16_CH1	EVENTOUT
	PA3	-	TSC_G4_IO2	-	-	-	-	TIM16_CH1N	EVENTOUT
	PA4	-	TSC_G4_IO1	-	-	-	AUDIOCLK	TIM16_CH1	EVENTOUT
	PA5	USART3_RX	TSC_G1_IO4	-	-	-	AUDIOCLK	LPTIM2_ETR	EVENTOUT
	PA6	USART3_CTS	TSC_G1_IO3	-	-	-	SAI1_MCLK_A	-	EVENTOUT
	PA7	USART3_TX	TSC_G1_IO2	-	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PA8	-	TSC_G1_IO1	OTG_SOF	-	-	SAI1_FS_A	-	EVENTOUT
	PA9	LPUART1_RTS_DE	-	-	-	-	-	-	EVENTOUT
	PA10	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PA11	-	-	-	RF_ANTSW1	-	-	LPTIM2_CH1	EVENTOUT
	PA12	-	TSC_G3_IO4	PTA_STATUS	RF_ANTSW0	COMP2_OUT	-	-	EVENTOUT
	PA13	-	-	PTA_PRIORITY	-	-	-	-	EVENTOUT
	PA14	-	-	PTA_STATUS	-	COMP2_OUT	-	-	EVENTOUT
	PA15	-	TSC_G3_IO3	PTA_STATUS	-	-	-	TIM17_BKIN	EVENTOUT

Table 25. Alternate functions (AF8 to AF15)(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1 /USART3	TSC	OTG/PTA	RF	COMP1/2 /PTA/TIM4	LPTIM2/SAI1 /TIM4	LPTIM2/ TIM3/16/17	EVENTOUT
B	PB0	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	-	-	-	-	-	EVENTOUT
	PB2	-	-	-	RF_ANTSW2	-	-	-	EVENTOUT
	PB3	-	TSC_G3_IO2	PTA_ACTIVE	-	-	-	TIM17_CH1N	EVENTOUT
	PB4	-	TSC_G3_IO1	PTA_PRIORITY	-	PTA_ACTIVE	SAI1_MCLK_B	TIM17_CH1	EVENTOUT
	PB5	LPUART1_TX	TSC_G5_IO4	-	-	-	SAI1_FS_B	-	EVENTOUT
	PB6	-	TSC_G5_IO3	-	-	TIM4_CH1	SAI1_SCK_B	-	EVENTOUT
	PB7	-	TSC_G5_IO2	-	-	TIM4_CH2	SAI1_SD_B	-	EVENTOUT
	PB8	-	TSC_G2_IO4	-	-	COMP1_OUT	TIM4_CH3	TIM16_CH1N	EVENTOUT
	PB9	LPUART1_RTS_DE	TSC_G2_IO3	-	-	TIM4_CH4	LPTIM2_IN1	TIM16_CH1	EVENTOUT
	PB10	USART3_TX	TSC_G4_IO3	-	-	-	-	TIM16_BKIN	EVENTOUT
	PB11	LPUART1_TX	-	-	-	-	-	-	EVENTOUT
	PB12	USART3_CK	TSC_SYNC	-	-	-	SAI1_SD_A	TIM3_ETR	EVENTOUT
	PB13	-	TSC_G6_IO2	-	-	-	-	-	EVENTOUT
	PB14	USART3_RTS_DE	TSC_G6_IO1	-	-	-	SAI1_SD_A	-	EVENTOUT
	PB15	LPUART1_CTS	-	PTA_GRANT	RF_EXTPABYP	-	-	TIM16_BKIN	EVENTOUT

Table 25. Alternate functions (AF8 to AF15)[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1 /USART3	TSC	OTG/PTA	RF	COMP1/2 /PTA/TIM4	LPTIM2/SAI1 /TIM4	LPTIM2/ TIM3/16/17	EVENTOUT
C	PC0	LPUART1_RX	-	-	-	-	-	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	-	-	-	SAI1_FS_A	LPTIM2_CH2	EVENTOUT
	PC5	-	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PC6	-	-	-	-	-	-	-	EVENTOUT
	PC7	-	-	-	-	-	-	LPTIM2_CH2	EVENTOUT
	PC8	-	-	-	-	-	-	-	EVENTOUT
	PC9	-	-	-	-	-	-	-	EVENTOUT
	PC10	-	-	-	-	-	-	-	EVENTOUT
	PC11	-	-	-	-	-	-	-	EVENTOUT
	PC12	-	-	-	-	-	-	-	EVENTOUT
	PC13	-	TSC_G5_IO1	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 25. Alternate functions (AF8 to AF15)(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1 /USART3	TSC	OTG/PTA	RF	COMP1/2 /PTA/TIM4	LPTIM2/SAI1 /TIM4	LPTIM2/ TIM3/16/17	EVENTOUT
D	PD0	-	TSC_G8_IO3	-	-	-	-	-	EVENTOUT
	PD1	-	TSC_G8_IO2	-	-	-	-	-	EVENTOUT
	PD2	-	TSC_SYNC	-	-	-	-	-	EVENTOUT
	PD3	-	TSC_G8_IO1	-	-	-	-	-	EVENTOUT
	PD4	-	-	-	-	-	-	-	EVENTOUT
	PD5	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	-
	PD7	-	-	-	-	-	-	-	-
	PD8	-	-	OTG_ID	-	-	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	EVENTOUT
	PD11	-		-	-	-	-	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	-	-	TIM4_CH1	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	-	TIM4_CH2	LPTIM2_CH1	EVENTOUT
	PD14	-	-	-	-	-	TIM4_CH3	-	EVENTOUT
	PD15	-	TSC_G8_IO4	-	-	-	TIM4_CH4	-	EVENTOUT
E	PE0	-	TSC_G7_IO4	-	-	-	TIM4_ETR	TIM16_CH1	EVENTOUT
	PE1	-	TSC_G7_IO3	-	-	-	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO2	-	-	-	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO1	-	-	-	SAI1_SD_B	-	EVENTOUT
	PE4	-	-	-	-	-	SAI1_FS_A	-	EVENTOUT
	PE5	-	-	-	-	-	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT

Table 25. Alternate functions (AF8 to AF15)[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1 /USART3	TSC	OTG/PTA	RF	COMP1/2 /PTA/TIM4	LPTIM2/SAI1 /TIM4	LPTIM2/ TIM3/16/17	EVENTOUT
G	PG2	-	-	-	-	-	SAI1_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PG4	-	-	-	-	-	SAI1_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	-	-	SAI1_SD_B	-	EVENTOUT
	PG6	LPUSRT1_RTS_DE	-	-	-	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	-	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	SAI1_SCK_A	-	EVENTOUT
	PG10	-	-	-	-	-	SAI1_FS_A	-	EVENTOUT
	PG11	-	-	-	-	-	SAI1_MCLK_A	-	EVENTOUT
	PG12	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PG13	-	-	-	-	-	-	-	EVENTOUT
	PG14	-	-	-	-	-	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	EVENTOUT
H	PH3	-	-	PTA_GRANT	RF_EXTPABYP	-	-	-	EVENTOUT

1. For AF0 to AF7 refer to *Table 24*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

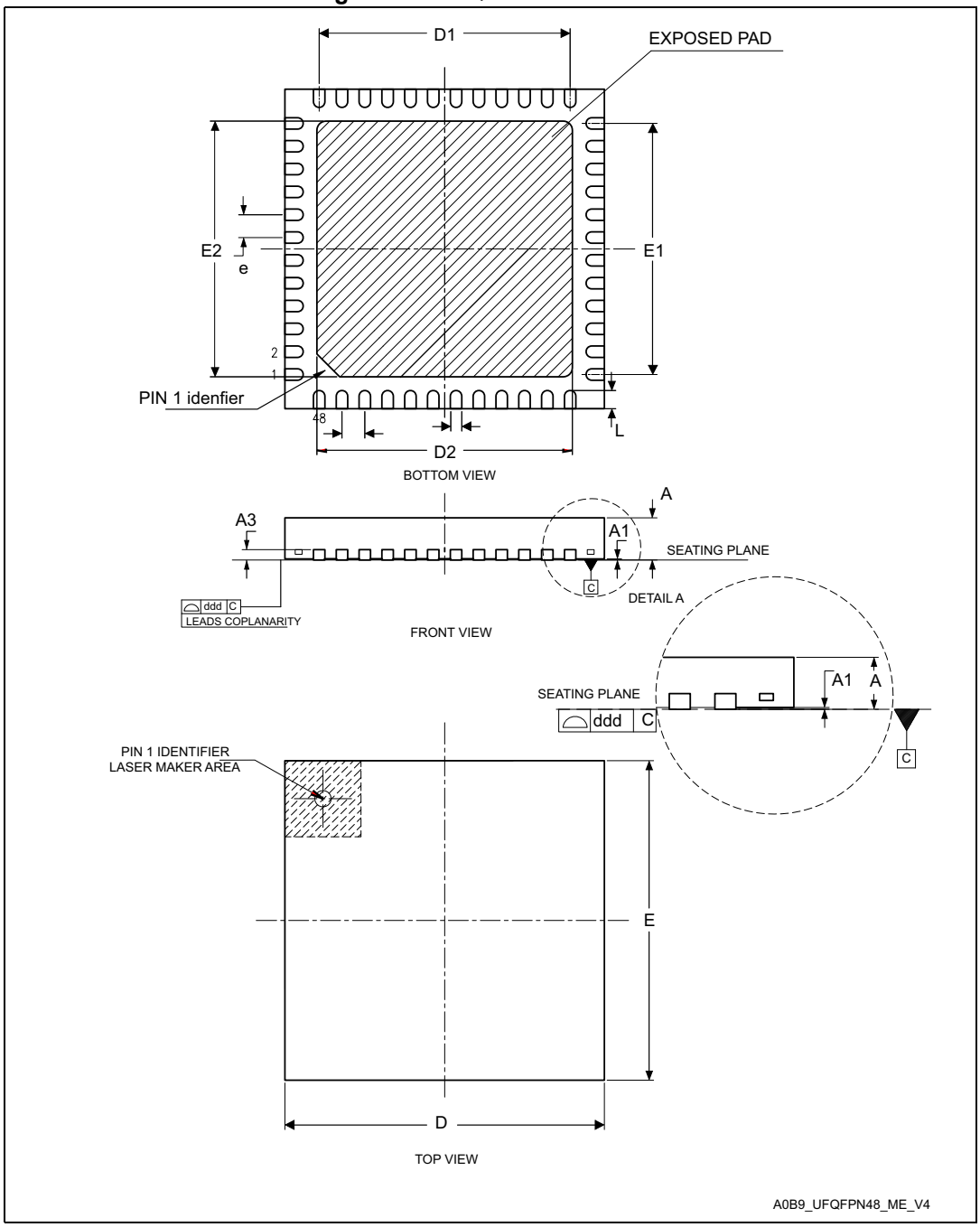
Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

5.2 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 16. UFQFPN48 – Outline



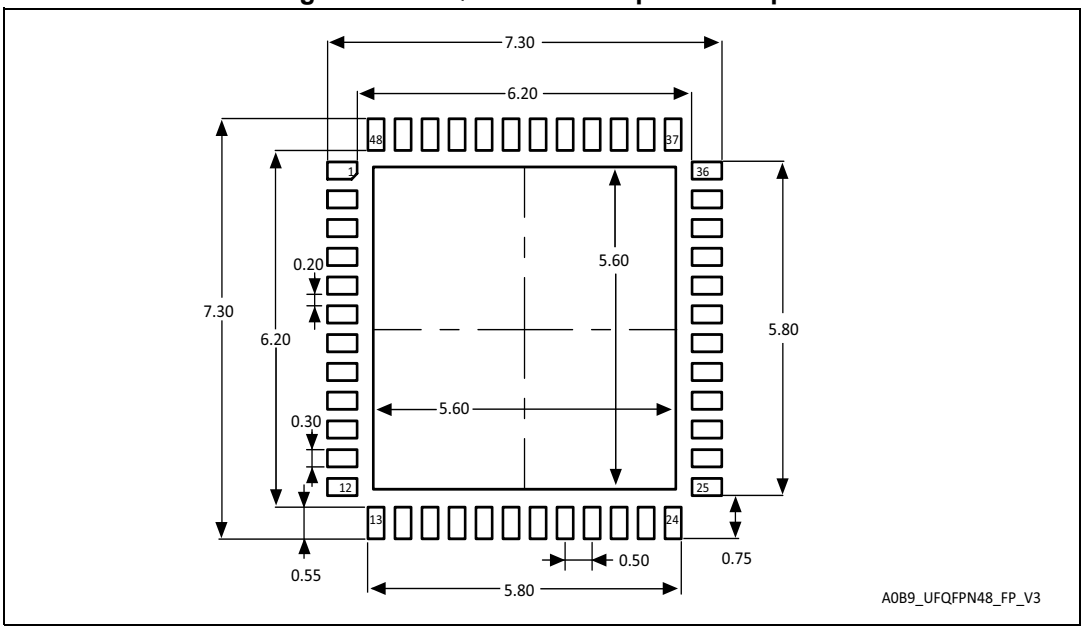
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 26. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
D1	5.400	5.500	5.600	0.2126	0.2165	0.2205
D2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
E[2]	6.900	7.000	7.100	0.2717	0.2756	0.2795
E1	5.400	5.500	5.600	0.2126	0.2165	0.2205
E2[3]	5.500	5.600	5.700	0.2165	0.2205	0.2244
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 17. UFQFPN48 – Footprint example

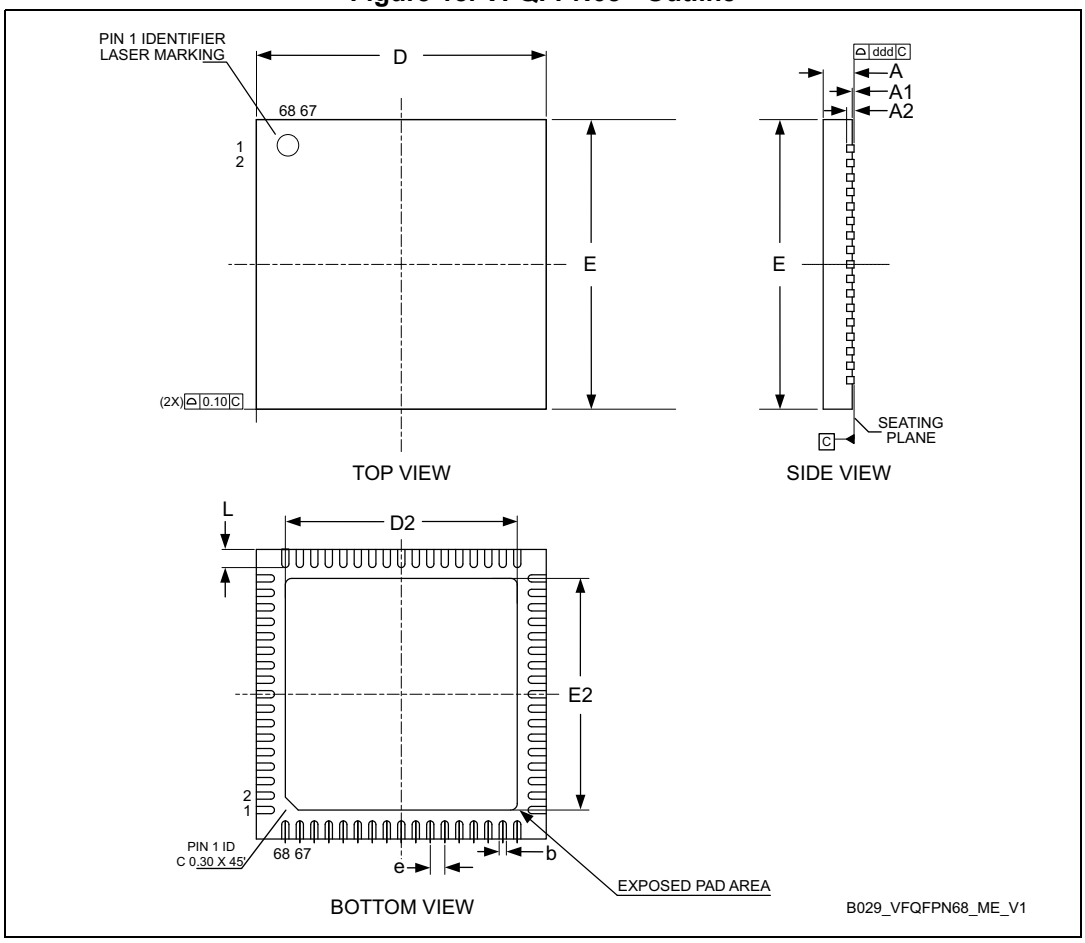


1. Dimensions are expressed in millimeters.

5.3 VFQFPN68 package information (B029)

This VFQFPN is a 68 pins, 8 x 8 mm, 0.4 mm pitch, very thin fine pitch quad flat package.

Figure 18. VFQFPN68 - Outline



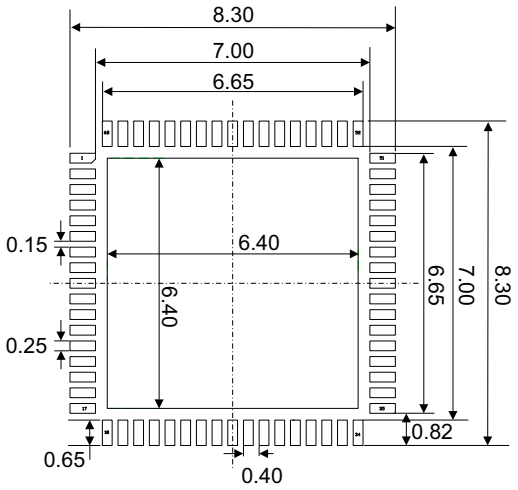
1. VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead. Sawed version. Very thin profile: 0.80 < A ≤ 1.00mm.
2. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body. Exact shape and size of this feature is optional.

Table 27. VFQFPN68 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0	0.02	0.05	0	0.0008	0.0020
A3	-	0.20	-	-	0.0008	-
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
D	7.85	8.00	8.15	0.3091	0.3150	0.3209
D2	6.30	6.40	6.50	0.2480	0.2520	0.2559
E	7.85	8.00	8.15	0.3091	0.3150	0.3209
E2	6.30	6.40	6.50	0.2480	0.2520	0.2559
e	-	0.40	-	-	0.0157	-
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. VFQFPN68 - Recommended footprint

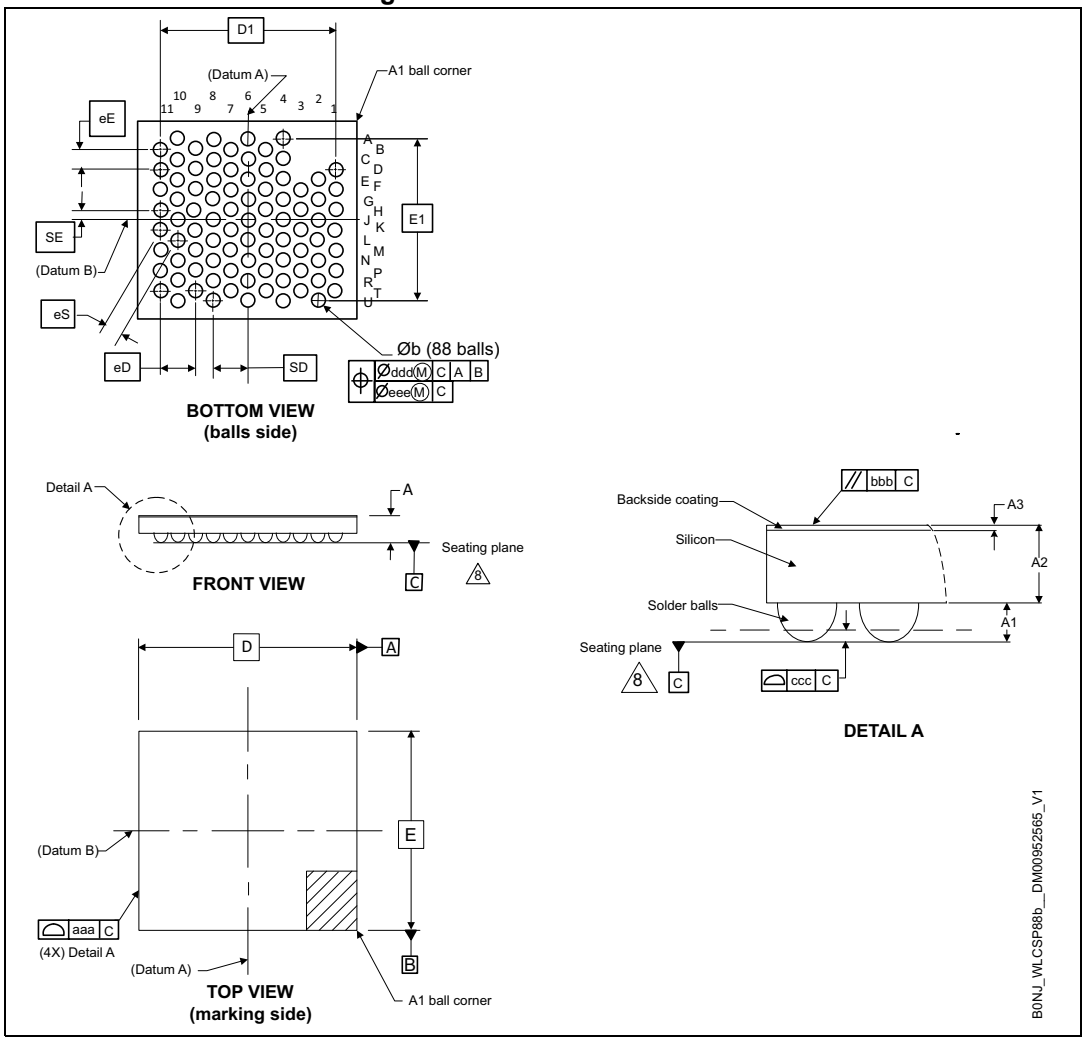


1. Dimensions are expressed in millimeters.

5.4 WLCSP88 package information (B0NJ)

This WLCSP is a 88-ball, 3.78 x 3.46 mm, 0.35 mm pitch, wafer level chip scale package.

Figure 20. WLCSP88 - Outline



1. Drawing is not to scale.

Table 28. WLCSP88 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.50	-	-	0.0197
A1[3]	0.12	-	-	0.0047	-	-
A2	-	0.30	-	-	0.0118	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.20	0.23	0.25	0.0079	0.0091	0.0098
D[5]	3.78 BSC			0.1488 BSC		
D1[5]	3.03 BSC			0.1193 BSC		
E[5]	3.46 BSC			0.1362 BSC		
E1[5]	2.80 BSC			0.1102 BSC		
eD[5][6]	0.61 BSC			0.0240 BSC		
eE[5][6]	0.35 BSC			0.0138 BSC		
eS[5][6]	0.35 BSC			0.0138 BSC		
N[7]	88					
SD[5][8]	0.61 BSC			0.0240 BSC		
SE[5][8]	0.175 BSC			0.0069 BSC		
aaa[9]	0.02			0.0008		
bbb[9]	0.06			0.0024		
ccc[9]	0.03			0.0012		
ddd[9]	0.015			0.0006		
eee[9]	0.05			0.0020		

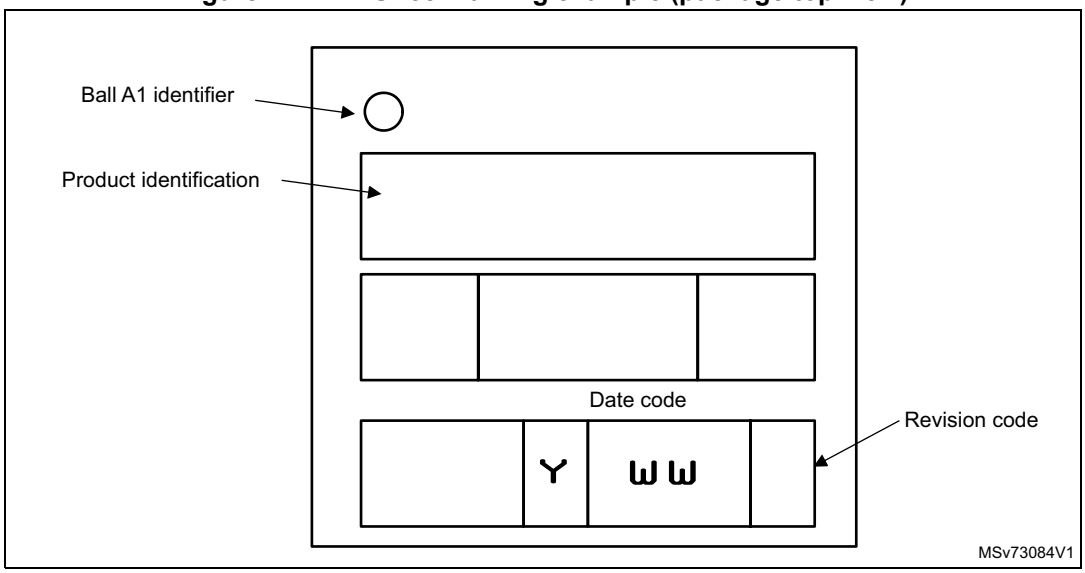
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances, refer to form and position table. On the drawing, these dimensions are framed. For the tolerances, refer to form and position values.
6. e represents the solder balls grid pitch(es).
7. N represents the total number of balls.
8. Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.
9. Tolerance of form and position drawing

Example of device marking for thin WLCSP88

Figure 21 gives an example of the locations and orientation of the marking areas versus ball A1, and allows engineering samples to be identified.

With the device text markings oriented as shown below, ball A1 is always located at top left.

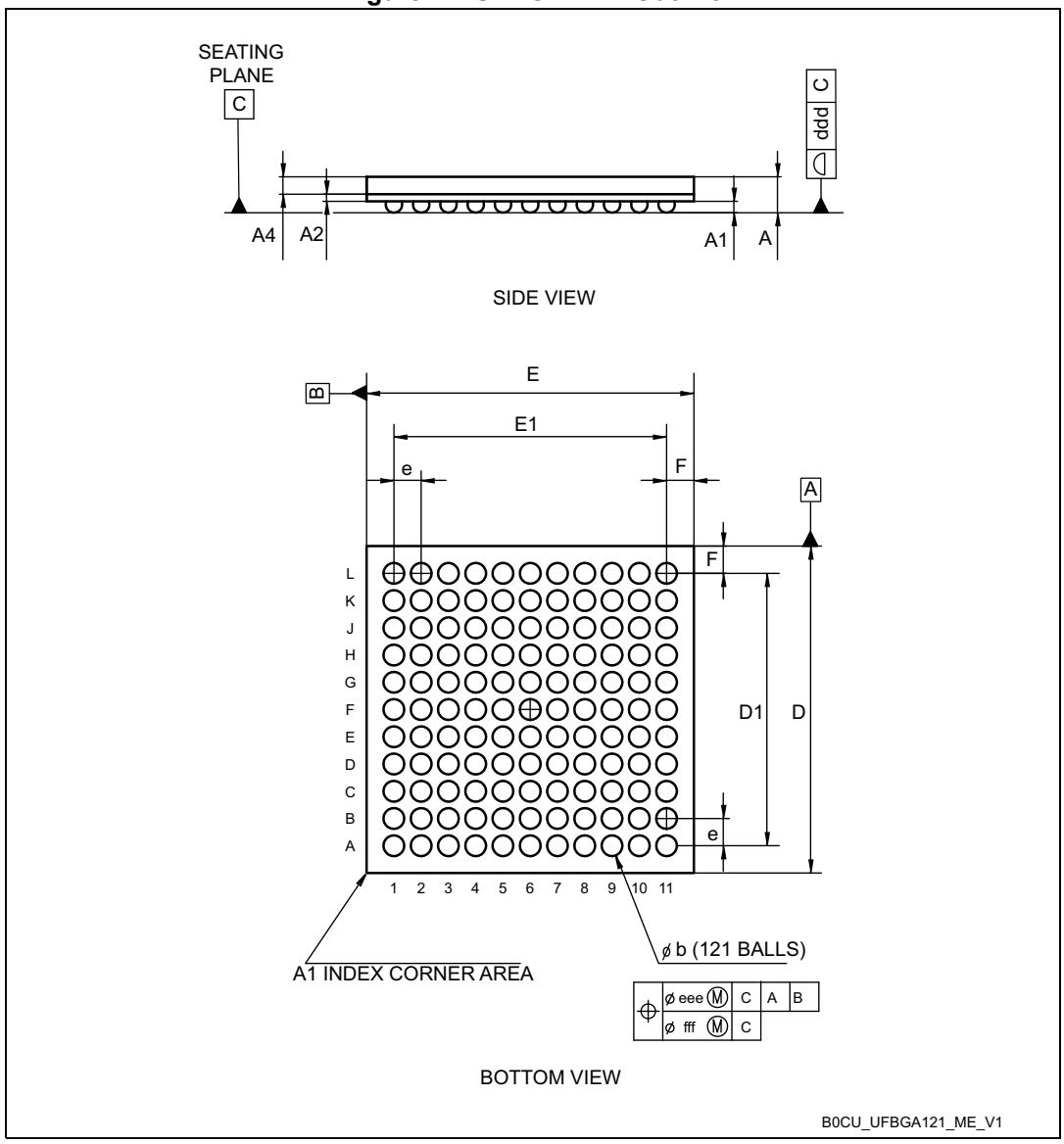
Figure 21. WLCSP88 marking example (package top view)



5.5 UFBGA121 package information (B0CU)

This UFBGA is a 121-ball, 6 x 6 mm, 0.5 mm pitch, fine pitch, square ball grid array package.

Figure 22. UFBGA121 - Outline



1. Drawing is not to scale.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 29. UFBGA121 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.60	-	-	0.0236
A1	-	-	0.11	-	-	0.0043
A2	-	0.13	-	-	0.0051	-
A4	-	0.32	-	-	0.0126	-
b[3]	0.24	0.29	0.34	0.0094	0.0114	0.0134
D	5.85	6.00	6.15	0.2303	0.2362	0.2421
D1	-	5.00	-	-	0.1969	-
E	5.85	6.00	6.15	0.2303	0.2362	0.2421
E1	-	5.00	-	-	0.1969	-
e	-	0.50	-	-	0.0197	-
F	-	0.50	-	-	0.0197	-
ddd	-	-	0.08	-	-	0.0031
eee[4]	-	-	0.15	-	-	0.0059
fff[5]	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to four decimal digits.
2. - UFBGA stands for Ultra-Thin Profile Fine Pitch Ball Grid Array.
   - Ultra Thin profile: 0.50 < A ≤ 0.65 mm / Fine pitch: e < 1.00 mm pitch.
   - The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A Max = A1 Typ + A2 Typ + A4 Typ + √ (A1² + A2² + A4² tolerance values)
3. The typical balls diameter before mounting is 0.20 mm
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datumC of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 23. UFBGA121 - Footprint example

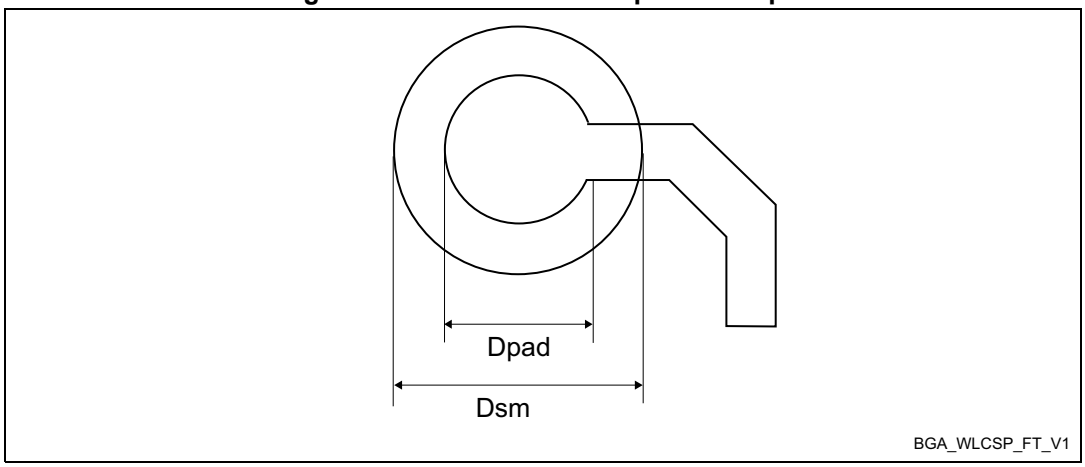


Table 30. UFBGA121 - Example of PCB design rules

Dimension	Values
Pitch	0.5 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

5.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the specified values.

T_J max (in Celsius degrees) can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max)
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt (this is the maximum chip internal power)

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 31. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient**	UFQFPN48 - 7 mm x 7 mm	28.4	°C/W
		VFQFPN68 - 8 mm x 8 mm	47.0	
		Thin WLCSP88	TBD	
		UFBGA121 - 6 mm x 6 mm	TBD	
Θ_{JB}	**Thermal resistance junction-board**	UFQFPN48 - 7 mm x 7 mm	12.8	
		VFQFPN68 - 8 mm x 8 mm	36.1	
		Thin WLCSP88	N/A	
		UFBGA121 - 6 mm x 6 mm	TBD	
Θ_{JC}	**Thermal resistance junction-case**	UFQFPN48 - 7 mm x 7 mm	10.0	
		VFQFPN68 - 8 mm x 8 mm	13.7	
		Thin WLCSP88	N/A	
		UFBGA121 - 6 mm x 6 mm	TBD	

6 Ordering information

Example: STM32 WB A65 C I U 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

A62 = Die A6, reduced set of features
A63 = Die A6, crossover SMPS
A64 = Die A6, full set of features LDO
A65 = Die A6, full set of features SMPS

Pin count

C = 48 pins
R = 68 pins
M = 88 pins
P = 121 pins

Flash memory size

I = 2 Mbytes

G = 1 Mbyte

Package

U = UFQFPN
V = VFQFPN
F = Thin WLCSP
I = UFBGA

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
7 = Industrial temperature range, -40 to 105 °C (125 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options, or for further information on any aspect of this device, contact your nearest ST sales office.

7 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on www.st.com for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
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8 Revision history

Table 32. Document revision history

Date	Revision	Changes
08-Nov-2024	1	Initial release.