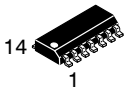
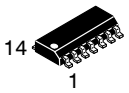
Hex Inverting Schmitt Trigger

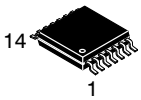
MM74HCT14



SOIC-14 NB
CASE 751A-03



SOIC-14
CASE 751EF



TSSOP-14 WB
CASE 948G

Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout-compatible with the standard 74LS logic family. Inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 10 ns
- Wide Power Supply Range: 4.5 V – 5.5 V
- Low Quiescent Current: 10 μA Maximum
- Low Input Current: 1 μA Maximum
- Fanout of 10 LS-TTL Loads
- Typical Hysteresis Voltage: 0.6 V at V_{CC} = 4.5 V
- TTL, LS Pin-out and Input Threshold Compatible
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Connection Diagram

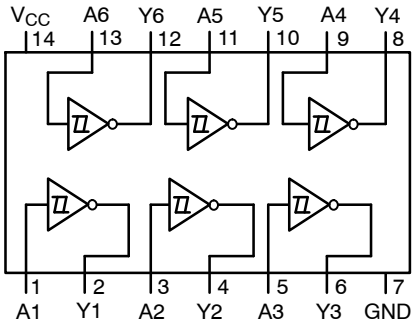


Figure 1. Pin Assignments

Schematic Diagram

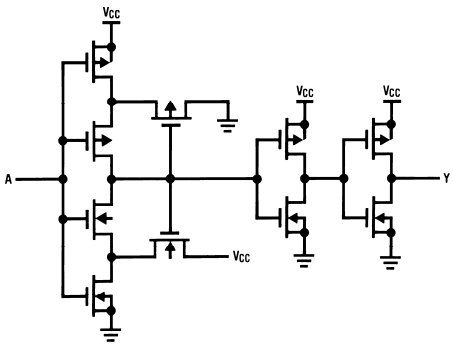
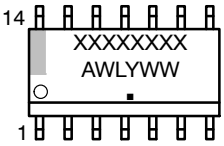
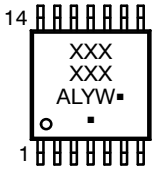


Figure 2. Schematic

MARKING DIAGRAMS



(SOIC-14, SOIC-14 NB)



(TSSOP-14 WB)

XXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	+6.5	V
V_{IN}	DC Input Voltage	−0.5	V_{CC} + 0.5	V
V_{OUT}	DC Output Voltage	−0.5	V_{CC} + 0.5	V
I_{IK}, I_{OK}	Clamp Diode Current		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC V_{CC} or GND Current, Per Pin		±50	mA
T_{STG}	Storage Temperature Range	−65	+150	°C
T_L	Lead Temperature (Soldering 10 second)		+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC}	T_A = +25 °C	T_A = −40 to +85 °C		Unit
				Typ	Guaranteed Limits		
V_{T+}	Positive-Going Threshold Voltage	Minimum	4.5	1.5	1.2	1.2	V
			5.5	1.7	1.4	1.4	
		Maximum	4.5	1.5	1.9	1.9	
			5.5	1.7	2.1	2.1	
V_{T-}	Negative-Going Threshold Voltage	Minimum	4.5	0.9	0.5	0.5	V
			5.5	1.0	0.6	0.6	
		Maximum	4.5	0.9	1.2	1.2	
			5.5	1.0	1.4	1.4	
V_H	Hysteresis Voltage	Minimum	4.5	0.6	0.4	0.4	V
			5.5	0.7	0.4	0.4	
		Maximum	4.5	0.6	1.4	1.4	
			5.5	0.7	1.5	1.5	
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	4.5	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA	4.5	4.20	3.98	3.84	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA	5.5	5.20	4.98	4.98	
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 20 μA	4.5	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.0 mA	4.5	0.2	0.26	0.33	
		V_{IN} = V_{IH} or V_{IL}, $\|I_{OUT}\|$ = 4.8 mA	5.5	0.2	0.26	0.33	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}	5.5		±0.1	±1.0	μA

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DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V_{CC}	T_A = +25 °C	T_A = −40 to +85 °C		Unit
				Typ	Guaranteed Limits		
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	5.5		1.0	10.0	μA
		V_{IN} = 2.4 V or 0.5 V			2.4	2.4	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25 °C, C_L = 15 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Typ	Guaranteed Limit	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay	10	18	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5.0 V ±10%, C_L = 50 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	T_A = +25 °C	T_A = −40 to +85 °C		Unit
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay			20	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	ns
C_{PD}	Power Dissipation Capacitance (Note 1)	Per Gate		25		pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. C_{PD} determines the no-load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Applications

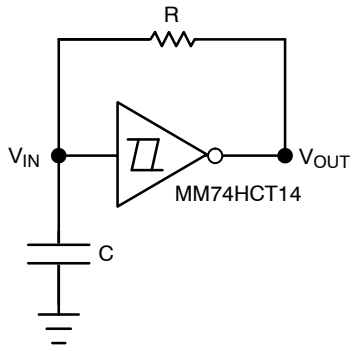


Figure 3. Low Power Oscillator

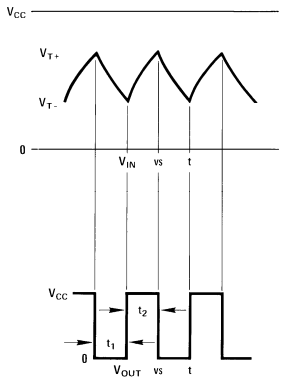


Figure 4. Oscillator Input and Output Waveforms

The following equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$:

$$t_2 \approx RC\ln\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \quad \text{(eq. 1)}$$

$$f \approx \frac{1}{RC\ln\frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \quad \text{(eq. 2)}$$

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ORDERING INFORMATION

Device	Marking	Package	Shipping†
MM74HCT14M	HCT14A	SOIC-14 NB, Case 751A-03 (Pb-Free and Halide Free)	55 Units / Tube
MM74HCT14MX	HCT14A	SOIC-14, Case 751EF (Pb-Free and Halide Free)	2500 / Tape & Reel
MM74HCT14MTCX	HCT 14A	TSSOP-14 WB, Case 948G (Pb-Free and Halide Free)	2500 / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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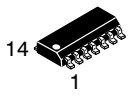
REVISION HISTORY

Revision	Description of Changes	Date
4	Edits to the package name labels	10/20/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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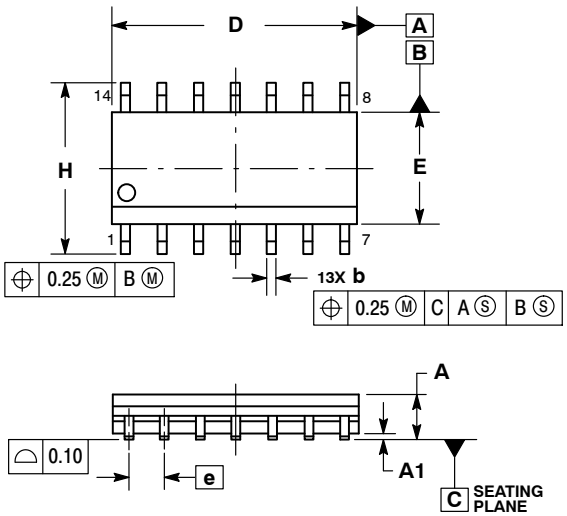
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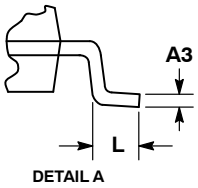


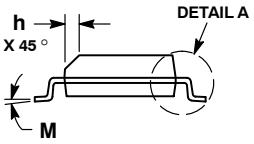
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SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



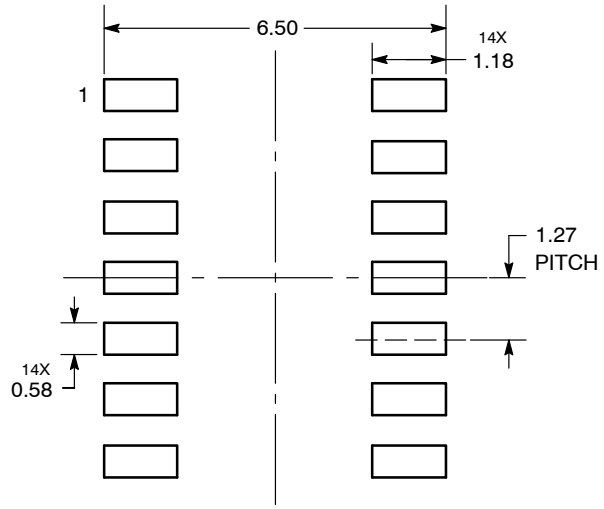




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

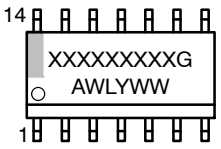
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
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5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
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3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
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7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
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12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
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14. ANODE

STYLE 7:
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12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
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6. ANODE/CATHODE
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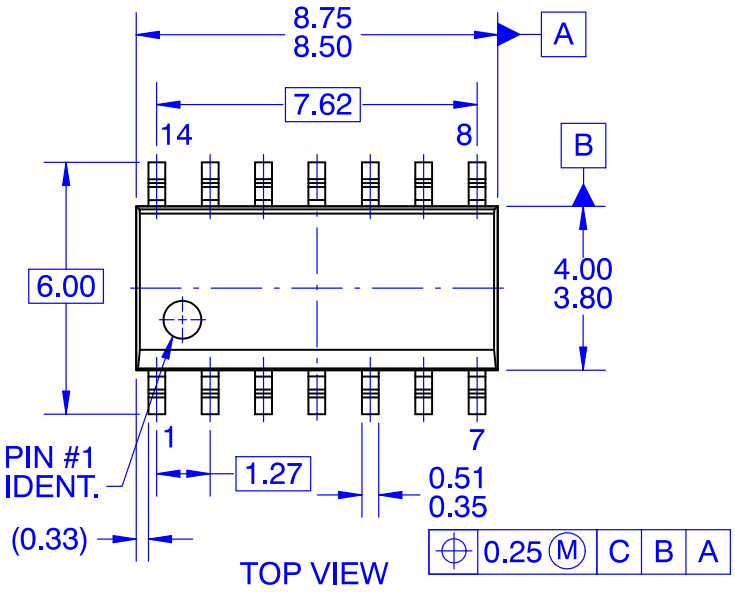
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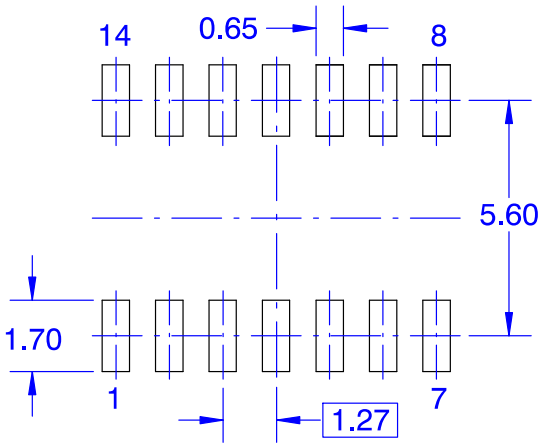
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SOIC14
CASE 751EF
ISSUE O

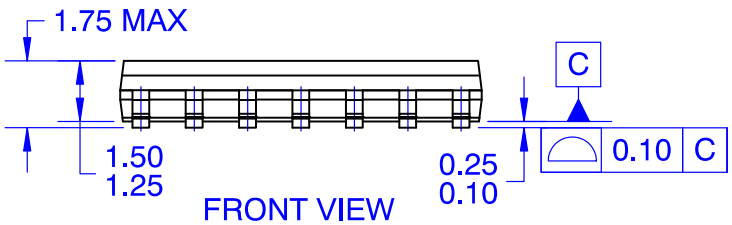
DATE 30 SEP 2016



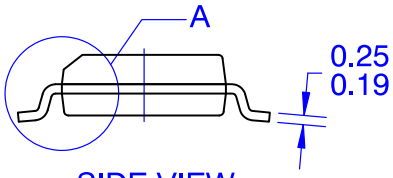
TOP VIEW



LAND PATTERN RECOMMENDATION

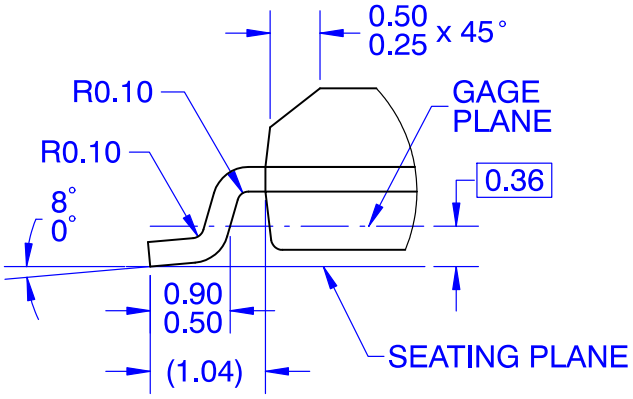


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS−012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145−14M
E. CONFORMS TO ASME Y14.5M, 2009

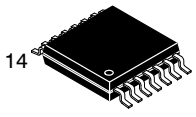


DETAIL A
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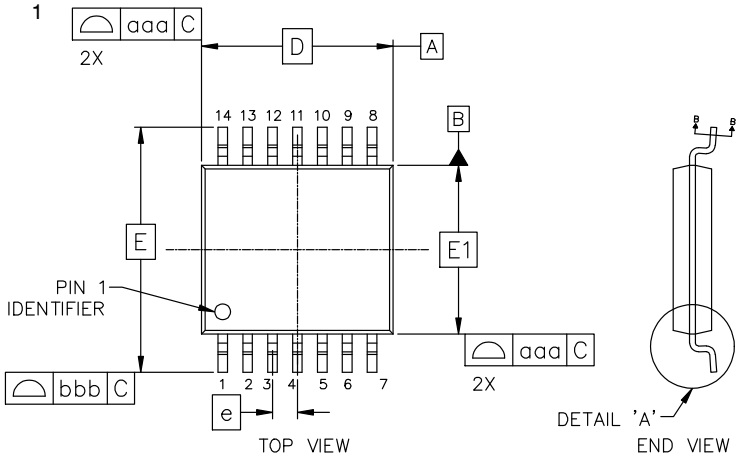
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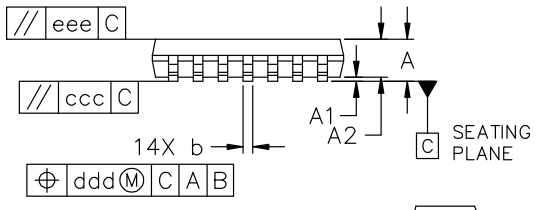
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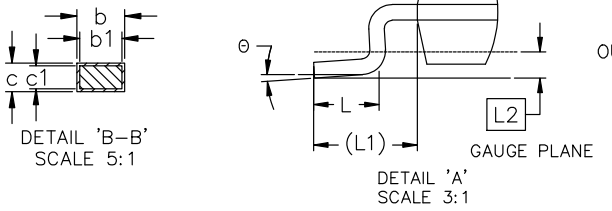


TSSOP−14 5.00x4.40x0.95, 0.65P
CASE 948G
ISSUE D

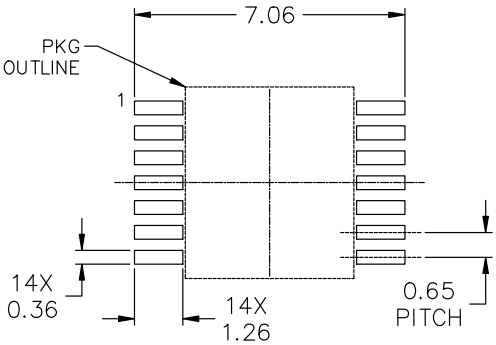
DATE 30 JUN 2026







MILLIMETERS			
DIM	MIN	NOM	MAX
A	−−−	−−−	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.19	0.25	0.30
b1	0.19	0.22	0.25
c	0.09	0.15	0.20
c1	0.09	0.12	0.16
D	5.00 BSC		
E	6.40 BSC		
E1	4.40 BSC		
e	0.65 BSC		
L	0.50	0.63	0.75
L1	1.00 REF		
L2	0.25 BSC		
θ	0°	4°	8°
TOLERANCE FORM & POSITION			
aaa	0.10		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.10		

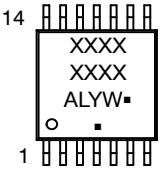


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D DOES NOT INCLIDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSSOP−14 5.00x4.40x0.95, 0.65P	PAGE 1 OF 1

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