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FAIRCHILD SEMICONDUCTOR®

October 2012

FAN73833
Half-Bridge Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 350 mA / 650 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative V_S Swing to -9.8 V for Signal Propagation at V_{DD}=V_{BS}=15 V
- 3.3 V and 5 V Input Logic Compatible
- Outputs in Phase with Input Signals
- Built-in UVLO Functions for Both Channels
- Built-on Shoot-Through Prevention Circuit
- Built-in Common-Mode dv/dt Noise Canceling Circuit
- Internal Dead-Time Typically 400 ns

Applications

- SMPS
- Motor Drive Inverter
- Fluorescent Lamp Ballast
- HID Ballast

Description

The FAN73833 is a half-bridge gate-drive IC for driving MOSFETs and IGBTs, operating up to +600 V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side driver under high dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to V_S=-9.8 V (typical) for V_{BS}=15 V.

The UVLO circuits for both channels prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 350 mA / 650 mA, respectively, which is suitable for all kinds of half- and full-bridge inverters.

8-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN73833M	8-SOP	-40°C to +125°C	Tube
FAN73833MX			Tape & Reel

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Typical Application Circuit

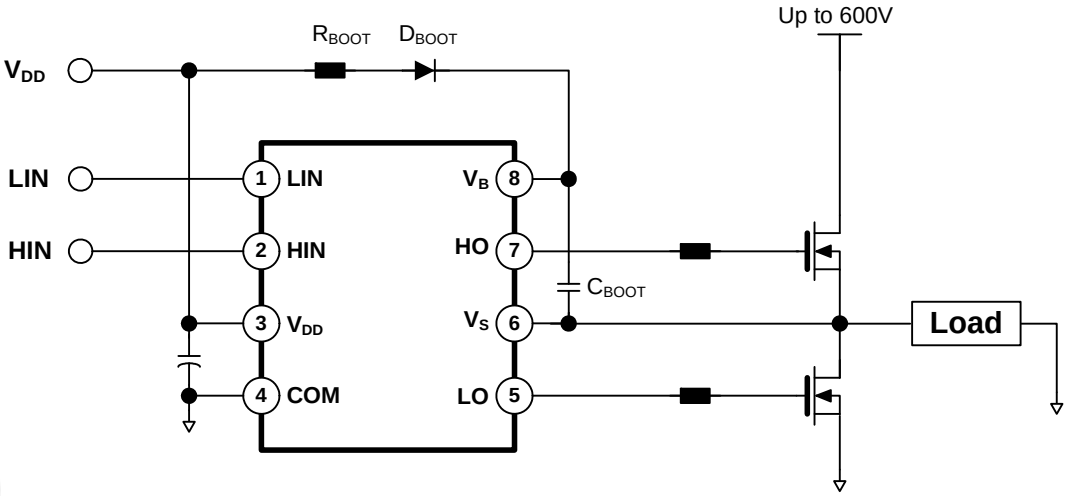


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

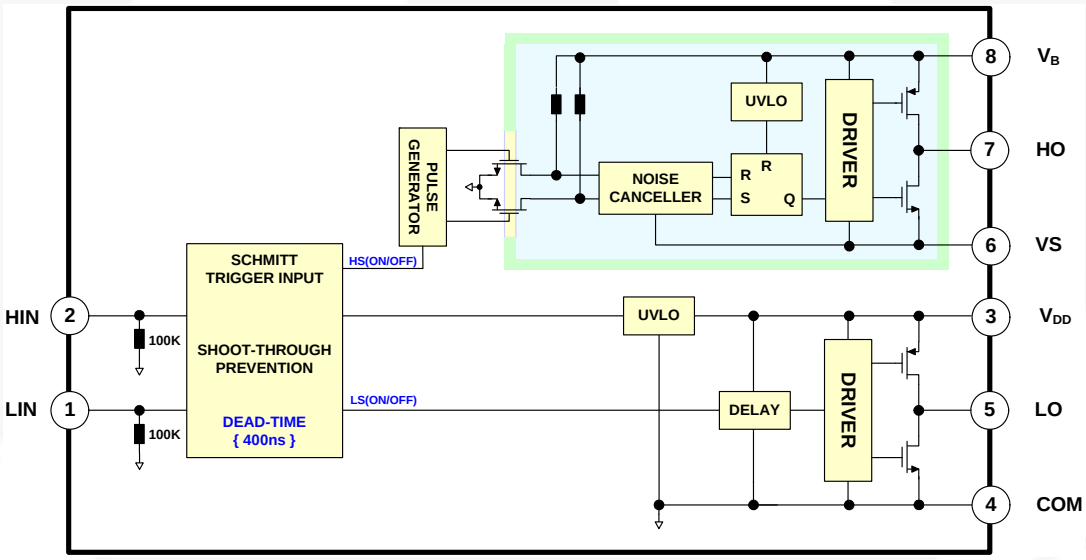


Figure 2. Functional Block Diagram

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Pin Configuration

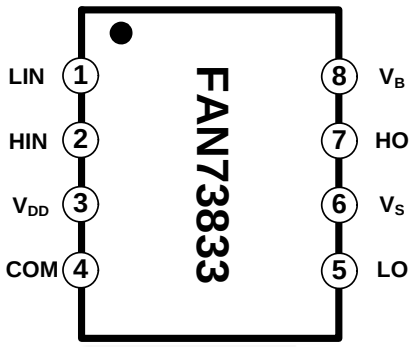


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	LIN	Logic Input for Low-Side Driver
2	HIN	Logic Input for High-Side Driver
3	V_{DD}	Low-Side Supply Voltage
4	COM	Logic Ground and Low-Side Driver Return
5	LO	Low-Side Driver Output
6	V_S	High-Side Floating Supply Return
7	HO	High-Side Driver Output
8	V_B	High-Side Floating Supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	V_B+0.3	V
V_B	High-side floating supply voltage	-0.3	625	V
V_{HO}	High-side floating output voltage HO	V_S-0.3	V_B+0.3	V
V_{DD}	Low-side and logic-fixed supply voltage	-0.3	25	V
V_{LO}	Low-side output voltage LO	-0.3	V_{DD}+0.3	V
V_{IN}	Logic input voltage (HIN/LIN)	-0.3	V_{DD}+0.3	V
COM	Logic ground and low-side driver return	V_{DD}-25	V_{DD}+0.3	V
dV_S/dt	Allowable offset voltage slew rate		50	V/ns
P_D (1)(2)(3)	Power dissipation		0.625	W
θ_{JA}	Thermal resistance, junction-to-ambient		200	°C/W
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature	-55	150	°C

Notes:

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
2. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-side floating supply voltage	V_S+11	V_S+20	V
V_S	High-side floating supply offset voltage	6-V_{DD}	600	V
V_{DD}	Low-side supply voltage	11	20	V
V_{HO}	High-side (HO) output voltage	V_S	V_B	V
V_{LO}	Low-side (LO) output voltage	COM	V_{DD}	V
V_{IN}	Logic input voltage (HIN/LIN)	COM	V_{DD}	V
T_A	Ambient temperature	-40	125	°C

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Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS}) = 15.0 V, and T_A=25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to respective outputs HO and LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT SECTION						
I_{QBS}	Quiescent V_{BS} supply current	V_{IN}=0 V or 5 V		35	100	µA
I_{QDD}	Quiescent V_{DD} supply current	V_{IN}=0 V or 5 V		80	200	µA
I_{PBS}	Operating V_{BS} supply current	f_{IN}=20 kHz, rms value		420	750	µA
I_{PDD}	Operating V_{DD} supply current	f_{IN}=20 kHz, rms value		420	750	µA
I_{LK}	Offset supply leakage current	V_B=V_S=600 V			10	µA
POWER SUPPLY SECTION						
V_{DDUV+} V_{BSUV+}	V_{DD} and V_{BS} supply under-voltage positive going threshold		8.2	9.2	10.1	V
V_{DDUV-} V_{BSUV-}	V_{DD} and V_{BS} supply under-voltage negative going threshold		7.2	8.3	9.2	V
V_{DDUVH} V_{BSUVH}	V_{DD} supply under-voltage lockout hysteresis			0.9		V
GATE DRIVER OUTPUT SECTION						
V_{OH}	High-level output voltage, V_{BIAS}-V_O	I_O=20 mA			1.0	V
V_{OL}	Low-level output voltage, V_O				0.6	V
I_{O+} (4)	Output high short-circuit pulse current	V_O=0 V, V_{IN}=5 V with PW<10 µs	250	350		mA
I_{O-} (4)	Output low short-circuit pulsed current	V_O=15 V, V_{IN}=0 V with PW<10 µs	500	650		mA
V_S	Allowable negative V_S pin voltage for IN signal propagation to HO			-9.8	-7.0	V
LOGIC INPUT SECTION (INPUT and SHUTDOWN)						
V_{IH}	Logic "1" input voltage		2.5			V
V_{IL}	Logic "0" input voltage				1.2	V
I_{IN+}	Logic "1" input bias current	V_{IN}=5 V		50	100	µA
I_{IN-}	Logic "0" input bias current	V_{IN}=0 V			2.0	µA
R_{PD}	Input pull-down resistance			100		KΩ

Note:

4. This parameter is guaranteed by design.

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Dynamic Electrical Characteristics

V_{BIAS} (V_{DD}, V_{BS})=15.0 V, V_S=COM, C_L=1000 pF, and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-on propagation delay time	V_S=0 V		150	270	ns
t_{OFF}	Turn-off propagation delay time	V_S=0 V		140	250	ns
t_R	Turn-on rising time			50	100	ns
t_F	Turn-off falling time			30	80	ns
DT	Dead-time		330	450	580	ns

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Typical Characteristics

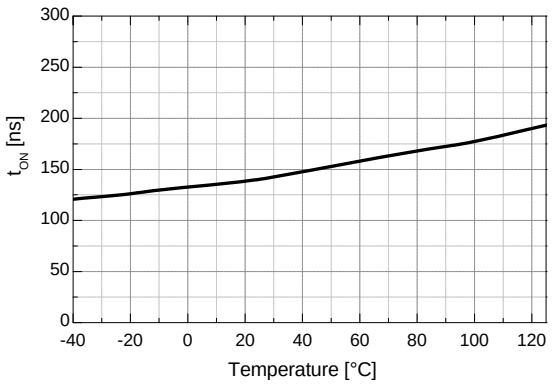


Figure 4. Turn-on Propagation Delay vs. Temp.

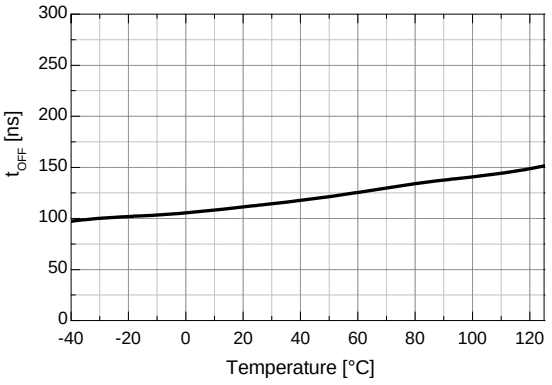


Figure 5. Turn-off Propagation Delay vs. Temp.

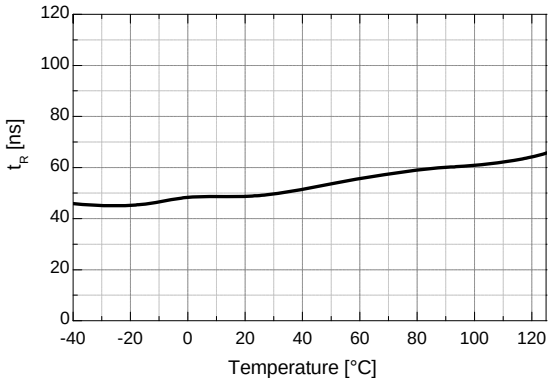


Figure 6. Turn-on Rise Time vs. Temp.

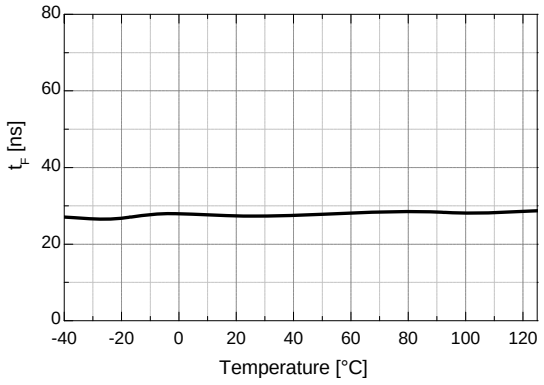


Figure 7. Turn-off Fall Time vs. Temp.

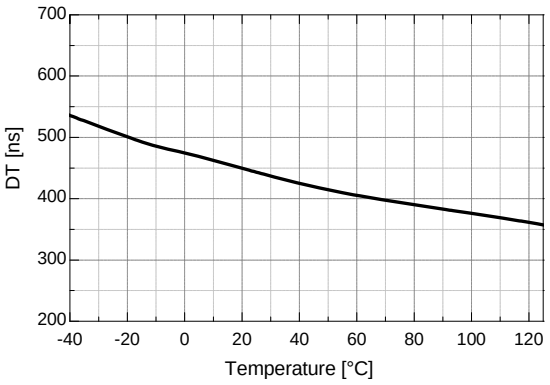


Figure 8. Dead Time vs. Temp.

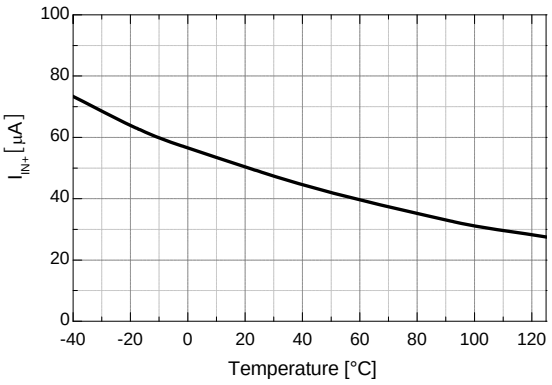


Figure 9. Logic Input High Bias Current vs. Temp.

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Typical Characteristics (Continued)

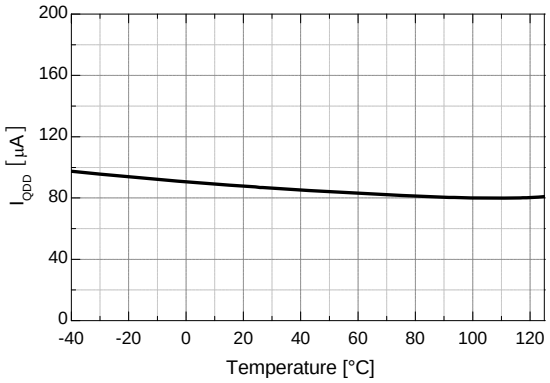


Figure 10. Quiescent V_{DD} Supply Current vs. Temp.

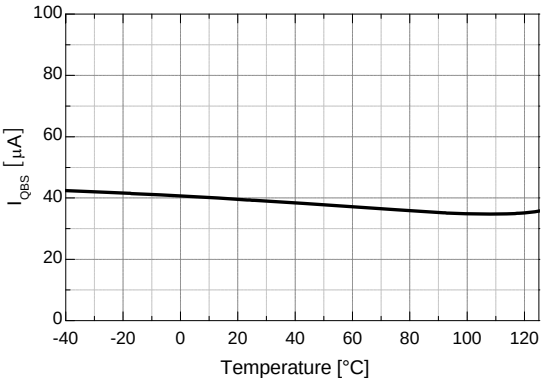


Figure 11. Quiescent V_{BS} Supply Current vs. Temp.

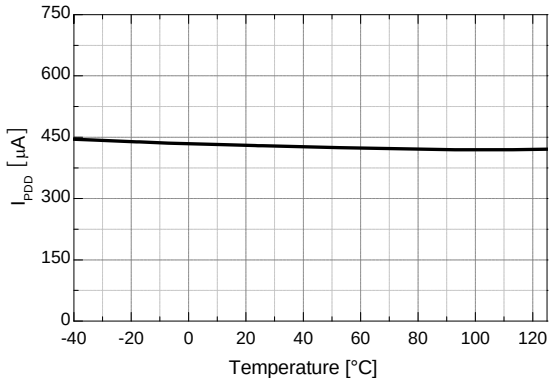


Figure 12. Operating V_{DD} Supply Current vs. Temp.

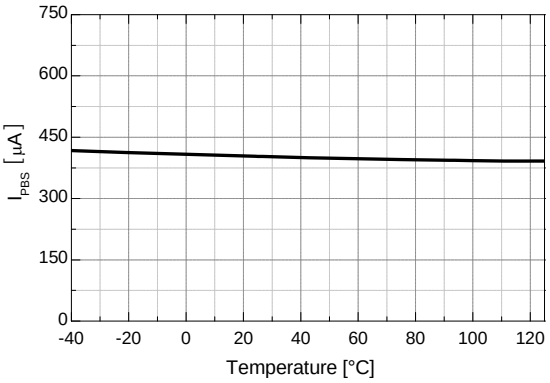


Figure 13. Operating V_{BS} Supply Current vs. Temp.

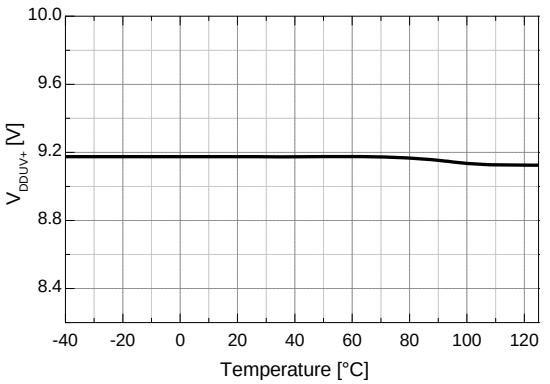


Figure 14. V_{DD} UVLO+ vs. Temp.

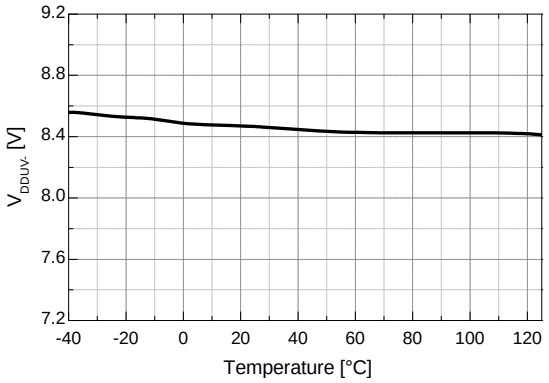


Figure 15. V_{DD} UVLO- vs. Temp.

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Typical Characteristics (Continued)

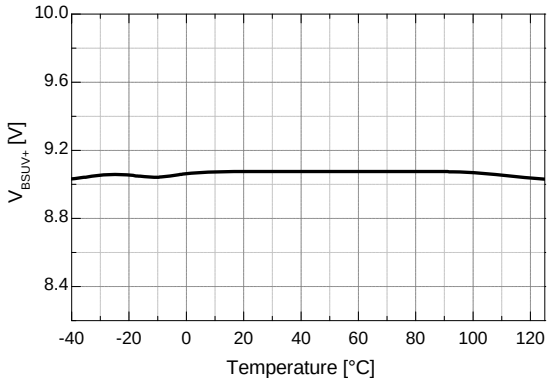


Figure 16. V_{BS} UVLO+ vs. Temp.

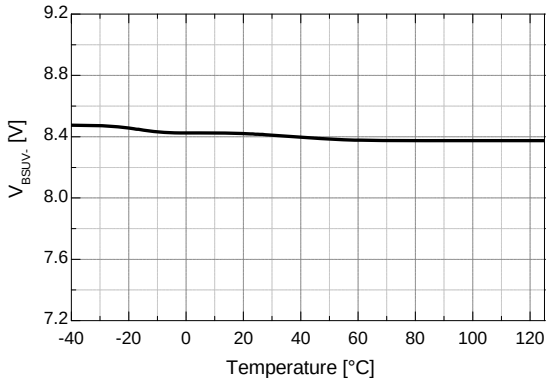


Figure 17. V_{BS} UVLO- vs. Temp.

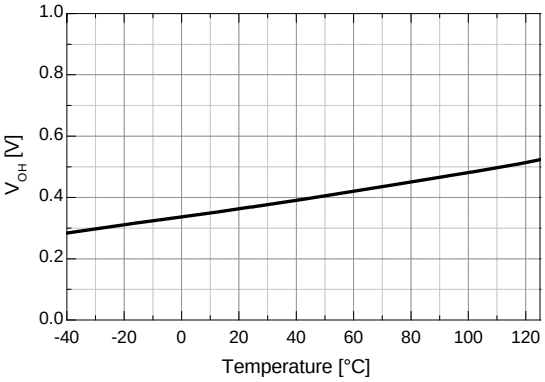


Figure 18. High-Level Output Voltage vs. Temp.

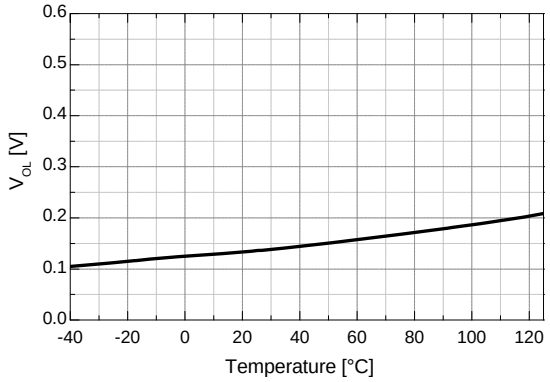


Figure 19. Low-Level Output Voltage vs. Temp.

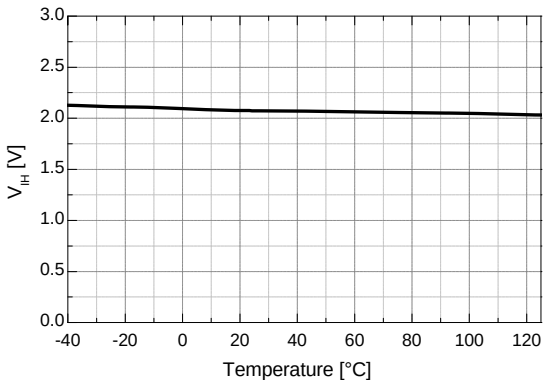


Figure 20. Logic High Input Voltage vs. Temp.

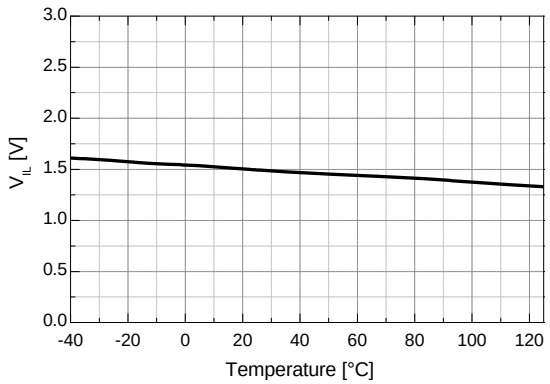


Figure 21. Logic Low Input Voltage vs. Temp.

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Typical Characteristics (Continued)

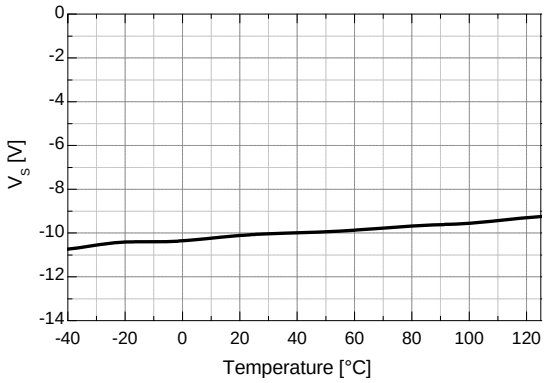


Figure 22. Allowable Negative V_S Voltage vs. Temp.

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Application Information

1. Protection Function

1.1 Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry for each channel that monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{BS}) independently. It can be designed prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage. The UVLO hysteresis prevent chattering during power supply transitions.

1.2 Shoot-Through Prevention Function

The FAN73833 has shoot-through prevention circuitry monitoring the high- and low-side control inputs. It can be designed to prevent outputs of high and low side from turning on at same time, as shown Figure 23 and 28.

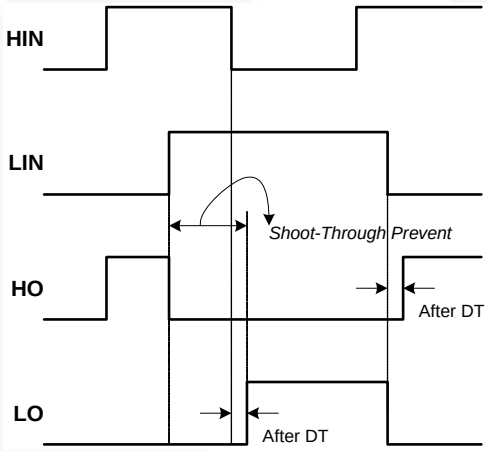


Figure 23. Waveforms for Shoot-Through Prevention

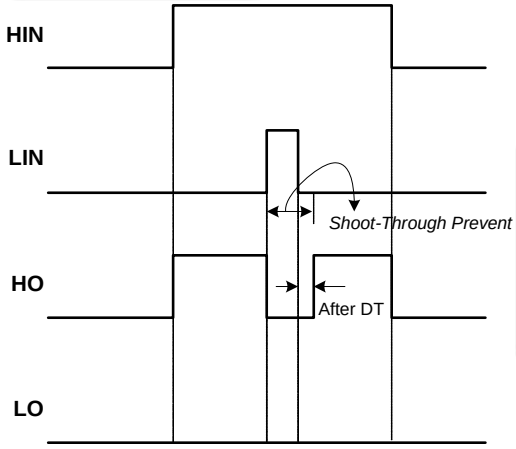


Figure 24. Waveforms for Shoot-Through Prevention

2. Switching Time Definitions

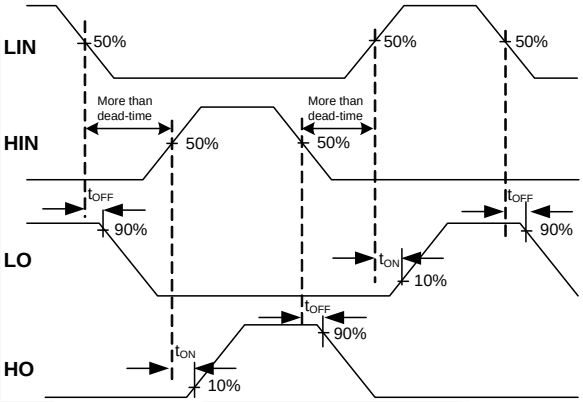


Figure 25. Switching Time Definition

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Mechanical Dimensions

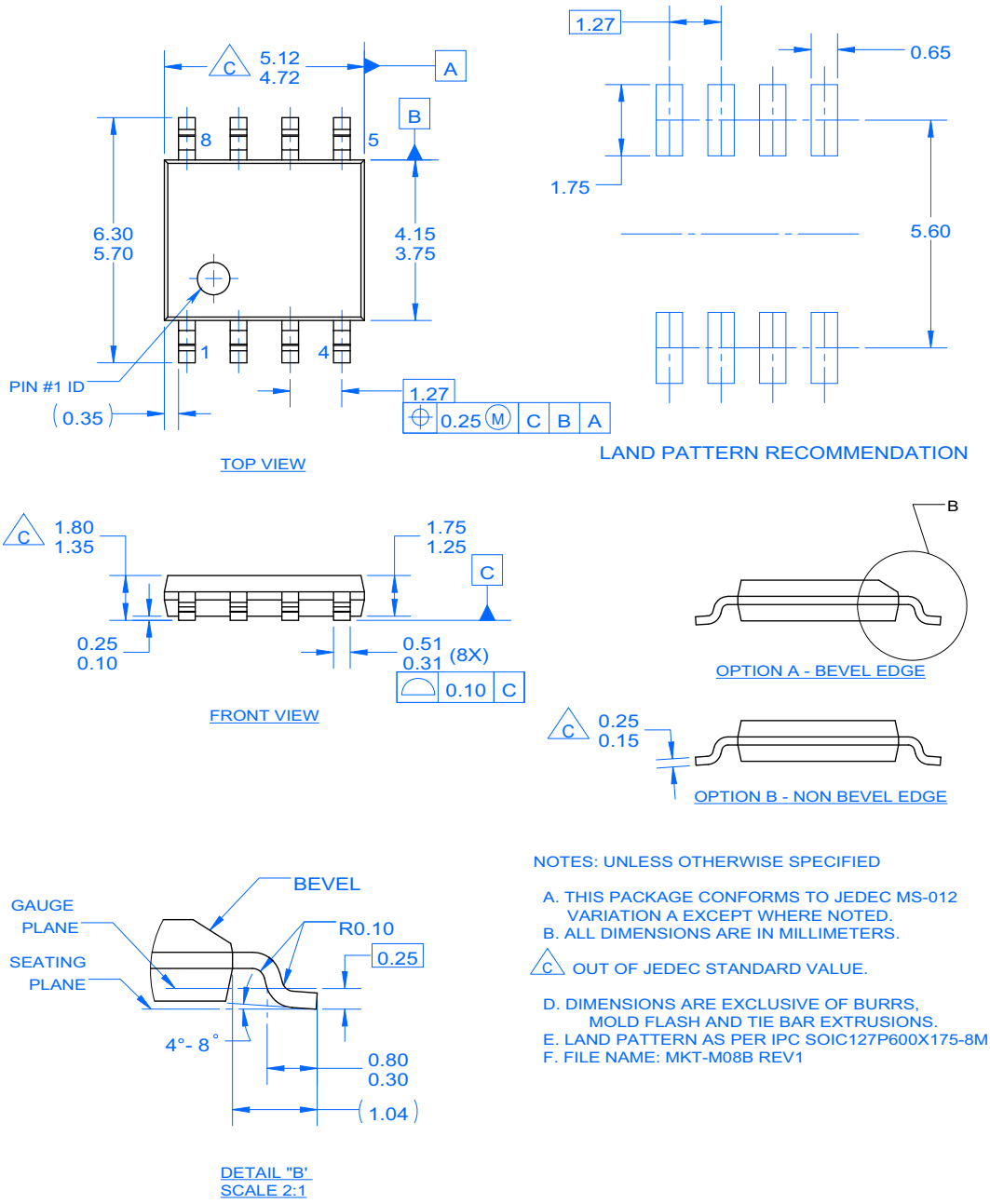


Figure 26. 8-Lead, Small Outline Package (SOP)

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the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
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Definition of Terms

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