# THCS253

IOHA:B 8B10B Serial Transceiver

## 1. Overview

The THCS253 is a transceiver IC with serializer and deserializer on a single chip that aggregates 32-bit GPIO and 2-wire serial interface signals and converts them into two pairs of differential signals for transmission and reception.

The THCS253 has two modes: SYNC mode and ASYNC mode. In SYNC mode, the uplink and downlink high-speed transmission signals operate synchronously, driven by the reference clock signal from the primary chip side. In ASYNC mode, the uplink and downlink high-speed transmission signals operate asynchronously, driven by the clock signals from both the primary and secondary chips. The reference clock can be selected from either the internal OSC clock or the external input clock.

By accessing internal registers via the 2-wire serial interface, the 32-bit GPIO direction and output buffer type can be customized for each pin.

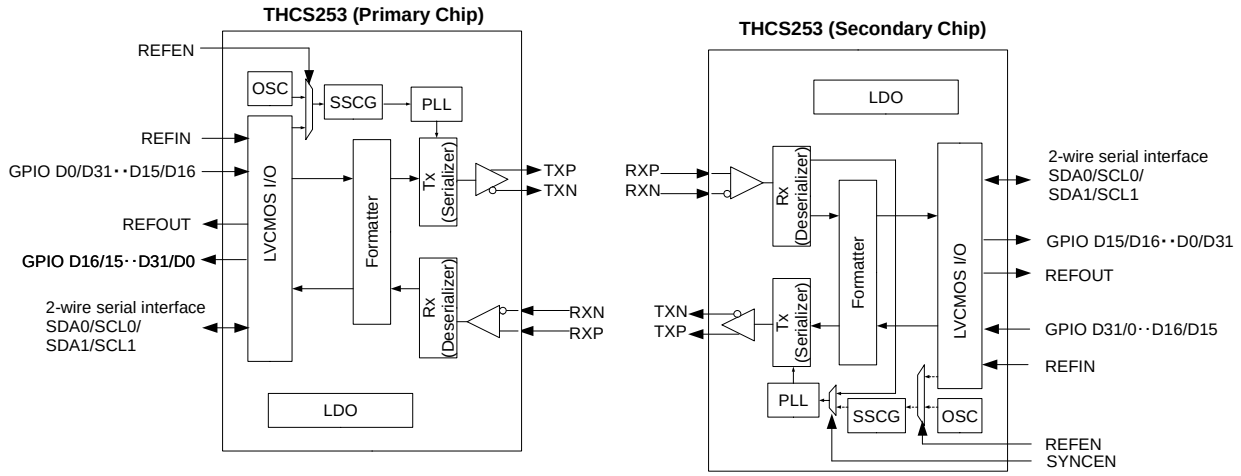
The 8B10B encoding and decoding used in the THCS253 provides high robustness, DC balanced signals, and easy connection to optical/wireless communication devices.

The built-in adaptive equalizer allows for flexible cable selection, and the CML driver with pre-emphasis allows for even longer cable transmissions.

## 2. Features

- Up to 32-bit GPIOs
- Internal oscillator mode requires no external clock signal input
- Uplink and downlink synchronous mode with one-sided reference clock drive
- Uplink and downlink asynchronous mode with both side reference clocks driven
- Output buffer selectable between open-drain and push-pull
- 2-wire serial interface fast mode can be bridged
- Standby mode for low-power operation
- Adaptive equalizer supports high-loss transmission media
- 8B10B encoding/decoding
- Digital noise filters can be set for input and output
- Error detection and notification
- External reference clock frequency: 9-133.3MHz
- Built-in spread spectrum clock generator
- Single power supply operation: 1.7 V - 3.6 V
- Operating ambient temperature range: -40°C to 85°C

## 3. Block diagram



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## Contents

1. Overview ..... 1
2. Features ..... 1
3. Block diagram ..... 1
4. Pin configuration ..... 4
5. Pin description ..... 5
6. Absolute maximum rating ..... 9
7. Recommended operatingconditions ..... 9
8. Electrical characteristics ..... 10
8.1. Current consumption ..... 10
8.2. LVCMOS/Analog input DC specifications ..... 12
8.3. LVCMOS AC characteristics ..... 13
8.4. CML DC characteristics ..... 17
8.5. CML AC characteristics ..... 17
8.6. 2-wire serial interface DC/AC characteristics ..... 21
9. CML Line diagram ..... 22
9.1. CML input diagram ..... 22
10. Function ..... 23
10.1. Function overview ..... 23
10.2. Power supply ..... 23
10.2.1. Internal regulator output/input function (CAPOUT, CAPINA, CAPINP) ..... 23
10.3. Chip Operating state ..... 24
10.4. Chip operation mode ..... 24
10.4.1. Chip configuration ..... 24
10.4.2. Operating clock mode select ..... 25
10.4.3. Operating clock select ..... 25
10.4.4. Combination of operating modes ..... 27
10.5. Pin setting and combination of chip mode ..... 30
10.6. Byte mode and frequency range ..... 31
10.7. 2-wire serial interface ..... 32
10.7.1. 2-wire serial interface setting ..... 32
10.7.2. Clock stretching ..... 33
10.7.3. Device Address ..... 33
10.7.4. 2-wire serial controller / target register address space ..... 34
10.7.5. 2-wire serial controller SCL frequency ..... 34

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10.7.6. 2-wire serial interface watch dog timer setting ..... 34
10.7.7. THCS253 internal register access protocol via 2-wire serial interface ..... 35
10.7.8. 2-wire serial expander ..... 42
10.8. Direction of GPIO ..... 43
10.9. IO configuration ..... 45
10.9.1. I/O digital noise filter ..... 45
10.9.2. LVCMOS Output buffer type configuration ..... 47
10.9.3. 5V tolerant IO ..... 48
10.9.4. LVCMOS Output drive strength setting ..... 48
10.9.5. CML output swing voltage and pre-emphasis setting ..... 48
10.10. Clock configuration ..... 49
10.10.1. Sampling clock select ..... 49
10.10.2. Clock edge select (RF_IN, RF_OUT) ..... 50
10.11. Spread spectrum clock generator and REFIN(pin) frequency ..... 51
10.12. PWM signal output function ..... 52
10.13. CRC ..... 52
10.14. Error detection and notification ..... 53
10.14.1. READY signal ..... 53
10.14.2. INTN signal ..... 53
10.15. Standby mode: STANDBY(register)=1 ..... 54
11. Register map ..... 56
12. Package ..... 60
13. Reference land pattern ..... 61
14. Notices and Requests ..... 62

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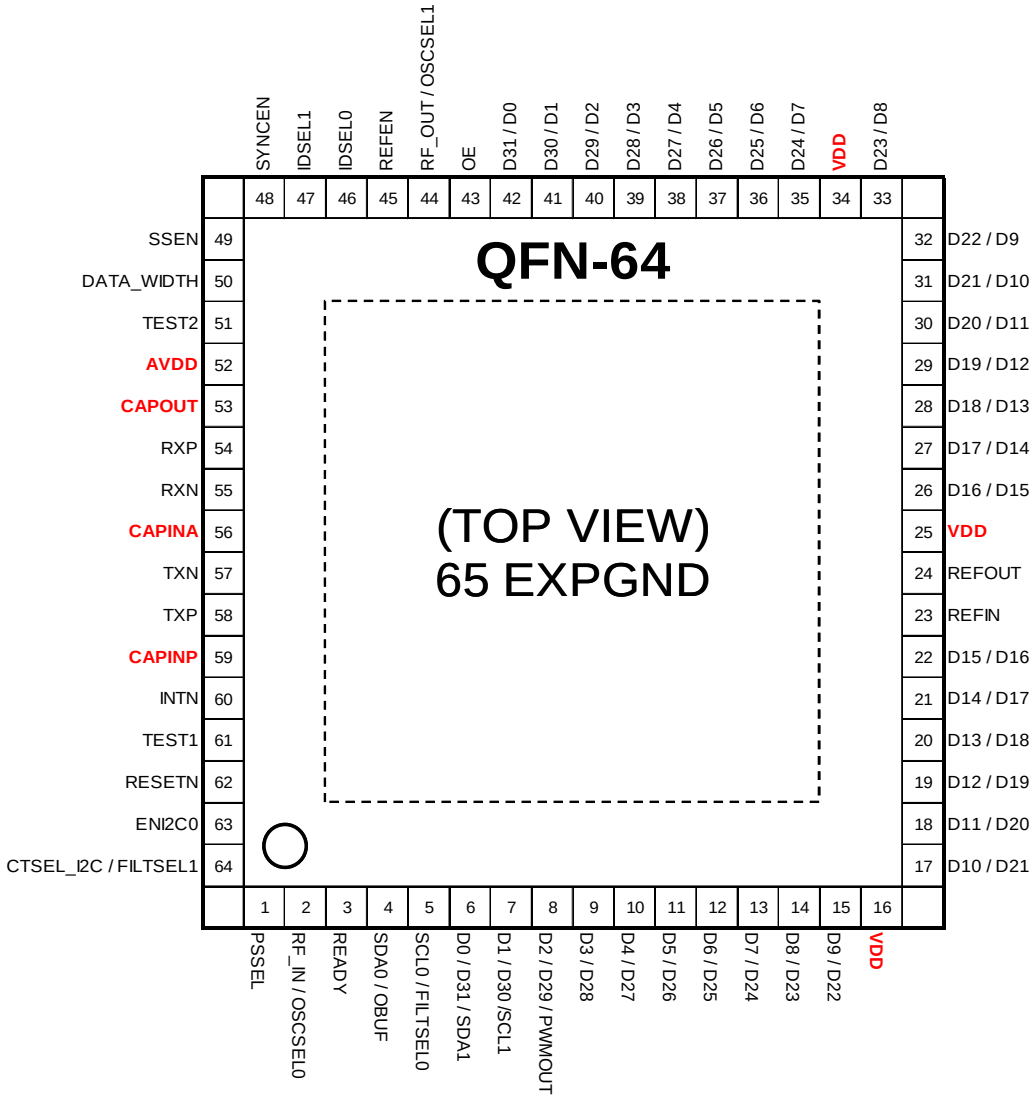
## 4. Pin configuration



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## 5. Pin description

| Pin Name | No. | Type | Description |
|---|---|---|---|
| TXP | 58 | CO | Differential P-ch output |
| TXN | 57 | CO | Differential N-ch output |
| RXP | 54 | CI | Differential P-ch input |
| RXN | 55 | CI | Differential N-ch input |
| RESETN | 62 | IL | Chip reset<br>0: Chip reset<br>1: Chip operation |
| PSSEL | 1 | IL | Chip mode select *Refer to SYNCEN<br>0: Primary chip mode<br>1: Secondary chip mode |
| SYNCEN | 48 | IL | Link mode select<br>When PSSEL=0 disable<br>When PSSEL=1 enable<br>0: AYNC mode<br>Driven by primary/secondary chip reference clocks<br>1: SYNC mode<br>Driven by primary chip reference clock |
| REFEN | 45 | IL | Reference clock select<br>0: Internal oscillator clock<br>1: External reference clock |
| DATAWIDTH | 50 | IL | Transmission Data width select<br>Primary and secondary DATAWIDTH should be set the same.<br>*Refer to Table 8, Table 9, Table 19 |
| ENI2C | 63 | IL | 2-wire serial interface permission<br>0: Disable<br>1: Enable |
| CTSEL_I2C/<br>FILTSEL1 | 64 | IL | CTSEL_I2C：2-wire serial Controller / Target select<br>0: 2-wire serial target（I2C controller device side）<br>1: 2-wire serial controller（I2C remote device side）<br>FILTSEL1：Digital noise filter setting<br>*Refer to Table 21Table 22 |
| IDSEL0 | 46 | IL | 2-wire serial interface device address select<br>*Refer to Table 14 |
| IDSEL1 | 47 | IL | 2-wire serial interface device address select<br>*Refer to Table 14 |
| RF_IN/<br>OSCSEL0 | 2 | IL | RF_IN: Input clock edge select<br>0: Rising edge<br>1: Falling edge<br>OSCSEL0: Internal oscillator clock select<br>*Refer to Table 9 |
| RF_OUT/<br>OSECSEL1 | 44 | IL | Output clock edge select<br>0: Rising edge<br>1: Falling edge<br>OSCSEL1: Internal oscillator clock select<br>*Refer to Table 9 |
| SDA0/<br>OBUF | 4 | BL | SDA0: SDA for 2-wire serial interface 0<br>OBUF: Output buffer type select<br>0: Open-drain<br>1: Push-pull |

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| | | | |
|---|---|---|---|
| SCL0/<br>FILTSEL0 | 5 | BL | SCL0: SCL for 2-wire serial interface 0<br>FILSET0: Digital noise filter setting<br>*Refer to Table 21, Table 22 |
| SSEN | 49 | IL | Spread spectrum clock generator<br>0: SSCG PLL disable<br>1: SSCG PLL enable |
| OE | 43 | IL | Output enable<br>0: LVCMOS output Hi-Z<br>1: LVCMOS output enable |
| REFIN | 23 | B | REFIN：External input clock |
| REFOUT | 24 | O | Pixel clock output |
| READY | 3 | B | CML Link state<br>0: Unlock<br>1: Lock |
| INTN | 60 | BO | Interrupt output *When READY=1<br>0: Error occurred<br>1: (Pull-up) : No Error |
| D0/<br>D31/<br>SDA1 | 6 | BT | D0: Primary chip mode data input/output<br>D31: Secondary chip mode data input/output<br>SDA1: SDA for 2-wire serial interface 1 |
| D1/<br>D30/<br>SCL1 | 7 | BT | D1: Primary chip mode data input/output<br>D30: Secondary chip mode data input/output<br>SCL1: SCL for 2-wire serial interface 1 |
| D2/D29/PWMOUT | 8 | BT | D2: Primary chip mode data input/output<br>D29: Secondary chip mode data input/output<br>PWMOUT: PWM output |
| D4/D27, D5/D26,<br>D6/D25, D7/D24,<br>D8/D23, D9/D22<br>D10/D21, D11/D20,<br>D12/D19, D13/D18,<br>D14/D17, D15/D16,<br>D16/D15, D17/D14,<br>D18/D13, D19/D12,<br>D20/D11, D21/D10,<br>D22/D9, D23/D8,<br>D24/D7, D25/D6,<br>D26/D5, D27/D4 | 10, 11,<br>12, 13,<br>14, 15,<br>17, 18,<br>19, 20,<br>21, 22,<br>26, 27<br>28, 29,<br>30, 31,<br>32, 33,<br>35, 36,<br>37, 38 | B | Primary chip mode data input and output / Secondary chip mode data input and output<br>Left side of "/" is in primary chip mode<br>Right side of "/" is in secondary chip mode |
| D3/D28<br>D28/D3, D29/D2,<br>D30/D1, D31/D0 | 9<br>39, 40,<br>41. 42 | BT | Primary chip mode data input and output / Secondary chip mode data input and output<br>Left side of "/" is in primary chip mode<br>Right side of "/" is in primary chip mode |
| TEST1 | 61 | IL | Shall be tied to Ground |
| TEST2 | 51 | AI | Shall be tied to Ground |
| CAPOUT | 53 | PWR | Decoupling capacitor Pin, 1.2V output |
| CAPINA | 56 | PWR | 1.2V Analog power supply input |
| CAPINP | 59 | PWR | 1.2V Analog power supply input |
| VDD | 16, 25,<br>34 | PWR | 1.7-3.6V Digital power supply input for LVCMOS I/O |
| AVDD | 52 | PWR | 1.7-3.6V Analog power supply input for on-chip regulator |
| EXPGND | 65 | GND | Exposed Pad Ground. Must be tied to the PCB ground plane through an array of via holes |

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Pin type definition
Analog Buffer
CO: CML Output buffer
CI: CML Input buffer
AI: Analog Input buffer

LVCMOS buffer
IL: Low speed schmitt trigger LVCMOS Input buffer
B: LVCMOS Bi-directional buffer
BO: Open-drain LVCMOS Bi-directional buffer
BL: Low speed 5V tolerant schmitt trigger LVCMOS Bi-directional buffer
BT: Low speed 5V tolerant LVCMOS Bi-directional buffer

Power/Ground
PWR: Power supply
GND : Ground

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**Table 1 Primary chip mode pin sharing**

| Pin number | Primary chip / Secondary chip | Primary chip mode | | | | | |
|---|---|---|---|---|---|---|---|
| | Sampling clock | Internal OSC | | | External input | | |
| | 2-wire serial (SDA0/SCL0) | Disable | Enable | Enable | Disable | Enable | Enable |
| | 2-wire serial (SDA1/SCL1) | | Disable | | | Disable | |
| 1 | PSSEL | 0 | 0 | 0 | 0 | 0 | 0 |
| 45 | REFEN | 0 | 0 | 0 | 1 | 1 | 1 |
| 63 | ENI2C | 0 | 1 | 1 | 0 | 1 | 1 |
| register | ENI2C1 | - | {0} | {1} | - | {0} | {1} |
| 2 | RF_IN/OSCSEL0 | OSCSEL0 | OSCSEL0 | OSCSEL0 | RF_IN | RF_IN | RF_IN |
| 44 | RF_OUT/OSCSEL1 | OSCSEL1 | OSCSEL1 | OSCSEL1 | REFIN | REFIN | REFIN |
| 4 | SDA0/OBUF | OBUF | SDA0 | SDA0 | OBUF | SDA0 | SDA0 |
| 5 | SCL0/FILTSEL0 | FILTSEL0 | SCL0 | SCL0 | FILTSEL0 | SCL0 | SCL0 |
| 64 | CTSEL_I2C/FILTSEL1 | FILTSEL1 | CTSEL_I2C | CTSEL_I2C | FILTSEL1 | CTSEL_I2C | CTSEL_I2C |
| 6 | D0/D31/SDA1 | D0 | D0 | SDA1 | D0 | D0 | SDA1 |
| 7 | D1/D30/SCL1 | D1 | D1 | SCL1 | D1 | D1 | SCL1 |
| [*1] | D2/D29-D31/D0 | D2-D32 | D2-D32 | D2-D32 | D2-D32 | D2-D32 | D2-D32 |

*1 Pin number：8-15、17-22、26-33、35-42

**Table 2 Secondary chip mode pin sharing**

| Pin number | Primary chip/Secondary chip | Secondary chip mode | | | | | |
|---|---|---|---|---|---|---|---|
| | Sampling clock | Internal OSC | | | External input | | |
| | 2-wire serial (SDA0/SCL0) | Disable | Enable | Enable | Disable | Enable | Enable |
| | 2-wire serial (SDA1/SCL1) | | Disable | | | Disable | |
| 1 | PSSEL | 1 | 1 | 1 | 1 | 1 | 1 |
| 45 | REFEN | 0 | 0 | 0 | 1 | 1 | 1 |
| 63 | ENI2C | 0 | 1 | 1 | 0 | 1 | 1 |
| register | ENI2C1 | - | {0} | {1} | - | {0} | {1} |
| 2 | RF_IN/OSCSEL0 | OSCSEL0 | OSCSEL0 | OSCSEL0 | RF_IN | RF_IN | RF_IN |
| 44 | RF_OUT/OSCSEL1 | OSCSEL1 | OSCSEL1 | OSCSEL1 | REFIN | REFIN | REFIN |
| 4 | SDA0/OBUF | OBUF | SDA0 | SDA0 | OBUF | SDA0 | SDA0 |
| 5 | SCL0/FILTSEL0 | FILTSEL0 | SCL0 | SCL0 | FILTSEL0 | SCL0 | SCL0 |
| 64 | CTSEL_I2C/FILTSEL1 | FILTSEL1 | CTSEL_I2C | CTSEL_I2C | FILTSEL1 | CTSEL_I2C | CTSEL_I2C |
| 6 | D0/D31/SDA1 | D31 | D31 | SDA1 | D31 | D31 | SDA1 |
| 7 | D1/D30/SCL1 | D30 | D30 | SCL1 | D30 | D30 | SCL1 |
| [*1] | D2/D29-D31/D0 | D29-D0 | D29-D0 | D29-D0 | D29-D0 | D29-D0 | D29-D0 |

* 1 Pin number：8-15、17-22、26-33、35-42

Setting value with brace (ex. {0}, {1}) requires register setting by 2-wire serial interface.
See following definition in each Tables.

| |
|---|
| Setting by Pin |
| Setting by register |



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## 6. Absolute maximum rating

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply voltage (VDD,AVDD) | -0.3 | - | 4.0 | V |
| LVCMOS input voltage | -0.3 | - | VDD+0.3 | V |
| LVCMOS output voltage | -0.3 | - | VDD+0.3 | V |
| 5V tolerant Bi-directional buffer input voltage | -0.3 | - | VDD+2.5 | V |
| 5V tolerant Bi-directional buffer output voltage | -0.3 | - | VDD+2.5 | V |
| Open-drain output voltage | -0.3 | - | 4.0 | V |
| CML receiver input voltage | -0.3 | - | CAPINA+0.3 | V |
| CML transmitter output voltage | -0.3 | - | CAPINP+0.3 | V |
| Output current | -50 | - | 50 | mA |
| Storage temperature | -55 | - | 125 | °C |
| Junction temperature | - | - | 125 | °C |
| Reflow peak temperature/time | - | - | 260/10 | °C/sec |
| θja (Junction to Ambient) | 29.1 [*1] | | | °C/W |
| Ψjt (Junction to Top of package) | 1.1 [*1] | | | °C/W |
| Maximum power dissipation @+25°C | 3.4[*1] | | | W |

"Absolute maximum ratings" are those values beyond which the safety of the device cannot be guaranteed.

They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

*1: Thermal parameters are not guaranteed value. This value assists board and system level designers.

## 7. Recommended operatingconditions

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply voltage (VDD,AVDD) | 1.7 | - | 3.6 | V |
| Operating ambient temperature | -40 | - | 85 | °C |

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# 8. Electrical characteristics

## 8.1. Current consumption

| Symbol | Parameter | Type | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Idd_w1 | Normal mode current<br>Primary chip DATAWIDTH=H<br>32bit Input (Full toggle40MHz)<br>REFIN mode(80MHz) | PWR | AVDD=3.3V<br>VDD=3.3V | - | 118 | - | mA |
| | Secondary chip<br>DATAWIDTH=H<br>32bit Output (Full toggle40MHz)<br>REFIN=80MHz | | | | 197 | | |
| Idd_w2 | Normal mode current<br>Primary chip DATAWIDTH=H<br>27bit Input (Full toggle40MHz)<br>5bit Output (Full toggle40MHz)<br>REFIN=80MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 126 | - | mA |
| | Normal mode current<br>Secondary chip<br>DATAWIDTH=H<br>5bit Input (Full toggle40MHz)<br>27bit Output (Full toggle40MHz)<br>REFIN=80MHz | | | | 184 | | |
| Idd_w3 | Normal mode current<br>Primary chip DATAWIDTH=H<br>10bitInput (Full toggle20MHz)<br>10bitOutput (Full toggle20MHz)<br>REFIN=80MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 128 | - | mA |
| | Normal mode current<br>Secondary chip<br>DATAWIDTH=H<br>10bitInput (Full toggle20MHz)<br>10bitOutput (Full toggle20MHz)<br>REFIN=80MHz | | | | 128 | | |
| Idd_w4 | Normal mode current<br>Primary chip DATAWIDTH=H<br>16bitInput (Full toggle1MHz)<br>16bitOutput (Full toggle1MHz)<br>REFIN=80MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 114 | - | mA |
| | Normal mode current<br>Secondary chip<br>DATAWIDTH=H<br>16bitInput (Full toggle1MHz)<br>16bitOutput (Full toggle1MHz)<br>REFIN=80MHz | | | | 114 | | |

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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Idd_w5 | Normal mode current<br>Primary chip DATAWIDTH=H<br>16bit Input (Full toggle1MHz)<br>16bit Output (Full toggle1MHz)<br>REFIN=40MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 85 | - | mA |
| | Normal mode current<br>Secondary chip DATAWIDTH=H<br>16bit Input (Full toggle1MHz)<br>16bit Output (Full toggle1MHz)<br>REFIN=40MHz | | | | 85 | | |
| Idd_w6 | Normal mode current<br>Primary chip DATAWIDTH=L<br>16bit Input (Full toggle1MHz)<br>16bit Output (Full toggle1MHz)<br>REFIN=80MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 87 | - | mA |
| | Normal mode current<br>Secondary chip DATAWIDTH=L<br>16bit Input (Full toggle1MHz)<br>16bit Output (Full toggle1MHz)<br>REFIN=80MHz | | | | 87 | | |
| Idd_w7 | Normal mode current<br>Primary chip DATAWIDTH=L<br>16bit Input (Full toggle66.67MHz)<br>16bit Output (Full toggle66.67MHz)<br>REFIN=133.34MHz | PWR | AVDD=3.3V<br>VDD=3.3V | - | 190 | - | mA |
| | Normal mode current<br>Secondary chip DATAWIDTH=L<br>16bit Input (Full toggle66.67MHz)<br>16bit Output (Full toggle66.67MHz)<br>REFIN=133.34MHz | | | | 190 | | |
| Idd_w8 | Standby mode current<br>8bit Input(Full toggle6.25kHz) | PWR | AVDD=3.3V<br>VDD=3.3V | - | 7 | - | mA |
| | Standby mode current<br>Secondary chip DATAWIDTH=L<br>8bit Output(Full toggle6.25kHz) | | | | 7 | | |
| Idd_w9 | Standby mode current<br>8bit Output(Full toggle6.25kHz) | PWR | AVDD=3.3V<br>VDD=3.3V | - | 7 | - | mA |
| | Standby mode current<br>Secondary _DATAWIDTH=L<br>8bit Input(Full toggle6.25kHz) | | | | 7 | | |

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## 8.2. LVCMOS/Analog input DC specifications

| Symbol | Parameter | Type | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VIH | High level input voltage | B,BT, BO | 1.7V≦VDD<2.0V | 0.65 VDD | - | VDD | V |
| | | | 2.0V≦VDD<3.0V | 0.70 VDD | - | VDD | V |
| | | | 3.0V≦VDD≦ 3.6V | 2.0 | - | VDD | V |
| | | IL,BL | 1.7V≦VDD≦ 3.6V | 0.70 VDD | - | VDD | V |
| VIL | Low level input voltage | B,BT, BO | 1.7V≦VDD<2.0V | 0 | - | 0.35 VDD | V |
| | | | 2.0V≦VDD<3.0V | 0 | - | 0.30 VDD | V |
| | | | 3.0V≦VDD≦ 3.6V | 0 | - | 0.8 | V |
| | | IL,BL | 1.7V≦VDD≦ 3.6V | 0 | - | 0.30 VDD | V |
| | | AI | 1.7V≦VDD≦ 3.6V | 0 | - | 0.15 VDD | V |
| VOH | High level output voltage | B,BT, BL | 1.7V≦VDD<2.0V TTLDRV(register) ={0} IOH=-2mA | VDD - 0.30 | - | VDD | V |
| | | | 1.7V≦VDD<2.0V TTLDRV(register) ={1} IOH=-4mA | VDD - 0.45 | - | VDD | V |
| | | | 2.0V≦VDD≦ 3.6V IOH=-4mA | VDD - 0.45 | - | VDD | V |
| VOL | Low level output voltage*1 | B,BT, BL | 1.7V≦VDD<2.0V TTLDRV(register) ={0} IOL=2mA | 0 | - | 0.30 | V |
| | | | 1.7V≦VDD<2.0V TTLDRV(register) ={1} IOL=4mA | 0 | - | 0.45 | V |
| | | | 2.0V≦VDD≦ 3.6V IOL=4mA | 0 | - | 0.45 | V |
| | | BO | 1.7V≦VDD≦ 3.6V IOL=2mA | 0 | - | 0.27 | V |
| IIH | Input leak current High | IL | VIN=VDD | -10 | - | 10 | uA |
| IIL | Input leak current Low | IL | VIN=0V | -10 | - | 10 | uA |
| IOZH | Output leak current High in Hi-Z | B,BT, BL,BO | VIN=VDD | -10 | - | 10 | uA |
| IOZL | Output leak current Low in Hi-Z | B,BT, BL,BO | VIN=0V | -10 | - | 10 | uA |

AI: Analog Input buffer
IL: Low speed schmitt trigger LVCMOS Input buffer
B: LVCMOS Bi-directional buffer
BO: Open-drain LVCMOS Bi-directional buffer
BL: Low speed 5V tolerant schmitt trigger LVCMOS Bi-directional buffer
BT: Low speed 5V tolerant LVCMOS Bi-directional buffer

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### 8.3. LVCMOS AC characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| tRSN | RESETN low time | - | | 3 | - | - | us |
| tTCIP | REFIN period | DATA_WIDTH(pin)=0<br>1.7V≦VDD≦2.25V and TTLDRV(register)={0} | | 10 | - | 66.6 | ns |
| | | DATA_WIDTH(pin)=0<br>2.25V≦VDD≦3.6V or TTLDRV(register)={1} | | 7.5 | - | 66.6 | ns |
| | | DATA_WIDTH（pin）=1 | | 12.5 | - | 111 | ns |
| tTCH | REFIN High time | - | | 0.35 tTCIP | 0.5 tTCIP | 0.65 tTCIP | ns |
| tTCL | REFIN Low time | - | | 0.35 tTCIP | 0.5 tTCIP | 0.65 tTCIP | ns |
| tTS | Data input setup to REFIN | Pin type: B | 1.7V≦VDD≦3.6V | 2.0 | - | - | ns |
| | | Pin type: BT | 1.7V≦VDD<2.25V | 25 | - | - | ns |
| | | | 2.25V≦VDD≦2.75V | 2.5 | - | - | ns |
| | | | 2.75V<VDD≦3.6V | 2.0 | - | - | ns |
| tTH | Data input hold to REFIN | - | | 1.0 | - | - | ns |
| tTPD | Power on to RESETN high delay | - | | 0 | - | - | ns |
| tOSC | Internal oscillator clock period | OSCSEL1(pin)=0<br>OSCSEL0(pin)=0 | | 41.67 | 50 | 62.5 | ns |
| | | OSCSEL1(pin)=1<br>OSCSEL0(pin)=0 | | 20.84 | 25 | 31.25 | ns |
| | | OSCSEL1(pin)=1<br>OSCSEL0(pin)=1 | | 10.42 | 12.5 | 15.62 | ns |
| tDCP | Data sampling clock period | REFEN(pin)=0 | | - | tOSC | - | ns |
| | | REFEN(pin)=1 | | - | tTCIP | - | ns |
| tFLTCK | Noise filter clock period | REFEN(pin)=0 | | 10.42 | 12.5 | 15.62 | ns |
| | | REFEN(pin)=1 | | - | tTCIP | - | ns |
| tTCD | Input data to output data delay<br>Note : Transmission delay between primary and secondary chips is not included. | FILTSEL1(pin)=0<br>FILTSEL0(pin)=0 | | 36.2 tDCP | - | 61.3 tDCP | ns |
| | | FILTSEL1(pin)=0<br>FILTSEL0(pin)=1 | | 46 tDCP | - | 73.7 tDCP | ns |
| | | FILTSEL1(pin)=1<br>FILTSEL0(pin)=0 | | 53.4 tDCP | - | 82.1 tDCP | ns |
| | | FILTSEL1(pin)=1<br>FILTSEL0(pin)=1 | | 68.1 tDCP | - | 100.5 tDCP | ns |
| tRCP | REFOUT period | - | | - | tDCP | - | ns |
| tRCH | REFOUT high time | - | | - | 0.5 tDCP | - | ns |
| tRCL | REFOUT low time | - | | - | 0.5 tDCP | - | ns |
| tDOUT | Data output period | - | | - | tDCP | - | ns |
| tRS | Data output setup to REFOUT | - | | 0.45 tDCP - 0.675 | - | - | ns |
| tRH | Data output hold to REFOUT | - | | 0.45 tDCP - 2.175 | - | - | ns |
| tRRDY | RESETN high to READY high delay | - | | - | - | 1 | ms |
| tNRDY | STANDBY low to READY high delay | - | | 0 | - | 10 | ms |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tSRDY | STANDBY high to READY high delay | - | 0 | - | 10 | ms |
| tTLH | Clock and data output low to high transition time | Clock , TTLDRV(register)={0} | - | - | 2.1 | ns |
| | | Data(Pin type=B) , TTLDRV(register)={0} | - | - | 4.2 | ns |
| | | Data(Pin type=BT) , TTLDRV(register)={0} | - | - | 5.9 | ns |
| | | Clock , TTLDRV(register)={1} | - | - | 1.1 | ns |
| | | Data(Pin type=B) , TTLDRV(register)={1} | - | - | 2.3 | ns |
| | | Data(Pin type=BT) , TTLDRV(register)={1} | - | - | 3.0 | ns |
| tTHL | Clock and data output high to low transition time | Clock , TTLDRV(register)={0} | - | - | 2.1 | ns |
| | | Data(Pin type=B) , TTLDRV(register)={0} | - | - | 4.3 | ns |
| | | Data(Pin type=BT) , TTLDRV(register)={0} | - | - | 6.1 | ns |
| | | Clock , TTLDRV(register)={1} | - | - | 1.1 | ns |
| | | Data(Pin type=B) , TTLDRV(register)={1} | - | - | 2.2 | ns |
| | | Data(Pin type=BT) , TTLDRV(register)={1} | - | - | 3.0 | ns |

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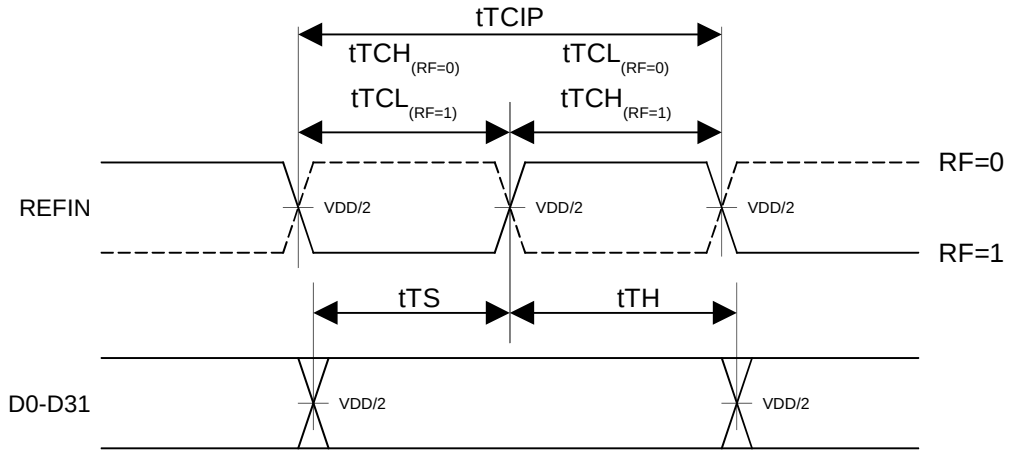


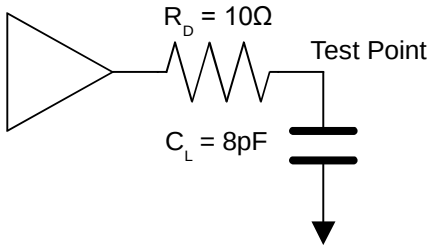


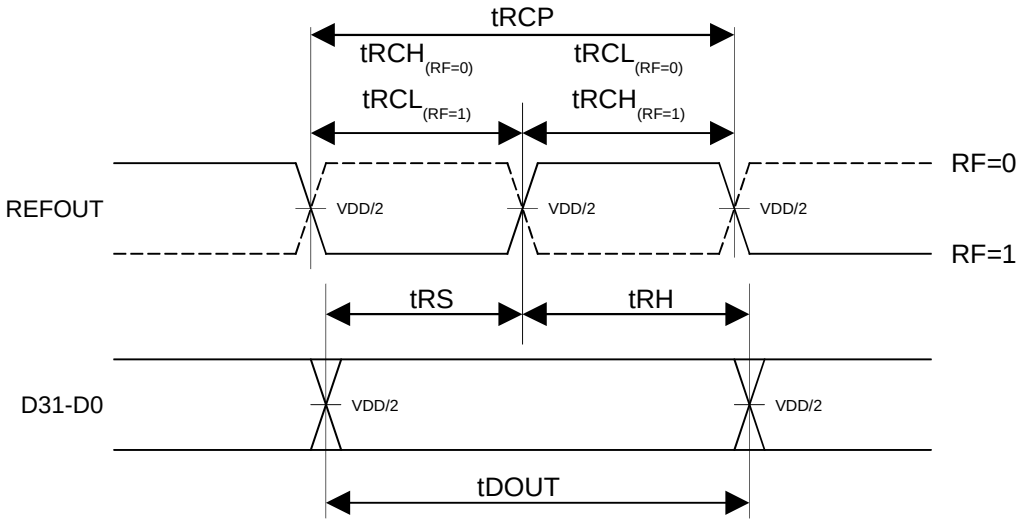




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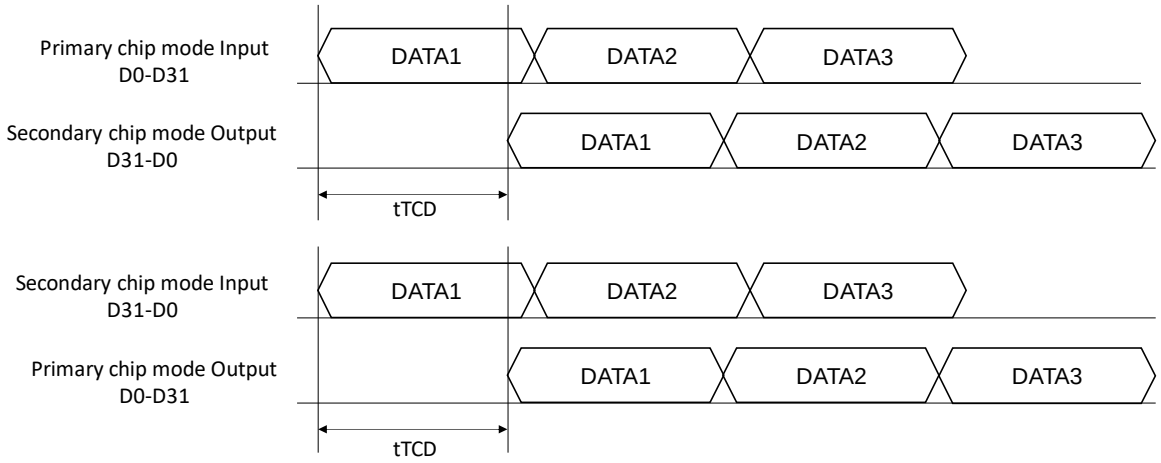




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### 8.4. CML DC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VTOD | CML differential output peak to peak signal | CMLDRV[1:0](register)={00} | 266 | 400 | 534 | mVpp |
| | | CMLDRV[1:0](register)={01} (default) | 400 | 600 | 800 | mVpp |
| | | CMLDRV[1:0](register)={10} | 600 | 800 | 1000 | mVpp |
| PRE | CML pre-emphasis level | PRE(register)={0} (default) | - | 0 | - | dB |
| | | PRE(register)={1} CMLDRV[1:0](register)={00} | - | 6 | - | dB |
| | | PRE(register)={1} CMLDRV[1:0](register)={01} | - | 3.52 | - | dB |
| VTOC | CML common mode output voltage | PRE(register)={0} (default) | - | 1200 - 0.5 VTOD | - | mV |
| | | PRE(register)={1} CMLDRV[1:0](register)={00} | - | 1200 - VTOD | - | mV |
| | | PRE(register)={1} CMLDRV[1:0](register)={01} | - | 1200 - 0.75 VTOD | - | mV |
| ITOH | CML output leak current high | RESETN(pin)=0 TXP/N(pin)=CAPINA(pin) | -30 | - | 30 | uA |
| ITOS | CML output short current | RESETN(pin)=0 TXP/N(pin)=0V | -80 | - | - | mA |
| VRTH | CML differential input high threshold | - | - | - | 50 | mV |
| VRTL | CML differential input low threshold | - | -50 | - | - | mV |
| IRIH | CML input leak current high | RESETN(pin)=0 RXP/N(pin)=CAPINA(pin) | -10 | - | 10 | uA |
| IRIL | CML input short current low | RESETN(pin)=0 RXP/N(pin)=0V | -10 | - | 10 | uA |
| IRRIH | CML input current high | RXP/N(pin)=CAPINA(pin) | - | - | 2 | mA |
| IRRIL | CML input current low | RXP/N(pin)=0V | -6 | - | - | mA |
| RRIN | CML differential input resistance | - | 80 | 100 | 120 | Ω |

### 8.5. CML AC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| tTRF | CML output rise and fall time (20%-80%) | - | 50 | - | 150 | ps |
| tTPLL0 | RESETN=H to CML output delay | - | - | - | 1 | ms |
| tTPLL1 | RESETN=L to CML output high fix | - | - | - | 200 | ns |
| tTNP0 | READY=L to training pattern output delay | - | - | - | 100 | us |
| tTBIT | Output unit interval | DATA_WIDTH(pin)=0 | - | tDCP÷30 | - | ns |
| | | DATA_WIDTH(pin)=1 | - | tDCP÷50 | - | ns |
| tRBIT | Input unit interval | - | 250 | - | 2222 | ps |

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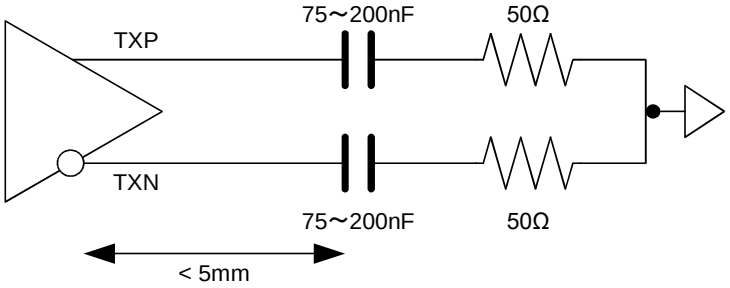


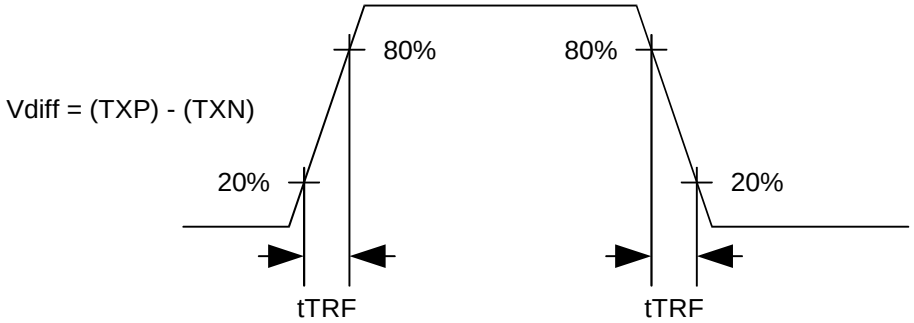


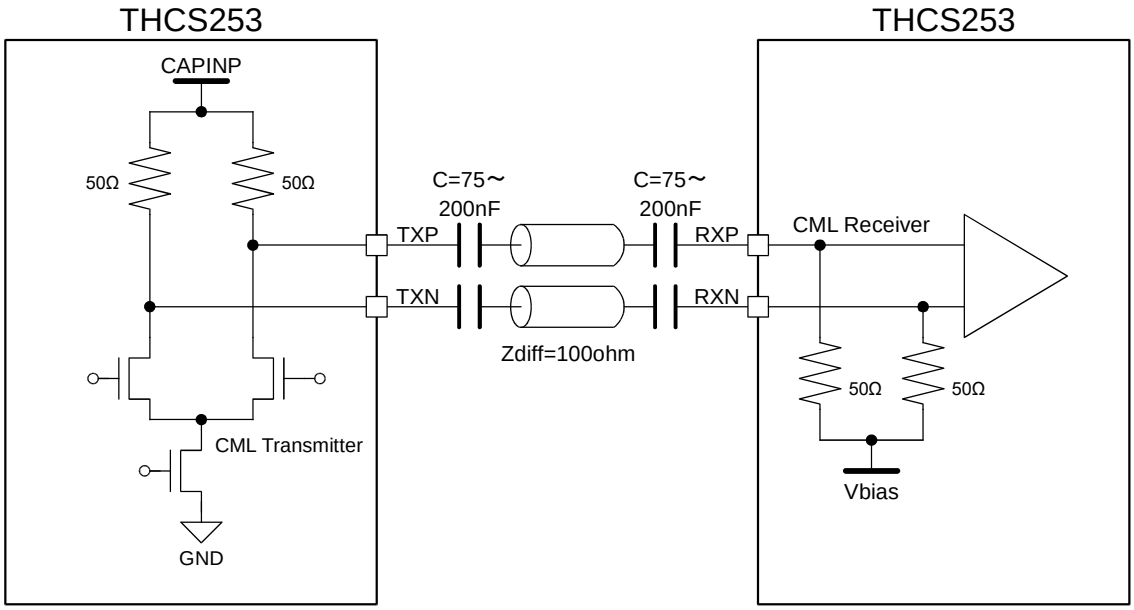




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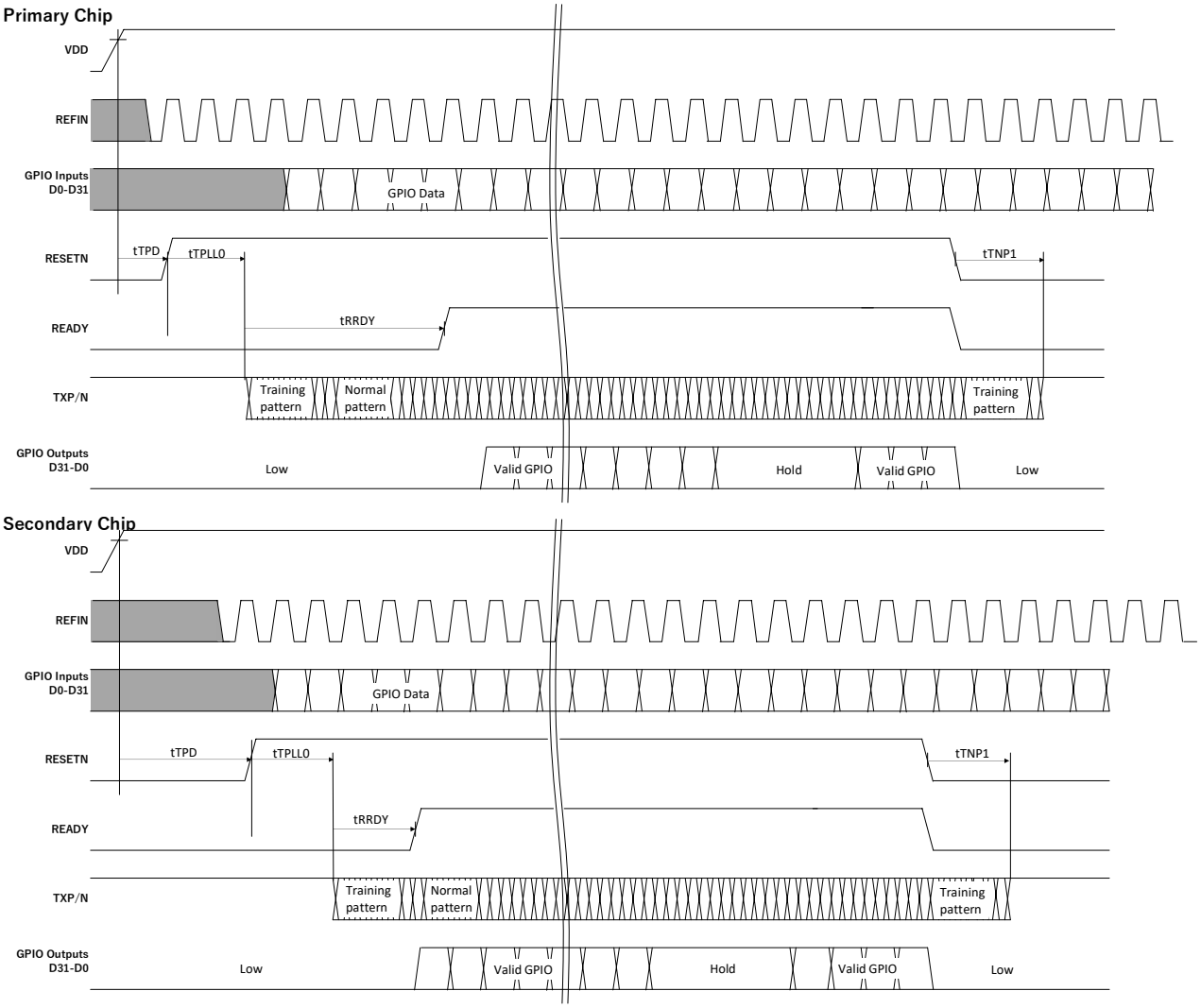
ASYNC mode

Training pattern output from the primary chip requires RESET=1 and REFIN frequency*1 input.

Training pattern output from the secondary chip requires RESET=1 and REFIN frequency*1 input as well as training pattern receive from the primary chip.

*1: In internal oscillator clock mode with REFEN=0, RESET=1 only.



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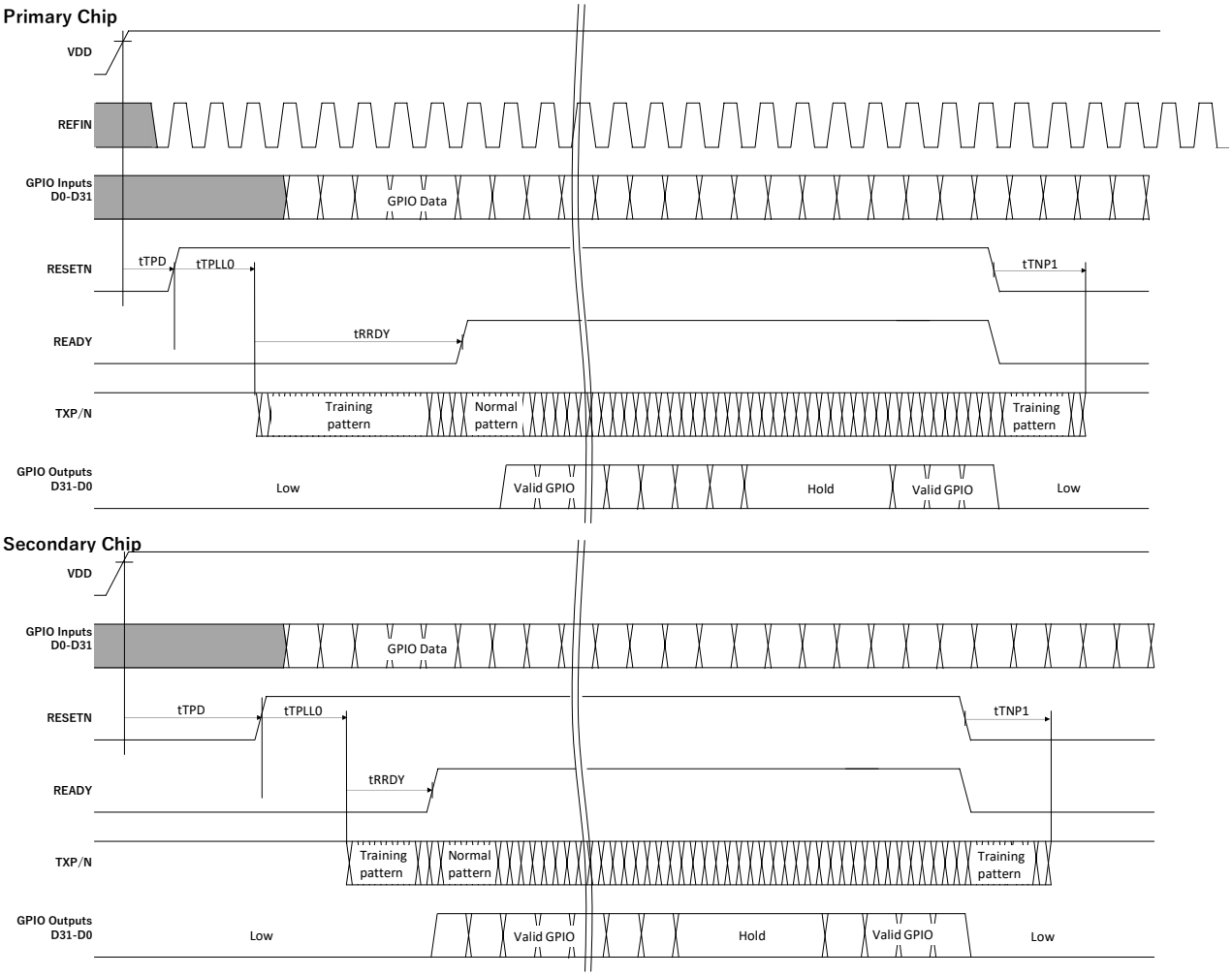
SYNC mode



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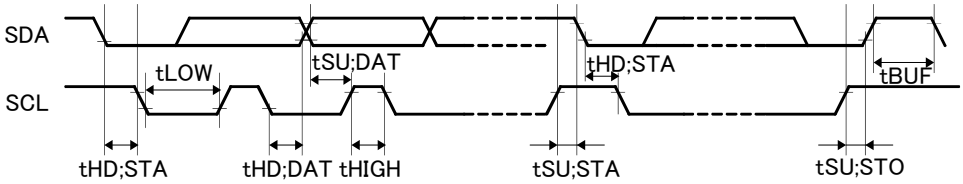
### 8.6. 2-wire serial interface DC/AC characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIL | Low level input voltage | - | 0 | - | 0.30 VDD | V |
| VIH | High level input voltage | - | 0.7 VDD | - | - | V |
| VOL | Low level output voltage | 1.7V≦VDD≦3.6V IOL=2mA | 0.00 | - | 0.26 | V |
| $I_i$ | Input current each I/O pin | - | -10 | - | +10 | uA |
| fSCL | Input current each I/O pin | - | 0 | - | 1000 | kHz |
| tHD;STA | Hold time (repeated) START condition | fSCL>400kHz | 0.46 | - | - | us |
| | | fSCL≦400kHz | 0.8 | - | - | us |
| tLOW | Low period of the SCL clock | fSCL>400kHz | 0.5 | - | - | us |
| | | fSCL≦400kHz | 1.3 | - | - | us |
| tHIGH | High period of the SCL clock | fSCL>400kHz | 0.26 | - | - | us |
| | | fSCL≦400kHz | 0.6 | - | - | us |
| tHD;DAT | Data hold time | - | 0 | - | - | us |
| tSU;DAT | Data setup time | fSCL>400kHz | 50 | - | - | ns |
| | | fSCL≦400kHz | 100 | - | - | ns |
| tSU;STO | Setup time for STOP condition | fSCL>400kHz | 0.26 | - | - | us |
| | | fSCL≦400kHz | 0.6 | - | - | us |
| tBUF | Bus free time between a STOP and START condition | fSCL>400kHz | 0.5 | - | - | us |
| | | fSCL≦400kHz | 1.3 | - | - | us |
| tr | Rise time of both SDA and SCL signals | - | - | - | 300 | ns |
| tf | Fall time of both SDA and SCL signals | - | - | - | 300 | ns |



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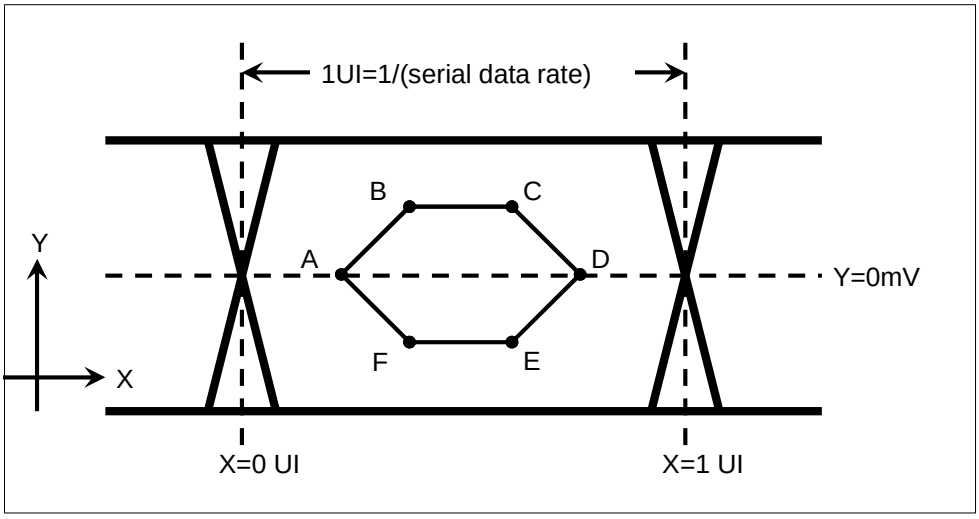
# 9. CML Line diagram

## 9.1. CML input diagram




| | X[UI] | Y[mV] |
|---|---|---|
| A | 0.25 | 0 |
| B | 0.3 | 50 |
| C | 0.7 | 50 |
| D | 0.75 | 0 |
| E | 0.7 | -50 |
| F | 0.3 | -50 |



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# 10. Function

## 10.1. Function overview

The THCS253 integrates a high-speed CML serializer and deserializer on a single chip. It is capable of aggregating and de-aggregating up to 32-bit parallel GPIO signals and a 2-wire serial interface with full-duplex communication using two pairs of differential signals with a minimum of external components. Low-power standby mode supports up to 8-bit low-speed GPIO signals and 2-wire serial interface. In addition, the internal oscillator mode does not require an external clock generator such as a crystal oscillator. Two THCS253s (one pair) can be used to monitor and control peripheral devices via a 2-wire serial interface or GPIO. In the event of a communication error, the GPIO signal is held and an interrupt signal is used to notify the user.

## 10.2. Power supply

### 10.2.1. Internal regulator output/input function (CAPOUT, CAPINA, CAPINP)

The internal regulator generates 1.2V (CAPOUT) for internal use only. Do not use for other external loads. CAPOUT should be bypassed to GND with 10uF as a power supply pin; AVDD should be bypassed to GND with 10uF or more.

CAPINP and CAPINA supply the reference voltage for the internal analog circuitry. To reduce high frequency noise, CAPINP/CAPINA should be bypassed to GND with 0.1uF as a power supply pin. CAPOUT, CAPINA and CAPINP should be wired as shown in the figure below.

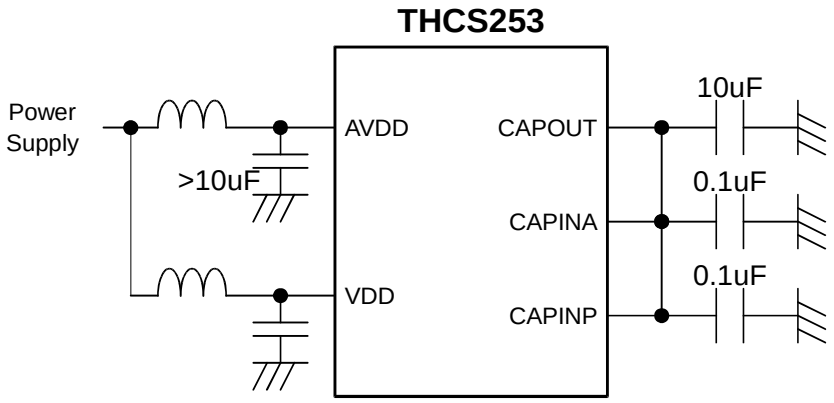


**Figure 1 Connection of CAPOUT, CAPINA, CAPINP and decoupling capacitor**



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### 10.3. Chip Operating state

**Basic operating states related to power consumption of the THCS253, such as reset, OE, and standby.**

**Table 3 Operating mode setting**

| Operating mode | Setting | | | | Description |
|---|---|---|---|---|---|
| | RESETN (pin) | ENI2C0 (pin) | STANDBY (register) | OE *1 (pin) | |
| RESET | 0 | - | - | - | Chip reset<br>2-wire serial interface disable<br>All outputs are Hi-Z |
| Normal operation (2-wire serial interface Disable) | 1 | 0 | 0 | 0 | Normal operation<br>2-wire serial interface disable<br>All outputs are Hi-Z |
| | 1 | 0 | 0 | 1 | Normal operation<br>2-wire serial interface disable<br>GPIO normal operation |
| Normal operation (2-wire serial interface enable) | 1 | 1 | {0} | 0 | Normal operation<br>2-wire serial interface enable<br>All outputs are Hi-Z |
| | 1 | 1 | {0} | 1 | Normal operation<br>2-wire serial interface enable<br>GPIO normal operation |
| Standby | 1 | 1 | {1} | 0 | Low power consumption/low frequency sampling rate operation<br>2-wire serial interface enable<br>GPIO 8bit Hi-Z |
| | 1 | 1 | {1} | 1 | Low power consumption/low frequency sampling rate operation<br>2-wire serial interface enable<br>GPIO 8bit low speed communication Enable |

*1 When OVERRIDE_OEN(register) = {1} is selected, the OE(pin) state is disabled.

### 10.4. Chip operation mode

#### 10.4.1. Chip configuration

The THCS253 has two modes, Primary chip mode and Secondary chip mode, which are selected by the PSSEL pin. The THCS253 is connected and used in a pair of Primary chip mode t and Secondary chip mode.

**Table 4 Primary chip and Secondary chip selection**

| PSSEL (pin) | Description |
|---|---|
| 0 | Primary chip mode |
| 1 | Secondary chip mode |

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### 10.4.2. Operating clock mode select

The THCS253 selects synchronous or asynchronous operation of downstream and upstream by the SYNCEN pin selection in the secondary chip mode.

**Synchronous mode**

The primary chip samples data by its own clock. The secondary chip samples data using the CDR (Clock Data Recovery) clock generated by the deserializer, and the downstream and upstream operate synchronously.

**Asynchronous mode**

Data sampling is performed with the clocks of both Primary chip and Secondary chip, and downstream and upstream operate asynchronously.

**Table 5 Downstream / Upstream synchronous setting**

| SYNCEN(pin) of Secondary chip | Description |
|---|---|
| 0 | Asynchronous mode : Operates at both clocks |
| 1 | Synchronous mode : Operates at the clock of the primary chip |

### 10.4.3. Operating clock select

THCS253 allows selection of the clock used to input data sampling and drive the serializer/deserializer.

**Table 6 Operating clock select**

| REFEN(pin) | Description |
|---|---|
| 0 | Internal Oscillator Clock Mode：20M/40M/80MHz |
| 1 | External reference clock mode：9-133MHz |

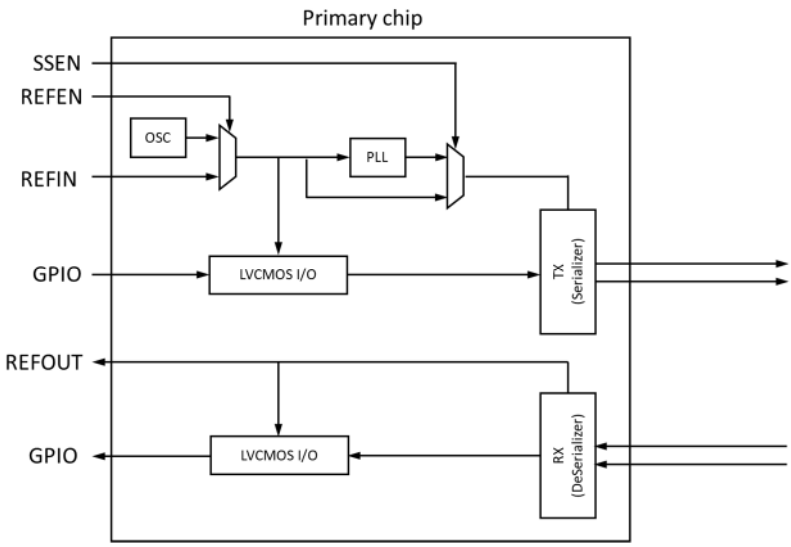


**Figure 2 Clock Tree diagram of Primary chip**



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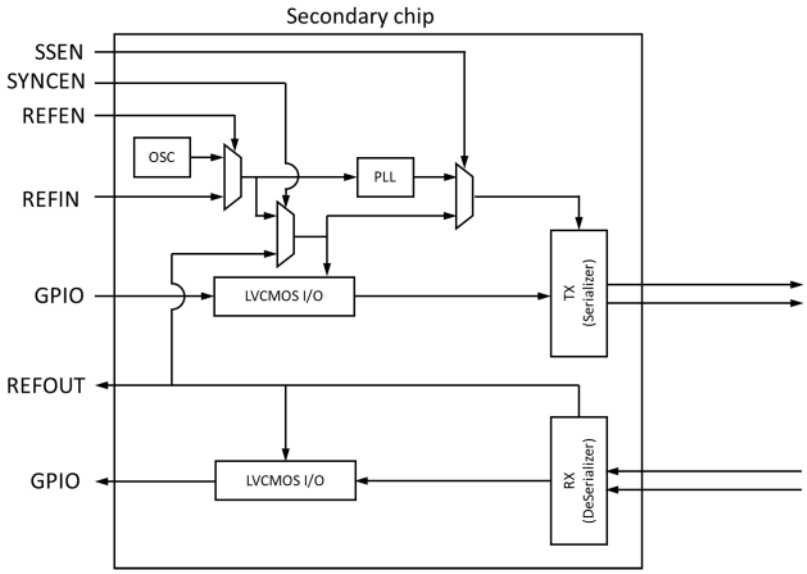


**Figure 3 Clock Tree diagram of Secondary chip**



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### 10.4.4. Combination of operating modes

Transmit operation of the THCS253 is determined by the combination of the PSSEL, REFEN, and SYNCEN pins.

**Asynchronous mode(SYNCEN=0 of secondary chip)／External reference clock mode(REFEN=1)**

Data sampling and driven by the REFIN input of each primary chip/secondary chip.

Different frequencies can be input to the Primary chip and Secondary chip.

Downstream and upstream can be taken and output synchronized to their respective REFIN inputs.

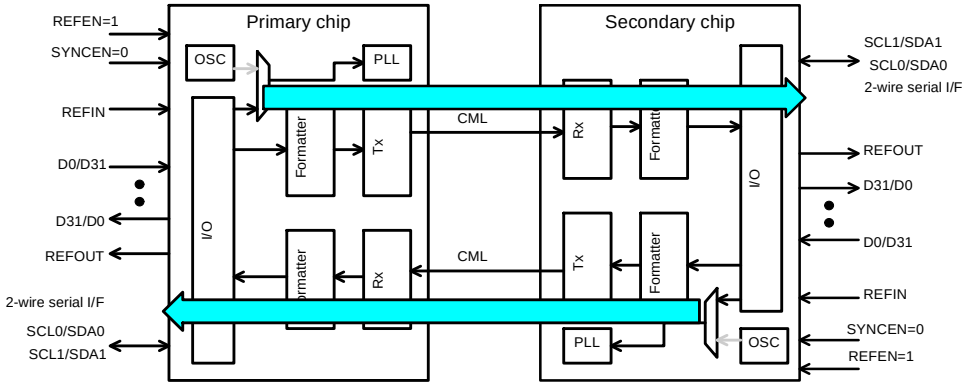


**Figure 4 ASYNC_MODE / Ext.REF_MODE Block diagram**

**Asynchronous mode(SYNCEN=0 of secondary chip)／Internal oscillator clock mode(REFEN=0)**

Data sampling and driven by the internal oscillator clock of each primary chip/secondary chip.

Selectable from 20/40/80MHz by OSCSEL [1:0] pin setting.

Different frequencies can be selected for the internal oscillator of the Primary chip/Secondary chip.

All input data is asynchronous acquisition because of sampling by the internal oscillator. Output data is synchronized with REFOUT.

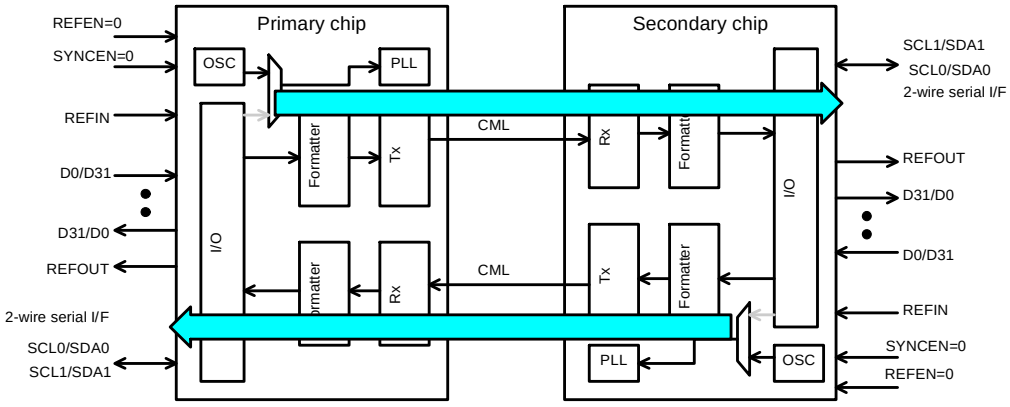


**Figure 5 ASYNC_MODE / Int.OSC_MODE Block diagram**



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**Asynchronous mode(SYNCEN=0 of secondary chip)／External reference clock mode(REFEN=1) and Internal oscillator clock mode(REFEN=0)**

Data sampling and driven by the REFIN input of either the Primary chip or the Secondary chip.

Either the primary chip/secondary chip is driven and sampled by the internal oscillator.

Selectable from 20/40/80MHz by OSCSEL [1:0] pin setting.

The external reference clock drive side can be synchronized with the REFIN input for take-up and output.

The internal oscillator drive side is all asynchronous acquisition. Output data is synchronized with REFOUT.

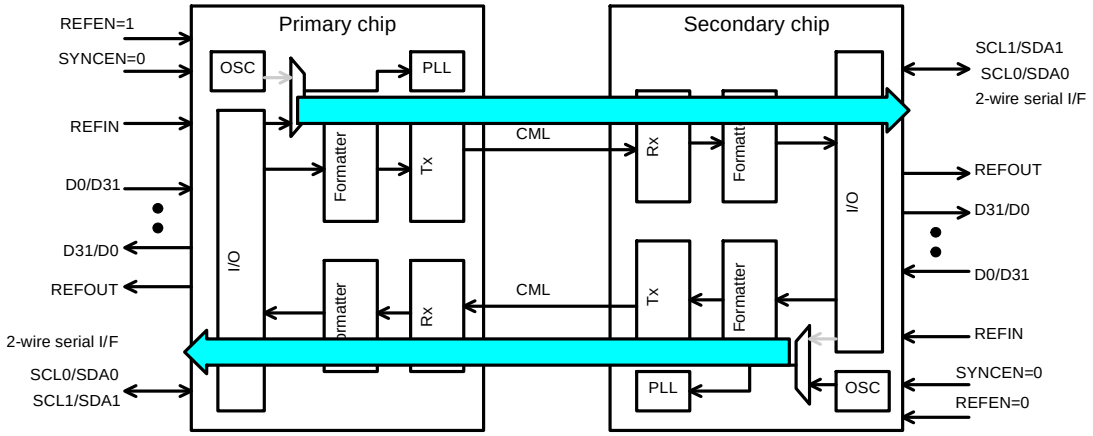


**Figure 6 ASYNC_MODE / Ext.REF_MODE & Int.OSC_MODE Block diagram**

**Synchronous mode(SYNCEN=1 of secondary chip)／External reference clock mode(REFEN=1)**

Driven and data sampling only by REFIN to the primary chip. (Input to REFIN of the secondary chip is prohibited)

Secondary chip uses the clock regenerated by the receiver for data sampling and driving the transmitter.

Downlink take-up and output synchronized with REFIN input.

The uplink is asynchronous acquisition due to sampling with the CDR-generated clock.

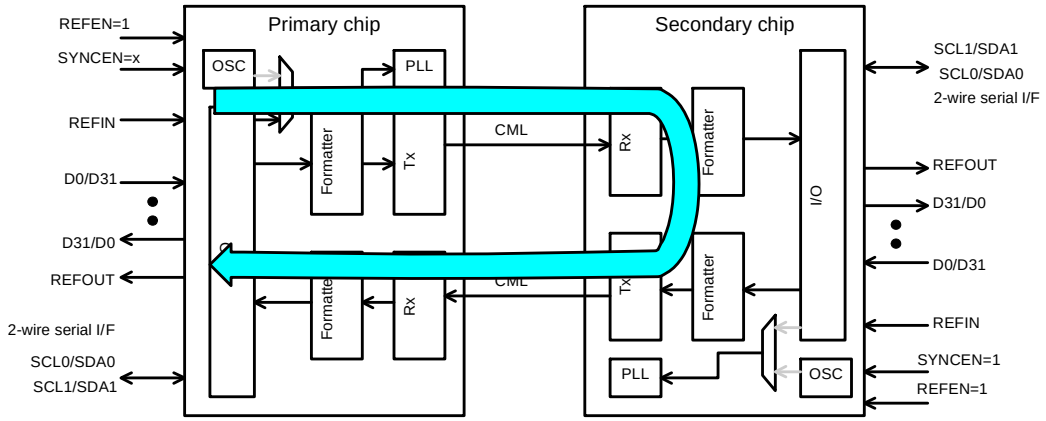


**Figure 7 SYNC_MODE / Ext.REF_MODE Block diagram**



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**Synchronous mode(SYNCEN=1 of secondary chip)／Internal oscillator clock mode(REFEN=0)**

It is sampled and driven by the built-in oscillator of the primary chip.

Selectable from 20/40/80MHz by OSCSEL [1:0] pin setting.

Secondary chip uses the clock regenerated by the receiver for data sampling and driving the transmitter.

All input data is asynchronous acquisition because of sampling by the internal oscillator. Output data is synchronized with REFOUT.

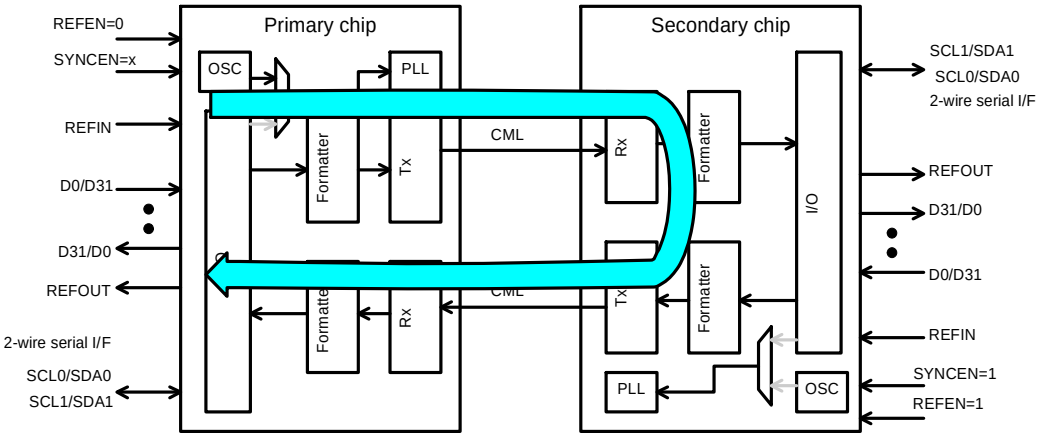


**Figure 8 SYNC_MODE / Int.OSC_MODE Block diagram**



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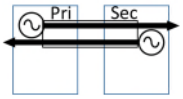
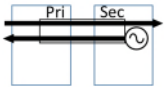
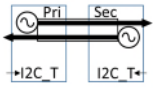
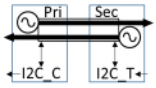
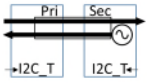
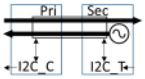
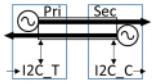
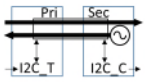
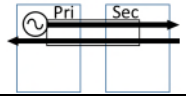
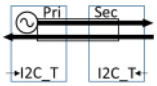
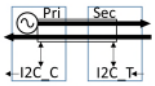
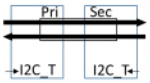
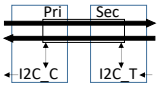
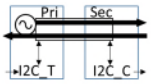
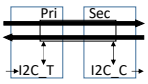
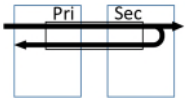
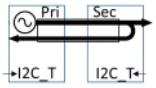
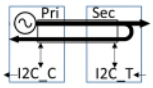
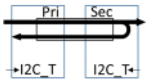
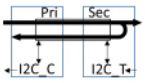
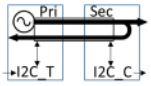
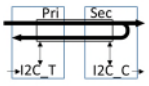
## 10.5. Pin setting and combination of chip mode

The following is a list of modes that can be combined between Primary chip and Secondary chip.

**Table 7 Primary Chip / Secondary Chip list of pair combination**

| | | | PSSEL=0 : Primary chip ﾓｰﾄﾞ（Pri） | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | REFEN | ENI2C | CTSEL_I2C | REFEN | ENI2C | CTSEL_I2C | REFEN | ENI2C | CTSEL_I2C | REFEN | ENI2C | CTSEL_I2C | REFEN | ENI2C | CTSEL_I2C | REFEN | ENI2C | CTSEL_I2C |
| | | | 0 | 0 | - | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | - | 1 | 1 | 0 | 1 | 1 | 1 |
| PSSEL=1 Secondary chip ﾓｰﾄﾞ（Sec） | SYNCEN | 0 |  | Prohibition | | Prohibition | | |  | Prohibition | | Prohibition | | | Prohibition | | | | | |
| | REFEN | 0 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 0 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | - | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 0 | Prohibition | | |  | | |  | | | Prohibition | | |  | | |  | | |
| | REFEN | 0 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 0 | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 0 | Prohibition | | |  | | | N/A | | | Prohibition | | |  | | | N/A | | |
| | REFEN | 0 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 1 | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 0 |  | | | Prohibition | | | Prohibition | | | | | | Prohibition | | | Prohibition | | |
| | REFEN | 1 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 0 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | - | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 0 | Prohibition | | |  | | |  | | | Prohibition | | |  | | |  | | |
| | REFEN | 1 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 0 | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 0 | Prohibition | | |  | | | N/A | | | Prohibition | | |  | | | N/A | | |
| | REFEN | 1 | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 1 | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 1 | | | | 禁止 | | | 禁止 | | |  | | | Prohibition | | | Prohibition | | |
| | REFEN | - | | | | | | | | | | | | | | | | | | |
| | ENI2C | 0 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | - | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 1 | Prohibition | | |  | | |  | | | Prohibition | | |  | | |  | | |
| | REFEN | - | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 0 | | | | | | | | | | | | | | | | | | |
| | SYNCEN | 1 | Prohibition | | |  | | | N/A | | | Prohibition | | |  | | | N/A | | |
| | REFEN | - | | | | | | | | | | | | | | | | | | |
| | ENI2C | 1 | | | | | | | | | | | | | | | | | | |
| | CTSEL_I2C | 1 | | | | | | | | | | | | | | | | | | |



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### 10.6. Byte mode and frequency range

The THCS253 switches between transmitter and receiver operating byte modes (3 bytes or 5 bytes) by selecting DATA_WIDTH (pin). The external reference clock frequency in each byte mode with REFEN (pin) = 1 and the operating frequency with OSCSEL [1:0] (pin) setting when REFEN (pin) = 0 are shown below.

**Table 8 DATAWIDTH select and external reference clock frequency range**

| DATA_WIDTH (pin) | REFIN frequency range | CML data rate |
|---|---|---|
| 0 | 15 - 133MHz | 450Mbps - 4Gbps |
| 1 | 9 - 80MHz | |

**Table 9 DATAWIDTH and OSCSEL[1:0] select**

| RF_OUT/OSCSEL1 (pin) | RF_IN/OSCSEL0 (pin) | DATA_WIDTH (pin) | OSC frequency | CML data rate |
|---|---|---|---|---|
| 0 | 0 | 0 | 20MHz±20% | 480Mbps - 720Mbps |
| | | 1 | | 800Mbps - 1200Mbps |
| 0 | 1 | 0 | 40MHz±20% | 960Mbps - 1440Mbps |
| | | 1 | | 1600Mbps - 2400Mbps |
| 1 | 0 | 0 | | 960Mbps - 1440Mbps |
| | | 1 | | 1600Mbps - 2400Mbps |
| 1 | 1 | 0 | 80MHz±20% | 1920Mbps - 2880Mbps |
| | | 1 | Prohibition | |

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## 10.7. 2-wire serial interface

### 10.7.1. 2-wire serial interface setting

THCS253 has two 2-wire serial interfaces (I2C0: SDA0/SCL0, I2C1: SDA1/SCL1)

**Table 10 2-wire serial interface Setting**

| ENI2C0(pin) | ENI2C1(register) | I2C0 (SCL0/SDA0) | I2C1 (SCL1/SDA1) |
|---|---|---|---|
| 0 | - | Disable | Disable |
| 1 | 0 | Enable | Disable |
| | 1 | Enable | Enable |

2-wire serial controller/target can be selected independently from Primary chip / Secondary chip mode settings.

**Table 11 2-wire serial interface controller / target select**

| CTSEL_I2C(pin) | I2C mode |
|---|---|
| 0 | Target |
| 1 | Controller |

I2C0 and I2C1 have different accessible ranges.

**Table 12 2-wire serial interface accessible range**

| | Primary chip register | Secondary chip register | Remote device register |
|---|---|---|---|
| **I2C0** | Accessible | accessible | accessible |
| **I2C1** | Unaccessible | Unaccessible | accessible |

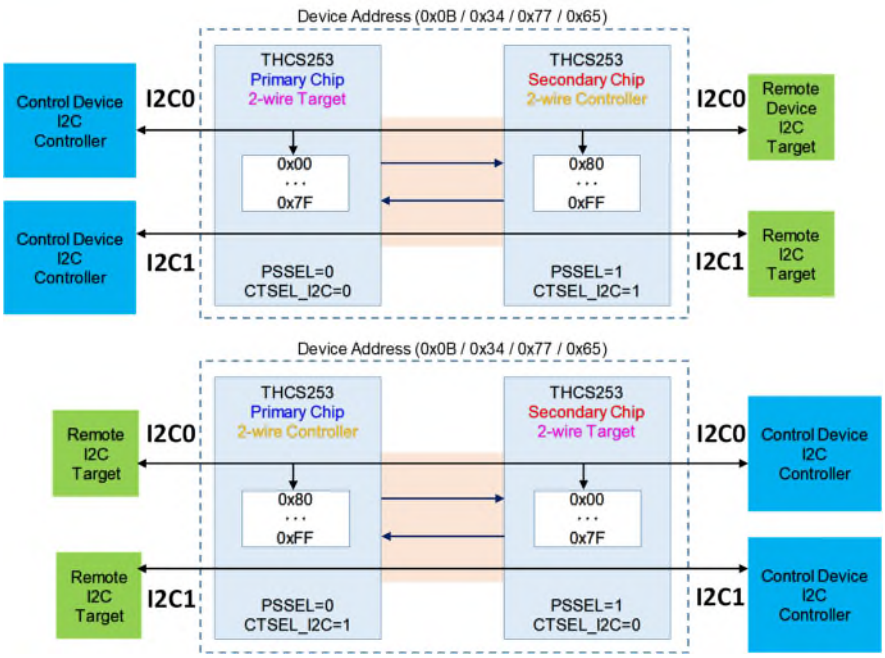


**Figure 9 2-wire serial interface accessible range**



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**Table 13 Combination of PSSEL(pin) and CTSEL_I2C(pin)**

| | Primary chip | Secondary chip | Internal register access | Remote device register access |
|---|---|---|---|---|
| 1 | 2-wire target | 2-wire controller | Cdv => Pch => Sch * | Cdv => Pch => Sch => Rdv * |
| 2 | 2-wire controller | 2-wire target | Pch <= Sch <= Cdv * | Rdv <= Pch <= Sch <= Cdv * |
| 3 | 2-wire target | 2-wire target | Cdv => Pch / Sch<= Cdv * | Not allowed |
| 4 | 2-wire controller | 2-wire controller | Not allowed | Not allowed |

*Pch : Primary chip / Sch : Secondary chip / Cdv : Control device / Rdv : Remote device

### 10.7.2. Clock stretching

**2-wire serial controller device connected to the THCS253 must support clock stretching.**

Access from the 2-wire serial target (control device side) to the 2-wire serial controller (remote device side) of the THCS253 involves a clock stretch every 8 bits.

Clock stretching period = (Sampling period) x 29 + 625 [ns]

Effective I2C frequency = 1 / (Clock stretching period +SCL period)

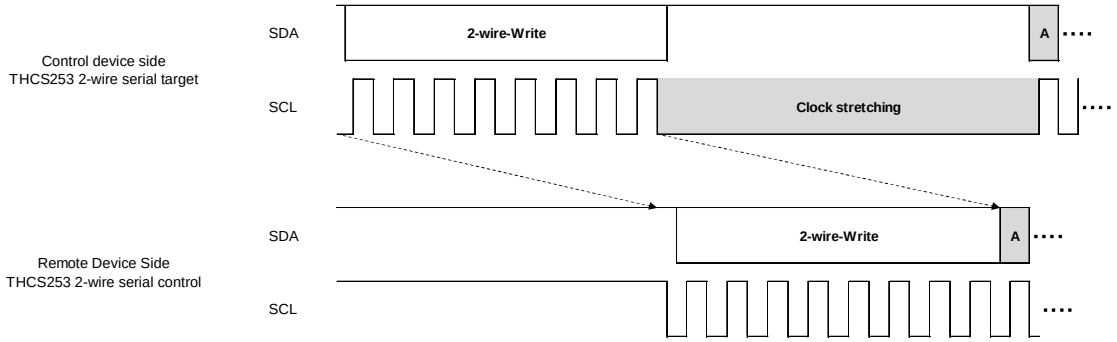


**Figure 10 Clock stretching of I2C communication**

### 10.7.3. Device Address

To access the THCS253 registers, IDSEL1 (pin) and IDSEL0 (pin) must be set and the device address must be selected. The device address must be set only on the 2-wire serial target set to CTSEL_I2C=0. The device address set on IDSEL1 and IDSEL0 cannot be used as the device address of a remote device.

**Table 14 Device ID setting**

| Setting | | Device address [6:0] (HEX) / (BIN) |
|---|---|---|
| IDSEL1 (pin) | IDSEL0 (pin) | |
| 0 | 0 | 0x0B / 000_1011 |
| 0 | 1 | 0x34 / 011_0100 |
| 1 | 0 | 0x77 / 111_0111 |
| 1 | 1 | 0x65 / 110_0101 |

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### 10.7.4. 2-wire serial controller / target register address space

The THCS253 identifies the 2-wire serial target (on the control device side) and the 2-wire serial controller (on the remote device side). Burst access across the boundary between the 2-wire serial target (control device side) and the 2-wire serial controller (remote device side) is prohibited.

**Table 15 Register address configuration**

| Register address | Description |
|---|---|
| 0x00 - 0x7F | 2-wire serial target (Control device side) |
| 0x80 - 0xFF | 2-wire serial controller (Remote device side) |

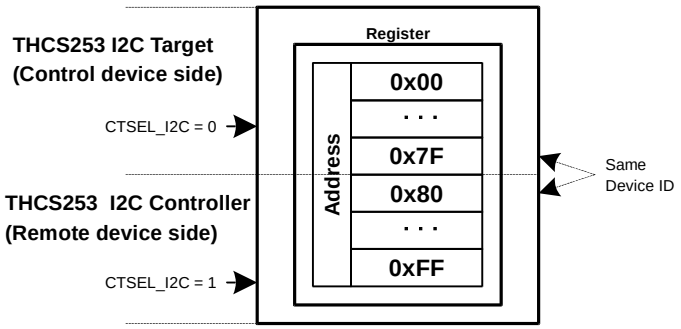


**Figure 11 Register address mapping**

### 10.7.5. 2-wire serial controller SCL frequency

2-wire serial controller chip with CTSEL_I2C=1 can set the SCL frequency in the register. The default is 156 kbps.

**Table 16 2-wire serial bitrate setting**

| Register Address | Name | Description |
|---|---|---|
| 0x26 | I2CPERIOD0 | 2-wire serial controller bit rate setting (SCL0)<br>10,000 / I2CPERIOD0 kbps |
| 0x27 | I2CPERIOD1 | 2-wire serial controller bit rate setting（SCL1）<br>10,000 / I2CPERIOD0 kbps |

### 10.7.6. 2-wire serial interface watch dog timer setting

The 2-wire serial interface of the THCS253 has a watchdog timer function that resets the internal state if communication stops for some reason, such as an external factor, and the internal state continues to not advance. The time until the watchdog timer is activated can be set in an internal register.

**Table 17 2-wire serial interface watch Dog Timer setting**

| Register Address | bit | Name | Description |
|---|---|---|---|
| 0x28 | 7:4 | I2C_WDT_STBY | 2-wire serial watch dog timer (standby)<br>0:Disable／50ms～1650s |
| | 3:0 | I2C_WDT | 2-wire serial watch dog timer (Normal mode)<br>Controller 0:Disable／0.0123ms - 403ms<br>Target 0:Disable／0.0246ms - 806ms |

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### 10.7.7. THCS253 internal register access protocol via 2-wire serial interface

The THCS253 2-wire serial interface protocol includes the following three types: (1) 2-wire serial target register access, (2) 2-wire serial controller access, and (3) 2-wire serial remote device access.

(1) THCS253 2-wire serial target register access

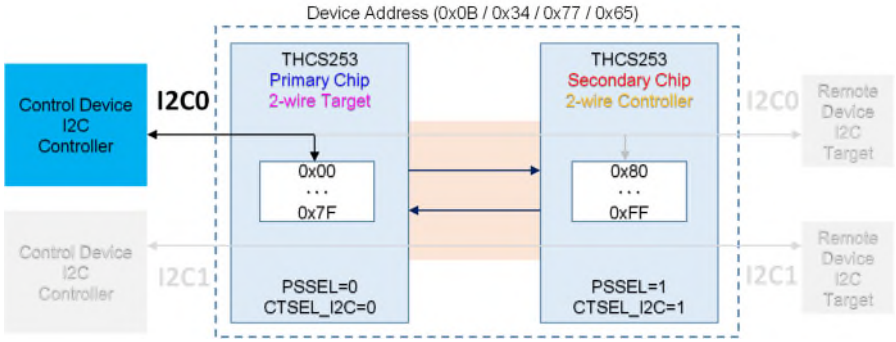
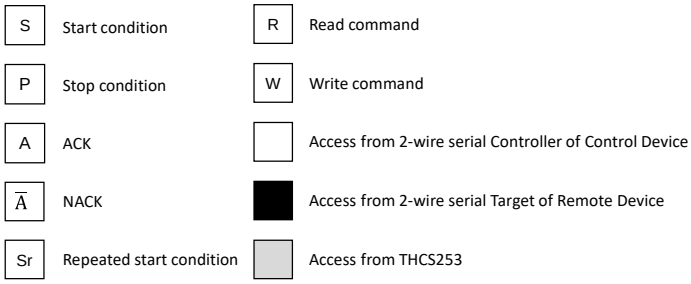
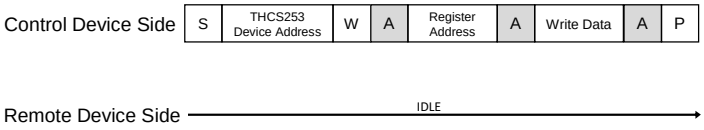


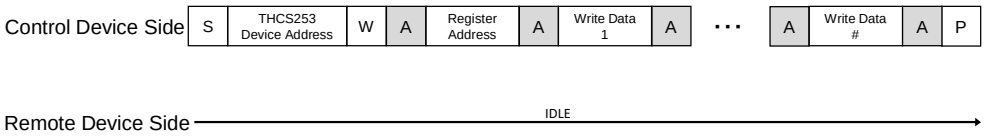

**Figure 12 2-wire serial target register access**




Single Byte write




Burst write



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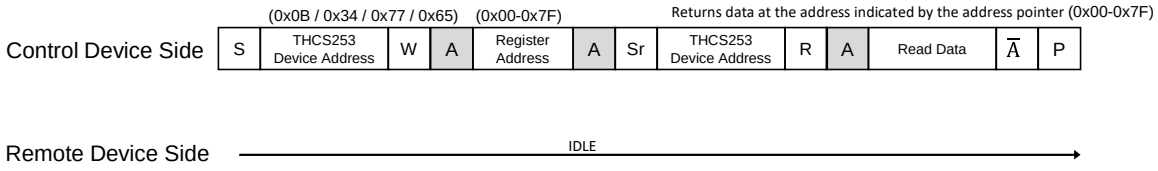
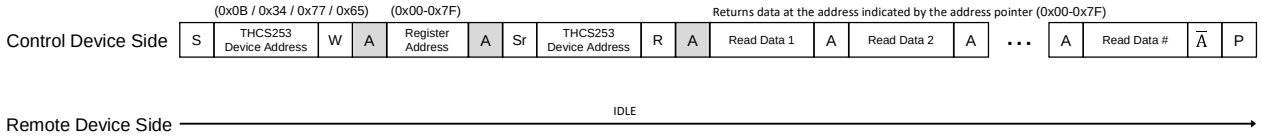
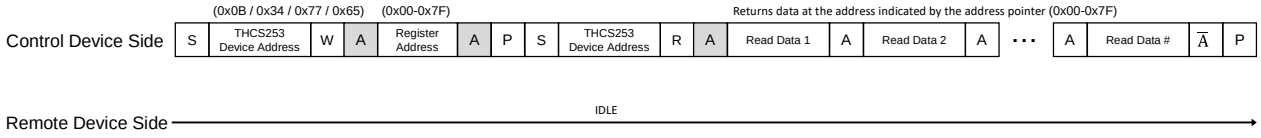
Single Byte read with repeated start command



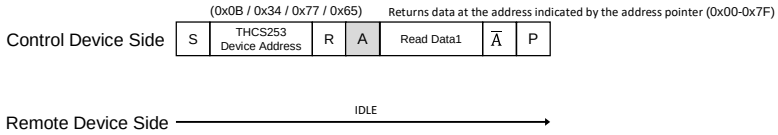

Burst read with repeated start command




Burst read with stop and start command




Single Byte read without repeated start condition




Burst read without repeated start condition

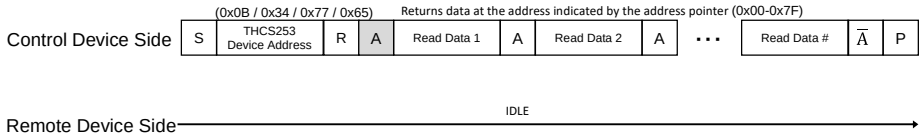



**Figure 13 2-wire serial target register access protocol**



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(2) THCS253 2-wire serial controller register access

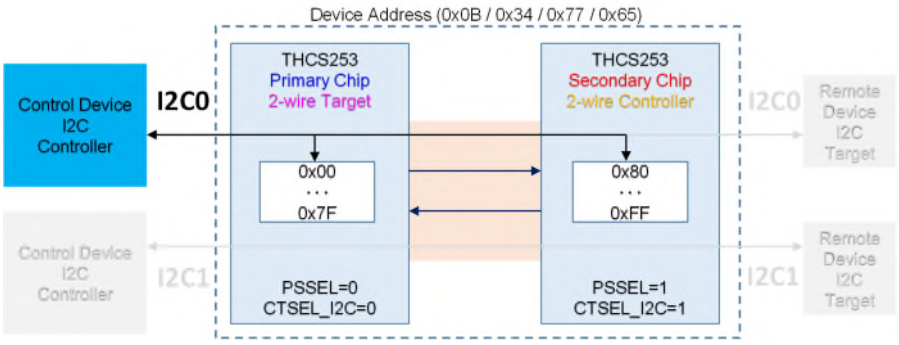
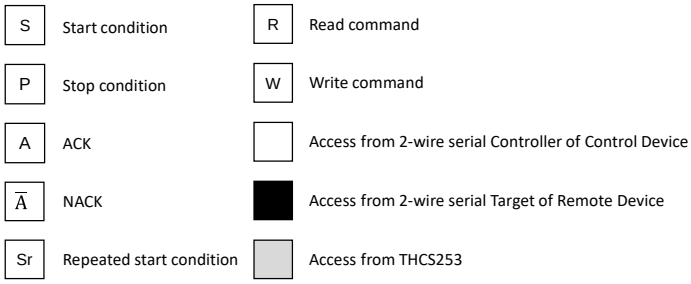
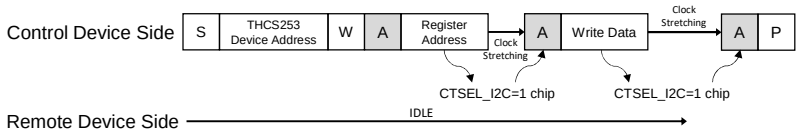


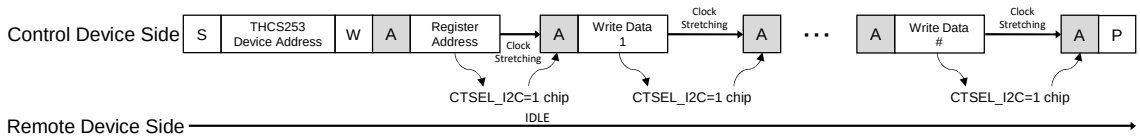

**Figure 14 2-wire serial controller register access**



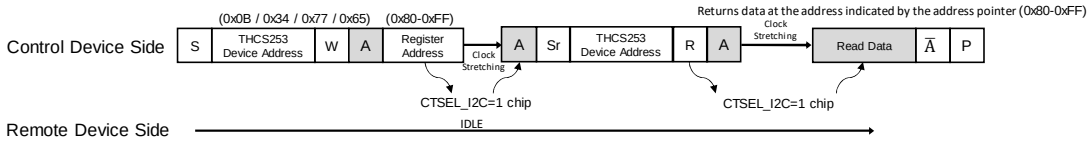

Single Byte write




Burst write




Single Byte read with repeated start command



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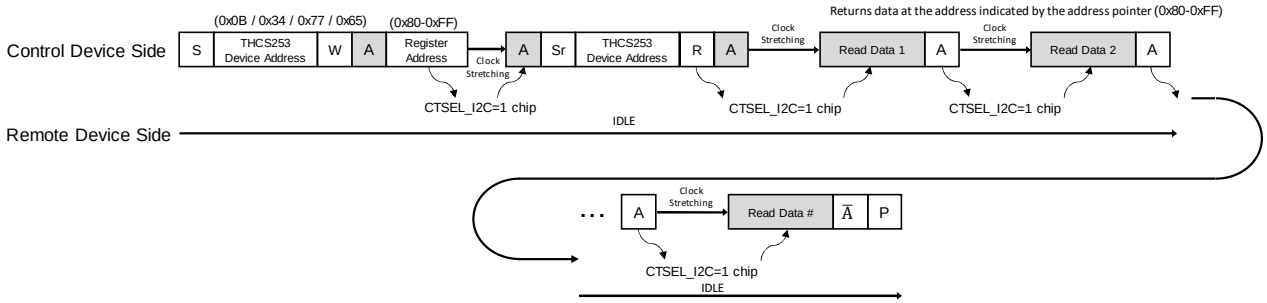
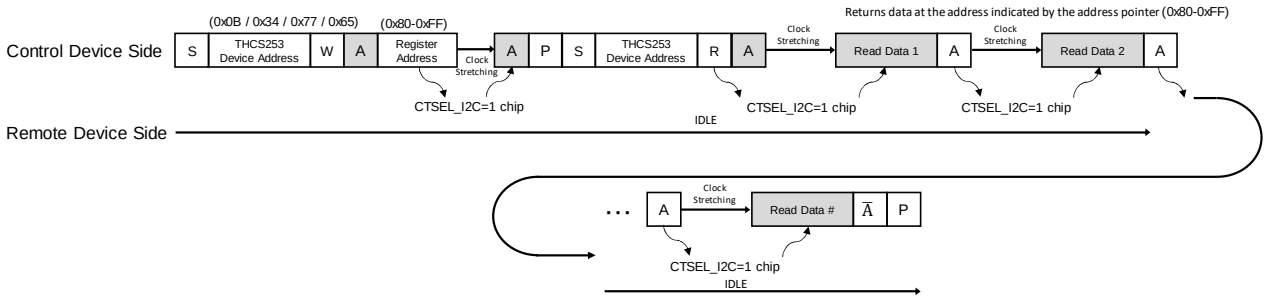
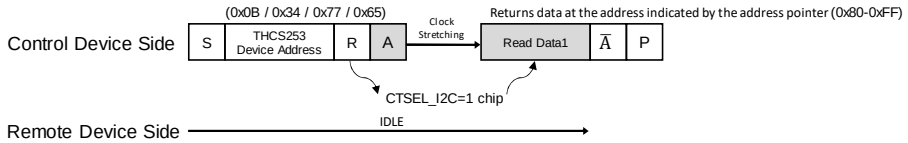
Burst read with repeated start command




Burst read with stop and start command




Single Byte read without repeated start condition




Burst read without repeated start condition

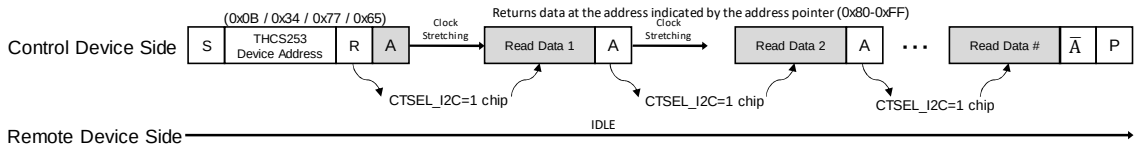



**Figure 15 2-wire serial controller register access protocol**



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(3) 2-wire serial remote device access.  Note: Partially includes access to THCS253.

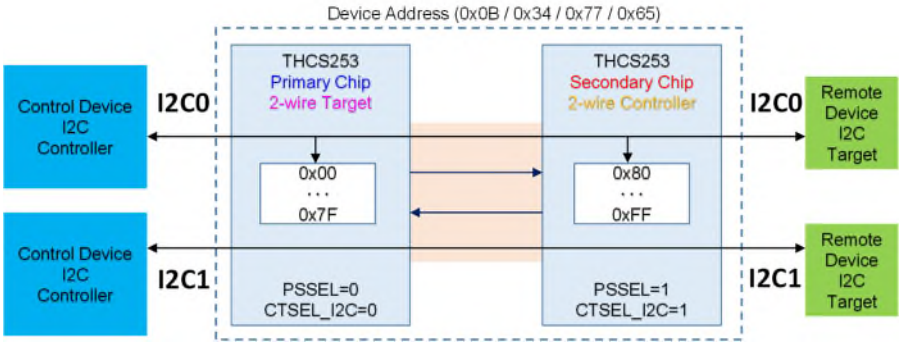
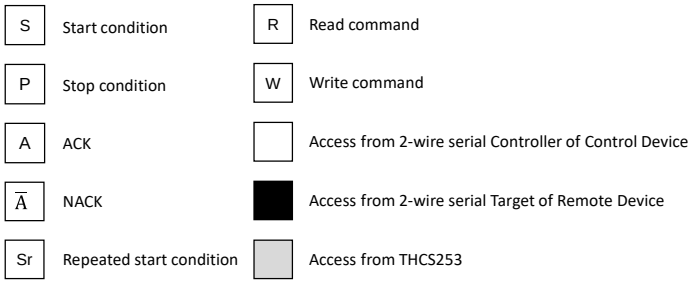
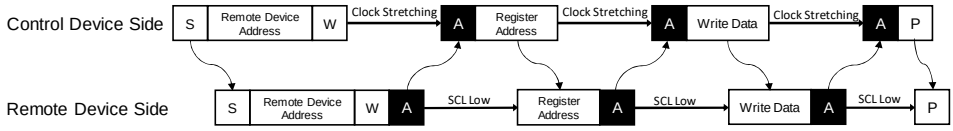


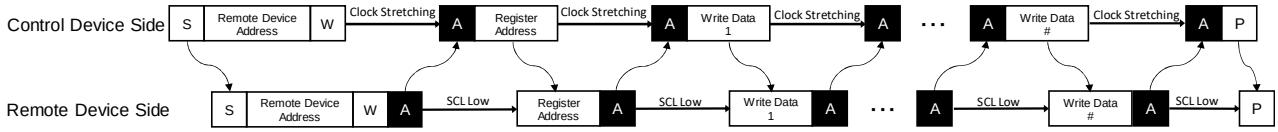

**Figure 16 2-wire serial remote device access**



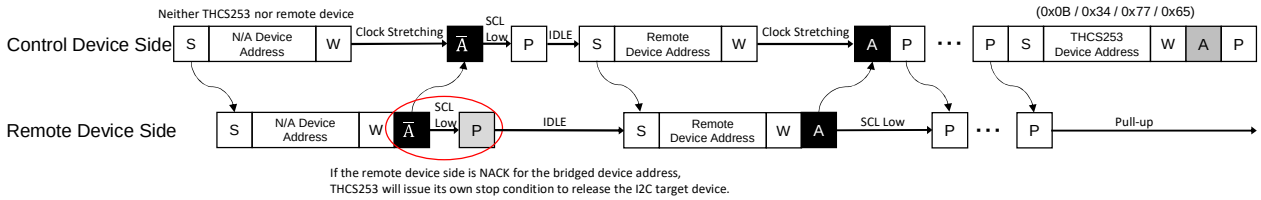

## Single Byte write




## Burst write




## I2C detect write command



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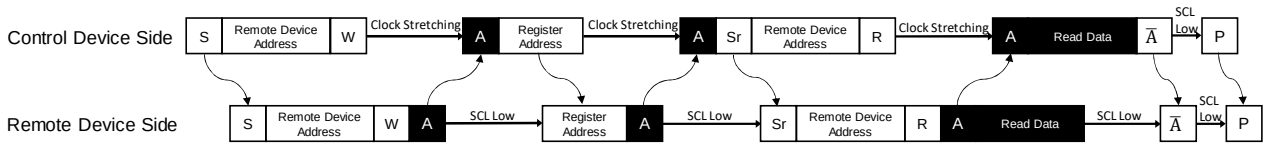
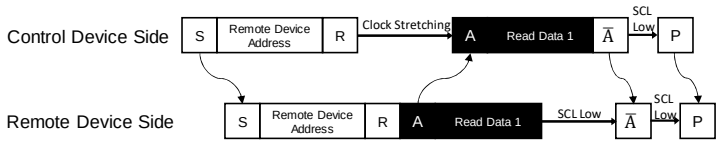
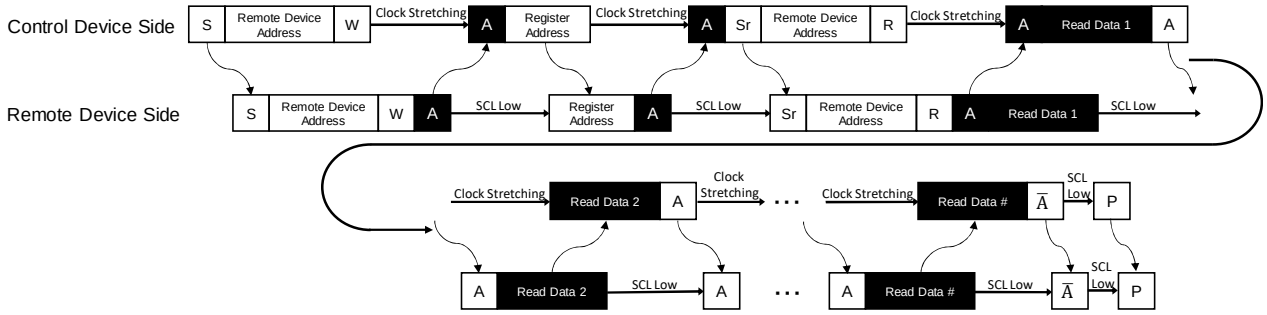
## Single Byte read with repeated start condition



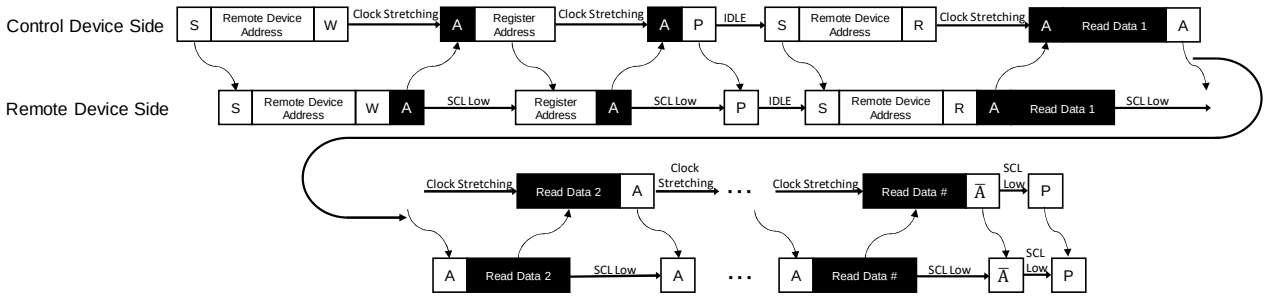

## Single Byte read without repeated start condition



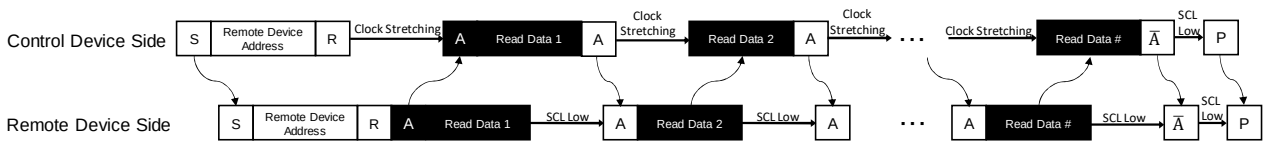

## Burst read with repeated start condition




## Burst read with stop and start condition




## Burst read without repeated start condition



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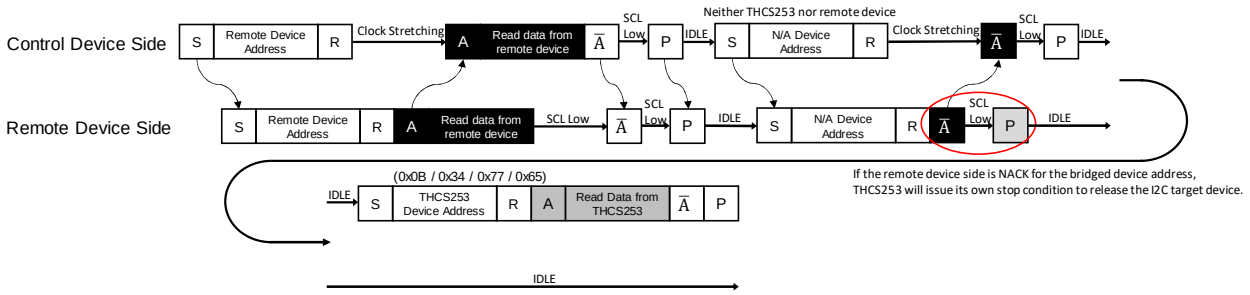
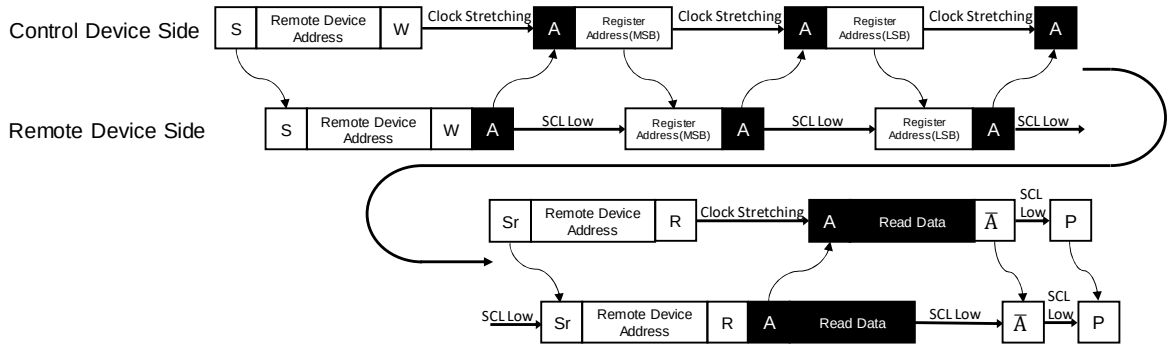
I2C detect read command




2Byte addressing device read with repeated start condition




2Byte addressing device read with stop and start condition

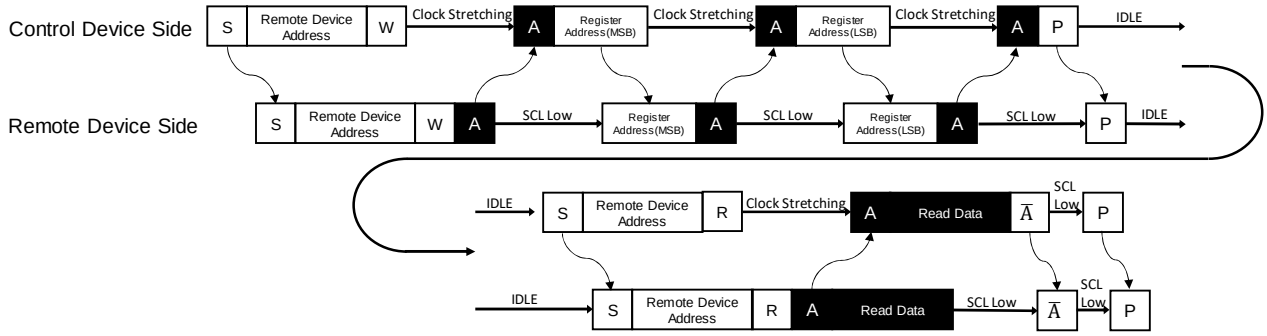



**Figure 17 2-wire serial remote device access protocol**



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### 10.7.8. 2-wire serial expander

The I2C_EXPAND (register) setting determines whether data transmission is performed through or used as an I2C expander. When used as an I2C expander, the value set in GPIO_OUT_*(*...0~3) is output from the data pins. The setting of GPIO_OBUF_*(*...0~3) is valid for the output buffer setting. Also, regardless of the I2C_EXPAND setting, data input is stored in GPIO_IN_*(*...0~3) and can be checked by I2C read. The above functions are available only when I2C is used (ENI2C0=1).

**Table 18 GPIO type setting**

| Function | Register Name | Description |
|---|---|---|
| GPIO function select | I2C_EXPAND | 0: Through(Default)<br>1: I2C Expander |

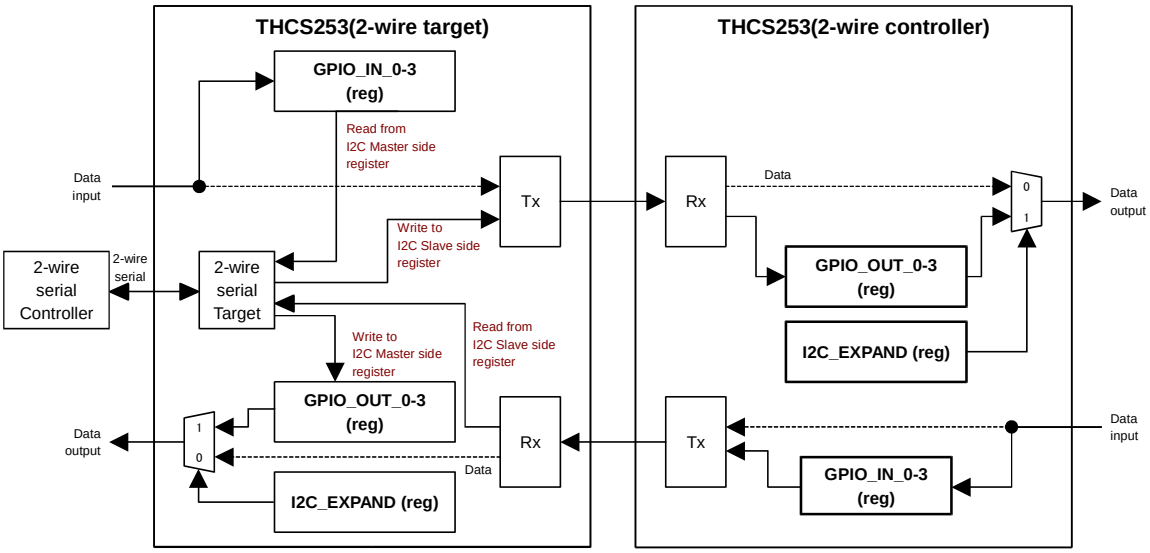


**Figure 18 2-wire serial expander function**



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## 10.8. Direction of GPIO

When DATA_WIDTH (pin) = 0, the CML line data rate is 30 times the sampling clock rate.

When DATA_WIDTH (pin) = 1, the CML line data rate is 50 times the sampling clock rate.

*Primary chip and secondary chip DATAWIDTH should be set the same.

The flow from the primary chip transmitter output to the secondary chip receiver input is defined as downstream.

The flow from the secondary chip transmitter output to the primary chip receiver input is defined as upstream.

By setting OVERRIDE_OEN (register) to 1, the GPIO direction can be freely set for each pin.

**Table 19 GPIO direction for each example**

| | Use case | A-1 | A-2 | B-1 | B-2 | | |
|---|---|---|---|---|---|---|---|
| Setting | DATA_WIDTH(pin) | 0 | 0 | 1 | 1 | | |
| | OVERRIDE_OE(register) | 0 | 1 | 0 | 1 | | |
| Mode | CML data rate | External reference clock mode 1/tTCIPx30 Internal oscillator clock mode 1/tOSCx30 | | External reference clock mode 1/tTCIPx50 Internal oscillator clock mode 1/tOSCx50 | | | |
| Data pin of primary chip | D0/D31/SDA1(pin) | => | => *2 | => | <=> *1 | D31/D0(pin) | Data pin of secondary chip |
| | D1/D30/SCL1(pin) | => | => *2 | => | <=> *1 | D30/D1(pin) | |
| | D2/D29(pin) | => | => *2 | => | <=> *1 | D29/D2(pin) | |
| | D3/D28(pin) | => | => *2 | => | <=> *1 | D28/D3(pin) | |
| | D4/D27(pin) | => | => *2 | => | <=> *1 | D27/D4(pin) | |
| | D5/D26(pin) | => | => *2 | => | <=> *1 | D26/D5(pin) | |
| | D6/D25(pin) | => | => *2 | => | <=> *1 | D25/D6(pin) | |
| | D7/D24(pin) | => | => *2 | => | <=> *1 | D24/D7(pin) | |
| | D8/D23(pin) | => | => *2 | => | <=> *1 | D23/D8(pin) | |
| | D9/D22(pin) | => | => *2 | => | <=> *1 | D22/D9(pin) | |
| | D10/D21(pin) | => | => *2 | => | <=> *1 | D21/D10(pin) | |
| | D11/D20(pin) | => | => *2 | => | <=> *1 | D20/D11(pin) | |
| | D12/D19(pin) | => | <=> *1 | => | <=> *1 | D19/D12(pin) | |
| | D13/D18(pin) | => | <=> *1 | => | <=> *1 | D18/D13(pin) | |
| | D14/D17(pin) | => | <=> *1 | => | <=> *1 | D17/D14(pin) | |
| | D15/D16(pin) | => | <=> *1 | => | <=> *1 | D16/D15(pin) | |
| | D16/D15(pin) | <= | <=> *1 | => | <=> *1 | D15/D16(pin) | |
| | D17/D14(pin) | <= | <=> *1 | => | <=> *1 | D14/D17(pin) | |
| | D18/D13(pin) | <= | <=> *1 | => | <=> *1 | D13/D18(pin) | |
| | D19/D12(pin) | <= | <=> *1 | => | <=> *1 | D12/D19(pin) | |
| | D20/D11(pin) | <= | <= *2 | => | <=> *1 | D11/D20(pin) | |
| | D21/D10(pin) | <= | <= *2 | => | <=> *1 | D10/D21(pin) | |
| | D22/D9(pin) | <= | <= *2 | => | <=> *1 | D9/D22(pin) | |
| | D23/D8(pin) | <= | <= *2 | => | <=> *1 | D8/D23(pin) | |
| | D24/D7(pin) | <= | <= *2 | => | <=> *1 | D7/D24(pin) | |
| | D25/D6(pin) | <= | <= *2 | => | <=> *1 | D6/D25(pin) | |
| | D26/D5(pin) | <= | <= *2 | => | <=> *1 | D5/D26(pin) | |
| | D27/D4(pin) | <= | <= *2 | <= | <=> *1 | D4/D27(pin) | |
| | D28/D3(pin) | <= | <= *2 | <= | <=> *1 | D3/D28(pin) | |
| | D29/D2(pin) | <= | <= *2 | <= | <=> *1 | D2/D29(pin) | |
| | D30/D1(pin) | <= | <= *2 | <= | <=> *1 | D1/D30/SCL1(pin) | |
| | D31/D0(pin) | <= | <= *2 | <= | <=> *1 | D0/D31/SDA1(pin) | |

"=>" is downstream (GPIO input to the primary chip is GPIO output from the secondary chip)
"<=" is upstream (GPIO input to the secondary chip is GPIO output from the primary chip)
"<=>" is a pin whose directionality can be selected one by one by internal register setting.
*1 The setting that contradicts the pin relationship between the primary chip and the secondary chip indicated by the pin name is not allowed.
*2 In the case of Example A-2, "=>" and "<=" other than "<=>" must also be set in the register as shown in the table.

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The following table shows the mapping between pins and registers that can be set by setting OVERRIDE_OEN (register) to 1.

**Table 20 GPIO OEN_0-3(register) mapping**

| Register Name | bit | Controlled terminal mapping | | Description |
|---|---|---|---|---|
| | | Primary chip mode | Secondary chip mode | |
| GPIO_OEN_0(register) | [0] | D0/D31/SDA1(pin) | D31/D0(pin) | GPIO direction select<br>{0} : Output<br>{1} : Input |
| | [1] | D1/D30/SCL1(pin) | D30/D1(pin) | |
| | [2] | D2/D29(pin) | D29/D2(pin) | |
| | [3] | D3/D28(pin) | D28/D3(pin) | |
| | [4] | D4/D27(pin) | D27/D4(pin) | |
| | [5] | D5/D26(pin) | D26/D5(pin) | |
| | [6] | D6/D25(pin) | D25/D6(pin) | |
| | [7] | D7/D24(pin) | D24/D7(pin) | |
| GPIO_OEN_1(register) | [0] | D8/D23(pin) | D23/D8(pin) | |
| | [1] | D9/D22(pin) | D22/D9(pin) | |
| | [2] | D10/D21(pin) | D21/D10(pin) | |
| | [3] | D11/D20(pin) | D20/D11(pin) | |
| | [4] | D12/D19(pin) | D19/D12(pin) | |
| | [5] | D13/D18(pin) | D18/D13(pin) | |
| | [6] | D14/D17(pin) | D17/D14(pin) | |
| | [7] | D15/D16(pin) | D16/D15(pin) | |
| GPIO_OEN_2(register) | [0] | D16/D15(pin) | D15/D16(pin) | |
| | [1] | D17/D14(pin) | D14/D17(pin) | |
| | [2] | D18/D13(pin) | D13/D18(pin) | |
| | [3] | D19/D12(pin) | D12/D19(pin) | |
| | [4] | D20/D11(pin) | D11/D20(pin) | |
| | [5] | D21/D10(pin) | D10/D21(pin) | |
| | [6] | D22/D9(pin) | D9/D22(pin) | |
| | [7] | D23/D8(pin) | D8/D23(pin) | |
| GPIO_OEN_3(register) | [0] | D24/D7(pin) | D7/D24(pin) | |
| | [1] | D25/D6(pin) | D6/D25(pin) | |
| | [2] | D26/D5(pin) | D5/D26(pin) | |
| | [3] | D27/D4(pin) | D4/D27(pin) | |
| | [4] | D28/D3(pin) | D3/D28(pin) | |
| | [5] | D29/D2(pin) | D2/D29(pin) | |
| | [6] | D30/D1(pin) | D1/D30/SCL1(pin) | |
| | [7] | D31/D0(pin) | D0/D31/SDA1(pin) | |

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## 10.9. IO configuration

### 10.9.1. I/O digital noise filter

The THCS253 has digital noise filters for GPIO input (CMOS input noise immunity) and output (CML line noise immunity), and the digital noise filters can be set simultaneously by setting FILTSEL1 (pin) and FILTSEL0 (pin). Each GPIO digital noise filter can be individually enabled by setting GPIO_I_FILTEN_0-3 (register) and GPIO_O_FILTEN_0-3 (register) with OVERRIDE_FILTEN (register)=1. The GPIO_I_FILTEN_0-3(register) and GPIO_O_FILTEN_0-3(register) settings enable each GPIO digital noise filter individually. The number of input/output filter tap can also be set by GPIO_I_FILTSET(register) and GPIO_O_FILTSET(register). The number of filter stages cannot be set for each pin individually.
The data width of (tap_num-1) tFLTCK or less is subject to filtering.

**Table 21 Input digital noise filter setting**

| Setting | | | | Function | Filter number of taps (tap_num) |
|---|---|---|---|---|---|
| OVERRIDE_I_FILTEN (register) | FILTSEL1 (pin) | FILTSEL0 (pin) | GPIO_I_FILTEN_0-3 (register) | | |
| {0} (default) | 0 | 0 | - | Digital noise filter simultaneous setting | Disable |
| | | 1 | | | 4 |
| | 1 | 0 | | | 8 |
| | | 1 | | | 16 |
| {1} | - | - | {0} | digital noise filter disable（Table 23） | GPIO_I_FILTSET (register)Setting |
| | | | {1} | digital noise filter enable（Table 23） | |

**Table 22 Output digital noise filter setting**

| Setting | | | | Function | Filter number of taps (tap_num) |
|---|---|---|---|---|---|
| OVERRIDE_O_FILTEN (register) | FILTSEL1 (pin) | FILTSEL0 (pin) | GPIO_O_FILTEN_0-3 (register) | | |
| {0} (default) | 0 | 0 | - | Digital noise filter simultaneous Setting | Disable |
| | | 1 | | | 4 |
| | 1 | 0 | | | 8 |
| | | 1 | | | 16 |
| {1} | - | - | {0} | Digital noise filter disable（Table 23） | GPIO_O_FILTSET (register) |
| | | | {1} | Digital noise filter enable（Table 23） | |

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**Table 23 GPIO_I_FILTEN_0-3(register) / GPIO_O_FILTEN_0-3(register) mapping**

| Register name | bit | Controlled terminal mapping | | Description |
|---|---|---|---|---|
| | | Primary chip mode | Secondary chip mode | |
| GPIO_I_FILTEN_0 (register) GPIO_O_FILTEN_0 (register) | [0] | D0/D31/SDA1(pin) | D31/D0(pin) | GPIO Input / output digital noise filter {0}:Disable {1}:Enable |
| | [1] | D1/D30/SCL1(pin) | D30/D1(pin) | |
| | [2] | D2/D29(pin) | D29/D2(pin) | |
| | [3] | D3/D28(pin) | D28/D3(pin) | |
| | [4] | D4/D27(pin) | D27/D4(pin) | |
| | [5] | D5/D26(pin) | D26/D5(pin) | |
| | [6] | D6/D25(pin) | D25/D6(pin) | |
| | [7] | D7/D24(pin) | D24/D7(pin) | |
| GPIO_I_FILTEN_1 (register) GPIO_O_FILTEN_1 (register) | [0] | D8/D23(pin) | D23/D8(pin) | |
| | [1] | D9/D22(pin) | D22/D9(pin) | |
| | [2] | D10/D21(pin) | D21/D10(pin) | |
| | [3] | D11/D20(pin) | D20/D11(pin) | |
| | [4] | D12/D19(pin) | D19/D12(pin) | |
| | [5] | D13/D18(pin) | D18/D13(pin) | |
| | [6] | D14/D17(pin) | D17/D14(pin) | |
| | [7] | D15/D16(pin) | D16/D15(pin) | |
| GPIO_I_FILTEN_2 (register) GPIO_O_FILTEN_2 (register) | [0] | D16/D15(pin) | D15/D16(pin) | |
| | [1] | D17/D14(pin) | D14/D17(pin) | |
| | [2] | D18/D13(pin) | D13/D18(pin) | |
| | [3] | D19/D12(pin) | D12/D19(pin) | |
| | [4] | D20/D11(pin) | D11/D20(pin) | |
| | [5] | D21/D10(pin) | D10/D21(pin) | |
| | [6] | D22/D9(pin) | D9/D22(pin) | |
| | [7] | D23/D8(pin) | D8/D23(pin) | |
| GPIO_I_FILTEN_3 (register) GPIO_O_FILTEN_3 (register) | [0] | D24/D7(pin) | D7/D24(pin) | |
| | [1] | D25/D6(pin) | D6/D25(pin) | |
| | [2] | D26/D5(pin) | D5/D26(pin) | |
| | [3] | D27/D4(pin) | D4/D27(pin) | |
| | [4] | D28/D3(pin) | D3/D28(pin) | |
| | [5] | D29/D2(pin) | D2/D29(pin) | |
| | [6] | D30/D1(pin) | D1/D30/SCL1(pin) | |
| | [7] | D31/D0(pin) | D0/D31/SDA1(pin) | |

**Table 24 Filter tap Setting**

| Register name | Description |
|---|---|
| GPIO_I_FILTSET(register) | Input digital noise filter setting<br>Number of filter tap(tap_num) = GPIO_I_FILTSET+1 |
| GPIO_O_FILTSET(register) | Output digital noise filter setting<br>Number of filter tap (tap_num) = GPIO_I_FILTSET+1 |

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### 10.9.2. LVCMOS Output buffer type configuration

The GPIO output buffer type can be selected between open-drain and push-pull. All output pins can be switched simultaneously by OBUF (pin), or each pin can be set by GPIO_OBUF_0-3 (register) via 2-wire serial interface.

**Table 25 Output buffer type configuration**

| Setting | | | Function |
|---|---|---|---|
| ENI2C | OBUF (pin) | GPIO_OBUF_0-3 (register) | |
| 0 | 0 | - | All output pins can be switched to open-drain simultaneously |
| | 1 | | All output pins can be switched to push-pull simultaneously |
| 1 | - | {0} | Set each GPIO output buffer type to open-drain |
| | | {1} | Set each GPIO output buffer type to push-pull |

**Table 26 GPIO_OBUF_0-3(register) mapping**

| Register name | Bit | Controlled terminal mapping | | Description |
|---|---|---|---|---|
| | | Primary chip mode | Primary chip mode | |
| GPIO_OBUF_0(register) | [0] | D0/D31/SDA1(pin) | D31/D0(pin) | GPIO output buffer type select {0}:open-drain {1}:push-pull |
| | [1] | D1/D30/SCL1(pin) | D30/D1(pin) | |
| | [2] | D2/D29(pin) | D29/D2(pin) | |
| | [3] | D3/D28(pin) | D28/D3(pin) | |
| | [4] | D4/D27(pin) | D27/D4(pin) | |
| | [5] | D5/D26(pin) | D26/D5(pin) | |
| | [6] | D6/D25(pin) | D25/D6(pin) | |
| | [7] | D7/D24(pin) | D24/D7(pin) | |
| GPIO_OBUF_1(register) | [0] | D8/D23(pin) | D23/D8(pin) | |
| | [1] | D9/D22(pin) | D22/D9(pin) | |
| | [2] | D10/D21(pin) | D21/D10(pin) | |
| | [3] | D11/D20(pin) | D20/D11(pin) | |
| | [4] | D12/D19(pin) | D19/D12(pin) | |
| | [5] | D13/D18(pin) | D18/D13(pin) | |
| | [6] | D14/D17(pin) | D17/D14(pin) | |
| | [7] | D15/D16(pin) | D16/D15(pin) | |
| GPIO_OBUF_2(register) | [0] | D16/D15(pin) | D15/D16(pin) | |
| | [1] | D17/D14(pin) | D14/D17(pin) | |
| | [2] | D18/D13(pin) | D13/D18(pin) | |
| | [3] | D19/D12(pin) | D12/D19(pin) | |
| | [4] | D20/D11(pin) | D11/D20(pin) | |
| | [5] | D21/D10(pin) | D10/D21(pin) | |
| | [6] | D22/D9(pin) | D9/D22(pin) | |
| | [7] | D23/D8(pin) | D8/D23(pin) | |
| GPIO_OBUF_3(register) | [0] | D24/D7(pin) | D7/D24(pin) | |
| | [1] | D25/D6(pin) | D6/D25(pin) | |
| | [2] | D26/D5(pin) | D5/D26(pin) | |
| | [3] | D27/D4(pin) | D4/D27(pin) | |
| | [4] | D28/D3(pin) | D3/D28(pin) | |
| | [5] | D29/D2(pin) | D2/D29(pin) | |
| | [6] | D30/D1(pin) | D1/D30/SCL1(pin) | |
| | [7] | D31/D3(pin) | D0/D31/SDA1(pin) | |

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### 10.9.3. 5V tolerant IO

Primary chip and Secondary chip are each equipped with 8 5V withstand voltage IOs.

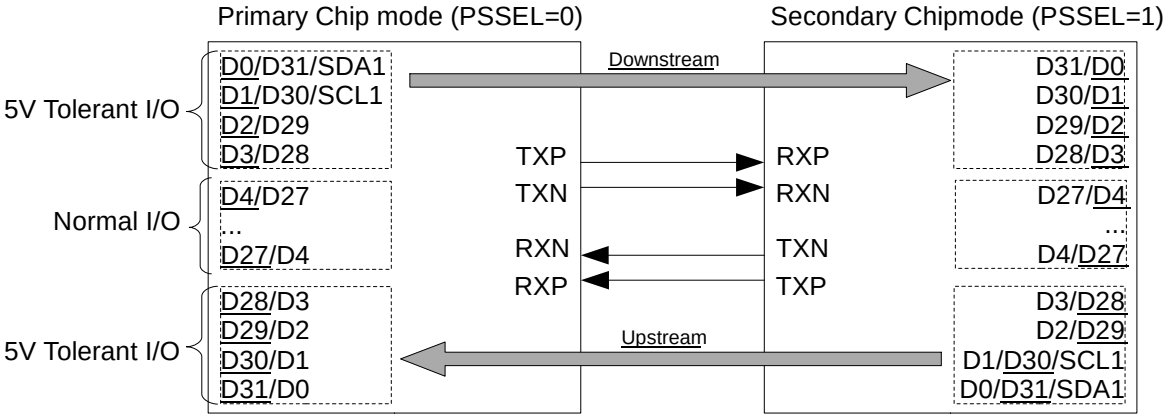


**Figure 19 5V tolerant IO**

### 10.9.4. LVCMOS Output drive strength setting

The THCS253 can set the output drive strength of REFOUT, D0 (pin) - D31 (pin), and READY pin with the TTLDRV (register). High drive setting is recommended when the reference clock frequency is 100 MHz or higher.

**Table 27 LVCMOS output drive strength setting**

| Setting<br>TTLDRV(register) | Description |
|---|---|
| {0} | Normal(default) |
| {1} | High |

### 10.9.5. CML output swing voltage and pre-emphasis setting

The CML output driver pre-emphasis compensates for the loss of high-frequency signal due to long-distance or high-speed transmission. The CML output swing voltage and pre-emphasis can be set by setting CMLDRV (register) and CMLPRE (register).

**Table 28 CML differential output and Pre-emphasis settings**

| Setting | | CML differential output peak to peak | Pre-emphasis | Description |
|---|---|---|---|---|
| CMLDRV [1:0] (register) | CMLPRE (register) | | | |
| {00} | {0} | 400mVpp | 0dB (0%) | - |
| | {1} | 400mVpp | 6dB (100%) | - |
| {01} | {0} | 600mVpp | 0dB (0%) | Default |
| | {1} | 600mVpp | 3.52dB (50%) | - |
| {10} | {0} | 800mVpp | 0dB (0%) | - |
| | {1} | 800mVpp | 0dB (0%) | - |
| {11} | {0} | Prohibition | | - |
| | {1} | Prohibition | | - |

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## 10.10. Clock configuration

### 10.10.1. Sampling clock select

Primary chip selects either external reference clock sampling or internal oscillator clock sampling with REFEN (pin).

Secondary chip uses SYNCEN (pin) to select whether to operate synchronously with the primary chip clock or asynchronously with the primary chip. If SYNCEN = 0 for asynchronous operation, REFEN (pin) is used to select external reference clock sampling or internal oscillator clock sampling.

When an external reference clock is used, the data sampling clock edge can be selected with RF_IN/OSCSEL0 (pin). Similarly, the data output clock edge is selected by RF_OUT/OSCSEL1 (pin). When internal oscillator clock sampling is selected by REFEN (pin) = 0, the internal oscillator clock frequency can be selected by RF_OUT/OSCSEL1 (pin) and RF_IN/OSCSEL0 (pin).

**Table 29 Sampling Clock and RF_OUT/OSCSEL1, RF_IN/OSCSEL0 Function**

| PSSEL (pin) | SYNCEN (pin) | REFEN (pin) | REFIN (pin) | RF_OUT/OSCSEL1 (pin) | RF_IN/OSCSEL0 (pin) | Description |
|---|---|---|---|---|---|---|
| 0 | Invalid | 0 | - | Int. OSC clock sampling frequency setting (OSCSEL1, OSCSEL0) | | Sampling with internal oscillator clock Frequency set by OSCSEL1 and OSCSEL0 (pin) |
| | Invalid | 1 | Ext. reference clock | Output data clock edge setting RF_OUT | Output data clock edge setting RF_IN | Sampling with external reference clock |
| 1 | 0 | 0 | - | Int. OSC clock sampling frequency setting (OSCSEL1, OSCSEL0) | | Sampling with internal oscillator clock Frequency set by OSCSEL1 and OSCSEL0 (pin) |
| | | 1 | Ext. reference clock | Output data clock edge setting RF_OUT | Output data clock edge setting RF_IN | Sampling with external reference clock |
| | 1 | Invalid | - | Invalid | | Sampling with CDR clock |
| | | Invalid | - | Invalid | Invalid | Sampling with CDR clock |

**Table 30 OSC Clock Sampling Frequency and External Clock Input frequency**

| REFEN (pin) | RF_OUT/OSCSEL1 (pin) | RF_IN/OSCSEL0 (pin) | DATA_WIDTH (pin) | OSC. frequency / Input frequency | CML data rate |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 20MHz±20% | 480Mbps - 720Mbps |
| | | | 1 | | 800Mbps - 1200Mbps |
| | 0 | 1 | 0 | 40MHz±20% | 960Mbps - 1440Mbps |
| | | | 1 | | 1600Mbps - 2400Mbps |
| | 1 | 0 | 0 | | 960Mbps - 1440Mbps |
| | | | 1 | | 1600Mbps - 2400Mbps |
| | 1 | 1 | 0 | 80MHz±20% | 1920Mbps - 2880Mbps |
| | | | 1 | Prohibition | |
| 1 | - | - | 0 | 15 - 133.3MHz | 0.45 - 4.0Gbps |
| | - | - | 1 | 9 - 80MHz | 0.45 - 4.0Gbps |

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### 10.10.2. Clock edge select (RF_IN, RF_OUT)

When REFEN=1 (external reference clock is used), clock edge switching function is Enable.

The RF_IN/OSCSEL0 pin can be used to set the input data sampling edge when an external reference clock is used, and the RF_OUT/OSCSEL1 pin can be used to set the REFOUT output clock edge. The polarity of RF_IN and RF_OUT is the clock edge that defines Setup/Hold timing.

**Table 31 RF Function**

| Pin name | Description |
|---|---|
| RF_IN<br>RF_OUT | 0 : Fall Edge (Default)<br>1 : Rise Edge |

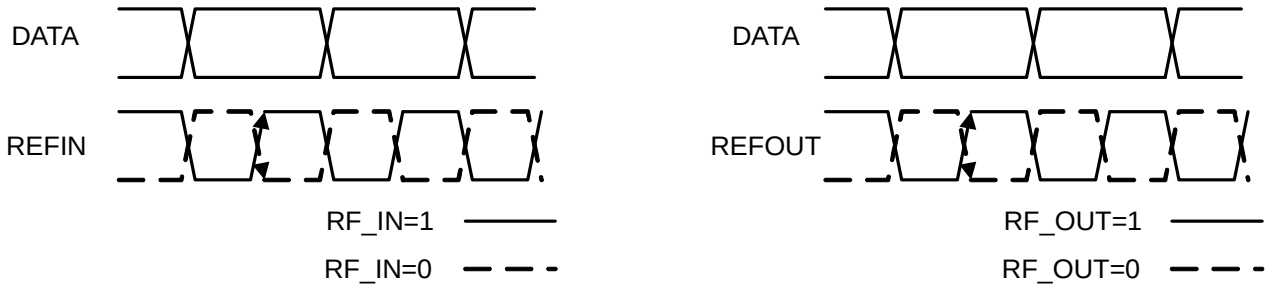


**Figure 20 RF_IN, RF_OUT Function**



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### 10.11. Spread spectrum clock generator and REFIN(pin) frequency

THCS253 enables spread spectrum clock output by enabling SSCG PLL with SSEN (pin). When 2-wire serial interface is enabled (ENI2C=1), the modulation frequency and modulation rate of the spread spectrum clock can be set.

When SYNCEN (pin) = 1, the spread spectrum clock is set only on the transmitter clock side of the primary chip.

When SYNCEN (pin) = 0, it can be multiplied to both primary and secondary chips.

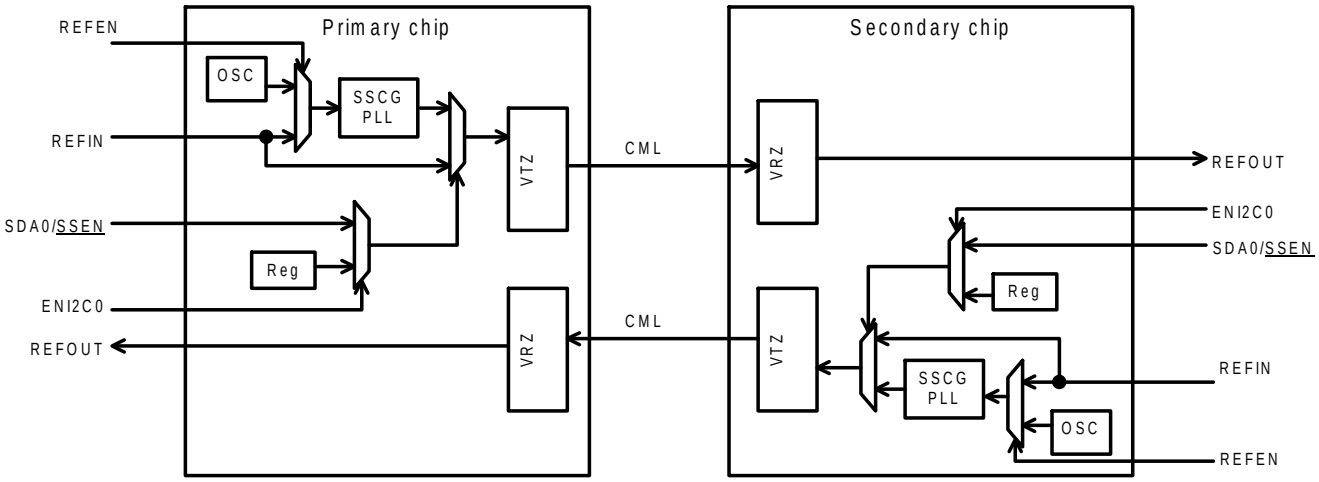


**Figure 21 Spread Spectrum Configuration**

**Table 32 Spread Spectrum Setting**

| Register name | Description |
|---|---|
| SPREAD[4:0] (register) | Modulation rate setting Modulation rate = SPREAD |
| FMOD[3:0] (register) | Modulation frequency setting |

The modulation frequency of the spread spectrum clock is determined by the following formula.

$$f_{mod} = \frac{f_{ref}}{512 \times FMOD}$$



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### 10.12. PWM signal output function

The THCS253 can output PWM signals from the D2/D29/PWMOUT pins.

Access the PWMH [7:0] and PWML [7:0] registers via the 2-wire serial interface to set the L/H period in 256 steps, and enable PWMOUT with the PWMEN register.

PWM High period = 1/(80MHz±20%) x PWMH(0～255)[ns]

PWM Low period = 1/(80MHz±20%) x PWML(0～255)[ns]

Except,

When PWML = 0x00 and PWMH = 0x00, D2/D29/PWMOUT pin is fixed low.

When PWML = 0x00 and PWMH = 0x01, D2/D29/PWMOUT pin is fixed high.

### 10.13. CRC

THCS253 adds CRC data (CRC8) to GPIO signals and during 2-wire serial communication to avoid outputting abnormal data when bit errors occur. The CRC is inserted once every 4 sampling clocks when DATAWIDTH=1 and once every 6 sampling clocks when DATAWIDTH=0. The CRC data insertion is shown in the figure below.

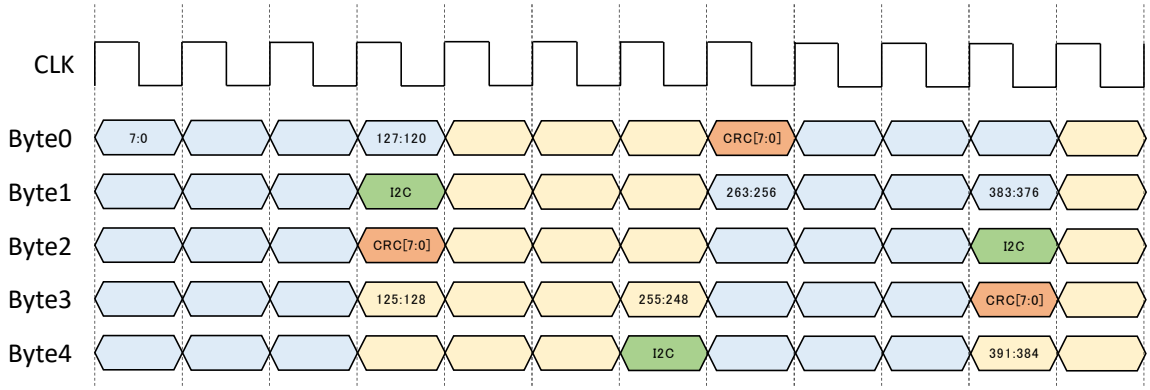


**Figure 22 CRC data when DATAWIDTH=1**

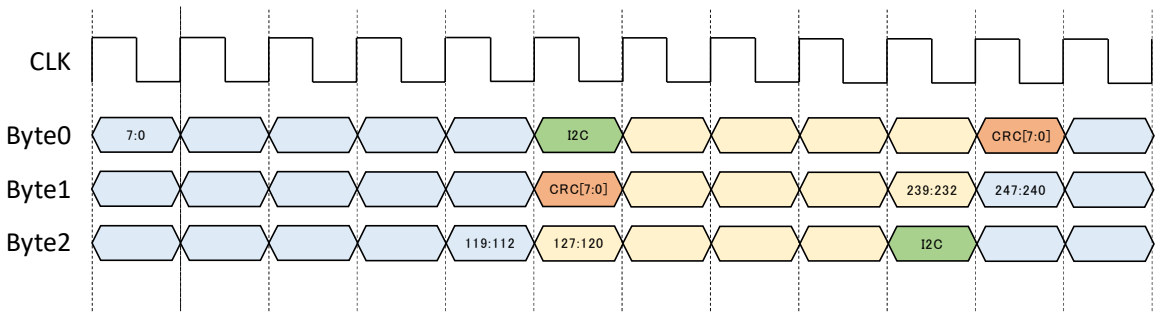


**Figure 23 CRC data when DATAWIDTH=0**



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## 10.14. Error detection and notification

### 10.14.1. READY signal

The THCS253 notifies with READY(pin) when the link between the Primary chip and the Secondary chip is established and data transmission and I2C transmission are possible. When the transmitter's PLL, receiver's CDR, and SSCG PLL (when the spread spectrum clock is enabled) are locked and normal pattern transmission is enabled, READY(pin)=H is displayed.

When there is no link error such as clock error or off-lock, the READY signal is output high, and data error is notified from INTN (pin). When a link error is detected, READY (pin) goes low and enters the re-link-up sequence.

During the READY(pin)=L period, data transmission, 2-wire serial communication across devices (access to internal registers of the chip set to the 2-wire serial interface controller with CTSEL_I2C=1, access to remote device registers) is prohibited. Access to the internal registers of the chip set to the 2-wire serial interface target (CTSEL_I2C=0) is possible. Notification from READY (pin) is possible for both Primary chip and Secondary chip.

**Table 33 Operation of READY(pin)**

| READY (pin) | Description |
|---|---|
| L | Link not established.<br>Data transmit and receive is inhibited.<br>I2C access to chips other than the chip set to CTSEL_I2C=0 is prohibited. |
| H | Link established.<br>Data transmit and receive, I2C access available. |

### 10.14.2. INTN signal

When the THCS253 detects errors in the CRC error check result on the CML line, it signals these as interrupt causes through INTN (pin). INTN signal is a low active open drain output.

When the 2-wire serial interface is enabled and the interrupt register is enabled, the INTN (pin) transitions from INTN (high) to low when an error that causes an interrupt occurs, and INTN (pin) = low is maintained until the interrupt status register is cleared.

When the 2-wire serial interface is disabled, INTN (pin) = L when any interrupt factor occurs. INTN (pin) = L is output until the data error is cleared, and returns to INTN (pin) = H (pull-up) when the data error is cleared. At this time, the GPIO output signal updates the output data only when INTN (pin) = High, and holds the output before the error occurs when INTN (pin) = Low.

The THCS253 detects CRC signals inserted in communication packets and notifies the user via INTN (pin). There are two types of CRC signals: one is embedded in the downstream/upstream GPIO error detection byte and the other is embedded in the 2-wire serial transmit/receive error detection byte. Normally, the CRC for 2-wire serial transmission and reception is an invalid signal when 2-wire serial communication is not being used. However, if noise is mixed in during transmission and the CRC data is corrupted, as it is during communication, a 2-wire serial communication CRC error may occur even if 2-wire serial communication is not being used.

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### 10.15. Standby mode: STANDBY(register)=1

Standby mode is an operation mode that enables data transmission at low sampling rate and low power consumption. The transition from normal mode to standby mode and from standby mode to normal mode is initiated by STANDBY (register) access via 2-wire serial. STANDBY(register) exists only on the 2-wire serial target side with CTSEL_I2C=0. In standby mode, handshake communication is performed between the primary chip and secondary chip. Operation can be selected between sampling and data transmission (polling) at intervals set by STBY_CYCLE (register) and data transmission by detecting changes in the pins for standby mode or I2C input. A maximum of eight GPIO signals can be used for data transmission. The number and direction of the number of signals used are set by the STBY_NUM_DS (register) and STBY_NUM_US (register) of the primary chip. The number of pins in the downstream direction is set by STBY_NUM_DS (register) and the number of pins in the upstream direction by STBY_NUM_US (register). Upon entry into standby mode, if the link was established in normal mode, the READY signal goes low once, and when handshake communication is established, the READY signal goes high again to enable signal transmission. The interrupt status register (transmission error generation interrupt, I2C interrupt, etc.) and INT are cleared during normal operation. If the opposing device exits from standby mode or power down after the READY signal goes high, the primary chip side detects no response from the secondary chip and the secondary chip side detects a timeout in the request interval from the primary chip and sets the READY signal low. The primary chip issues the first request command 1.5 ms (typ) after entering standby mode. The sampling interval for polling operation can be changed by setting the STBY_CYCLE register on the primary chip side. No setting is required on the secondary chip side.

**Table 34 Standby Mode Operation Select**

| STANDBY (register) | STBY_MODE (register) | Description |
|---|---|---|
| 0 | Ignore | Normal operation |
| 1 | 0 (default) | Only polling operation |
| | 1 | Polling and external trigger operation |

**Table 35 STBY_NUM_DS, STBY_NUM_US vs Standby mode data pin state example**

| STBY_NUM_DS (register) | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 4 | 4 | 4 | 4 | 4 | 8 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STBY_NUM_US (register) | 0 | 0 | 1 | 2 | 7 | 8 | 8 | 0 | 1 | 2 | 7 | 8 | 0 | 1 | 8 |
| D0/D31/SDA1 | Normal terminal handling | Down | Down | Down | Down | Down | Up | Down | Down | Down | Down | Down | Down | Down | Down |
| D1/D30/SCL1 | | Normal terminal handling | Normal terminal handling | Normal terminal handling | Up | Up | Up | Down | Down | Down | Down | Down | Down | Down | Down |
| D2/D29 | | | | | Up | Up | Up | Down | Down | Down | Down | Down | Down | Down | Down |
| D3/D28 | | | | | Up | Up | Up | Down | Down | Down | Down | Down | Down | Down | Down |
| D28/D3 | | | | | Up | Up | Up | Normal terminal handling | Normal terminal handling | Normal terminal handling | Up | Up | Down | Down | Down |
| D29/D2 | | | | | Up | Up | Up | | | | Up | Up | Down | Down | Down |
| D30/D1 | | | | Up | Up | Up | Up | | | Up | Up | Up | Down | Down | Down |
| D31/D0 | | | Up | Up | Up | Up | Up | | Up | Up | Up | Up | Down | Down | Down |



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**Table 36 Output of normal data pin in standby mode**

| STBY_DOUT (register) | Description |
|---|---|
| 0 | Hi-Z(Default) |
| 1 | Holds status before standby mode entry |

**Table 37 Standby Mode Sampling Rate Setting (Primary chip only)**

| Register name | Description |
|---|---|
| STBY_CYCLE (register) | 000 : 50ms<br>001 : 100ms(Default)<br>010 : 150ms<br>011 : 200ms<br>100 : 250ms<br>101 : 300ms<br>110 : 350ms<br>111 : 400ms<br>Values are Typical values. Guaranteed value is ±20% of the above value due to OSC variation. |

**Table 38 Registers that need to be set in standby mode**

| Register Name | Primary chip | Secondary chip |
|---|---|---|
| STBY_DRV | As required | As required |
| STBY_NUM_DS | Required | Not Required |
| STBY_NUM_US | Required | Not Required |
| STBY_CYCLE | Required | Not Required |
| STBY_DOUT | As required | As required |
| STBY_MODE | As required | Prohibition |
| STANBY | Required | Required |

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## 11. Register map

| Target address (Hex) | Controller address (Hex) | Bit # | R/W | Default (Hex) | Register name | Description |
|---|---|---|---|---|---|---|
| 0x00 | 0x80 | 3 | R | - | STBY_READY | READY signal status in standby mode<br>0: READY=L or Normal mode<br>1: READY=H |
| | | 2 | R | - | LINK_READY | READY signal status in normal mode<br>0: READY=L or standby mode<br>1: READY=H |
| | | 0 | R | - | INT | INT status (INTN(pin) inversion)<br>0: No error<br>1: Error occurred |
| 0x01 | 0x81 | 2 | R/W | 0 | I2C_CRC | 0: 2-wire serial com error occurred<br>1: Error clear |
| | | 1 | R/W | 0 | US_CRC | 0: Upstream error occurred<br>1: Error clear |
| | | 0 | R/W | 0 | DS_CRC | 0: Downstream error occurred<br>1: Error clear |
| 0x02 | 0x82 | 2 | R/W | 0 | I2C_CRC_EN | 0: 2-wire serial come error interrupt enable<br>1: 2-wire serial come error interrupt disable |
| | | 1 | R/W | 0 | US_CRC_EN | 0: Upstream error interrupt enable<br>1: Upstream error interrupt disable |
| | | 0 | R/W | 0 | DS_CRC_EN | 0: Downstream error interrupt enable<br>1: Downstream error interrupt disable |
| 0x03 | 0x83 | 0 | R/W | 0 | ENI2C1 | 2-wire serial interface SDA1/SCL1<br>0: Disable<br>1: Enable |
| 0x04 | 0x84 | 0 | R/W | 0 | I2C_EXPAND | I/O Expander mode<br>0: Disable（GPIO transceiver mode）<br>1: Enable |
| 0x05 | 0x85 | 7:0 | R | 0x00 | GPIO_IN_0 | GPIO[7:0] input status monitor |
| 0x06 | 0x86 | 7:0 | R | 0x00 | GPIO_IN_1 | GPIO[15:8]input status monitor |
| 0x07 | 0x87 | 7:0 | R | 0x00 | GPIO_IN_2 | GPIO[23:16]input status monitor |
| 0x08 | 0x88 | 7:0 | R | 0x00 | GPIO_IN_3 | GPIO[31:24]input status monitor |
| 0x09 | 0x89 | 7:0 | R/W | 0x00 | GPIO_OUT_0 | GPIO[7:0] output setting (Applicable only to I/O expansion mode) |
| 0x0A | 0x8A | 7:0 | R/W | 0x00 | GPIO_OUT_1 | GPIO[15:8] output setting (Applicable only to I/O expansion mode) |
| 0x0B | 0x8B | 7:0 | R/W | 0x00 | GPIO_OUT_2 | GPIO[23:16] output setting (Applicable only to I/O expansion mode) |
| 0x0C | 0x8C | 7:0 | R/W | 0x00 | GPIO_OUT_3 | GPIO[31:24] output setting (Applicable only to I/O expansion mode) |
| 0x0D | 0x8D | 7:0 | R/W | 0xFF | GPIO_OEN_0 | GPIO [7:0] direction select<br>0:output 1:input |
| 0x0E | 0x8E | 7:0 | R/W | 0xFF | GPIO_OEN_1 | GPIO [15:8] direction select<br>0:output 1:input |
| 0x0F | 0x8F | 7:0 | R/W | 0xFF | GPIO_OEN_2 | GPIO [23:16] direction select<br>0:output 1:input |
| 0x10 | 0x90 | 7:0 | R/W | 0xFF | GPIO_OEN_3 | GPIO [31:24] direction select<br>0:output 1:input |
| 0x11 | 0x91 | 0 | R/W | 0 | OVERRIDE_OEN | GPIO_OEN setting method select<br>0: Input/output default values per use case<br>1: Register setting GPIO_OEN_0-3 |
| 0x12 | 0x92 | 7:0 | R/W | 0xFF | GPIO_OBUF_0 | GPIO [7:0] Output buffer type select<br>0:Open Drain 1:Pushpull |
| 0x13 | 0x93 | 7:0 | R/W | 0xFF | GPIO_OBUF_1 | GPIO [15:8] Output buffer type select0:Open Drain 1:Pushpull |
| 0x14 | 0x94 | 7:0 | R/W | 0xFF | GPIO_OBUF_2 | GPIO [23:16] Output buffer type select0:Open Drain 1:Pushpull |
| 0x15 | 0x95 | 7:0 | R/W | 0xFF | GPIO_OBUF_3 | GPIO [31:24] Output buffer type select0:Open Drain 1:Pushpull |
| 0x16 | 0x96 | 7:0 | R/W | 0x00 | Reserved | Must be 0 |
| 0x17 | 0x97 | 7:0 | R/W | 0xFF | GPIO_I_FILTEN_0 | GPIO [7:0] input digital noise filter<br>0:Disable 1:Enable |

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| | | | | | | |
|---|---|---|---|---|---|---|
| 0x18 | 0x98 | 7:0 | R/W | 0xFF | GPIO_I_FILTEN_1 | GPIO [15:8] input digital noise filter<br>0:Disable 1:Enable |
| 0x19 | 0x99 | 7:0 | R/W | 0xFF | GPIO_I_FILTEN_2 | GPIO [23:16] input digital noise filter<br>0:Disable 1:Enable |
| 0x1A | 0x9A | 7:0 | R/W | 0xFF | GPIO_I_FILTEN_3 | GPIO[31:24] input digital noise filter<br>0:Disable 1:Enable |
| 0x1B | 0x9B | 7:0 | R/W | 0x03 | GPIO_I_FILTSET | Input digital noise filter setting<br>Number of filter tap = GPIO_I_FILTSET+1 |
| 0x1C | 0x9C | 0 | R/W | 0 | OVERRIDE_I_FILTEN | Input digital noise filter enable setting method<br>0: FILTSEL1(pin) and FILTSEL0(pin)<br>1: GPIO_I_FILTEN_0-3(register) |
| 0x1D | 0x9D | 7:0 | R/W | 0xFF | GPIO_O_FILTEN_0 | GPIO[7:0] output digital noise filter<br>0:Disable 1:Enable |
| 0x1E | 0x9E | 7:0 | R/W | 0xFF | GPIO_O_FILTEN_1 | GPIO[15:8] output digital noise filter<br>0:Disable 1:Enable |
| 0x1F | 0x9F | 7:0 | R/W | 0xFF | GPIO_O_FILTEN_2 | GPIO[23:16] output digital noise filter<br>0:Disable 1:Enable |
| 0x20 | 0xA0 | 7:0 | R/W | 0xFF | GPIO_O_FILTEN_3 | GPIO[31:24] output digital noise filter<br>0:Disable 1:Enable |
| 0x21 | 0xA1 | 7:0 | R/W | 0x03 | GPIO_O_FILTSET | Output digital noise filter setting<br>Number of filter tap =<br>GPIO_O_FILTSET+1 |
| 0x22 | 0xA2 | 0 | R/W | 0 | OVERRIDE_O_FLTEN | Output digital noise filter enable setting method<br>0: FILTSEL1(pin) and FILTSEL0(pin)<br>1: GPIO_I_FILTEN_0-3(register) |
| 0x23 | 0xA3 | 7:0 | R | 0x00 | CRC_ERROR_COUNT[15:8] | Number of CRC error (MSB 8bit) |
| 0x24 | 0xA4 | 7:0 | R | 0x00 | CRC_ERROR_COUNT[7:0] | Number of CRC error (LSB 8bit) |
| 0x25 | 0xA5 | 0 | W | - | CRC_ERROR_COUNT_CLEAR | 1 Write : CRC ERROR COUNT[15:0] clear |
| 0x26 | 0xA6 | 7:0 | R/W | 0x64 | I2CPERIOD0 | I2C0 Controller Bit Rate<br>10,000/I2CPERIOD0 kbps |
| 0x27 | 0xA7 | 7:0 | R/W | 0x64 | I2CPERIOD1 | I2C1 Controller Bit Rate<br>10,000/I2CPERIOD0 kbps |

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| | | | | | | |
|---|---|---|---|---|---|---|
| 0x28 | 0xA8 | 7:4 | R/W | 0x6 | I2C_WDT_STBY | 2-wire serial controller / target watch dog timer (Standby)<br>0 : Watch dog timer disable<br>1: 50ms<br>2: 151ms<br>3: 352ms<br>4: 755ms<br>5: 1.56s<br>6: 3.17s<br>7: 6.39s<br>8: 12.8s<br>9: 25.7s<br>10: 51.5s<br>11: 103s<br>12: 206s<br>13: 412s<br>14: 825s<br>15 : 1650s |
| | | 3:0 | R/W | 0xF | I2C_WDT | 2-wire serial controller / target watch dog timer (Normal operation)<br>Setting value of controller >= Setting value of target<br>0: Watch dog timer disable<br>Controller Target<br>1: 0.0123ms 0.0246ms<br>2: 0.0369ms 0.0738ms<br>3: 0.0860ms 0.172ms<br>4: 0.184ms 0.368ms<br>5: 0.381ms 0.762ms<br>6: 0.774ms 1.55ms<br>7: 1.56ms 3.12ms<br>8: 3.13ms 6.26ms<br>9: 6.28ms 12.6ms<br>10: 12.6ms 25.2ms<br>11: 25.2ms 50.4ms<br>12: 50.3ms 101ms<br>13: 101ms 202ms<br>14: 201ms 402ms<br>15: 403ms 806ms |
| 0x29 | 0xA9 | 4 | R/W | 0 | STBY_DRV | Standby mode CML differential output voltage setting<br>0: 200mV 1: 300mV |
| | | 3 | R/W | 0 | CMLPRE | Normal mode CML differential Pre-emphasis setting<br>0:0dB (default) 1: Depends on the CMLDRV |
| | | 2:1 | R/W | 0x1 | CMLDRV | Normal mode CML differential output voltage setting<br>0x0: 200mV<br>0x1: 300mV<br>0x2: 400mV<br>0x3: Prohibition |
| | | 0 | R/W | 0 | TTLDRV | LVCMOS output drive strength setting<br>0: Normal<br>1: High |
| 0x2A | 0xAA | 0 | R/W | 0 | Reserved | Must be 0 |
| 0x2B | 0xAB | 4:0 | R/W | 0x05 | SPREAD | SSCG modulation rate setting<br>Modulation rate = SPREAD * ±0.1%<br>Maximum ±0.5% |
| 0x2C | 0xAC | 2:0 | R/W | 0x6 | FMOD | SSCG modulation frequency(fmod)Setting<br>Maximum 30kHz<br>$f_{mod} = \frac{f_{ref}}{512 \times FMOD}$ |
| 0x2D | 0xAD | 1 | R/W | 0 | Reserved | Must be 0 |
| | | 0 | R/W | 0 | Reserved | Must be 0 |



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| | | | | | | |
|---|---|---|---|---|---|---|
| 0x2E | 0xAE | 7:0 | R/W | 0x00 | PWMH | PWMH period<br>0x00: When PWML=0x00, L fixed<br>0x01: H period 1 clock, (When PWML=0x00, H fixed)<br>~<br>0xFF: H period 255 clock |
| 0x2F | 0xAF | 7:0 | R/W | 0x00 | PWML | PWML period<br>0x00: When PWML=0x00, L fixed, When PWMH=0x01, H fixed.<br>0x01: H period 1 clock,<br>~<br>0xFF: H period 255 clock |
| 0x30 | 0xB0 | 0 | R/W | 0 | PWM_EN | PWM output enable |
| 0x31 | 0xB1 | 7:4 | R/W | 0x4 | STBY_NUM_DS | Number of Standby mode downstream GPIO setting: Maximum 0x8<br>(0x9-0xF is considered 0x8)<br>*Set primary chip only |
| | | 3:0 | R/W | 0x4 | STBY_NUM_US | Number of Standby mode upstream GPIO setting: Maximum 0x8<br>(0x9-0xF is considered 0x8)<br>*Set primary chip only |
| 0x32 | 0xB2 | 2:0 | R/W | 0x1 | STBY_CYCLE | Standby mode polling period setting<br>*Set primary chip only<br>0x0: 50ms<br>0x1: 100ms<br>0x2: 150ms<br>0x3: 200ms<br>0x4: 250ms<br>0x5: 300ms<br>0x6: 350ms<br>0x7: 400ms |
| 0x33 | 0xB3 | 0 | R/W | 0 | STBY_DOUT | Standby mode static GPIO output status<br>*Set by primary chip/secondary chip respectively<br>0: Hi-Z (default)<br>1: Holds status before standby mode entry |
| 0x34 | 0xB4 | 0 | R/W | 0 | STBY_MODE | Standby mode hand shake com start condition<br>0: Polling operation<br>1: Polling operation and external trigger |
| 0x35 | 0xB5 | 0 | R/W | 0 | STANDBY | 0: Normal operation 1: Standby |
| 0x36 | 0xB6 | 0 | R/W | 0 | Reserved | Must be 0 |
| 0x37 | 0xB7 | 7:4 | R | 0 | Reserved | Must be 0 |
| | | 3:0 | R | 0 | Reserved | Must be 0 |
| 0x38 | 0xB8 | 7:0 | R/W | 0x0F | Reserved | 0x0F fixed |
| 0x39 | 0xB9 | 7:0 | R/W | 0x1F | Reserved | 0x1F fixed |
| 0x3A | 0xBA | 3:0 | R/W | 0x4 | Reserved | 0x4 fixed |
| 0x3B | 0xBB | 7:0 | R | 0 | Reserved | Must be 0 |
| 0x3C | 0xBC | 4:0 | R | 0 | Reserved | Must be 0 |
| 0x3D | 0xBD | 7:0 | R/W | 0x00 | Reserved | Must be 0 |

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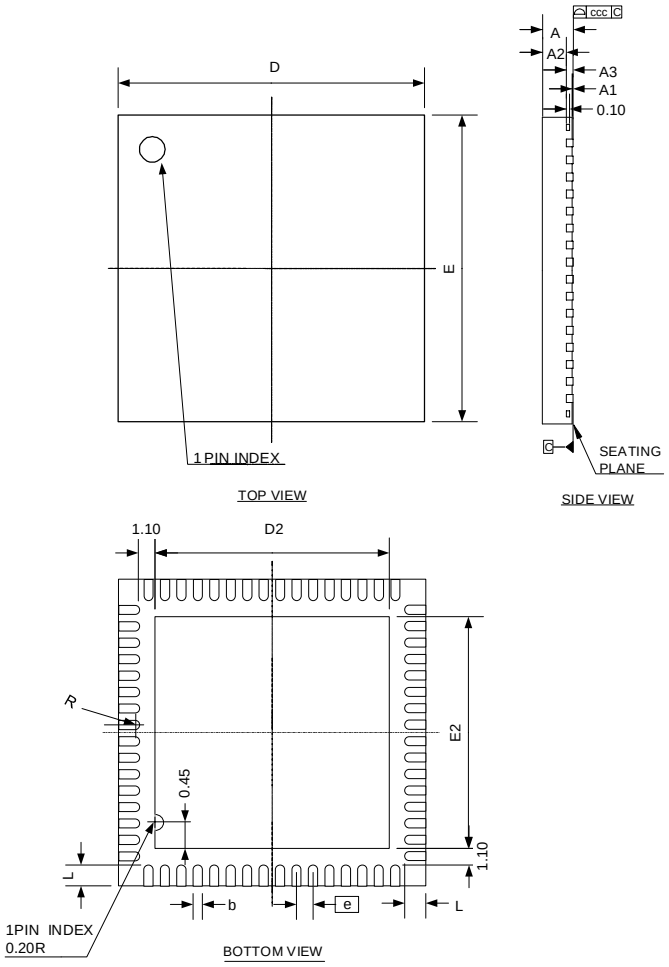
## 12. Package




Unit mm

| Symbol | Items | Min. | Nom. | Max. |
|---|---|---|---|---|
| A | Mounting Height | - | - | 0.90 |
| A1 | Standoff | - | - | 0.05 |
| A2 | - | - | 0.65 | 0.70 |
| A3 | - | | (0.20) | |
| b | Terminal Width | 0.18 | 0.25 | 0.30 |
| D | Body Length | | 9.00 BSC | |
| D2 | Exposed Length | 5.90 | 6.00 | 6.10 |
| E | Body Width | | 9.00 BSC | |
| E2 | Exposed Width | 5.90 | 6.00 | 6.10 |
| L | - | 0.35 | 0.40 | 0.45 |
| e | Pitch | | 0.50 BSC | |
| R | - | 0.09 | - | - |
| ccc | Coplanarity | | 0.05 | |

**Figure 24 64-pin QFN package physical dimension**

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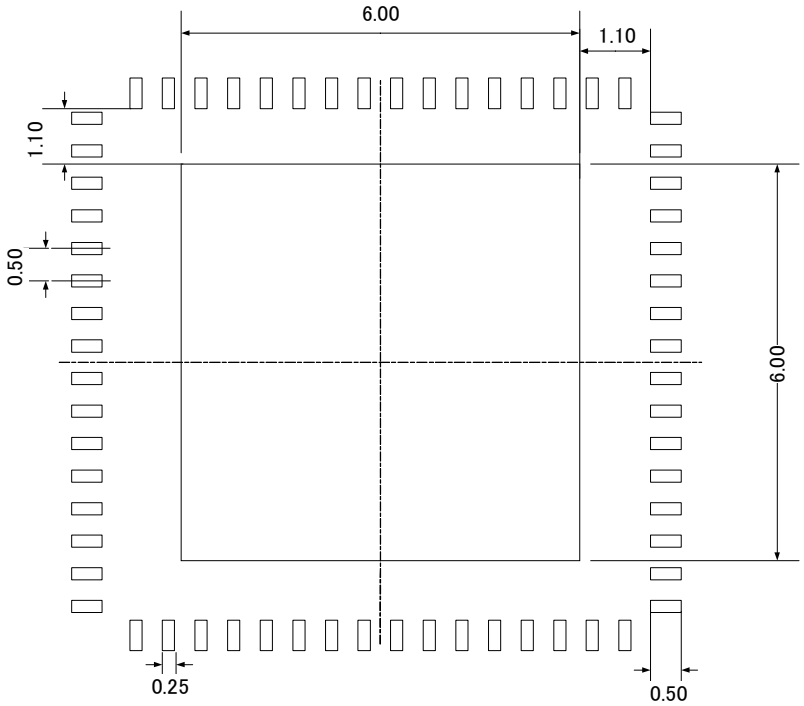
## 13. Reference land pattern




(Note)
Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjusts the Land Pattern at your own risk.
If there is any inconsistency or conflict between the English and Japanese versions, the English version shall prevail.

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