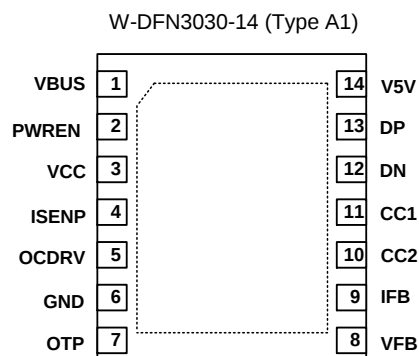


Description

The AP43771H, pin-to-pin upgrade part from AP43771V (W-DFN3030-14 (Type A1)), is a highly integrated USB Type-C® power delivery (PD) controller and targeted for premium USB Type-C adapter and charger applications. It supports USB power delivery specification Rev 3.1 V1.6 Extended Power Range (EPR) 28V (including AVS capability of 100mV/Step support).

The enhancements of AP43771H over existing AP43771V include efficiency improvement with R_{sense} 5mΩ option and enlarged SRAM size (1.5KB). Furthermore, the AP43771H implements a new CC1/CC2-short-to-VBUS protection up to 34V. To address higher output voltage and power requirements, AP43771H supports up PD3.1 to 28V VBUS output with AVS capability (100mV/Step).

Pin Assignments



Top View

Features

- Pin-to-Pin Upgrade to AP43771V
- Compatible with USB PD Rev 3.1 V1.6 (TID = 9275)
- 16KB OTP and 1.5KB SRAM to Support Software Encryption
- OTP for Main Firmware and MTP for System Configuration
- Built-in Regulator for CV and CC Control
- Two Options of Current Sensing Resistor (5mΩ or 10mΩ)
- Support SCP/OTP/OVP/UVP with Auto Restart
- CC1/CC2 Pins Short Protection to VBUS (Up to 34V)
- Support Power-Saving Mode
- Support e-Marker Cable Detection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact_us@diodes.com) or your local Diodes representative.**
<https://www.diodes.com/quality/product-definitions/>

Applications

- Type-C USB PD3.1 (EPR) 28V chargers

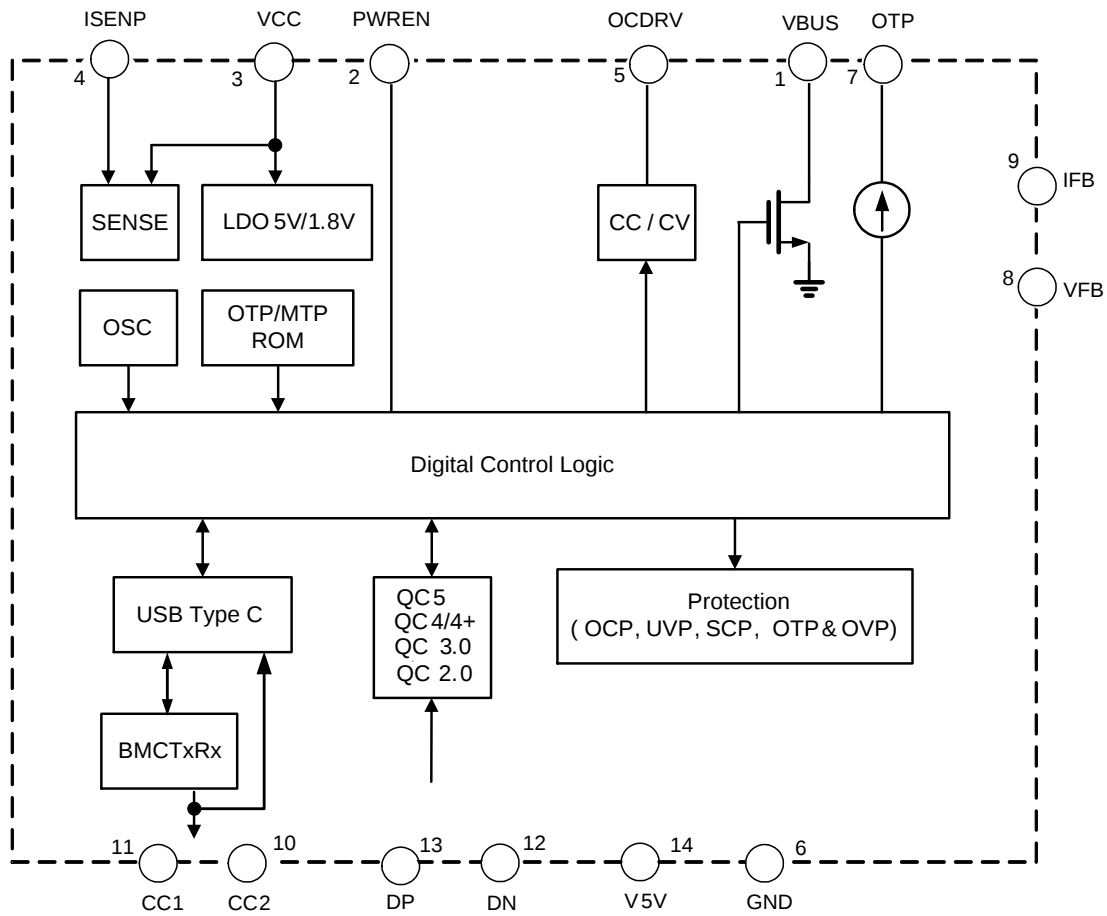
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

[illegible]

Figure 1. Single-Port USB PD Offline Charging with Analog Feedback Application

Pin Number	Pin Name	Function
1	VBUS	Output Terminal for Discharge Path.
2	PWREN	External nMOS Gate Driver. To control external MOS switch, 1: To enable VBUS voltage; 0: Disconnect VBUS.
3	VCC	The Power Supply of the Entire IC and the Input of Current Sense Negative Node. Connected to a ceramic capacitor.
4	ISENP	Input Current Sense Positive Node.
5	OCDRV	CC/CV Output. Open Drain Output for Optocoupler.
6	GND	Ground
7	OTP	Source Current to External NTC (Negative Temperature Coefficient) Resistor for OTP (Overtemperature Protection) management applications.
8	VFB	CV Input. Negative Node of CV OPAMP for Optocoupler.
9	IFB	CC Input. Negative Node of CC OPAMP for Optocoupler.
10	CC2	Type-C_CC2
11	CC1	Type-C_CC1
12	DN	Type-C_DN
13	DP	Type-C_DP
14	V5V	LDO-5V Output

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V _{CC}	Input Voltage at VCC Pin	-0.3 to 34	V
V _{FB} , V _{IFB}	Input Voltage at VFB, IFB Pins	-0.3 to 7	V
V _{BUS} , V _{ISENP} , V _{OCDRV}	Input Voltage at VBUS, ISENP, OCDRV Pins	-0.3 to 34	V
V _{PWREN}	Input Voltage at PWREN Pin	-0.3 to 36	V
V _{V5V}	Input Voltage at V5V Pin	-0.3 to 7	V
V _{DP} , V _{DN}	Input Voltage at DP, DN Pins	-0.3 to 7	V
V _{CC1} , V _{CC2}	Input Voltage at CC1, CC2 Pins	-0.3 to 34	V
V _{OTP}	Input Voltage at OTP Pin	-0.3 to 7	V
T _J	Operating Junction Temperature	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ _{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	54	°C/W
θ _{JC}	Thermal Resistance (Junction to Case) (Note 5)	34	°C/W
—	ESD (Human Body Model) Voltage on DP, DN Pins	8	kV
—	ESD (Human Body Model) Voltage on CC1, CC2 Pins	4	kV
—	ESD (Human Body Model) Voltage on VBUS, ISENP, PWREN, VCC, OCDRV, OTP, V5V, IFB, VFB Pins	2	kV
—	ESD (Charged Device Model)	750	V

- Notes:
- Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
 - Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	Power Supply Voltage	3.3	34	V
T _{OP}	Operating Temperature Range	-40	+85	°C

Electrical Characteristics (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC PIN SECTION						
V _{ST}	Startup Voltage	—	2.5	2.8	3.2	V
V _{UVLO}	Minimum Operating Voltage	—	2.4	2.7	3	V
V _{CC_HYS}	V _{CC} Hysteresis (V _{ST} -V _{UVLO})	—	0.05	—	—	V
I _{CC_DEEP SLEEP}	V _{IN} Current in Deep Sleep Mode	CC1/2 Detach after 3s V _{CC} = 5V	—	550	900	μA
I _{CC_OPR}	Operating Supply Current	V _{CC} = 5V	—	3.3	6	mA
VOLTAGE CONTROL LOOP SECTION						
V _{REF_CV5}	Reference Voltage for 5V CV Control	—	4.85	5	5.15	V
V _{REF_CV9}	Reference Voltage for 9V CV Control	—	8.73	9	9.27	V
V _{REF_CV20}	Reference Voltage for 20V CV Control	—	19.4	20	20.6	V
V _{CABLE}	Cable Compensation (Notes 6 & 7)	—	—	30	—	mV/A
I _{OS}	Maximum OCDRV Pin Sink Current	V _{OUT} = 5V	1.2	4	6	mA
PROTECTION FUNCTION SECTION						
V _{OVP5V}	OVP_5V Enable Voltage (Note 8)	—	5.6	6	6.6	V
V _{OVP9V}	OVP_9V Enable Voltage (Note 8)	—	9.9	10.8	12.1	V
V _{OVP20V}	OVP_20V Enable Voltage (Note 8)	—	22	24	26	V
t _{DEBOUNCE_OVP}	OVP Debounce Time (Note 9)	—	—	90	—	ms
V _{UVP5V}	UVP_5V Enable Voltage	—	3.3	3.7	4.4	V
V _{UVP9V}	UVP_9V Enable Voltage	—	5.9	6.8	7.7	V
V _{UVP20V}	UVP_20V Enable Voltage	—	13.2	15.2	16.7	V
I _{OVD}	Overvoltage Discharge Current	V _{CC} = 5V	150	200	250	mA
t _{OCP}	OCP Deglitch Time (Note 7)	—	—	30	—	ms
t _{RESTART_INTERVAL_SCP}	Restart Interval Time under SCP (Note 7)	—	—	0.8	—	s
T _{OTP}	Internal OTP Temperature	—	—	+140	—	°C
I _{OTP_EXTERNAL}	External OTP Current	—	90	100	110	μA
PROTECTION FUNCTION SECTION						
T _{HYS}	OTP Recovery Hysteresis Temperature	—	—	+25	—	°C
t _{SLEEP}	Enter Sleep Mode Time after Cable Detached (Note 7)	—	—	3	—	s
t _{OV_DELAY}	Delay from OVP Threshold Trip to nMOS Gate Turn-Off (Note 7)	—	—	—	50	μs
t _{UV_DELAY}	Delay from UVP Threshold Trip to nMOS Gate Turn-Off (Note 7)	—	—	30	—	ms
CC1/CC2, DP/DN PIN SECTION						
V _{L_RD3A}	Low Voltage Threshold Used to Distinguish R _D Attached or Detached for 3A Delivery	—	—	1.35	—	V
V _{H_RD3A}	High Voltage Threshold Used to Distinguish R _D Attached or Detached for 3A Delivery	—	—	2.0	—	V
I _{RD3A}	CC1/CC2 Current Source for 3A Advertisement	V _{CC} = 5V	304	330	356	μA
V _{OVP_DN}	DN Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V
V _{OVP_DP}	DP Line Overvoltage Protection Threshold	—	4.1	4.5	4.8	V

- Notes:
6. Cable compensation voltage can be adjusted by setting from 0 to V_{CABLE} * N (N: 0 to 7).
 7. Guaranteed by design.
 8. 120% OVP setting & 76% UVP setting.
 9. OVP blanking time during V_O transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

Functional Description

AP43771H Improvement Overview

The enhanced Power Delivery (PD) controller AP43771H is a new generation PD controller enhanced with key features suitable for various applications over previous versions (AP43771V). Most noticeable desired improvements are efficiency, protection, ease of manufacturing and inventory management, system BOM optimization for multiple-port charging applications.

AP43771H's CC1/CC2 pins support strong overvoltage protection to VBUS (up to 34V).

Due to the pin-to-pin compatible design, the AP43771H (W-DFN3030-14 (Type A1)) could be conveniently used for replacing existing AP43771V (W-DFN3030-14 (Type A1)) design with little fine tuning effort for CV and CC loops.

System Power-on Sequence

When the external power source is turned on through VCC pin, the AP43771H wakes up, and the USB PD controller and MCU is initialized. All analog control blocks are ready and waiting for PD negotiation process. Meanwhile, the AP43771H monitors the voltage and current conditions to avoid abnormal conditions. Once any unacceptable condition happens, the AP43771H goes into protection procedure according to the types of abnormal conditions.

Voltage Transition

According to USB PD protocol, the PD device requests different power profile and the AP43771H's power control blocks will change voltage and current values. The AP43771H provides corresponding Overvoltage Protection (OVP), Overcurrent Protection (OCP) scheme, and feedback system stability to guarantee monotonic voltage transition and avoid violating USB PD electrical specification.

The AP43771H provides zero-mismatch voltage methodology that is more flexible to meet system design requirements. When UFP/DFP makes an acceptable power request deal, the AP43771H changes the VFB pin voltage according to the USB PD command. The voltage regulator control loop regulates the required VBUS voltage according to VFB. In addition, the shunt regulator is built-in to minimize the total external components and cost.

Protection

The AP43771H provides OVP/UVP/OCP/SCP/OTP functions and support Constant Current (CC) function. All of the protection thresholds depend on the requested power profile, and provide the most reliable protection scheme.

The AP43771H provides OVP feature by turning off the power switch when VBUS is higher than OVP enable voltage. Meanwhile, it provides internal discharge path to reduce the overvoltage duration, and terminates discharge current as soon as VBUS reaches the target voltage. To prevent the VBUS pin from working abnormally, the AP43771H provides UVP function whenever VBUS drops to UVP enable voltage.

To ensure the safe operation of USB PD, the AP43771H provides programmable OCP function to make sure output current will not be higher than the allowed maximum current. Once OCP conditions happen, the AP43771H will shut down the USB PD system and send "Hard Reset" to the Upstream-Facing Port (UFP) device.

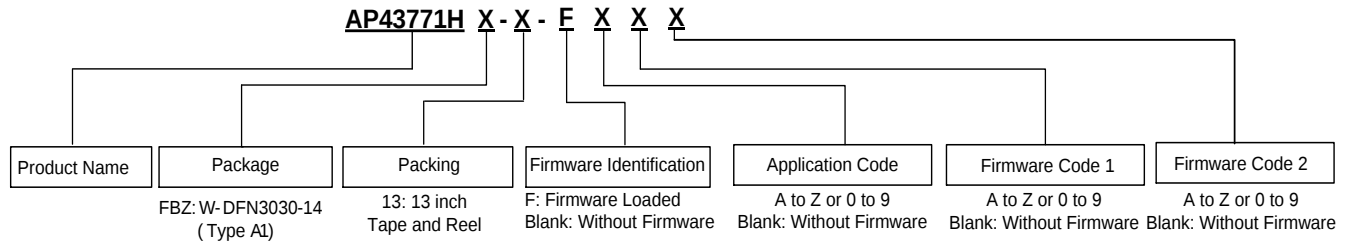
To prevent inadvertent short between CC1/2 pins with adjacent high-voltage pins (VBUS) due to foreign objects, CC1 and CC2 pins for the AP43771H are further protected up to 34V.

CV/CC Feedback Loop Configuration

The AP43771H supports Constant Voltage (CV) and Constant Current (CC) functions to control the output voltage and the output current by the control pin OCDRV. During the CV mode, the AP43771H operates in fixed PDO, and the output voltage is regulated to the request voltage if the output current is below the allowed maximum current. Once the sink device draws more than I_{OCP}, the overcurrent protection occurs. When the CC mode function is enabled, the output voltage drops, and the source current is limited within 150mA whenever output current exceeds the allowed maximum current. When the output voltage drops below UVP, constant current limit turns off VBUS and starts error recovery procedure. The AP43771H resets if the voltage continues dropping to UVLO threshold.

Figure 1 shows a typical analog feedback configuration in a flyback power. The CV/CC loop of the charger is formed by connecting OCDRV pin of the AP43771H to drive optocoupler to drive FB pin of the associated PWM controller to achieve desired output voltage and current, which is the analog feedback approach.

Ordering Information

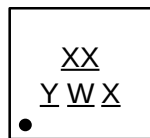


Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP43771HFBZ-13-FXXX	W-DFN3030-14 (Type A1)	4T	3000	Tape and Reel

Marking Information

W-DFN3030-14 (Type A1)

(Top View)

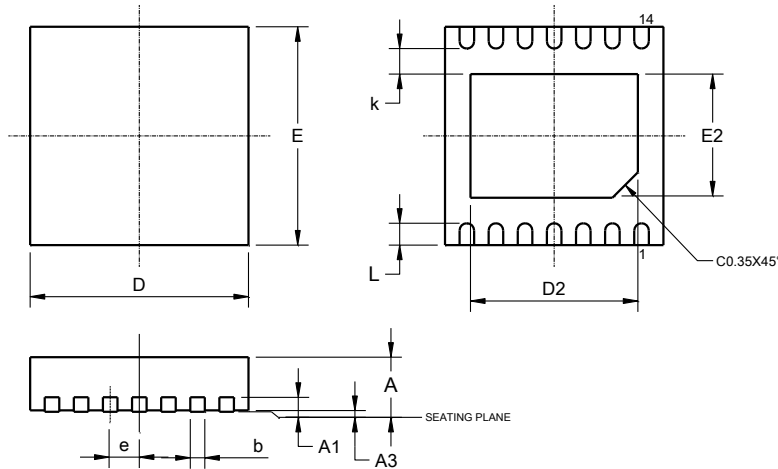


XX : Identification Code
 Y : Year : 0 to 9 (ex: 3 = 2023)
 W : Week : A to Z : week 1 to 26;
 a to z : week 27 to 52; z represents
 week 52 and 53
 X : Internal Code

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-14 (Type A1)

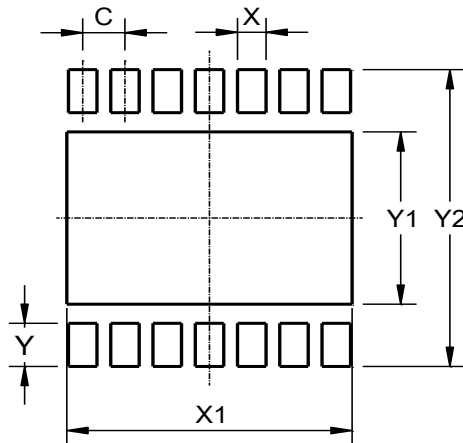


W-DFN3030-14 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-14 (Type A1)



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 (e3)
- Weight: 0.017 grams (Approximate)

IMPORTANT NOTICE

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).
2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.
3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.
4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.
5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.
7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.
8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.
9. This Notice may be periodically updated with the most recent version available at <https://www.diodes.com/about/company/terms-and-conditions/important-notice>

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.
All other trademarks are the property of their respective owners.
© 2023 Diodes Incorporated. All Rights Reserved.

www.diodes.com