

# NTTFS4929N

## MOSFET – Power, Single, N-Channel, $\mu$ 8FL 30 V, 34 A

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- DC-DC Converters
- Power Load Switch
- Notebook Battery Management
- Motor Control

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain Current R <sub>θJA</sub> (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	10.6	A
		T <sub>A</sub> = 85°C		7.7	
Power Dissipation R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 25°C	P <sub>D</sub>	2.11	W
Continuous Drain Current R <sub>θJA</sub> ≤ 10 s (Note 1)		T <sub>A</sub> = 25°C	I <sub>D</sub>	14.3	A
		T <sub>A</sub> = 85°C		10.3	
Power Dissipation R <sub>θJA</sub> ≤ 10 s (Note 1)		T <sub>A</sub> = 25°C	P <sub>D</sub>	3.83	W
Continuous Drain Current R <sub>θJA</sub> (Note 2)		T <sub>A</sub> = 25°C	I <sub>D</sub>	6.6	A
		T <sub>A</sub> = 85°C		4.7	
Power Dissipation R <sub>θJA</sub> (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.81	W
Continuous Drain Current R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 25°C	I <sub>D</sub>	34	A
	T <sub>C</sub> = 85°C	25			
Power Dissipation R <sub>θJC</sub> (Note 1)	T <sub>C</sub> = 25°C	P <sub>D</sub>	22.3	W	
Pulsed Drain Current	T <sub>A</sub> = 25°C, t <sub>p</sub> = 10 μs		I <sub>DM</sub>	115	A
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)			I <sub>S</sub>	22	A
Drain to Source dV/dt			dV/dt	6.0	V/ns

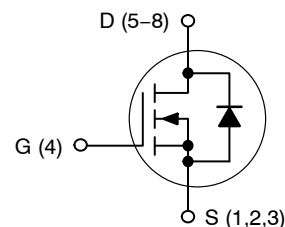


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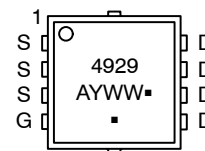
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	11 m $\Omega$ @ 10 V	34 A
	17 m $\Omega$ @ 4.5 V	

### N-Channel MOSFET



WDFN8  
( $\mu$ 8FL)  
CASE 511AB

### MARKING DIAGRAM



4929 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTTFS4929NTAG	WDFN8 (Pb-Free)	1500/Tape & Reel
NTTFS4929NTWG	WDFN8 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

Parameter	Symbol	Value	Unit
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}$ , $V_{DD} = 50\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_L = 18\text{ A}_{pk}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	16.2	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

**THERMAL RESISTANCE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	5.6	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	59.2	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	155	
Junction-to-Ambient – ( $t \leq 10\text{ s}$ ) (Note 3)	$R_{\theta JA}$	32.6	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
4. Surface-mounted on FR4 board using the minimum recommended pad size (40 mm<sup>2</sup>, 1 oz. Cu).

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			24		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS** (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1.2	1.6	2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.3		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	8.8	11	m $\Omega$
			$I_D = 8\text{ A}$	8.8		
		$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$	12.7	17	
			$I_D = 8\text{ A}$	12.7		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}$ , $I_D = 15\text{ A}$		26		S

**CHARGES AND CAPACITANCES**

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ , $V_{DS} = 15\text{ V}$		920		pF
Output Capacitance	$C_{oss}$			337		
Reverse Transfer Capacitance	$C_{rss}$			175		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}$ , $V_{DS} = 15\text{ V}$ , $I_D = 20\text{ A}$		8.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			3.1		
Gate-to-Source Charge	$Q_{GS}$			2.8		
Gate-to-Drain Charge	$Q_{GD}$			4.4		

5. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .
6. Switching characteristics are independent of operating junction temperatures.

# NTTFS4929N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### CHARGES AND CAPACITANCES

Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		16.3		nC
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### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		9.6		ns
Rise Time	t <sub>r</sub>			24		
Turn-Off Delay Time	t <sub>d(off)</sub>			14		
Fall Time	t <sub>f</sub>			6.1		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		6.4		ns
Rise Time	t <sub>r</sub>			18.7		
Turn-Off Delay Time	t <sub>d(off)</sub>			17.8		
Fall Time	t <sub>f</sub>			3.9		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 25°C		0.9	1.1	V
			T <sub>J</sub> = 125°C		0.80		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dI <sub>t</sub> = 100 A/μs, I <sub>S</sub> = 20 A			22		ns
Charge Time	t <sub>a</sub>				9.5		
Discharge Time	t <sub>b</sub>				12.3		
Reverse Recovery Charge	Q <sub>RR</sub>				9.1		nC

### PACKAGE PARASITIC VALUES

Source Inductance	L <sub>S</sub>	T <sub>A</sub> = 25°C		0.38		nH
Drain Inductance	L <sub>D</sub>			0.054		
Gate Inductance	L <sub>G</sub>			1.3		
Gate Resistance	R <sub>G</sub>			0.6		Ω

5. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

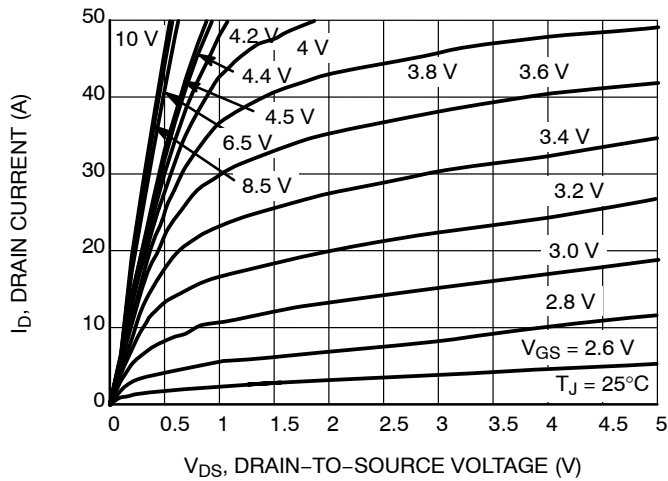


Figure 1. On-Region Characteristics

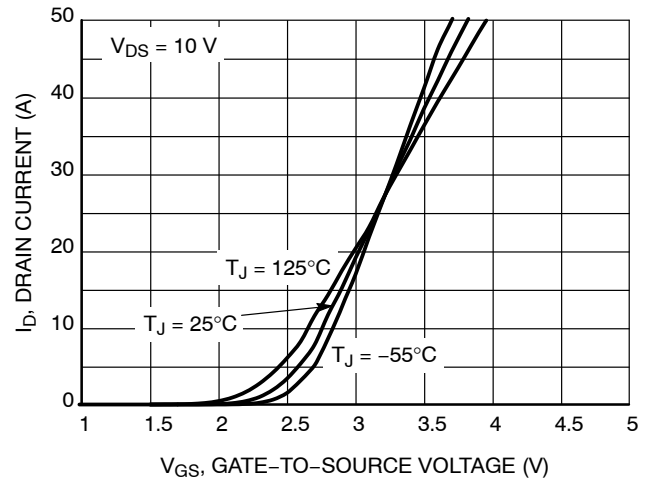


Figure 2. Transfer Characteristics

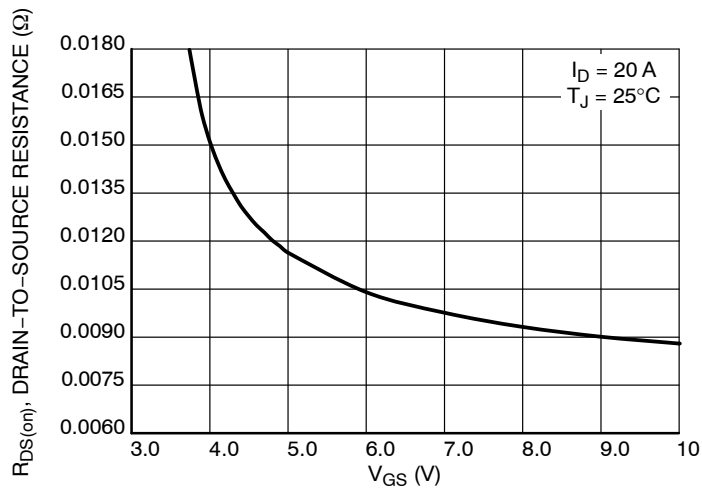


Figure 3. On-Resistance vs.  $V_{GS}$

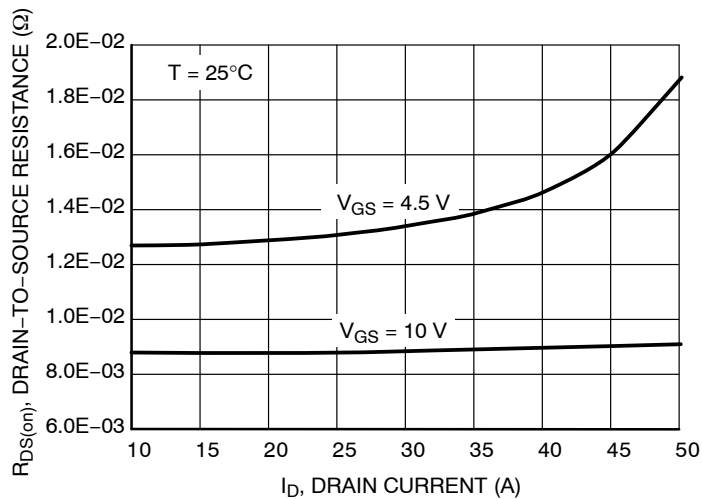


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS

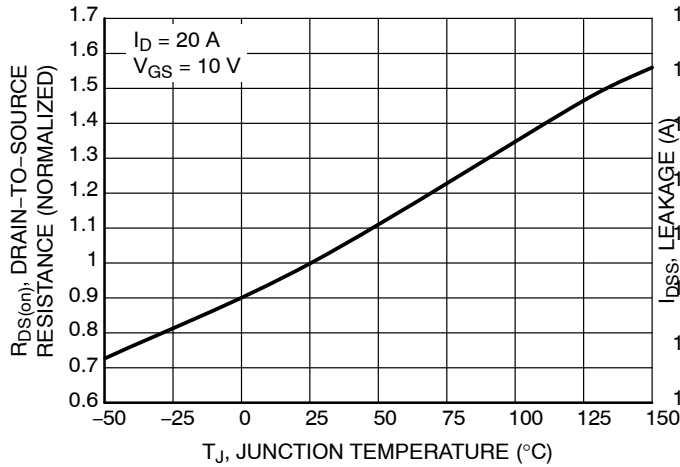


Figure 5. On-Resistance Variation with Temperature

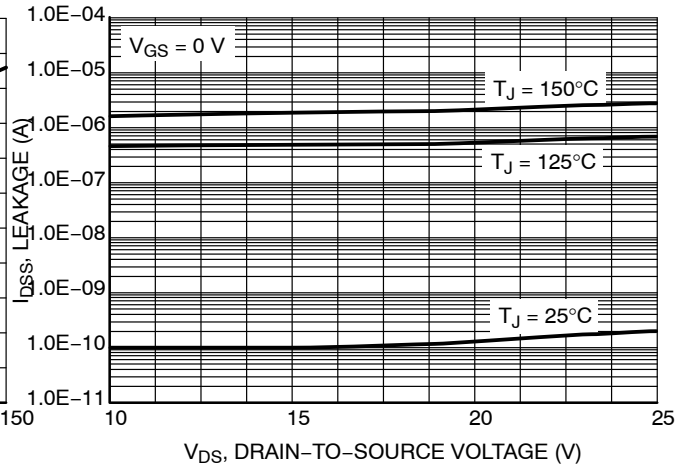


Figure 6. Drain-to-Source Leakage Current vs. Voltage

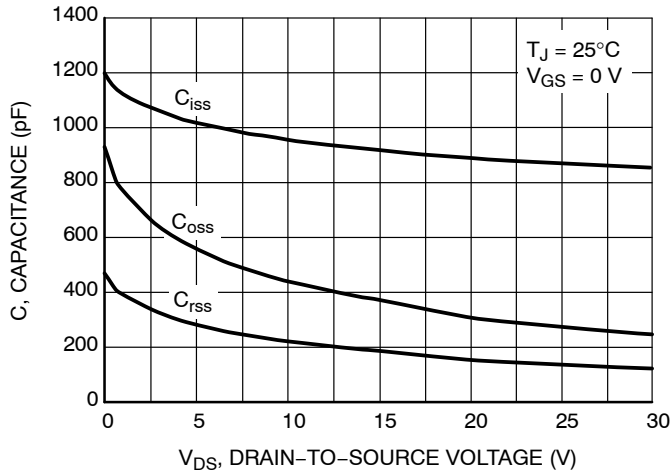


Figure 7. Capacitance Variation

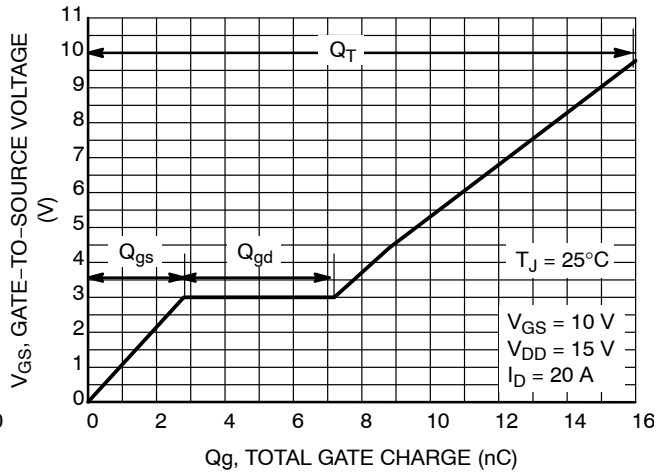


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

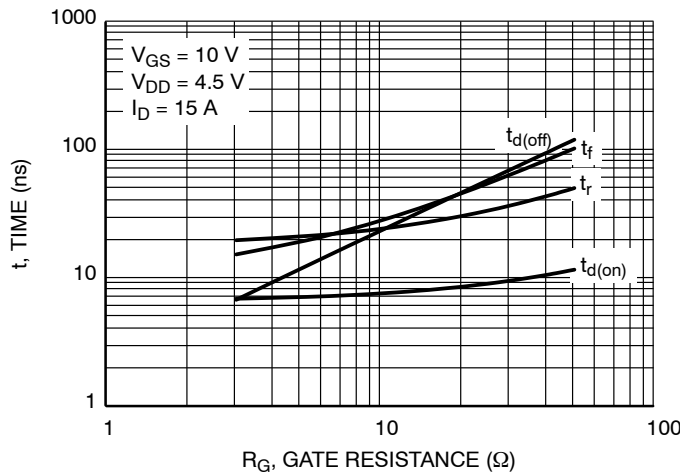


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

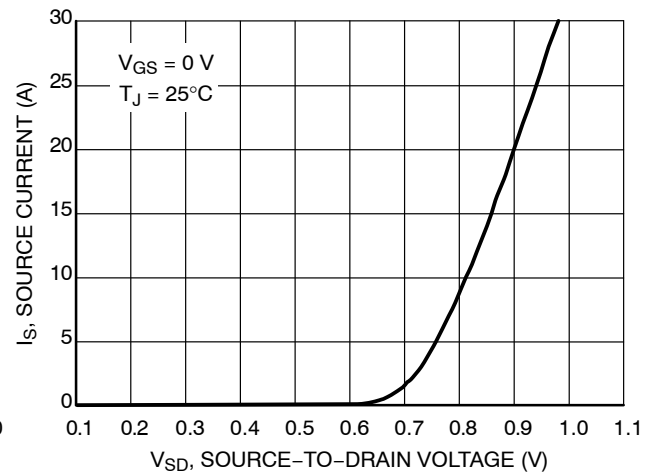


Figure 10. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

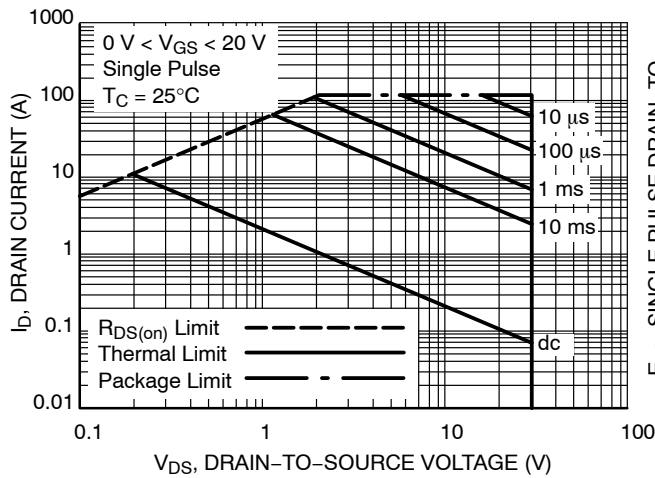


Figure 11. Maximum Rated Forward Biased Safe Operating Area

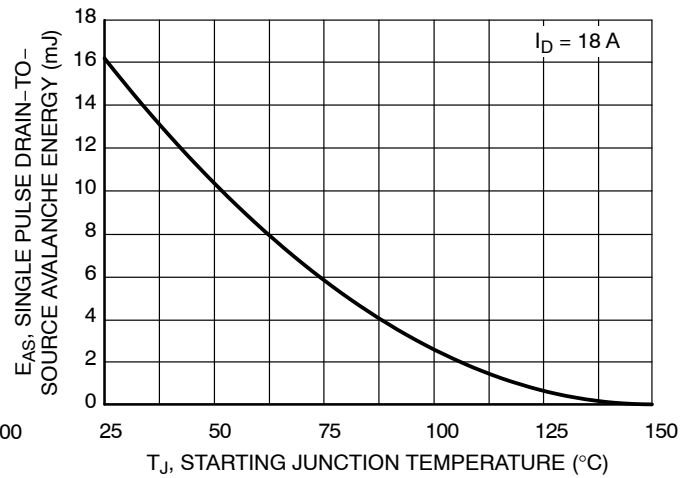


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

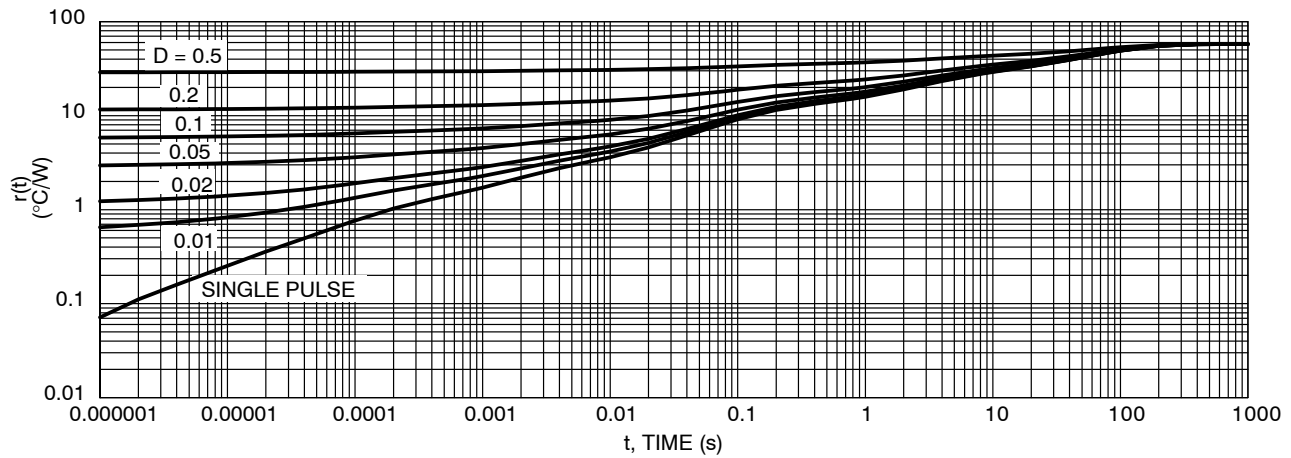


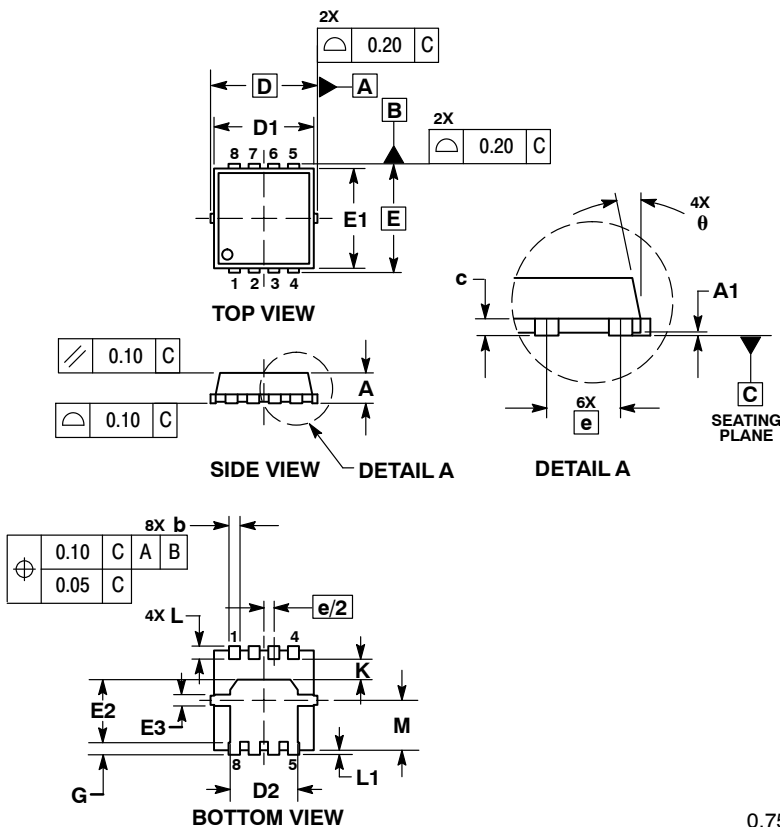
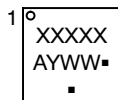
Figure 13. Thermal Response



SCALE 2:1

**WDFN8 3.3x3.3, 0.65P**  
CASE 511AB  
ISSUE D

DATE 23 APR 2012


**GENERIC MARKING DIAGRAM\***


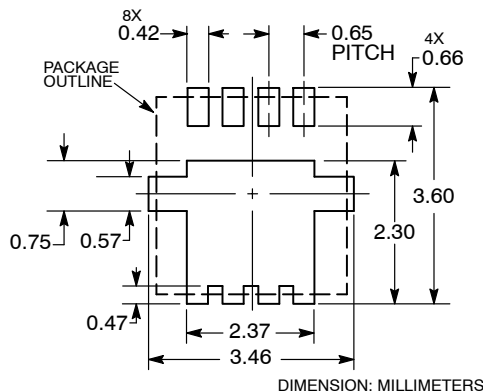
XXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

**SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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