16-Bit, Multi-Channel ΔΣ Analog-to-Digital Converter with I^2C™ Interface and On-Board Reference

**Features**

- 16-bit ΔΣ ADC with Differential Inputs:
  - 2 channels: MCP3426 and MCP3427
  - 4 channels: MCP3428
- Differential Input Full Scale Range: \(-\text{V}_{\text{REF}}\) to \(+\text{V}_{\text{REF}}\)
- Self Calibration of Internal Offset and Gain per Each Conversion
- On-Board Voltage Reference (\(\text{V}_{\text{REF}}\)):
  - Accuracy: 2.048V ± 0.05%
  - Drift: 15 ppm/°C
- On-Board Programmable Gain Amplifier (PGA):
  - Gains of 1, 2, 4 or 8
- INL: 10 ppm of Full Scale Range
- Programmable Data Rate Options:
  - 15 SPS (16 bits)
  - 60 SPS (14 bits)
  - 240 SPS (12 bits)
- One-Shot or Continuous Conversion Options
- Low Current Consumption (\(\text{V}_{\text{DD}}=3\) V):
  - Continuous Conversion: 135 \(\mu\)A typical
  - One-Shot Conversion with 1 SPS:
    - 9 \(\mu\)A typical for 16 bit mode
    - 2.25 \(\mu\)A typical for 14 bit mode
    - 0.56 \(\mu\)A typical for 12 bit mode
- On-Board Oscillator
- I^2C™ Interface:
  - Standard, Fast and High Speed Modes
  - User configurable two external address selection pins for MCP3427 and MCP3428
- Single Supply Operation: 2.7V to 5.5V
- Extended Temperature Range: \(-40°C\) to \(+125°C\)

**Typical Applications**

- Portable Instrumentation and Consumer Goods
- Temperature Sensing with RTD, Thermistor, and Thermocouple
- Bridge Sensing for Pressure, Strain, and Force
- Weigh Scales and Battery Fuel Gauges
- Factory Automation Equipment

**Description**

The MCP3426, MCP3427 and MCP3428 devices (MCP3426/7/8) are the low noise and high accuracy 16-Bit Delta-Sigma Analog-to-Digital (ΔΣ A/D) Converter family members of the MCP342X series from Microchip Technology Inc. These devices can convert analog inputs to digital codes with up to 16 bits of resolution.

The MCP3426 and MCP3427 devices have two differential input channels and the MCP3428 has four differential input channels. All electrical properties of these three devices are the same except for differences in the number of input channels and I^2C address bit selection options.

These devices can output analog-to-digital conversion results at rates of 15 (16-bit mode), 60 (14-bit mode), or 240 (12-bit mode) samples per second depending on the user controllable configuration bit settings using the two-wire I^2C serial interface. During each conversion, the device calibrates offset and gain errors automatically. This provides accurate conversion results from conversion to conversion over variations in temperature and power supply fluctuation.

The device has an on-board 2.048V reference voltage, which enables an input range of ± 2.048V differentially (full scale range = 4.096/PGA).

The user can select the gain of the on-board programmable gain amplifier (PGA) using the configuration register bits (gain of \(x1, x2, x4,\) or \(x8\)). This allows the MCP3426/7/8 devices to convert a very weak input signal with high resolution.

The MCP3426/7/8 devices have two conversion modes: (a) One-Shot Conversion mode and (b) Continuous Conversion mode. In the One-Shot conversion mode, the device performs a single conversion and enters a low current standby (shutdown) mode automatically until it receives another conversion command. This reduces current consumption greatly during idle periods. In continuous conversion mode, the conversion takes place continuously at the configured conversion speed. The device updates its output buffer with the most recent conversion data.

The devices operate from a single 2.7V to 5.5V power supply and have a two-wire I^2C compatible serial interface for a standard (100 kHz), fast (400 kHz), or high-speed (3.4 MHz) mode.
The I²C address bits for the MCP3427 and MCP3428 are selected by using two external I²C address selection pins (Adr0 and Adr1). The user can configure the device to one of eight available addresses by connecting these two address selection pins to V_DD, V_SS or float. The I²C address bits of the MCP3426 are programmed at the factory during production.

The MCP3426 is available in 8-pin SOIC, DFN, and MSOP packages. The MCP3427 is available in 10-pin DFN, and MSOP packages. The MCP3428 is available in 14-pin SOIC and TSSOP packages.

Packaging Information

<table>
<thead>
<tr>
<th>Package Type</th>
<th>MCP3426</th>
<th>MCP3427</th>
<th>MCP3428</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSOP, SOIC</td>
<td>2x3 DFN</td>
<td>3x3 DFN</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>CH1+</td>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>CH1-</td>
<td>3</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>SDA</td>
<td>4</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>SCL</td>
<td>5</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

* Includes Exposed Thermal Pad (EP); see Table 3-1.

MCP3426 Functional Block Diagram
MCP3427 Functional Block Diagram

MCP3428 Functional Block Diagram
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VDD.................................................................7.0V
All inputs and outputs ..............VSS –0.4V to VDD+0.4V
Differential Input Voltage .........................|VDD - VSS|
Output Short Circuit Current ......................Continuous
Current at Input Pins ........................................2 mA
Current at Output and Supply Pins .............±10 mA
Storage Temperature .........................-65°C to +150°C
Ambient Temp. with power applied ..........-55°C to +125°C
ESD protection on all pins ..........≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (TJ) ............+150°C

†Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Inputs</td>
<td>FSR</td>
<td>±2.048/PGA-</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Input Voltage Range</td>
<td>VSS-0.3-</td>
<td>VDD+0.3</td>
<td>V</td>
<td>(Note 1)</td>
<td></td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>ZIND (f)</td>
<td>2.25/PGA-</td>
<td>MΩ</td>
<td>During normal mode operation (Note 2)</td>
<td></td>
</tr>
<tr>
<td>Common Mode input Impedance</td>
<td>ZINC (f)</td>
<td>25</td>
<td>MΩ</td>
<td>PGA = 1, 2, 4, 8</td>
<td></td>
</tr>
</tbody>
</table>

System Performance

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution and No Missing Codes (Effective Number of Bits) (Note 3)</td>
<td>12</td>
<td>—</td>
<td>—</td>
<td>Bits</td>
<td>DR = 240 SPS</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>—</td>
<td>—</td>
<td>Bits</td>
<td>DR = 60 SPS</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>—</td>
<td>—</td>
<td>Bits</td>
<td>DR = 15 SPS</td>
</tr>
<tr>
<td>Data Rate (Note 4)</td>
<td>DR</td>
<td>176</td>
<td>240</td>
<td>328</td>
<td>SPS</td>
</tr>
<tr>
<td></td>
<td>44</td>
<td>60</td>
<td>82</td>
<td>SPS</td>
<td>14 bits mode</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>15</td>
<td>20.5</td>
<td>SPS</td>
<td>16 bits mode</td>
</tr>
<tr>
<td>Output Noise</td>
<td>—</td>
<td>2.5</td>
<td>—</td>
<td>µV RMS</td>
<td>TX = +25°C, DR = 15 SPS, PGA = 1, VIN+ = VIN- = GND</td>
</tr>
<tr>
<td>Integral Non-Linearity</td>
<td>INL</td>
<td>10</td>
<td>—</td>
<td>ppm of FSR</td>
<td>DR = 15 SPS (Note 5)</td>
</tr>
<tr>
<td>Internal Reference Voltage</td>
<td>VREF</td>
<td>—</td>
<td>2.048</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Gain Error (Note 6)</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>%</td>
<td>PGA = 1, DR = 15 SPS</td>
</tr>
<tr>
<td>PGA Gain Error Match (Note 6)</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>%</td>
<td>Between any 2 PGA settings</td>
</tr>
<tr>
<td>Gain Error Drift (Note 6)</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>ppm/°C</td>
<td>PGA=1, DR=15 SPS</td>
</tr>
</tbody>
</table>

Note 1: Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
Note 2: This input impedance is due to 3.2 pF internal input sampling capacitor.
Note 3: This parameter is ensured by design and not 100% tested.
Note 4: The total conversion speed includes auto-calibration of offset and gain.
Note 5: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
Note 6: Includes all errors from on-board PGA and VREF.
ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for $T_A = -40°C$ to $+85°C$, $V_{DD} = +5.0V$, $V_{SS} = 0V$, $CHn+ = CHn- = V_{REF}/2$, $V_{INCOM} = V_{REF}/2$. All ppm units use $2V_{REF}$ as differential full scale range.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Error</td>
<td>$V_{OS}$</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>$\mu V$</td>
<td>PGA = 1, DR = 15 SPS</td>
</tr>
<tr>
<td>Offset Drift vs. Temperature</td>
<td></td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>nV/°C</td>
<td>at DC and PGA =1,</td>
</tr>
<tr>
<td>Common-Mode Rejection</td>
<td></td>
<td>—</td>
<td>105</td>
<td>—</td>
<td>dB</td>
<td>at DC and PGA =8, $T_A = +25°C$</td>
</tr>
<tr>
<td>Gain vs. $V_{DD}$</td>
<td></td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ppm/V</td>
<td>$T_A = +25°C$, $V_{DD} = 2.7V$ to $5.5V$, PGA = 1</td>
</tr>
<tr>
<td>Power Supply Rejection at DC Input</td>
<td></td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>dB</td>
<td>$T_A = +25°C$, $V_{DD} = 2.7V$ to $5.5V$, PGA = 1</td>
</tr>
</tbody>
</table>

Power Requirements

| Voltage Range                           | $V_{DD}$ | 2.7 | —   | 5.5 | V     |                               |
| Supply Current during Conversion        | $I_{DDA}$ | —   | 145 | 180 | $\mu A$ | $V_{DD} = 5.0V$ |
| Supply Current during Standby Mode      | $I_{DDS}$ | —   | 0.3 | 1   | $\mu A$ | $V_{DD} = 5.0V$ |

I2C Digital Inputs and Digital Outputs

| High level input voltage               | $V_{IH}$ | 0.7$V_{DD}$ | —   | $V_{DD}$ | V | at SDA and SCL pins |
| Low level input voltage                | $V_{IL}$ | —             | —   | 0.3$V_{DD}$ | V | at SDA and SCL pins |
| Low level output voltage               | $V_{OL}$ | —             | —   | 0.4      | V | $I_{OL} = 3 mA$ |
| Hysteresis of Schmidt Trigger for inputs (Note 7) | $V_{HYST}$ | 0.05$V_{DD}$ | —   | —   | V | $f_{SCL} = 100 kHz$ |
| Supply Current when I2C bus line is active | $I_{I\!\!\!DB}$ | —   | —   | 10     | $\mu A$ | Device is in standby mode while I2C bus is active |
| Input Leakage Current                  | $I_{ILH}$ | —   | —   | 1     | $\mu A$ | $V_{IH} = 5.5V$ |
|                                       | $I_{ILL}$ | -1  | —   | —     | $\mu A$ | $V_{IL} = GND$ |

Logic Status of I2C Address Pins (Note 8)

| Adr0 and Adr1 Pins                      | Addr_Low | $V_{SS}$ | —   | 0.2$V_{DD}$ | V | The device reads logic low. |
| Adr0 and Adr1 Pins                      | Addr_High | 0.75$V_{DD}$ | —   | $V_{DD}$ | V | The device reads logic high. |
| Adr0 and Adr1 Pins                      | Addr_Float | 0.35$V_{DD}$ | —   | 0.6$V_{DD}$ | V | Read pin voltage if voltage is applied to the address pin. (Note 9) |

| Pin Capacitance and I2C Bus Capacitance | $C_{PIN}$ | —   | 4   | 10  | pF   |                               |
|                                        | $C_{B}$   | —   | 400 | pF  |       |

Note 1: Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.

Note 2: This parameter is ensured by design and not 100% tested.

Note 3: This parameter is ensured by characterization and not 100% tested.

Note 4: The total conversion speed includes auto-calibration of offset and gain.

Note 5: This parameter is ensured by characterization and not 100% tested.

Note 6: This parameter is ensured by characterization and not 100% tested.

Note 7: Includes all errors from on-board PGA and $V_{REF}$.

Note 8: This parameter is ensured by characterization and not 100% tested.

Note 9: Addr_Float voltage is applied at address pin.

Note 10: Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins.
## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = +5.0\text{V}$, $V_{SS} = 0\text{V}$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td><strong>Thermal Package Resistances</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-DFN (2x3)</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>84.5</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>211</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-SOIC</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>149.5</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 10L-DFN (3x3)</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>57</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 10L-MSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>202</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-SOIC</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 14L-TSSOP</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = -40^\circ C$ to $+85^\circ C$, $V_{DD} = +5.0V$, $V_{SS} = 0V$, $CHn^+ = CHn^- = V_{REF}/2$, $V_{INCOM} = V_{REF}/2$.

**FIGURE 2-1:** INL vs. Supply Voltage ($V_{DD}$).

**FIGURE 2-2:** INL vs. Temperature.

**FIGURE 2-3:** Offset Error vs. Temperature.

**FIGURE 2-4:** Output Noise vs. Input Voltage.

**FIGURE 2-5:** Total Error vs. Input Voltage.

**FIGURE 2-6:** Gain Error vs. Temperature.
**Note:** Unless otherwise indicated, $T_A = -40°C$ to $+85°C$, $V_{DD} = +5.0V$, $V_{SS} = 0V$, $CHn+ = CHn- = V_{REF}/2$, $V_{INCOM} = V_{REF}/2$.

**FIGURE 2-7:** $I_{DDA}$ vs. Temperature.

**FIGURE 2-8:** $I_{DDS}$ vs. Temperature.

**FIGURE 2-9:** $I_{DDB}$ vs. Temperature.

**FIGURE 2-10:** Oscillator Drift vs. Temperature.

**FIGURE 2-11:** Frequency Response.
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP3426</th>
<th>MCP3427</th>
<th>MCP3428</th>
<th>Sym</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFN</td>
<td>MSOP, SOIC</td>
<td>DFN</td>
<td>MSOP</td>
<td>SOIC, TSSOP</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CH1+</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>CH1-</td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>CH2+</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>5</td>
<td>4</td>
<td>CH2-</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>3</td>
<td>5</td>
<td>VSS</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>VDD</td>
</tr>
<tr>
<td>4</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>SDA</td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>SCL</td>
</tr>
<tr>
<td>—</td>
<td>9</td>
<td>9</td>
<td>9</td>
<td>Adr0</td>
</tr>
<tr>
<td>—</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>Adr1</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>11</td>
<td>CH3+</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>CH3-</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>13</td>
<td>CH4+</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>14</td>
<td>CH4-</td>
</tr>
<tr>
<td>9</td>
<td>11</td>
<td>—</td>
<td>—</td>
<td>EP</td>
</tr>
</tbody>
</table>

3.1 Analog Inputs (CHn+, CHn-)

CHn+ and CHn- are differential input pins for channel n. The user can also connect CHn- pin to VSS for a single-ended operation. See Figure 6-4 for differential and single-ended connection examples.

The maximum voltage range on each differential input pin is from VSS–0.3V to VDD+0.3V. Any voltage below or above this range will cause leakage currents through the Electrostatic Discharge (ESD) diodes at the input pins.

This ESD current can cause unexpected performance of the device. The input voltage at the input pins should be within the specified operating range defined in Section 1.0 “Electrical Characteristics” and Section 4.0 “Description of Device Operation”.

See Section 4.5 “Input Voltage Range” for more details of the input voltage range.

Figure 3-1 shows the input structure of the device. The device uses a switched capacitor input stage at the front end. CPIN is the package pin capacitance and typically about 4 pF. D1 and D2 are the ESD diodes. CSAMPLE is the differential input sampling capacitor.

3.2 Supply Voltage (VDD, VSS)

VDD is the power supply pin for the device. This pin requires an appropriate bypass ceramic capacitor of about 0.1 μF to ground to attenuate high frequency noise presented in application circuit board. An additional 10 μF capacitor (tantalum) in parallel is also recommended to further attenuate current spike noises. The supply voltage (VDD) must be maintained in the 2.7V to 5.5V range for specified operation.

VSS is the ground pin and the current return path of the device. The user must connect the VSS pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the VSS pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.
FIGURE 3-1: Equivalent Analog Input Circuit.

3.3 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I2C interface. The device acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the slave device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the VDD line to the SCL pin. Refer to Section 5.3 “I2C Serial Communications” for more details on I2C Serial Interface communication.

3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I2C interface. The SDA pin is used for input and output data. In read mode, the conversion result is read from the SDA pin (output). In write mode, the device configuration bits are written (input) though the SDA pin. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the VDD line to the SDA pin. Except for start and stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to Section 5.3 “I2C Serial Communications” for more details on I2C Serial Interface communication.

The typical range of the pull-up resistor value for SCL and SDA is from 5 kΩ to 10 kΩ for standard (100 kHz) and fast (400 kHz) modes, and less than 1 kΩ for high speed mode (3.4 MHz).

3.5 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the VSS pin; they must be connected to the same potential on the Printed Circuit Board (PCB).
4.0 DESCRIPTION OF DEVICE OPERATION

4.1 General Overview

The MCP3426/7/8 devices are differential multi-channel low-power, 16-Bit Delta-Sigma A/D converters with an I2C serial interface. The devices contain an input channel selection multiplexer (mux), a programmable gain amplifier (PGA), an on-board voltage reference (2.048V), and an internal oscillator.

When the device powers up (POR is set), it automatically resets the configuration bits to default settings.

4.1.1 DEVICE DEFAULT SETTINGS ARE:

- Conversion bit resolution: 12 bits (240 sps)
- Input channel: Channel 1
- PGA gain setting: x1
- Continuous conversion

Once the device is powered-up, the user can reprogram the configuration bits using I2C serial interface any time. The configuration bits are stored in the volatile memory.

4.1.2 USER SELECTABLE OPTIONS ARE:

- Conversion bit resolution: 12, 14, or 16 bits
- Input channel selection: CH1, CH2, CH3, or CH4.
- PGA Gain selection: x1, x2, x4, or x8
- Continuous or one-shot conversion

In the Continuous Conversion mode, the device converts the inputs continuously. While in the One-Shot Conversion mode, the device converts the input one time and stays in the low-power standby mode until it receives another command for a new conversion. During the standby mode, the device consumes less than 1 µA maximum.

4.2 Power-On-Reset (POR)

The device contains an internal Power-On-Reset (POR) circuit that monitors power supply voltage (VDD) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device resets all configuration register bits to default settings as soon as the POR is set.

The POR has built-in hysteresis and a timer to give a high degree of immunity to potential ripples and noises on the power supply. A 0.1 µF decoupling capacitor should be mounted as close as possible to the VDD pin for additional transient immunity.

The threshold voltage is set at 2.2V with a tolerance of approximately ±5%. If the supply voltage falls below this threshold, the device will be held in a reset condition. The typical hysteresis value is approximately 200 mV.

The POR circuit is shut down during the low-power standby mode. Once a power-up event has occurred, the device requires additional delay time (approximately 300 µs) before a conversion takes place. During this time, all internal analog circuitries are settled before the first conversion occurs. Figure 4-1 illustrates the conditions for power-up and power-down events under typical start-up conditions.

4.3 Internal Voltage Reference

The device contains an on-board 2.048V voltage reference. This reference voltage is for internal use only and not directly measurable. The specification of the reference voltage is part of the device’s gain and drift specifications. Therefore, there is no separate specification for the on-board reference.

4.4 Analog Input Channels

The user can select the input channel using the configuration register bits. Each channel can be used for differential or single-ended input.

Each input channel has a switched capacitor input structure. The internal sampling capacitor (3.2 pF for PGA = 1) is charged and discharged to process a conversion. The charging and discharging of the input sampling capacitor creates dynamic input currents at each input pin. The current is a function of the differential input voltages, and inversely proportional to the internal sampling capacitance, sampling frequency, and PGA setting.
4.5 Input Voltage Range

The differential (\(V_{IN}\)) and common mode voltage (\(V_{INCOM}\)) at the input pins without considering PGA setting are defined by:

\[
V_{IN} = (CH_{n+}) - (CH_{n-})
\]

\[
V_{INCOM} = \frac{(CH_{n+}) + (CH_{n-})}{2}
\]

Where:

\(n = \) nth input channel (n=1, 2, 3, or 4)

The input signal levels are amplified by the internal programmable gain amplifier (PGA) at the front end of the \(\Delta\Sigma\) modulator.

The user needs to consider two conditions for the input voltage range: (a) Differential input voltage range and (b) Absolute maximum input voltage range.

4.5.1 Differential Input Voltage Range

The device performs conversions using its internal reference voltage (\(V_{REF} = 2.048V\)). Therefore, the absolute value of the differential input voltage (\(V_{IN}\)), with PGA setting is included, needs to be less than the internal reference voltage. The device will output saturated output codes (all 0s or all 1s except sign bit) if the absolute value of the input voltage (\(V_{IN}\)), with PGA setting is included, is greater than the internal reference voltage (\(V_{REF} = 2.048V\)). The input full scale voltage range is given by:

\[
-V_{REF} \leq (V_{IN} \cdot PGA) \leq (V_{REF} - 1LSB)
\]

Where:

\(V_{IN} = CH_{n+} - CH_{n-}\)

\(V_{REF} = 2.048V\)

If the input voltage level is greater than the above limit, the user can use a voltage divider and bring down the input level within the full scale range. See Figure 6-7 for more details of the input voltage divider circuit.

4.5.2 Absolute Maximum Input Voltage Range

The input voltage at each input pin must be less than the following absolute maximum input voltage limits:

- Input voltage < \(V_{DD} + 0.3V\)
- Input voltage > \(V_{SS} - 0.3V\)

Any input voltage outside this range can turn on the input ESD protection diodes, and result in input leakage current, causing conversion errors, or permanently damage the device. Care must be taken in setting the input voltage ranges so that the input voltage does not exceed the absolute maximum input voltage range.

4.6 Input Impedance

The device uses a switched-capacitor input stage using a 3.2 pF sampling capacitor. This capacitor is switched (charged and discharged) at a rate of the sampling frequency that is generated by on-board clock. The differential input impedance varies with the PGA settings. The typical differential input impedance during a normal mode operation is given by:

\[
Z_{IN}(f) = 2.25 \text{ M} \Omega /\text{PGA}
\]

Since the sampling capacitor is only switching to the input pins during a conversion process, the above input impedance is only valid during conversion periods. In a low power standby mode, the above impedance is not presented at the input pins. Therefore, only a leakage current due to ESD diode is presented at the input pins.

The conversion accuracy can be affected by the input signal source impedance when any external circuit is connected to the input pins. The source impedance adds to the internal impedance and directly affects the time required to charge the internal sampling capacitor. Therefore, a large input source impedance connected to the input pins can degrade the system performance, such as offset, gain, and Integral Non-Linearity (INL) errors. Ideally, the input source impedance should be zero. This can be achievable by using an operational amplifier with a closed-loop output impedance of tens of ohms.

4.7 Aliasing and Anti-aliasing Filter

Aliasing occurs when the input signal contains time-varying signal components with frequency greater than half the sample rate. In the aliasing conditions, the device can output unexpected output codes. For applications that are operating in electrical noise environments, the time-varying signal noise or high frequency interference components can be easily added to the input signals and cause aliasing. Although the device has an internal first order sinc filter, the filter response (Figure 2-11) may not give enough attenuation to all aliasing signal components. To avoid the aliasing, an external anti-aliasing filter, which can be accomplished with a simple RC low-pass filter, is typically used at the input pins. The low-pass filter cuts off the high frequency noise components and provides a band-limited input signal to the input pins.

4.8 Self-Calibration

The device performs a self-calibration of offset and gain for each conversion. This provides reliable conversion results from conversion-to-conversion over variations in temperature as well as power supply fluctuations.
4.9 Digital Output Codes and Conversion to Real Values

4.9.1 DIGITAL OUTPUT CODE FROM DEVICE

The digital output code is proportional to the input voltage and PGA settings. The output data format is a binary two’s complement. With this code scheme, the MSB can be considered a sign indicator. When the MSB is a logic '0', the input is positive. When the MSB is a logic '1', the input is negative. The following is an example of the output code:

(a) for a negative full scale input voltage: 100...000
   Example: (CHn+ - CHn-) • PGA = -2.048V
(b) for a zero differential input voltage: 000...000
   Example: (CHn+ - CHn-) = 0
(c) for a positive full scale input voltage: 011...111
   Example: (CHn+ - CHn-) • PGA = 2.048V

The MSB (sign bit) is always transmitted first through the I2C serial data line. The resolution for each conversion is 16, 14, or 12 bits depending on the conversion rate selection bit settings by the user.

The output codes will not roll-over even if the input voltage exceeds the maximum input range. In this case, the code will be locked at 0111...11 for all voltages greater than (VREF - 1 LSB)/PGA and 1000...00 for voltages less than -VREF/PGA.

Table 4-2 shows an example of output codes of various input levels for 16-bit conversion mode. Table 4-3 shows an example of minimum and maximum output codes for each conversion rate option.

The number of output code is given by:

**EQUATION 4-2:**

\[
\text{Number of Output Code} = (\text{Maximum Code} + 1) \times \text{PGA} \times \frac{(CHn+ - CHn-)}{2.048V}
\]

Where:

See Table 4-3 for Maximum Code

The LSB of the data conversion is given by:

**EQUATION 4-3:**

\[
\text{LSB} = \frac{2 \times V_{\text{REF}}}{2^N} = \frac{2 \times 2.048V}{2^N}
\]

Where:

\[N = \text{Resolution, which is programmed in the Configuration Register: 12, 14, or 16.}\]

---

Table 4-1 shows the LSB size of each conversion rate setting. The measured unknown input voltage is obtained by multiplying the output codes with LSB. See the following section for the input voltage calculation using the output codes.

<table>
<thead>
<tr>
<th>Resolution Setting</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 bits</td>
<td>1 mV</td>
</tr>
<tr>
<td>14 bits</td>
<td>250 µV</td>
</tr>
<tr>
<td>16 bits</td>
<td>62.5 µV</td>
</tr>
</tbody>
</table>

**TABLE 4-2: EXAMPLE OF OUTPUT CODE FOR 16 BITS (NOTE 1, NOTE 2)**

<table>
<thead>
<tr>
<th>Input Voltage: [CHn+ - CHn-] • PGA</th>
<th>Digital Output Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥ VREF</td>
<td>0111111111111111</td>
</tr>
<tr>
<td>VREF - 1 LSB</td>
<td>0111111111111111</td>
</tr>
<tr>
<td>2 LSB</td>
<td>0000000000000010</td>
</tr>
<tr>
<td>1 LSB</td>
<td>0000000000000001</td>
</tr>
<tr>
<td>0</td>
<td>0000000000000000</td>
</tr>
<tr>
<td>-1 LSB</td>
<td>1111111111111111</td>
</tr>
<tr>
<td>-2 LSB</td>
<td>1111111111111110</td>
</tr>
<tr>
<td>- VREF</td>
<td>1000000000000000</td>
</tr>
<tr>
<td>&lt; -VREF</td>
<td>1000000000000000</td>
</tr>
</tbody>
</table>

**Note 1:**

- MSB is a sign indicator:
  - 0: Positive input (CHn+ > CHn-)
  - 1: Negative input (CHn+ < CHn-)

**Note 2:**

- Output data format is binary two’s complement.

**TABLE 4-3: MINIMUM AND MAXIMUM OUTPUT CODES (NOTE)**

<table>
<thead>
<tr>
<th>Resolution Setting</th>
<th>Data Rate</th>
<th>Minimum Code</th>
<th>Maximum Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>240 SPS</td>
<td>-2048</td>
<td>2047</td>
</tr>
<tr>
<td>14</td>
<td>60 SPS</td>
<td>-8192</td>
<td>8191</td>
</tr>
<tr>
<td>16</td>
<td>15 SPS</td>
<td>-32768</td>
<td>32767</td>
</tr>
</tbody>
</table>

**Note:**

Maximum n-bit code = 2^{N-1} - 1
Minimum n-bit code = -1 \times 2^{N-1}
4.9.2 CONVERTING THE DEVICE OUTPUT CODE TO INPUT SIGNAL VOLTAGE

When the user gets the digital output codes from the device as described in Section 4.9.1 “Digital output code from device”, the next step is converting the digital output codes to a measured input voltage. Equation 4-4 shows an example of converting the output codes to their corresponding input voltage.

If the sign indicator bit (MSB) is ‘0’, the input voltage is obtained by multiplying the output code with the LSB and divided by the PGA setting.

If the sign indicator bit (MSB) is ‘1’, the output code needs to be converted to two’s complement before multiplied by LSB and divided by the PGA setting. Table 4-4 shows an example of converting the device output codes to input voltage.

**Table 4-4: Example of Converting Output Code to Voltage (with 16 bit setting)**

<table>
<thead>
<tr>
<th>Input Voltage [CHn+ - CHn-] • PGA</th>
<th>Digital Output Code</th>
<th>MSB</th>
<th>Example of Converting Output Codes to Input Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>≥ VREF</td>
<td>0111111111111111</td>
<td>0</td>
<td>((2^{14}\times2^{13}\times2^{12}\times2^{11}\times2^{10}\times2^{9}\times2^{8}\times2^{7}\times2^{6}\times2^{5}\times2^{4}\times2^{3}\times2^{2}\times2^{1}\times2^{0})\times) LSB(62.5μV)/PGA = 2.048 (V) for PGA = 1</td>
</tr>
<tr>
<td>VREF - 1 LSB</td>
<td>0111111111111111</td>
<td>0</td>
<td>((2^{14}\times2^{13}\times2^{12}\times2^{11}\times2^{10}\times2^{9}\times2^{8}\times2^{7}\times2^{6}\times2^{5}\times2^{4}\times2^{3}\times2^{2}\times2^{1}\times2^{0})\times) LSB(62.5μV)/PGA = 2.048 (V) for PGA = 1</td>
</tr>
<tr>
<td>2 LSB</td>
<td>0000000000000010</td>
<td>0</td>
<td>((0+0+0+0+0+0+0+0+0+0+0+0+0+2^{1}+0)\times) LSB(62.5μV)/PGA = - 125 (μV) for PGA = 1</td>
</tr>
<tr>
<td>1 LSB</td>
<td>0000000000000001</td>
<td>0</td>
<td>((0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^{0})\times) LSB(62.5μV)/PGA = - 62.5 (μV) for PGA = 1</td>
</tr>
<tr>
<td>0</td>
<td>0000000000000000</td>
<td>0</td>
<td>((0+0+0+0+0+0+0+0+0+0+0+0+0+0+0+0)\times) LSB(62.5μV)/PGA = 0 V (V) for PGA = 1</td>
</tr>
<tr>
<td>-1 LSB</td>
<td>1111111111111111</td>
<td>1</td>
<td>(-(0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^{0})\times) LSB(62.5μV)/PGA = - 62.5 (μV) for PGA = 1</td>
</tr>
<tr>
<td>-2 LSB</td>
<td>1111111111111110</td>
<td>1</td>
<td>(-(0+0+0+0+0+0+0+0+0+0+0+0+0+2^{1})\times) LSB(62.5μV)/PGA = - 125 (μV) for PGA = 1</td>
</tr>
<tr>
<td>-VREF</td>
<td>1000000000000000</td>
<td>1</td>
<td>(-(2^{15}+0+0+0+0+0+0+0+0+0+0+0+0+0+0)\times) LSB(62.5μV)/PGA = - 2.048 (V) for PGA = 1</td>
</tr>
<tr>
<td>≤ -VREF</td>
<td>1000000000000000</td>
<td>1</td>
<td>(-(2^{15}+0+0+0+0+0+0+0+0+0+0+0+0+0+0)\times) LSB(62.5μV)/PGA = - 2.048 (V) for PGA = 1</td>
</tr>
</tbody>
</table>

**Note:** MSB = sign bit (1: “-”, 0: “+”)
5.0 USING THE DEVICES

5.1 Operating Modes

The user operates the device by setting up the device configuration register using a write command (see Figure 5-3) and reads the conversion data using a read command (see Figure 5-4). The device operates in two modes: (a) Continuous Conversion Mode or (b) One-Shot Conversion Mode (single conversion). This mode selection is made by setting the O/C bit in the Configuration Register. Refer to Section 5.2 “Configuration Register” for more information.

5.1.1 CONTINUOUS CONVERSION MODE (O/C BIT = 1)

The device performs a Continuous Conversion if the O/C bit is set to logic “high”. Once the conversion is completed, RDY bit is toggled to ‘0’ and the result is placed at the output data register. The device immediately begins another conversion and overwrites the output data register with the most recent result. The device clears the data ready flag (RDY bit = 0) when the conversion is completed. The device sets the ready flag bit (RDY bit = 1), if the latest conversion result has been read by the Master.

- When writing configuration register:
  - Setting RDY bit in continuous mode does not affect anything.
- When reading conversion data:
  - RDY bit = 0 means the latest conversion result is ready.
  - RDY bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the RDY bit will be cleared when the new conversion is done.

5.1.2 ONE-SHOT CONVERSION MODE (O/C BIT = 0)

Once the One-Shot Conversion (single conversion) Mode is selected, the device performs only one conversion, updates the output data register, clears the data ready flag (RDY = 0), and then enters a low power standby mode. A new One-Shot Conversion is started again when the device receives a new write command with RDY = 1.

- When writing configuration register:
  - The RDY bit needs to be set to begin a new conversion in one-shot mode.
- When reading conversion data:
  - RDY bit = 0 means the latest conversion result is ready.
  - RDY bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the RDY bit will be cleared when the new conversion is done.

This One-Shot Conversion Mode is highly recommended for low power operating applications where the conversion result is needed by request on demand. During the low current standby mode, the device consumes less than 1 µA maximum (or 300 nA typical). For example, if the user collects 16-bit conversion data once a second in One-Shot Conversion mode, the device draws only about one-fifteenth of the operating currents for the continuous conversion mode. In this example, the device consumes approximately 9 µA (135 µA / 15 SPS = 9 µA), when the device performs only one conversion per second (1 SPS) in 16-bit conversion mode with 3V power supply.
5.2 Configuration Register

The device has an 8-bit wide configuration register to select for: input channel, conversion mode, conversion rate, and PGA gain. This register allows the user to change the operating condition of the device and check the status of the device operation.

REGISTER 5-1: CONFIGURATION REGISTER

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDY</td>
<td>C1</td>
<td>C0</td>
<td>O/C</td>
<td>S1</td>
<td>S0</td>
<td>G1</td>
<td>G0</td>
</tr>
<tr>
<td>*</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

bit 7  
RDY: Ready Bit
This bit is the data ready flag. In read mode, this bit indicates if the output register has been updated with a latest conversion result. In One-Shot Conversion mode, writing this bit to "1" initiates a new conversion.

Reading RDY bit with the read command:
1 = Output register has not been updated.
0 = Output register has been updated with the latest conversion result.

Writing RDY bit with the write command:
Continuous Conversion mode: No effect
One-Shot Conversion mode:
1 = Initiate a new conversion.
0 = No effect.

bit 6-5  
C1-C0: Channel Selection Bits
00 = Select Channel 1 (Default)
01 = Select Channel 2
10 = Select Channel 3 (MCP3428 only, treated as “00” by the MCP3426/MCP3427)
11 = Select Channel 4 (MCP3428 only, treated as “01” by the MCP3426/MCP3427)

bit 4  
O/C: Conversion Mode Bit
1 = Continuous Conversion Mode (Default). The device performs data conversions continuously.
0 = One-Shot Conversion Mode. The device performs a single conversion and enters a low power standby mode until it receives another write or read command.

bit 3-2  
S1-S0: Sample Rate Selection Bit
00 = 240 SPS (12 bits) (Default)
01 = 60 SPS (14 bits)
10 = 15 SPS (16 bits)

bit 1-0  
G1-G0: PGA Gain Selection Bits
00 = x1 (Default)
01 = x2
10 = x4
11 = x8

* Default Configuration after Power-On Reset

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
-n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown
If the configuration byte is read repeatedly by clocking continuously after reading the data bytes (i.e., after the 4th byte in the 16-bit conversion mode), the state of the RDY bit indicates whether the device is ready with new conversion result. When the Master finds the RDY bit is cleared, it can send a not-acknowledge (NAK) bit and a stop bit to exit the current read operation and send a new read command for the latest conversion data. Once the conversion data has been read, the ready bit toggles to ‘1’ until the next new conversion data is ready. The conversion data in the output register is overwritten every time a new conversion is completed.

Figure 5-3 shows an example of writing configuration register, and Figure 5-4 shows an example of reading conversion data. The user can rewire the configuration byte any time for a new setting. Table 5-1 and Table 5-2 show the examples of the configuration bit operation.

### TABLE 5-1: WRITE CONFIGURATION BITS

<table>
<thead>
<tr>
<th>R/W</th>
<th>O/C</th>
<th>RDY</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No effect if all other bits remain the same - operation continues with the previous settings.</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Initiate One-Shot Conversion.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Initiate Continuous Conversion.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Initiate Continuous Conversion.</td>
</tr>
</tbody>
</table>

### TABLE 5-2: READ CONFIGURATION BITS

<table>
<thead>
<tr>
<th>R/W</th>
<th>O/C</th>
<th>RDY</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>New conversion result in One-Shot conversion mode has just been read. The RDY bit remains low until set by a new write command.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>One-Shot Conversion is in progress. The conversion result is not updated yet. The RDY bit stays high until the current conversion is completed.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>New conversion result in Continuous Conversion mode has just been read. The RDY bit changes to high after reading the conversion data.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>The conversion result in Continuous Conversion mode was already read. The next new conversion data is not ready. The RDY bit stays high until a new conversion is completed.</td>
</tr>
</tbody>
</table>

### 5.3 I²C Serial Communications

The device communicates with the Master (microcontroller) through a serial I²C (Inter-Integrated Circuit) interface and support standard (100 kbits/sec), fast (400 kbits/sec) and high-speed (3.4 Mbits/sec) modes. The serial I²C is a bidirectional 2-wire data bus communication protocol using open-drain SCL and SDA lines.

The device can only be addressed as a slave. Once addressed, it can receive configuration bits with a write command or transmit the latest conversion results with a read command. The serial clock pin (SCL) is an input only and the serial data pin (SDA) is bidirectional. The Master starts communication by sending a START bit and terminates the communication by sending a STOP bit. In read mode, the device releases the SDA line after receiving NAK and STOP bits.

An example of a hardware connection diagram is shown in Figure 6-1. More details of the I²C bus characteristic is described in Section 5.6 “I²C Bus Characteristics”.

#### 5.3.1 I²C DEVICE ADDRESSING

The first byte after the START bit is always the address byte of the device, which includes the device code (4 bits), address bits (3 bits), and R/W bit. The device code for the devices is 1101, which is programmed at the factory. The I²C address bits (A2, A1, A0 bits) are as follows:

- MCP3426: Programmed at factory
- MCP3427 and MCP3428: Programmed by the user. It is determined by the logic status of the two external address selection pins on the user’s application board (A30 and A31 pins). The Master must know the A30 and A31 pin conditions before sending read or write command.

See Section 5.3.2 “Device Address Bits (A2, A1, A0) and Address Selection Pins (MCP3427 and MCP3428)” for more details.

Figure 5-1 shows the details of the address byte.

The three I²C address bits allow up to eight devices on the same I²C bus line. The (R/W) bit determines if the Master device wants to read the conversion data or write to the Configuration register. If the (R/W) bit is set (read mode), the device outputs the conversion data in the following clocks. If the (R/W) bit is cleared (write mode), the device expects a configuration byte in the following clocks. When the device receives the correct address byte, it outputs an acknowledge bit after the R/W bit.
5.3.2 DEVICE ADDRESS BITS (A2, A1, A0)
AND ADDRESS SELECTION PINS
(MCP3427 AND MCP3428)

The MCP3427 and MCP3428 have two external device address pins (Adr1, Adr0). These pins can be set to a logic high (or tied to VDD), low (or tied to VSS), or left floating (not connected to anything, or tied to VDD/2). These combinations of logic level using the two pins allow eight possible addresses. Table 5-3 shows the device address depending on the logic status of the address selection pins.

The device samples the logic status of the Adr0 and Adr1 pins in the following events:
(a) Device power-up.
(b) General Call Reset
   (See Section 5.4 “General Call”).
(c) General Call Latch
   (See Section 5.4 “General Call”).

The device samples the logic status (address pins) during the above events, and latches the values until a new latch event occurs. During normal operation (after the address pins are latched), the address pins are internally disabled from the rest of the internal circuit.

It is recommended to issue a General Call Reset or General Call Latch command once after the device has powered up. This will ensure that the device reads the address pins in a stable condition, and avoid latching the address bits while the power supply is ramping up. This might cause inaccurate address pin detection.

When the address pin is left “floating”:

When the address pin is left “floating”, the address pin momentarily outputs a short pulse with an amplitude of about VDD/2 during the latch event. The device also latches this pin voltage at the same time.

If the “floating” pin is connected to a large parasitic capacitance (> 20 pF) or to a long PCB trace, this short floating voltage output can be altered. As a result, the device may not latch the pin correctly.

It is strongly recommended to keep the “floating” pin pad as short as possible in the customer application PCB and minimize the parasitic capacitance to the pin as small as possible (< 20 pF).

Figure 5-2 shows an example of the Latch voltage output at the address pin when the address pin is left “floating”. The waveform at the Adr0 pin is captured by using an oscilloscope probe with 15 pF of capacitance. The device latches the floating condition immediately after the General Call Latch command.
### 5.3.3 WRITING A CONFIGURATION BYTE TO THE DEVICE

When the Master sends an address byte with the R/W bit low (R/W = 0), the device expects one configuration byte following the address. Any byte sent after this second byte will be ignored. The user can change the operating mode of the device by writing the configuration register bits.

If the device receives a write command with a new configuration setting, the device immediately begins a new conversion and updates the conversion data.

---

#### TABLE 5-3: ADDRESS BITS VS. ADDRESS SELECTION PINS FOR (MCP3427 AND MCP3428 ONLY) (NOTE 1, 2, 3)

<table>
<thead>
<tr>
<th>I²C Device Address Bits</th>
<th>Logic Status of Address Selection Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2 A1 A0</td>
<td>Adr0 Pin</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0 (Addr_Low)</td>
</tr>
<tr>
<td>0 0 1</td>
<td>0 (Addr_Low)</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0 (Addr_Low)</td>
</tr>
<tr>
<td>1 0 0</td>
<td>1 (Addr_High)</td>
</tr>
<tr>
<td>1 0 1</td>
<td>1 (Addr_High)</td>
</tr>
<tr>
<td>1 1 0</td>
<td>1 (Addr_High)</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Float</td>
</tr>
<tr>
<td>1 1 1</td>
<td>Float</td>
</tr>
<tr>
<td>0 0 0</td>
<td>Float</td>
</tr>
</tbody>
</table>

**Note 1:** Float: (a) Leave pin without connecting to anything (left floating), or (b) apply Addr_Float voltage.

**Note 2:** The user can tie the pins to VSS or VDD:
- Tie to VSS for Addr_Low
- Tie to VDD for Addr_High

**Note 3:** See Addr_Low, Addr_High, and Addr_Float parameters in Electrical Characteristics Table.

---

**FIGURE 5-3:** Timing Diagram For Writing To The MCP3426/7/8.

- **Note:**
  - Stop bit can be issued any time during writing.
  - MCP3426/7/8 device code is 1101 (programmed at the factory).
  - See Figure 5-1 for details in Address Byte.
5.3.4 READING OUTPUT CODES AND CONFIGURATION BYTE FROM THE DEVICE

When the Master sends a read command \( \text{R/W} = 1 \), the device outputs both the conversion data and configuration bytes. Each byte consists of 8 bits with one acknowledge (ACK) bit. The ACK bit after the address byte is issued by the device and the ACK bits after each conversion data bytes are issued by the Master.

When the device receives a read command, it outputs two data bytes followed by a configuration register. In 16-bit conversion mode, the MSB (= sign bit) of the first data byte is D15. In 14-bit conversion mode, the first two bits in the first data byte are repeated MSB bits and can be ignored, and the 3rd bit (D13) is the MSB (=sign bit) of the conversion data. In 12-bit conversion mode, the first four bits are repeated MSB bits and can be ignored. The 5th bit (D11) of the byte represents the MSB (= sign bit) of the conversion data. Table 5-4 summarizes the conversion data output of each conversion mode.

### TABLE 5-4: OUTPUT CODES OF EACH RESOLUTION OPTION

<table>
<thead>
<tr>
<th>Conversion Option</th>
<th>Digital Output Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-bits</td>
<td>D15 ( \sim ) D8 (1st data byte) - D7 ( \sim ) D0 (2nd data byte) - Configuration byte. (Note 1)</td>
</tr>
<tr>
<td>14-bits</td>
<td>MMD13D ( \sim ) D8 (1st data byte) - D7 ( \sim ) D0 (2nd data byte) - Configuration byte. (Note 2)</td>
</tr>
<tr>
<td>12-bits</td>
<td>MMMMD11 ( \sim ) D8 (1st data byte) - D7 ( \sim ) D0 (2nd data byte) - Configuration byte. (Note 3)</td>
</tr>
</tbody>
</table>

**Note 1:** D15 is MSB (= sign bit).

**Note 2:** D13 is MSB (= sign bit), M is repeated MSB of the data byte.

**Note 3:** D11 is MSB (= sign bit), M is repeated MSB of the data byte.
FIGURE 5-4: Timing Diagram For Reading From The MCP3426/7/8 With 12-Bit to 16-Bit Modes.

Note:
- MCP3426/7/8 device code is 1101.
- See Figure 5-1 for details in Address Byte.
- Stop bit or NAK bit can be issued at the end of each output byte.
- In 14-bit mode, D15 and D14 are repeated MSB and can be ignored.
- In 12-bit mode, D15-D12 are repeated MSB and can be ignored.
- Configuration byte repeats as long as clock is provided after the 4th byte.

© 2009 Microchip Technology Inc.
5.4 General Call

The device acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. Refer to Figure 5-5. The device supports the following three general calls.

For more information on the general call, or other I^C modes, refer to the Philips I^C specification.

5.4.1 GENERAL CALL RESET

The general call reset occurs if the second byte is ’00000110’ (06h). At the acknowledgement of this byte, the device will abort current conversion and perform the following tasks:

(a) Internal reset similar to a Power-On-Reset (POR). All configuration and data register bits are reset to default values.
(b) Latch the logic status of external address selection pins (Adr0 and Adr1 pins).

5.4.2 GENERAL CALL LATCH (MCP3427 AND MCP3428)

The general call latch occurs if the second byte is ’00000100’ (04h). The device will latch the logic status of the external address selection pins (Adr0 and Adr1 pins), but will not perform a reset.

5.4.3 GENERAL CALL CONVERSION

The general call conversion occurs if the second byte is ’00001000’ (08h). All devices on the bus initiate a conversion simultaneously. When the device receives this command, the configuration will be set to the One-Shot Conversion mode and a single conversion will be performed. The PGA and data rate settings are unchanged with this general call.

5.5 High-Speed (HS) Mode

The I^C specification requires that a high-speed mode device must be ‘activated’ to operate in high-speed mode. This is done by sending a special address byte of "00001XXX" following the START bit. The "XXX" bits are unique to the High-Speed (HS) mode Master. This byte is referred to as the High-Speed (HS) Master Mode Code (HSMMC). The MCP3426/7/8 devices do not acknowledge this byte. However, upon receiving this code, the device switches on its HS mode filters and communicates up to 3.4 MHz on SDA and SCL bus lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I^C modes, refer to the Philips I^C specification.

5.6 I^C Bus Characteristics

The I^C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition

Accordingly, the following bus conditions have been defined using Figure 5-6.

5.6.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

5.6.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

5.6.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations can be ended with a STOP condition.

5.6.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition.

---

FIGURE 5-5: General Call Address Format.

Note: The I^C specification does not allow ‘00000000’ (00h) in the second byte.
5.6.5 ACKNOWLEDGE AND NON-ACKNOWLEDGE

The Master (microcontroller) and the slave (MCP3426/7/8) use an acknowledge pulse (ACK) as a handshake of communication for each byte. The ninth clock pulse of each byte is used for the acknowledgement. The clock pulse is always provided by the Master (microcontroller) and the acknowledgement is issued by the receiving device of the byte (Note: The transmitting device must release the SDA line during the acknowledge pulse.). The acknowledgement is achieved by pulling-down the SDA line “LOW” during the 9th clock pulse by the receiving device.

During reads, the Master (microcontroller) can terminate the current read operation by not providing an acknowledge bit (not Acknowledge (NAK)) on the last byte. In this case, the MCP3426/7/8 devices release the SDA line to allow the Master (microcontroller) to generate a STOP or repeated START condition.

The non-acknowledgement (NAK) is issued by providing the SDA line to “HIGH” during the 9th clock pulse.

![Figure 5-6: Data Transfer Sequence on I²C Serial Bus.](image)
### TABLE 5-5: I2C SERIAL TIMING SPECIFICATIONS

**Electrical Specifications:** Unless otherwise specified, all limits are specified for $T_A = -40$ to $+85^\circ$C, $V_{DD} = +2.7$V to $+5.0$V, $V_{SS} = 0$V, $CHn+ = CHn- = V_{REF}/2$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Standard Mode (100 kHz)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$f_{SCL}$</td>
<td>0</td>
<td>—</td>
<td>100</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Clock high time</td>
<td>$T_{HIGH}$</td>
<td>4000</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Clock low time</td>
<td>$T_{LOW}$</td>
<td>4700</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SDA and SCL rise time</td>
<td>$T_R$</td>
<td>—</td>
<td>—</td>
<td>1000</td>
<td>ns</td>
<td>From $V_{IL}$ to $V_{IH}$ <em>(Note 1)</em></td>
</tr>
<tr>
<td>SDA and SCL fall time</td>
<td>$T_F$</td>
<td>—</td>
<td>—</td>
<td>300</td>
<td>ns</td>
<td>From $V_{IH}$ to $V_{IL}$ <em>(Note 1)</em></td>
</tr>
<tr>
<td>START condition hold time</td>
<td>$T_{HD:STA}$</td>
<td>4000</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>After this period, the first clock pulse is generated.</td>
</tr>
<tr>
<td>Repeated START condition setup time</td>
<td>$T_{SU:STA}$</td>
<td>4700</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Only relevant for repeated Start condition</td>
</tr>
<tr>
<td>Data hold time</td>
<td>$T_{HD:DAT}$</td>
<td>0</td>
<td>—</td>
<td>3450</td>
<td>ns</td>
<td><em>(Note 3)</em></td>
</tr>
<tr>
<td>Data input setup time</td>
<td>$T_{SU:DAT}$</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>STOP condition setup time</td>
<td>$T_{SU:STO}$</td>
<td>4000</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output valid from clock</td>
<td>$T_{AA}$</td>
<td>0</td>
<td>—</td>
<td>3750</td>
<td>ns</td>
<td><em>(Note 2, Note 3)</em></td>
</tr>
<tr>
<td>Bus free time</td>
<td>$T_{BUF}$</td>
<td>4700</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Time between START and STOP conditions.</td>
</tr>
<tr>
<td><strong>Fast Mode (400 kHz)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock frequency</td>
<td>$T_{SCL}$</td>
<td>0</td>
<td>—</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Clock high time</td>
<td>$T_{HIGH}$</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Clock low time</td>
<td>$T_{LOW}$</td>
<td>1300</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SDA and SCL rise time</td>
<td>$T_R$</td>
<td>$20 + 0.1C_p$</td>
<td>—</td>
<td>300</td>
<td>ns</td>
<td>From $V_{IL}$ to $V_{IH}$ <em>(Note 1)</em></td>
</tr>
<tr>
<td>SDA and SCL fall time</td>
<td>$T_F$</td>
<td>$20 + 0.1C_p$</td>
<td>—</td>
<td>300</td>
<td>ns</td>
<td>From $V_{IH}$ to $V_{IL}$ <em>(Note 1)</em></td>
</tr>
<tr>
<td>START condition hold time</td>
<td>$T_{HD:STA}$</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>After this period, the first clock pulse is generated</td>
</tr>
<tr>
<td>Repeated START condition setup time</td>
<td>$T_{SU:STA}$</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Only relevant for repeated Start condition</td>
</tr>
<tr>
<td>Data hold time</td>
<td>$T_{HD:DAT}$</td>
<td>0</td>
<td>—</td>
<td>900</td>
<td>ns</td>
<td><em>(Note 4)</em></td>
</tr>
<tr>
<td>Data input setup time</td>
<td>$T_{SU:DAT}$</td>
<td>100</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>STOP condition setup time</td>
<td>$T_{SU:STO}$</td>
<td>600</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output valid from clock</td>
<td>$T_{AA}$</td>
<td>0</td>
<td>—</td>
<td>1200</td>
<td>ns</td>
<td><em>(Note 2, Note 3)</em></td>
</tr>
<tr>
<td>Bus free time</td>
<td>$T_{BUF}$</td>
<td>1300</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Time between START and STOP conditions.</td>
</tr>
<tr>
<td>Input filter spike suppression</td>
<td>$T_{SP}$</td>
<td>0</td>
<td>—</td>
<td>50</td>
<td>ns</td>
<td>SDA and SCL pins <em>(Note 5)</em></td>
</tr>
</tbody>
</table>

**Note:**

1. This parameter is ensured by characterization and not 100% tested.
2. This specification is not a part of the I2C specification. This specification is equivalent to the Data Hold Time ($T_{HD:DAT}$) plus SDA Fall (or rise) time: $T_{AA} = T_{HD:DAT} + T_F$ (or $T_R$).
3. If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time ($T_{LOW}$) can be affected.
4. For Data Input: This parameter must be longer than $T_{SP}$. If this parameter is too long, the Data Input Setup ($T_{SU:DAT}$) or Clock Low time ($T_{LOW}$) can be affected.
   For Data Output: This parameter is characterized, and tested indirectly by testing $T_{AA}$ parameter.
5. This parameter is ensured by characterization and not 100% tested. This parameter is not available for Standard Mode.
### TABLE 5-5: \(^2\)C SERIAL TIMING SPECIFICATIONS (CONTINUED)

**Electrical Specifications:** Unless otherwise specified, all limits are specified for \(T_A = -40 \text{ to } +85^\circ\text{C} \), \(V_{DD} = +2.7\text{V} \text{ to } +5.0\text{V} \), \(V_{SS} = 0\text{V} \), \(V \text{REF}/2 \).  

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency</td>
<td>(f_{SCL})</td>
<td>0</td>
<td>—</td>
<td>3.4</td>
<td>MHz</td>
<td>(C_B = 100 \text{ pF})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>—</td>
<td>1.7</td>
<td>MHz</td>
<td>(C_B = 400 \text{ pF})</td>
</tr>
<tr>
<td>Clock high time</td>
<td>(T_{HIGH})</td>
<td>60</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>120</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>Clock low time</td>
<td>(T_{LOW})</td>
<td>160</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>320</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>(C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>SCL rise time (Note 1)</td>
<td>(T_R)</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>ns</td>
<td>From (V_L) to (V_H), (C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>80</td>
<td>ns</td>
<td>From (V_L) to (V_H), (C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>SCL fall time (Note 1)</td>
<td>(T_F)</td>
<td>—</td>
<td>—</td>
<td>40</td>
<td>ns</td>
<td>From (V_H) to (V_L), (C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>80</td>
<td>ns</td>
<td>From (V_H) to (V_L), (C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>SDA rise time (Note 1)</td>
<td>(T_{R:DAT})</td>
<td>—</td>
<td>—</td>
<td>80</td>
<td>ns</td>
<td>From (V_L) to (V_H), (C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>160</td>
<td>ns</td>
<td>From (V_L) to (V_H), (C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>SDA fall time (Note 1)</td>
<td>(T_{F:DATA})</td>
<td>—</td>
<td>—</td>
<td>80</td>
<td>ns</td>
<td>From (V_H) to (V_L), (C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>160</td>
<td>ns</td>
<td>From (V_H) to (V_L), (C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>Data hold time (Note 4)</td>
<td>(T_{HD:DAT})</td>
<td>0</td>
<td>—</td>
<td>70</td>
<td>ns</td>
<td>(C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>150</td>
<td>ns</td>
<td>(C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>Output valid from clock (Notes 2 and 3)</td>
<td>(T_{AA})</td>
<td>—</td>
<td>—</td>
<td>150</td>
<td>ns</td>
<td>(C_B = 100 \text{ pF}, f_{SCL} = 3.4 \text{ MHz})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>310</td>
<td>ns</td>
<td>(C_B = 400 \text{ pF}, f_{SCL} = 1.7 \text{ MHz})</td>
</tr>
<tr>
<td>START condition hold time</td>
<td>(T_{HD:STA})</td>
<td>160</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>After this period, the first clock pulse is generated</td>
</tr>
<tr>
<td>Repeated START condition setup time</td>
<td>(T_{SU:STA})</td>
<td>160</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>Only relevant for repeated Start condition</td>
</tr>
<tr>
<td>Data input setup time</td>
<td>(T_{SU:DAT})</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>STOP condition setup time</td>
<td>(T_{SU:STO})</td>
<td>160</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Input filter spike suppression</td>
<td>(T_{SP})</td>
<td>0</td>
<td>—</td>
<td>10</td>
<td>ns</td>
<td>SDA and SCL pins (Note 5)</td>
</tr>
</tbody>
</table>

**Note:**
1. This parameter is ensured by characterization and not 100% tested.
2. This specification is not a part of the \(^2\)C specification. This specification is equivalent to the Data Hold Time (\(T_{HD:DAT}\)) plus SDA Fall (or rise) time: \(T_{AA} = T_{HD:DAT} + T_{F} \text{ (or } T_{R})\).
3. If this parameter is too short, it can create an unintended Start or Stop condition to other devices on the bus line. If this parameter is too long, Clock Low time (\(T_{LOW}\)) can be affected.
4. For Data Input: This parameter must be longer than \(t_{SP}\). If this parameter is too long, the Data Input Setup (\(T_{SU:DAT}\)) or Clock Low time (\(T_{LOW}\)) can be affected.
   For Data Output: This parameter is characterized, and tested indirectly by testing \(T_{AA}\) parameter.
5. This parameter is characterized, and tested indirectly by testing \(T_{AA}\) parameter.
FIGURE 5-7:  \( \text{I}^2\text{C} \) Bus Timing Data.
6.0 BASIC APPLICATION CONFIGURATION

The MCP3426/7/8 devices can be used for various precision analog-to-digital converter applications. These devices operate with very simple connections to the application circuit. The following sections discuss the examples of the device connections and applications.

6.1 Connecting to the Application Circuits

6.1.1 BYPASS CAPACITORS ON VDD PIN

For an accurate measurement, the application circuit needs a clean supply voltage and must block any noise signal to the MCP3426/7/8 devices. Figure 6-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) on the VDD line of the MCP3428. These capacitors are helpful to filter out any high frequency noises on the VDD line and also provide the momentary bursts of extra currents when the device needs from the supply. These capacitors should be placed as close to the VDD pin as possible (within one inch). If the application circuit has separate digital and analog power supplies, the VDD and VSS of the MCP3426/7/8 devices should reside on the analog plane.

6.1.2 CONNECTING TO I²C BUS USING PULL-UP RESISTORS

The SCL and SDA pins of the MCP3426/7/8 are open-drain configurations. These pins require a pull-up resistor as shown in Figure 6-1. The value of these pull-up resistors depends on the operating speed (standard, fast, and high speed) and loading capacitance of the I²C bus line. Higher value of pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus. Therefore, it can limit the bus operating speed. The lower value of resistor, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long bus line or high number of devices connected to the bus, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 5 kΩ and 10 kΩ ranges for standard and fast modes, and less than 1 kΩ for high speed mode depending on the presence of bus loading capacitance.

6.1.3 I²C ADDRESS SELECTION PINS (MCP3427 AND MCP3428)

The user can tie the Adr0 and Adr1 pins to VSS, VDD, or left floating. See more details in Section 5.3.2 “Device Address Bits (A2, A1, A0) and Address Selection Pins (MCP3427 and MCP3428)”.

![Figure 6-1: Typical Connection](image)

![Figure 6-2: Example of Multiple Device Connection on I²C Bus](image)
6.1.4 DEVICE CONNECTION TEST
The user can test the presence of the MCP3426/7/8 on the I^2C bus line without performing an input data conversion. This test can be achieved by checking an acknowledge response from the MCP3426/7/8 after sending a read or write command. Here is an example using Figure 6-3:

a. Set the R/W bit “HIGH” in the address byte.
b. Check the ACK pulse after sending the address byte.
   If the device acknowledges (ACK = 0), then the device is connected, otherwise it is not connected.
c. Send STOP or START bit.

![Figure 6-3: I^2C Bus Connection Test.](image)

6.1.5 DIFFERENTIAL AND SINGLE-ENDED CONFIGURATION
Figure 6-4 shows typical connection examples for differential and single-ended inputs. Differential input signals can be connected to the CHn+ and CHn- input pins, where n = the channel number (1, 2, 3, or 4). For the single-ended input, the input signal is applied to one of the input pins (typically connected to the CHn+ pin) while the other input pin (typically CHn- pin) is grounded. All device characteristics hold for the single-ended configuration, but this configuration loses one bit resolution because the input can only stand in positive half scale. Refer to Section 1.0 “Electrical Characteristics”.

![Figure 6-4: Differential and Single-Ended Input Connections.](image)
6.2 Application Examples

The MCP3426/7/8 devices can be used for broad ranges of sensor and data acquisition applications.

Figure 6-5 shows a circuit example measuring both the battery voltage and current using the MCP3426 device. Channels 1 and 2 are measuring the voltage and the current, respectively.

When the input voltage is greater than the internal reference voltage \( V_{\text{REF}} = 2.048V \), it needs a voltage divider circuit to prevent the output code from being saturated. In the example, \( R_1 \) and \( R_2 \) form a voltage divider. The \( R_1 \) and \( R_2 \) are set to yield \( V_{\text{IN}} \) to be less than the internal reference voltage \( V_{\text{REF}} = 2.048V \).

For the current measurement, the device measure the voltage across the current sensor, and converts it by dividing the measured voltage by a known resistance value. The voltage drops across the sensor is waste.

Therefore, the current measurement often prefers to use a current sensor with smaller resistance value, which, in turn, requires high resolution ADC device.

The device can measure the input voltage as low as 7.8 \( \mu \)V range (or current in \( \sim \) \( \mu \)A range) with 16 bit resolution and PGA = 8 settings.

The MSB (= sign bit) of the output code determines the direction of the current, which identifies the charging or the discharging current.

**FIGURE 6-5:** Battery Voltage and Charging/Discharging Current Measurement.
Figure 6-6, shows an example of using the MCP3428 for four-channel thermocouple temperature measurement applications.

**FIGURE 6-6: Four-Channel Thermocouple Applications.**

With Type K thermocouple, it can measure temperature from 0°C to +1250°C degrees. The full scale output range of the Type K thermocouple is about 50 mV. This provides 40 µV/°C (= 50 mV/1250°C) of measurement resolution. **Equation 6-1** shows the measurement budget for sensor signal using the MCP3426/7/8 device with 16 bits and PGA = 8 settings. With this configuration, the MCP3428 can detect the input signal level as low as approximately 7.8 µV. By setting the internal PGA option to x8, the 40 µV/°C input from the thermocouple is amplified internally to 320 µV/°C before the conversion takes place. This results in about 5 LSB output codes per 1°C of change in temperature, with 16-bit conversion mode.

**EQUATION 6-1:**

\[
\text{Detectable Input Signal Level} = \frac{62.5\, \mu V}{\text{PGA}} = 7.8125\, \mu V \text{ for PGA} = 8
\]

**Input Signal Level after gain of 8:**

\[
= \left(40\, \mu V/°C \right) \times 8 = 320\, \mu V/°C
\]

\[
\text{No. of LSB}/°C = \frac{320\, \mu V/°C}{62.5\, \mu V} = 5.12 \text{ Codes/°C}
\]

Where:

1 LSB = 62.5 µV with 16 bit configuration
Equation 6-2 shows an example of calculating the expected number of output code with various PGA gain settings for Type K thermocouple output.

**EQUATION 6-2: EXPECTED NUMBER OF OUTPUT CODE FOR TYPE K THERMOCOUPLE**

\[
\text{Expected Number of Output Code} = \log_2 \left( \frac{50 \text{ mV}}{62.5 \mu V} \right)
\]

\[
= \left( \frac{\ln(800 \cdot \text{PGA})}{\ln(2)} \right)
\]

= 9.6 bits for PGA = 1
= 10.6 bits for PGA = 2
= 11.6 bits for PGA = 4
= 12.6 bits for PGA = 8

Where:

1 LSB = 62.5 µV with 16 Bit configuration.

**FIGURE 6-7:** Example of Pressure and Temperature Measurement.
Figure 6-7 shows an example of measuring both pressure and temperature. The pressure is measured by using NPP 301 (manufactured by GE NovaSensor), and temperature is measured by a thermistor. The pressure sensor output is 20 mV/V. This gives 100 mV of full scale output for VDD of 5V (sensor excitation voltage). Equation 6-3 shows an example of calculating the number of output code for the full scale output of the NPP301.

**EQUATION 6-3: EXPECTED NUMBER OF OUTPUT CODE FOR NPP301 PRESSURE SENSOR**

\[
\text{Expected Number of Output Code} = \log_2 \left( \frac{100 \, \text{mV}}{62.5 \, \mu\text{V}} \right) \frac{PGA}{\ln(2)}
\]

\[
= \ln(1600 \cdot PGA) \frac{PGA}{\ln(2)}
\]

\[
= 10.6 \text{ bits for PGA = 1}
\]

\[
= 11.6 \text{ bits for PGA = 2}
\]

\[
= 12.6 \text{ bits for PGA = 4}
\]

\[
= 13.6 \text{ bits for PGA = 8}
\]

Where:

1 LSB = 62.5 µV with 16 Bit configuration.

The thermistor temperature sensor can measure the temperature range from -100°C to +300°C. The resistance of the thermistor sensor decreases as temperature increases (negative temperature coefficient). As shown in Figure 6-7, the thermistor (R2) forms a voltage divider with R1.

The thermistor sensor is simple to use and widely used for the temperature measurement applications. It has both linear and non-linear responses over temperature range. R1 is used to adjust the linear region of interest for measurement.
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Legend:
- **XX...X**: Customer-specific information
- **Y**: Year code (last digit of calendar year)
- **YY**: Year code (last 2 digits of calendar year)
- **WW**: Week code (week of January 1 is week ‘01’)
- **NNN**: Alphanumeric traceability code
- **e3**: Pb-free JEDEC designator for Matte Tin (Sn)
- *****: This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Example:

- **8-Lead DFN (2x3) (MCP3426)**
  - Example:
    - XXX
    - YWW
    - NNN

- **8-Lead MSOP (MCP3426)**
  - Example:
    - XXXXX
    - YWWNNN

- **8-Lead SOIC (300 mil) (MCP3426)**
  - Example:
    - XXXXXXXX
    - XXXYYYWW
    - NNN

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Package Marking Information (Continued)

14-Lead SOIC (150 mil) (**MCP3428**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

14-Lead TSSOP (4.4 mm) (**MCP3428**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

10-Lead DFN (3x3) (**MCP3427**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

10-Lead MSOP (**MCP3427**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

10-Lead MSOP (**MCP3427**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

14-Lead SOIC (150 mil) (**MCP3428**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```

14-Lead TSSOP (4.4 mm) (**MCP3428**)  
Example: 

```
+---+---+---+---+---+---+---+---+---+---+
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
```
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

### Dimensions

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   **BSC:** Basic Dimension. Theoretically exact value shown without tolerances.
   **REF:** Reference Dimension, usually without tolerance, for information purposes only.

---

© 2009 Microchip Technology Inc.
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**RECOMMENDED LAND PATTERN**

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com-packaging

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N 8</td>
</tr>
<tr>
<td>Pitch</td>
<td>e 0.65 BSC</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A 1.10</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2 0.75 0.85 0.95</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1 0.00 0.15</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E 4.90 BSC</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1 3.00 BSC</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D 3.00 BSC</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L 0.40 0.60 0.80</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1 0.95 REF</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ 0° 8°</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c 0.08</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b 0.22</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>GX</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. CD4-2111A
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B
10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**RECOMMENDED LAND PATTERN**

<table>
<thead>
<tr>
<th>Units</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td>0.50 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
<td>2.48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
<td>1.55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
<td>3.10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
<td>0.30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
<td>0.65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
<td>0.20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063A
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>A1</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B
14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td></td>
<td></td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td></td>
<td></td>
<td>1.27 BSC</td>
<td>1.75</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td>1.00</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td></td>
<td></td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
<td></td>
<td></td>
<td>0.10</td>
<td>0.25</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td></td>
<td></td>
<td>6.00 BSC</td>
<td></td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
<td></td>
<td></td>
<td>3.90 BSC</td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td></td>
<td></td>
<td>8.65 BSC</td>
<td></td>
</tr>
<tr>
<td>Chamfer (optional)</td>
<td>h</td>
<td></td>
<td></td>
<td>0.25</td>
<td>0.50</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
<td></td>
<td></td>
<td>0.40</td>
<td>1.27</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
<td></td>
<td></td>
<td>1.04 REF</td>
<td></td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
<td></td>
<td></td>
<td>0°</td>
<td>8°</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
<td></td>
<td></td>
<td>0.17</td>
<td>0.25</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
<td></td>
<td></td>
<td>0.31</td>
<td>0.51</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
<td></td>
<td></td>
<td>5°</td>
<td>15°</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
<td></td>
<td></td>
<td>5°</td>
<td>15°</td>
</tr>
</tbody>
</table>

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**RECOMMENDED LAND PATTERN**

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dimension Limits</strong></td>
<td>MIN</td>
</tr>
<tr>
<td><strong>Contact Pitch</strong></td>
<td>E</td>
</tr>
<tr>
<td><strong>Contact Pad Spacing</strong></td>
<td>C</td>
</tr>
<tr>
<td><strong>Contact Pad Width</strong></td>
<td>X</td>
</tr>
<tr>
<td><strong>Contact Pad Length</strong></td>
<td>Y</td>
</tr>
<tr>
<td><strong>Distance Between Pads</strong></td>
<td>Gx</td>
</tr>
<tr>
<td><strong>Distance Between Pads</strong></td>
<td>G</td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A
14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Molded Package Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**RECOMMENDED LAND PATTERN**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X28)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X28)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A
APPENDIX A: REVISION HISTORY

Revision A (December 2009)

• Original Release of this Document.
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>-X</th>
<th>/XX</th>
<th>Device</th>
<th>Temperature Range</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3426: 2-Channel 16-Bit ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3426T: 2-Channel 16-Bit ADC (Tape and Reel)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3427: 2-Channel 16-Bit ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3427T: 2-Channel 16-Bit ADC (Tape and Reel)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3428: 4-Channel 16-Bit ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MCP3428T: 4-Channel 16-Bit ADC (Tape and Reel)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Temperature Range: **E** = -40°C to +125°C

Package:
- **MC** = Plastic Dual Flat, No Lead (2x3 DFN), 8-lead
- **MS** = Plastic Micro Small Outline (MSOP), 8-lead
- **MF** = Plastic Dual Flat, No Lead (3x3 DFN) 10-lead
- **UN** = Plastic Micro Small Outline (MSOP), 10-lead
- **SL** = Plastic Small Outline SOIC (150 mil Body), 14-lead
- **ST** = Plastic TSSOP (4.4mm Body), 14-lead

**Examples:**

a) MCP3426A0-E/MC: 2-Channel ADC, 8LD DFN package.
b) MCP3426A0T-E/MC: Tape and Reel, 2-Channel ADC, 8LD DFN package.
c) MCP3426A0-E/MS: 2-Channel ADC, 8LD MSOP package.
d) MCP3426A0T-E/MS: Tape and Reel, 2-Channel ADC, 8LD MSOP package.
e) MCP3426A0-E/SN: 2-Channel ADC, 8LD SOIC package.
f) MCP3426A0T-E/SN: Tape and Reel, 2-Channel ADC, 8LD SOIC package.

g) MCP3427-E/MF: 2-Channel ADC, 10LD DFN package.
h) MCP3427T-E/MF: Tape and Reel, 2-Channel ADC, 10LD DFN package.
i) MCP3427-E/UN: 2-Channel ADC, 10LD MSOP package.
j) MCP3427T-E/UN: Tape and Reel, 2-Channel ADC, 10LD MSOP package.

k) MCP3428-E/SL: 4-Channel ADC, 14LD SOIC package.
l) MCP3428T-E/SL: Tape and Reel, 4-Channel ADC, 14LD SOIC package.
m) MCP3428-E/ST: 4-Channel ADC, 14LD TSSOP package.
p) MCP3428T-E/ST: Tape and Reel, 4-Channel ADC, 14LD TSSOP package.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, Hi-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Octopus, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, PICs2 logo, REAL ICE, rLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
### WORLDWIDE SALES AND SERVICE

#### AMERICAS
**Corporate Office**
2355 West Chandler Blvd.
Chandler, AZ  85224-6199
Tel:  480-792-7200
Fax:  480-792-7277

Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

**Atlanta**
Duluth, GA
Tel:  768-957-9614
Fax:  768-957-1455

**Boston**
Westborough, MA
Tel:  774-760-0087
Fax:  774-760-0088

**Chicago**
Itasca, IL
Tel:  630-285-0071
Fax:  630-285-0075

**Cleveland**
Independence, OH
Tel:  216-447-0464
Fax:  216-447-0643

**Dallas**
Addison, TX
Tel:  972-818-7423
Fax:  972-818-2924

**Detroit**
Farmington Hills, MI
Tel:  248-538-2260
Fax:  248-538-2260

**Kokomo**
Kokomo, IN
Tel:  765-864-8360
Fax:  765-864-8387

**Los Angeles**
Mission Viejo, CA
Tel:  949-462-9523
Fax:  949-462-9608

**Santa Clara**
Santa Clara, CA
Tel:  408-961-6444
Fax:  408-961-6445

**Toronto**
Mississauga, Ontario, Canada
Tel:  905-673-0699
Fax:  905-673-6509

#### ASIA/PACIFIC
**Asia Pacific Office**
Suites 3707-14, 37th Floor
Tower 6, The Gateway Harbour City, Kowloon
Hong Kong
Tel:  852-2401-1200
Fax:  852-2401-3431

**Australia - Sydney**
Tel:  61-2-9868-6733
Fax:  61-2-9868-6755

**China - Beijing**
Tel:  86-10-8528-2100
Fax:  86-10-8528-2104

**China - Chengdu**
Tel:  86-28-8665-5511
Fax:  86-28-8665-7889

**China - Hong Kong SAR**
Tel:  852-2401-1200
Fax:  852-2401-3431

**China - Nanjing**
Tel:  86-25-8473-2460
Fax:  86-25-8473-2470

**China - Qingdao**
Tel:  86-6672-8502-7355
Fax:  86-6672-8502-7205

**China - Shanghai**
Tel:  86-21-5407-5533
Fax:  86-21-5407-5066

**China - Shenyang**
Tel:  86-24-2334-2829
Fax:  86-24-2334-2393

**China - Shenzhen**
Tel:  86-755-8203-2660
Fax:  86-755-8203-1760

**China - Wuhan**
Tel:  86-27-5980-5300
Fax:  86-27-5980-5118

**China - Xiamen**
Tel:  86-592-2388138
Fax:  86-592-2388130

**China - Xian**
Tel:  86-29-8833-7252
Fax:  86-29-8833-7256

**China - Zhuhai**
Tel:  86-756-3210040
Fax:  856-756-3210049

#### ASIA/PACIFIC
**India - Bangalore**
Tel:  91-80-3090-4444
Fax:  91-80-3090-4080

**India - New Delhi**
Tel:  91-11-4160-8631
Fax:  91-11-4160-8632

**India - Pune**
Tel:  91-20-2566-1512
Fax:  91-20-2566-1513

**Japan - Yokohama**
Tel:  81-45-471-6166
Fax:  81-45-471-6122

**Korea - Daegu**
Tel:  82-53-744-4301
Fax:  82-53-744-4302

**Korea - Seoul**
Tel:  82-2-554-7200
Fax:  82-2-558-5932 or 82-2-558-5934

**Malaysia - Kuala Lumpur**
Tel:  60-3-6201-9857
Fax:  60-3-6201-9859

**Malaysia - Penang**
Tel:  60-4-227-8870
Fax:  60-4-227-4068

**Philippines - Manila**
Tel:  63-2-634-9065
Fax:  63-2-634-9069

**Singapore**
Tel:  65-6334-8870
Fax:  65-6334-8850

**Taiwan - Hsin Chu**
Tel:  886-3-6578-300
Fax:  886-3-6578-370

**Taiwan - Kaohsiung**
Tel:  886-7-536-4818
Fax:  886-7-536-4803

**Taiwan - Taipei**
Tel:  886-2-2500-6610
Fax:  886-2-2508-0102

**Thailand - Bangkok**
Tel:  66-2-694-1351
Fax:  66-2-694-1350

#### EUROPE
**Austria - Wels**
Tel:  43-7242-2244-39
Fax:  43-7242-2244-393

**Denmark - Copenhagen**
Tel:  45-4450-2828
Fax:  45-4485-2829

**France - Paris**
Tel:  33-1-69-53-63-20
Fax:  33-1-69-30-90-79

**Germany - Munich**
Tel:  49-89-627-144-0
Fax:  49-89-627-144-44

**Italy - Milan**
Tel:  39-0331-742611
Fax:  39-0331-466781

**Netherlands - Drunen**
Tel:  31-416-690399
Fax:  31-416-690340

**Spain - Madrid**
Tel:  34-91-708-08-90
Fax:  34-91-708-08-91

**UK - Wokingham**
Tel:  44-118-921-5869
Fax:  44-118-921-5820

---

03/26/09