NCL30288

Power Factor Corrected Quasi-Resonant Primary Side Current-Mode Controller for LED Lighting

The NCL30288 is a compact driver for power−factor corrected flyback and non−isolated buck−boost and SEPIC converters. The controller operates in a quasi−resonant mode to provide optimal efficiency, and embeds a proprietary control method which allows the LED current to be tightly regulated from the primary side, thus eliminating the need for a secondary−side feedback circuitry and for an optocoupler.

Housed in a TSOP−6 package, the device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs.

Features

- Quasi−resonant Peak Current−mode Control Operation
- Constant Current Control with Primary Side Feedback
- Tight LED Constant Current Regulation of ±2% typical
- Near−Unity Power Factor (>0.95 typically)
- Optimized for Line Wide−range Applications
- Line Feedforward for Enhanced Regulation Accuracy
- Low Start−up Current (10 μA typ.)
- Wide V_{CC} Range
- 300 mA / 500 mA Totem Pole Driver with 12 V Gate Clamp
- Robust Protection Features
  - OVP on V_{CC}
  - Programmable Over Voltage / LED Open Circuit Protection
  - Cycle by cycle peak current limit
  - Winding Short Circuit Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Thermal Shutdown
  - V_{CC} Undervoltage Lockout
  - Brown−Out Detection
- Pb−Free, Halide−Free MSL1 Product

Typical Application

- Integral LED Bulbs and Tubes
- LED Light Engines
- LED Drivers / Power Supplies

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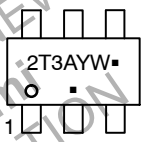
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CASE 318G−02

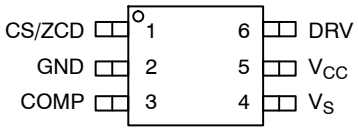
MARKING DIAGRAM



2T3 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCL30288BSNT1G	TSOP−6 (Pb−Free/ Halide Free)	3000 / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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TYPICAL APPLICATION SCHEMATIC

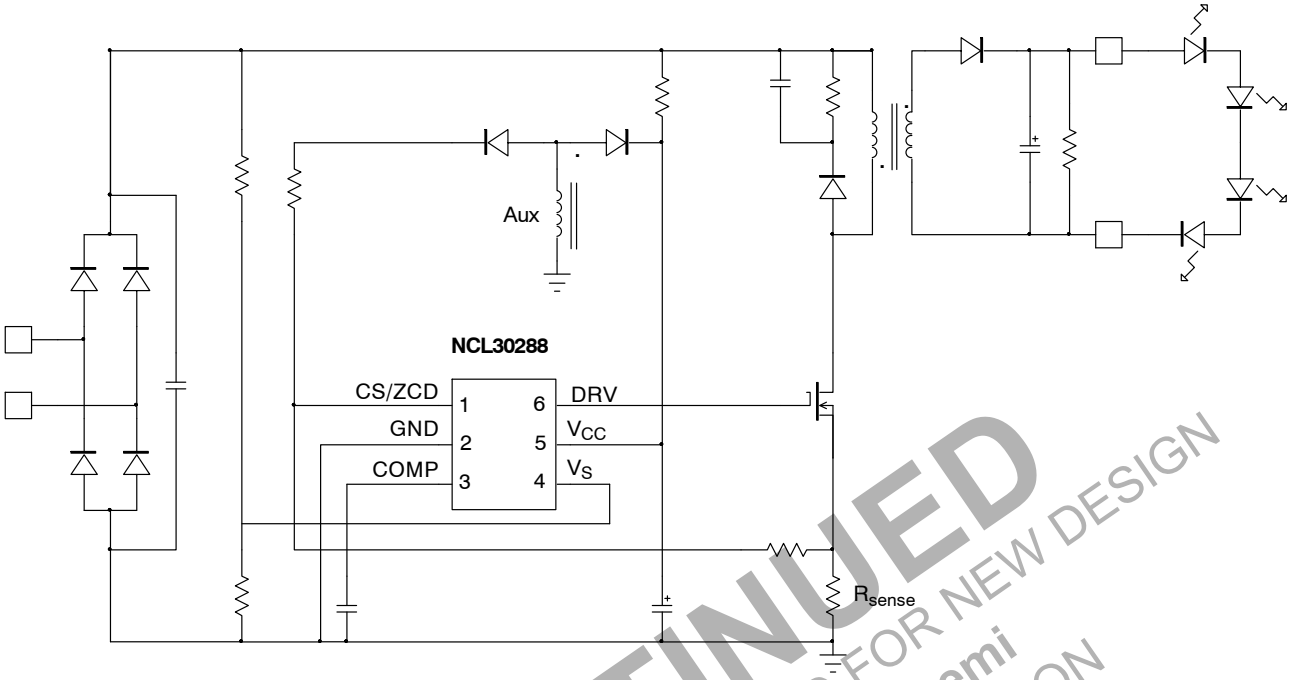


Figure 1. Typical Application Schematic in a Flyback Converter

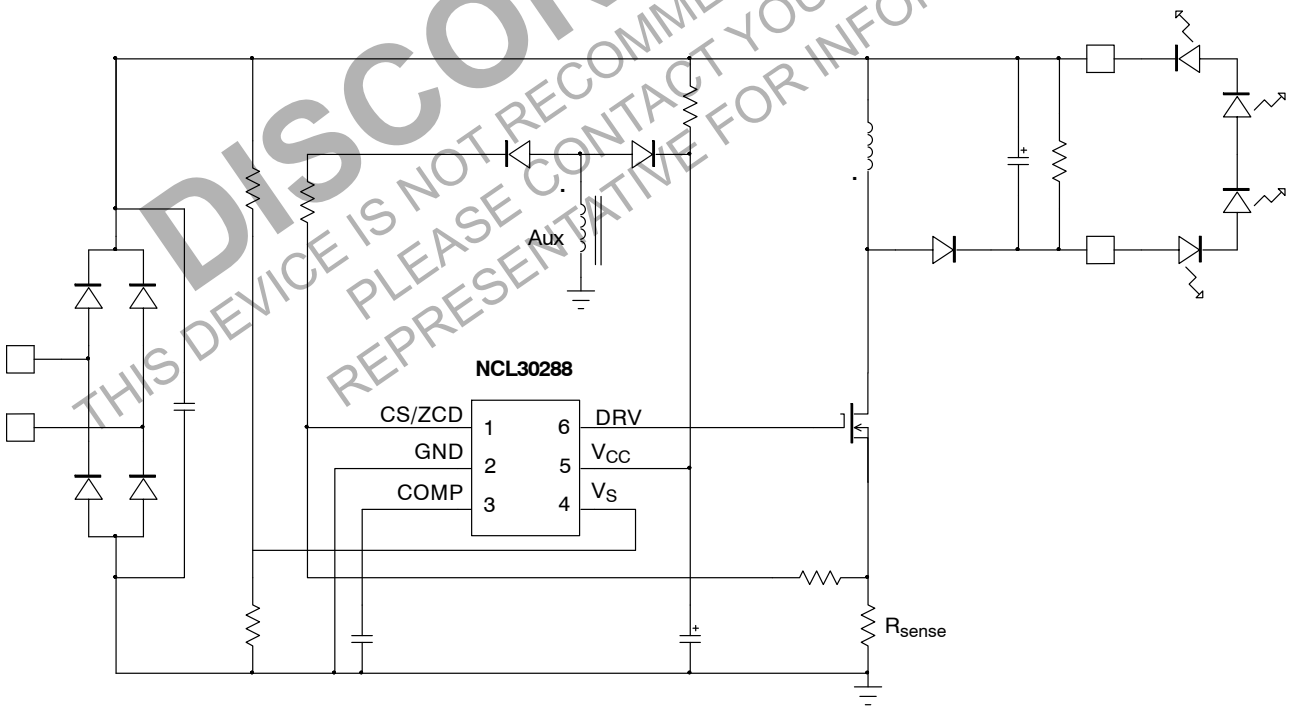


Figure 2. Typical Application Schematic in a Buck−Boost Converter

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Table 1. PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	CS/ZCD	Current Sense and Zero Current Detection	This multi−function pin is designed to monitor the primary peak current for protection and output current control and the auxiliary winding voltage for zero current detection
2	GND		Controller ground pin
3	COMP	Filtering Capacitor	This pin receives a filtering capacitor for power factor correction. Typical values ranges from 0.47 − 4.70 μF
4	V_S	Input Voltage Sensing	This pin observes the input voltage rail and protects the LED driver in case of too low mains conditions (brown−out). This pin also observes the input voltage rail for: − Power Factor Correction − Line Range Detection
5	V_{CC}	IC Supply Pin	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 18 V and turns off when V_{CC} goes below 8.8 V (typical values). After start−up, the operating range is 9.4 V up to 25.5 V ($V_{CC(OVP)}$ minimum level).
6	DRV	Driver Output	The driver's output to an external MOSFET

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INTERNAL CIRCUIT ARCHITECTURE

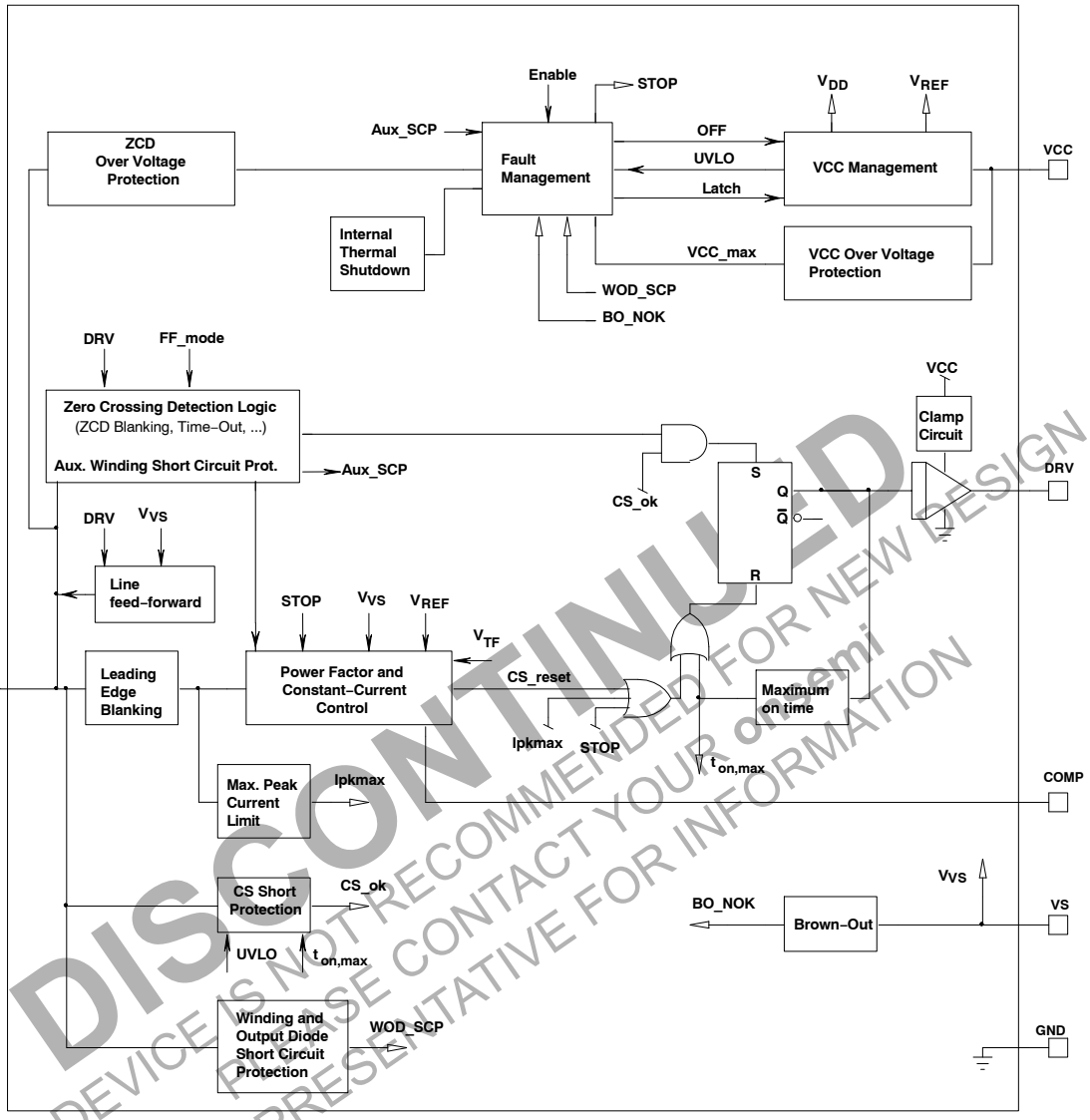


Figure 3. Internal Circuit Architecture

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Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Units
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, V_{CC} pin, continuous voltage Maximum current for V_{CC} pin	−0.3 to 30 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 1) −300, +500	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except DRV and V_{CC} pins) Current range for low power pins (except DRV and V_{CC} pins)	−0.3, 5.5 (Notes 2 and 5) −2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	360	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (HBM) (Note 3)	3.5	kV
	ESD Capability, Machine Model (MM) (Note 3)	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.
2. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5 V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the −2 mA / 5 mA range.
3. This device contains ESD protection and exceeds the following tests: Human Body Model 3500 V per JEDEC Standard JESD22−A114E, Machine Model Method 250 V per JEDEC Standard JESD22−A115B.
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
5. Recommended maximum V_S voltage for optimal operation is 4 V.

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Table 3. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, $V_{CS/ZCD}$ = 0 V
For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
Startup and Supply Circuits						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	16.0	18.0	20.0	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.2	8.8	9.4	
Hysteresis $V_{CC(on)} - V_{CC(off)}$	V_{CC} decreasing	$V_{CC(HYS)}$	8.0	–	–	
Internal logic reset	V_{CC} decreasing	$V_{CC(reset)}$	4.0	4.8	6.0	
Threshold for V_{CC} Over Voltage Protection		$V_{CC(OVP)}$	25.5	26.8	28.5	V
$V_{CC(off)}$ noise filter		$t_{VCC(off)}$	–	5	–	μs
$V_{CC(reset)}$ noise filter		$t_{VCC(reset)}$	–	20	–	
Startup current	V_{CC}=15.9 V	$I_{CC(start)}$	–	13	30	μA
Startup current in fault mode		$I_{CC(sFault)}$	–	58	75	μA
Supply Current						mA
Device Disabled / Fault	$V_{CC} > V_{CC(off)}$	I_{CC1}	1.15	1.34	1.55	
Device Enabled / No output load on pin 5	F_{sw} = 65 kHz	I_{CC2}	–	2.0	3.5	
Device Switching	C_{DRV} = 470 pF, F_{sw} = 65 kHz	I_{CC3}	–	2.5	4.0	
Current Sense						
Maximum Internal current limit		V_{ILIM}	0.94	0.99	1.04	V
Leading Edge Blanking Duration for Current Sensing		t_{LEB}	220	275	340	ns
Propagation delay from current detection to gate off−state		t_{ILIM}	–	100	150	ns
Maximum on−time		$t_{on(MAX)}$	26	36	46	μs
Threshold for immediate fault protection activation		$V_{CS(stop)}$	1.35	1.50	1.65	V
Leading Edge Blanking Duration for $V_{CS(stop)}$ (Note 1)		t_{BCS}	–	175	–	ns
Current source for CS to GND short detection		$I_{CS(short)}$	420	520	620	μA
Current sense threshold for CS to GND short detection	V_{CS} rising	$V_{CS(low)}$	30	90	150	mV
Gate Drive						
Drive Resistance						Ω
DRV Sink		R_{SNK}	–	13	–	
DRV Source		R_{SRC}	–	30	–	
Drive current capability						mA
DRV Sink (Note GBD)		I_{SNK}	–	500	–	
DRV Source (Note GBD)		I_{SRC}	–	300	–	
Rise Time (10 % to 90 %)	C_{DRV} = 470 pF	t_r	–	40	–	ns
Fall Time (90 % to 10 %)	C_{DRV} = 470 pF	t_f	–	30	–	ns
DRV Low Voltage	$V_{CC} = V_{CC(off)}$+0.2 V C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	$V_{CC} = V_{CC(MAX)}$ C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(high)}$	10	12	14	V
Zero Voltage Detection Circuit						
Upper ZCD threshold voltage	V_{ZCD} rising	$V_{ZCD(rising)}$	–	90	150	mV
Lower ZCD threshold voltage	V_{ZCD} falling	$V_{ZCD(falling)}$	35	55	–	mV
ZCD hysteresis		$V_{ZCD(HYS)}$	15	–	–	mV

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Table 3. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, $V_{CS/ZCD}$ = 0 V
For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing	t_{DEM}	–	200	300	ns
Blanking delay after on−time (normal operation)		$t_{ZCD(blank1)}$	1.12	1.50	1.88	μs
Blanking delay after on−time (startup phase)		$t_{ZCD(blank2)}$	2.24	3.00	3.76	μs
Timeout after last DEMAG transition		t_{TIMO}	6.0	7.3	9.0	μs
Time for which the CS/ZCD pin is grounded when the DRV turns low	DRV falling	T_1	200	325	450	ns
Watch Dog Timer (restart timer in the absence of demagnetization signal like for instance in startup or short circuit conditions)		t_{WDG}	40	55	70	μs
Pulling−down resistor	V_{ZCD} = $V_{ZCD(falling)}$	$R_{ZCD(pd)}$		200		kΩ
Constant Current and Power Factor Control						
Reference Voltage at T_j = 25°C		V_{REF}	195	200	205	mV
Reference Voltage at T_j = 25°C to 100°C		V_{REF}	192.5	200.0	207.5	mV
Reference Voltage at T_j = −20°C to 125°C		V_{REF}	190	200	210	mV
Reference Voltage T_j = −40°C to 125°C		V_{REF}	187.5	200.0	212.5	mV
$V_{control}$ to current setpoint division ratio		V_{ratio}	–	4	–	–
Error amplifier gain	V_{REFX}=V_{REF}	G_{EA}	44	54	64	μS
Error amplifier current capability	V_{REFX}=V_{REF}	I_{EA}		±60		μA
COMP Pin Start−up Current Source	COMP pin grounded	I_{EA_STUP}		125		μA
Line Feed Forward						
V_{VS} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	9.8	10.9	11.8	μS
Line feed−forward current on CS pin	DRV high, V_{VS} = 2 V	I_{LFF}	19.5	22.0	24.5	μA
Offset current maximum value	V_{VS} > 5 V	$I_{offset(MAX)}$	44	53	64	μA
Line Range Detection						
Threshold for high−line range (HL) detection	V_{VS} rising	V_{HL}	1.9	2.0	2.1	V
Threshold for low−line range (LL) detection	V_{VS} falling	V_{LL}	1.8	1.9	2.0	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms
Fault Protection						
Thermal Shutdown (Note 2)	F_{SW} = 65 kHz	T_{SHDN}	130	150	170	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	–	50	–	°C
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.94	0.99	1.04	V
Short circuit detection Timer	V_{ZCD} < $V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery timer duration		$t_{recovery}$	3	4	5	s
CS/ZCD OVP Threshold		V_{OVP2}	4.32	4.50	4.68	V
Brown−Out ON level (IC start pulsing)	V_S rising	$V_{BO(on)}$	0.95	1.00	1.05	V
Brown−Out OFF level (IC shuts down)	V_S falling	$V_{BO(off)}$	0.85	0.90	0.95	V
BO comparators delay		$t_{BO(delay)}$		30		μs
Brown−Out blanking time		$t_{BO(blank)}$	15	25	35	ms
V_S pin Pulling−down Current	V_S = $V_{BO(on)}$	$I_{BO(bias)}$	50	250	450	nA

1. The CS/ZCD pin is grounded for the t_{BCS} duration
2. Guaranteed by Design

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APPLICATION INFORMATION

The NCL30288 is designed to control flyback−, buck−boost− and SEPIC−based LED drivers. A proprietary circuitry ensures accurate primary−side regulation of the output current (without the need for a secondary−side feedback) and near−unity power factor correction. The circuit contains a suite of powerful protections to ensure a robust LED driver design without the need for extra components or overdesign.

- Quasi−Resonance Current−Mode Operation:
  implementing quasi−resonance operation in peak current−mode control, the NCL30288 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage in low−line conditions. When in high line, the circuit skips one valley to lower the switching frequency.
- Primary Side Constant Current Control with Power Factor Correction:
  proprietary circuitry allows the LED driver to achieve both near−unity power factor correction and accurate regulation of the output current without requiring any secondary−side feedback (no optocoupler needed). A power factor as high as 0.99 and an output current deviation below ±2% are typically obtained.
- Main protection features:
  - Programmable Over−Voltage Protection (OVP2):
    The CS/ZCD pin provides a programmable OVP protection. Adjust the external ZCD resistors divider or add a Zener diode to adjust the protection threshold: if the CS/ZCD pin voltage exceeds 4.5 V (during the demagnetization time) for 4 consecutive switching cycles, the controller stops operating for the 4−s auto−recovery delay.
  - Cycle−by−cycle peak current limit:
    when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is immediately turned off (cycle by cycle current limitation).
  - Winding or Output Diode Short−Circuit Protection (WODSCP):
    an additional comparator senses the CS signal and stops the controller if it exceeds 150% x V_{ILIM} for 4 consecutive cycles. This feature can protect the converter if a winding is shorted or if the output diode is shorted or simply if the transformer saturates.
  - Auxiliary Short−circuit protection (AUX_SCP):
    If the ZCD pin voltage remains low for a 90 ms time interval, the controller detects that the output or the ZCD pin is grounded and hence, stops pulsating until a 4 s time has elapsed.
  - Open LED protection:
    if the LED string is open, the output voltage will rise and lead the programmable over−voltage protection (OVP2) or the V_{CC} OVP to trip (V_{CC} OVP trips when the V_{CC} pin voltage exceeds the $V_{CC(OVP)}$ threshold − 26.8 V typically). In such a case, the controller shuts down and waits 4 seconds before restarting switching operation.
  - Floating or Short Pin Detection:
    the circuit can detect most of these situations which helps pass safety tests.

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Constant Current Control

The NCL30288 embeds an analog/digital block to control the power factor and regulate the output current by monitoring the ZCD, V_S and CS pin voltages (signals ZCD, V_S and V_{CS} of Figure 4). This circuitry generates the current setpoint ($V_{CONTROL}$) and compares it to the current sense signal (V_{CS}) to dictate the MOSFET turning off event when V_{CS} exceeds $V_{CONTROL}$.

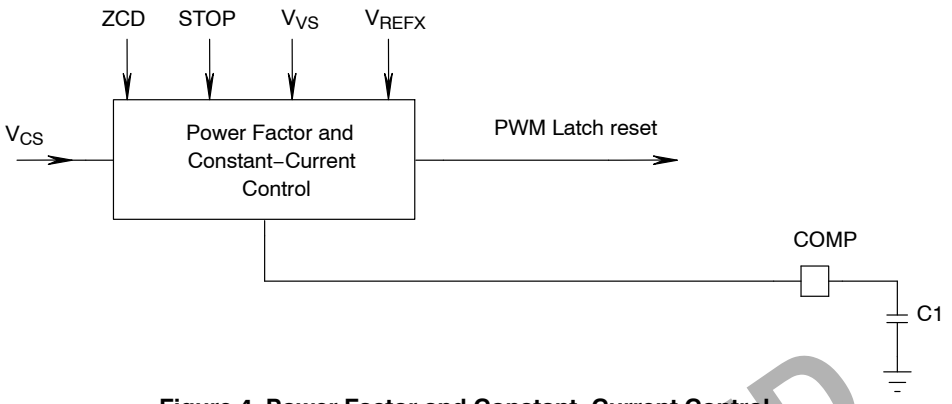


Figure 4. Power Factor and Constant−Current Control

As illustrated in Figure 4, the V_S pin provides the sinusoidal reference necessary for shaping the input current. The obtained current reference is further modulated so that when averaged over a half−line period, it is equal to the output current reference (V_{REFX}). This averaging process is made by an internal Operational Trans−conductance Amplifier (OTA) and the capacitor connected to the COMP pin (C1 of Figure 4). Typical COMP capacitance is 1 μF and should not be less than 470 nF to ensure stability. The COMP ripple does not affect the power factor performance as the circuit digitally eliminates it when generating the current setpoint.

If the V_S pin properly conveys the sinusoidal shape, power factor will be close to unity and the Total Harmonic Distortion (THD) will be low. In any case, the output current will be well regulated following the equation below:

$$I_{out} = \frac{V_{REF}}{2\, N_{PS}\, R_{sense}} \qquad \text{(eq. 1)}$$

Where:

- N_{PS} is the secondary to primary transformer turns $N_{PS} = N_S / N_P$
- R_{sense} is the current sense resistor (see Figure 1).
- V_{REF} is the output current internal reference (200 mV).

Whenever a major fault is detected which forces the auto−recovery mode, the COMP pin is grounded for the 4−s interruption. This is also the case if one of these situations is detected: brown−out, UVLO, TSD fault. This ensures a clean start−up when the circuit resumes operation.

Start−up Sequence

Generally an LED lamp is expected to emit light in < 1 s and typically within 500 ms. The start−up phase consists of the time to charge the V_{CC} capacitor, to begin switching and the time to charge the output capacitor until sufficient current flows into the LED string. To speed−up this phase, the following characteristics define the start−up sequence:

- The COMP pin is grounded when the circuit is off. The average COMP voltage needs to exceed the V_S pin peak value to have the LED current properly regulated (whatever the current target is). To speed−up the COMP capacitance charge and shorten the start−up phase, an internal 80 μA current source adds to the OTA sourced current (60 μA max typically) to charge up the COMP capacitance. The 80 μA current source remains on until the OTA starts to sink current as a result of the COMP pin voltage sufficient rise. At that moment, the COMP pin being near its steady−state value, only the OTA drives the COMP pin.
- If the load is shorted, the circuit will operate in hiccup mode with V_{CC} oscillating between $V_{CC(off)}$ and $V_{CC(on)}$ until the Auxiliary Short Circuit Protection, AUX_SCP, forces the 4 s auto−recovery delay to reduce the operation duty−ratio (AUX_SCP trips if the ZCD pin voltage does not exceed 1 V within a 90 ms active period of time thus indicating a short to ground of the ZCD pin or an excessive load preventing the output voltage from rising). Figure 5 illustrates a start−up sequence with the output shorted to ground.

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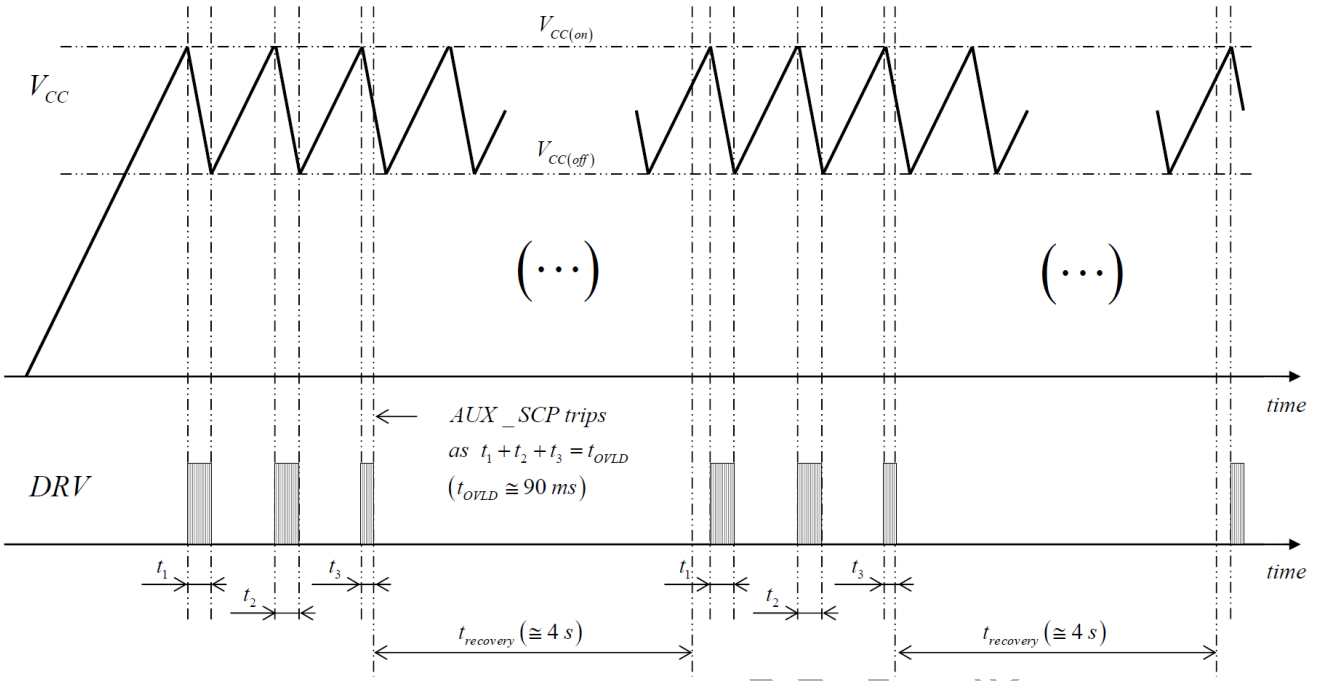


Figure 5. Start−up Sequence in a Load Short−circuit Situation

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Zero Crossing Detection Block

The CS/ZCD pin detects when the drain−source voltage of the power MOSFET reaches a valley by crossing down the 55 mV internal threshold and initiates a new DRV pulse at that moment. At startup and in overload conditions, the ZCD comparator may not be able to detect the demagnetization signal. To allow a new DRV pulse to occur, the NCL30288 features a watchdog timer which initiates a DRV pulse if the CS/ZCD pin voltage does not trig the ZCD comparator for the watchdog time. The watchdog duration is typically 55 μs at low line. It increases to 62 μs when the line range is detected (see next section).

As detailed in next section, the NCL30288 operates in QR mode at low line and at valley 2 in high−line conditions. If the auxiliary winding free oscillations are extremely damped, the ZCD comparator may not be able to detect the second valley as necessary at high line. To overcome this high−line situation, the NCL30288 features a time−out circuit to initiate a DRV pulse if once the demagnetization is detected, the CS/ZCD pin voltage stays below the ZCD comparator internal threshold for about 7.3 μs. Hence, the time−out acts as a substitute clock for valley−2 detection.

In other words:

- The timeout timer initiates a DRV pulse at high line if valley 1 is detected but valley 2 cannot be detected.
- The watchdog timer prevents the circuit from keeping permanently off if no demagnetization signal can be detected (e.g. at startup).

Whenever the controller enters operation (cold startup, restart after a failure to startup at the first attempt or operation recovery after a fault), the ZCD blanking time is $t_{ZCD(blank2)}$ (3 μs typically) and keeps this value until the ZCD signal is high enough to be detected by the ZCD comparator (higher than $V_{ZCD(rising)}$, 90 mV typically). At that moment, the ZCD blanking time recovers its nominal level ($t_{ZCD(blank1)}$ =1.5 μs, typically).

If the ZCD pin or the auxiliary winding happen to be shorted, the watchdog function would normally make the controller keep switching and hence lead to improper LED current regulation. The “AUX_SCP” protection prevents such a stressful operation: a timer starts counting which is only reset when the ZCD voltage exceeds the $V_{ZCD(short)}$ threshold (1 V typically). If this timer reaches 90 ms (no ZCD voltage pulse having exceeded $V_{ZCD(short)}$ for this time period), the controller detects a fault and stops operation for 4 seconds.

The CS/ZCD pin is grounded for 325 ns (time T_1 of the parametric table) when the drive turns low. This prevents a possible CS residual voltage to be taken into account by the ZCD comparator, which could otherwise occur in particular if a filtering capacitor was added to the pin. Similarly, the CS/ZCD pin is “reset” when the drive turns high. Practically, the pin is grounded for the 175 ns t_{BCS} time (Leading Edge Blanking Duration for $V_{CS(stop)}$) to in this case, avoid that a V_{AUX} remaining voltage alters the current sense block operation.

For an optimal operation, the maximum ZCD level should be maintained below 5 V to stay safely below the built in clamping voltage of the pin.

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Line Range Detection

As sketched in Figure 6, this circuit detects the low−line range if the V_S pin remains below the V_{LL} threshold (1.9 V typical) for more than the 25 ms blanking time. The high−line range is detected ("HL" of Figure 6 is high) as soon as the V_S pin voltage exceeds V_{HL} (2.0 V typical). These levels roughly correspond to 152 V rms and 160 V rms line voltages if the external resistors divider applied to the V_S pin is designed to provide a 1 V peak value at 80 V rms.

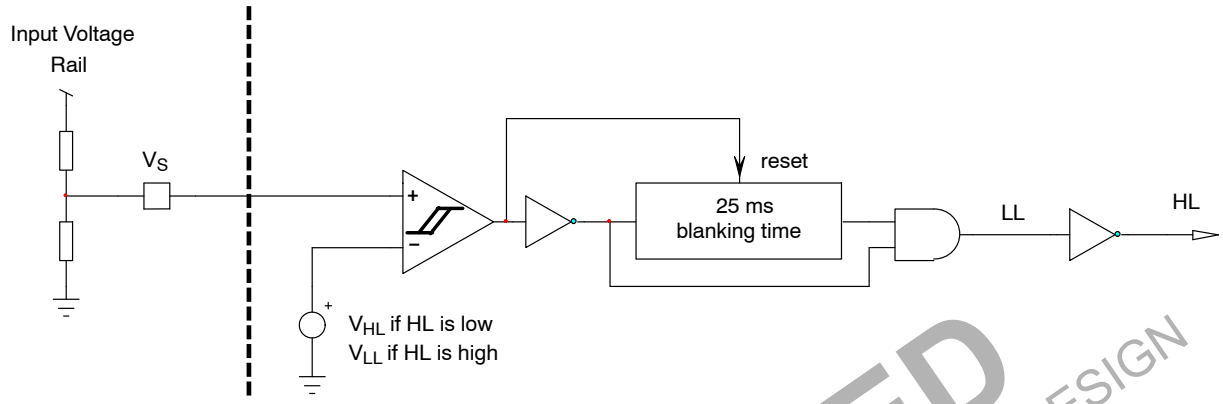


Figure 6. Line Range Detection Circuitry

In the low−line range, conduction losses are generally dominant. Adding a dead−time would further increase these losses by forcing increased switching current. In high−line conditions, switching losses generally are the most critical. It is thus efficient to skip one valley to lower the switching frequency. Hence, under normal operation, the NCL30288 optimizes the efficiency over the line range by turning on the MOSFET at the first valley in low−line conditions and at the second valley in the high−line case. This is illustrated by Figure 7 that sketches the MOSFET Drain−source voltage in both cases.



Figure 7. Quasi−resonant Mode in Low Line (left), Turn on at Valley 2 when in High Line (right)

In addition, the gain of the current control block is divided by two when the high−line range is detected. This allows for an optimal resolution of the output current over the line range.

Line Feedforward

The NCL30288 computes the current setpoint ($V_{control}$) for power factor correction and proper regulation of the LED current. Now, the MOSFET cannot turn off at the very moment when the current−sense voltage exceeds $V_{control}$. There actually exists a propagation delay for which the primary current keeps rising. As a result, the primary current does not exactly peak to the expected ($V_{control}$ / R_{SENSE}) value but to a higher level. The NCL30288 features the line feedforward function to compensate for this effect.

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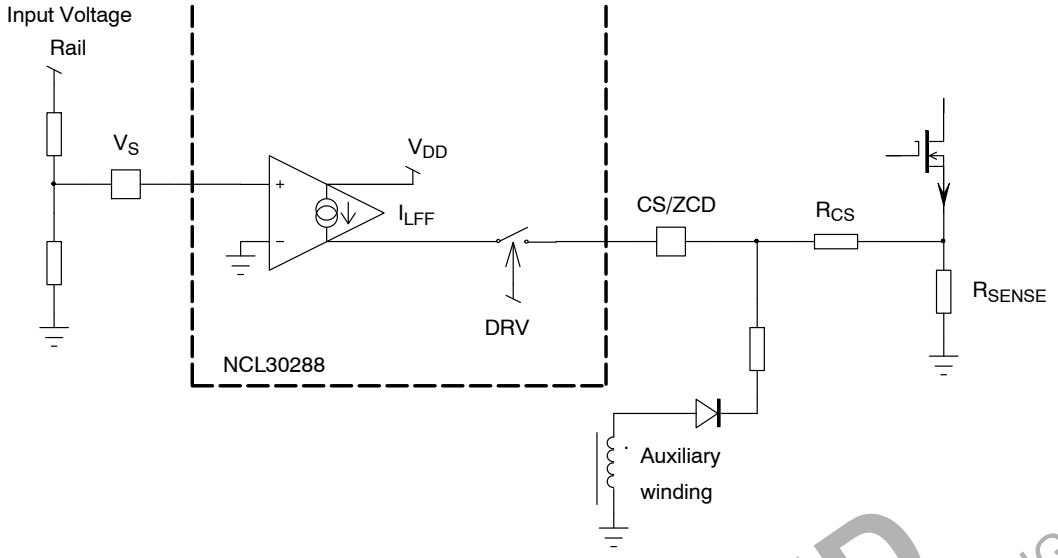


Figure 8. Line Feed−Forward Schematic

As illustrated by Figure 8, the input voltage is sensed by the V_S pin and converted into a current (I_{LFF}) which is sourced by the CS/ZCD pin during the MOSFET on−time. An external resistor (R_{CS}) being placed between the MOSFET current sense resistor (R_{SENSE}) and the CS pin, this current produces a voltage offset proportional to the input voltage which is added to the CS signal. This effectively compensates for the over−currents caused by the switching delays. For optimal output current accuracy over the line range, R_{CS} must thus be optimized as a function of the application switching delays.

Protections

The circuit incorporates a large variety of protections to make the LED driver very rugged. Among them, we can list:

- Output Short Circuit Situation
  An overload fault is detected if the CS/ZCD pin voltage remains below $V_{ZCD(short)}$ for 90 ms. The signal is compared to $V_{ZCD(short)}$ during the off time after the ZCD blanking time is elapsed. In such a situation, the circuit stops generating pulses until the 4 s delay auto−recovery time has elapsed.
- Winding or Output Diode Short Circuit Protection(WODSCP)
  If a transformer winding happens to be shorted, the primary inductance will collapse leading the current to ramp up in a very abrupt manner. The V_{ILIM} comparator (current limitation threshold) will trip to open the MOSFET and eventually stop the current rise. However, because of the abnormally steep slope of the current, internal propagation delays and the MOSFET turn−off time will make possible the current rise up to 50% or more of the nominal maximum value set by V_{ILIM}. As illustrated in Figure 9, the circuit uses this current overshoot to detect a winding short circuit. The leading edge blanking (LEB) time for short circuit protection is significantly shorter than the LEB time for cycle−by−cycle protection (LEB2 lasts for T_{BCS} − 175 ns typically – while LEB1 lasts for T_{LEB} − 275 ns typically). Practically, if four consecutive switching periods lead the CS pin voltage to exceed $V_{CS(stop)}$ ($V_{CS(stop)}$=150% *V_{ILIM}), the controller enters auto−recovery mode (4 s operation interruption between active bursts). Similarly, this function can also protect the power supply if the output diode is shorted or if the transformer simply saturates.

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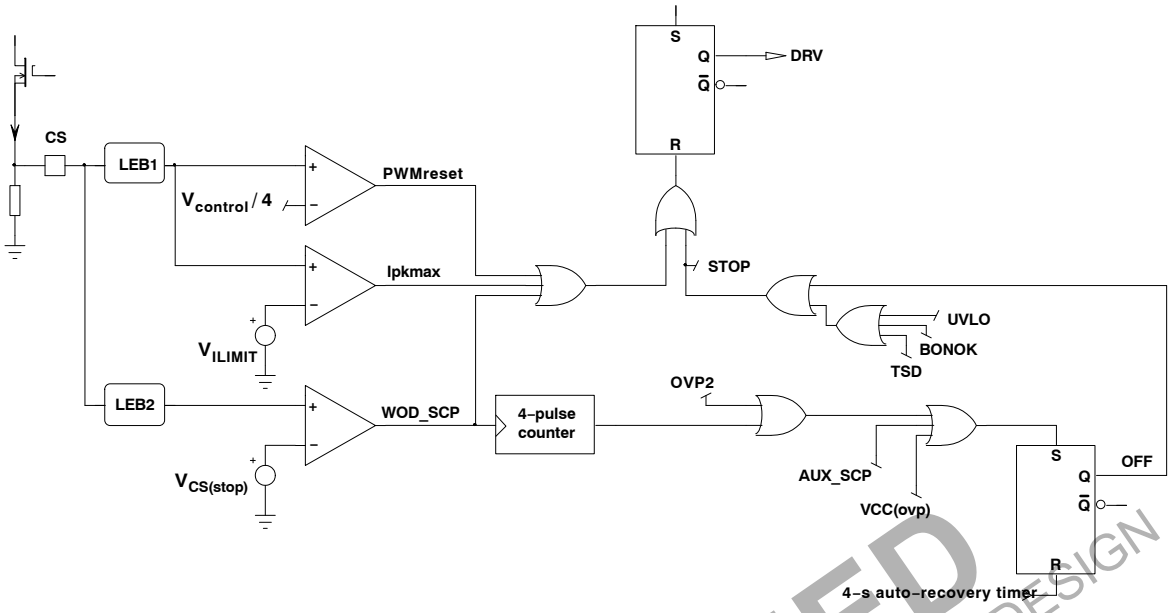


Figure 9. Winding Short Circuit Protection, Max. Peak Current Limit Circuits

- V_{CC} Over Voltage Protection
  The circuit stops generating pulses if V_{CC} exceeds $V_{CC(OVP)}$ and enters auto−recovery mode. This feature protects the circuit if the output LED string happens to open or is disconnected.
- Programmable Over Voltage Protection (OVP2)
  The ZCD signal is compared to an internal 4.5 V threshold. If V_{ZCD} exceeds this threshold for more than 1 μs (after the ZCD blanking time), an OVP event is detected. If this happens for 4 consecutive switching cycles, an OVP fault is detected and the system enters auto−recovery mode.
- Cycle−by−Cycle Current Limit
  When the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- Brown−Out Protection
  The NCL30288 prevents operation when the line voltage is too low for proper operation. As sketched in Figure 10, the circuit detects a brown−out situation (BONOK is high) if the V_S pin remains below the $V_{BO(off)}$ threshold (0.9 V typical) for more than the 25 ms blanking time. In this case, the controller stops operating. Operation resumes as soon as the V_S pin voltage exceeds $V_{BO(on)}$ (1.0 V typical) and V_{CC} is higher than $V_{CC(on)}$. To ease recovery, the circuit overrides the V_{CC} normal sequence (no need for V_{CC} cycling down below $V_{CC(off)}$). Instead, its consumption immediately reduces to $I_{CC(start)}$ so that V_{CC} rapidly charges up to $V_{CC(on)}$. Once done, the circuit re−starts operating.

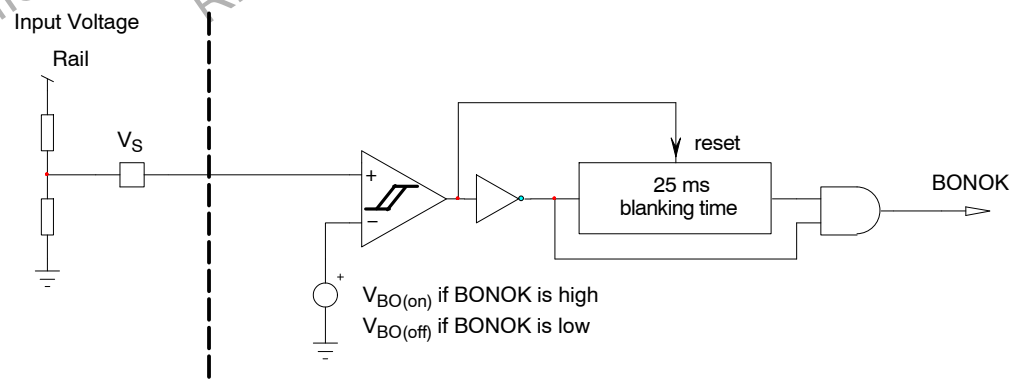


Figure 10. Brown−out Protection Circuit

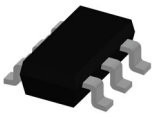
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- Die Over Temperature (TSD)
  The circuit stops operating if the junction temperature (T_J) exceeds 150°C typically. The controller remains off until T_J goes below nearly 100°C.
- Pin connection faults
  The circuit addresses most pin connection fault cases. In particular, the circuit detects the CS pin short to ground situations by sensing the CS/ZCD pin impedance every time it starts−up and after DRV pulses are terminated by the 36 μs maximum on−time. If the measured impedance does not exceed 170 Ω typically, the circuit stops operating. In practice, it is recommended to place a minimum of 500 Ω in series between the CS pin and the current sense resistor to take into account possible parametric deviations.

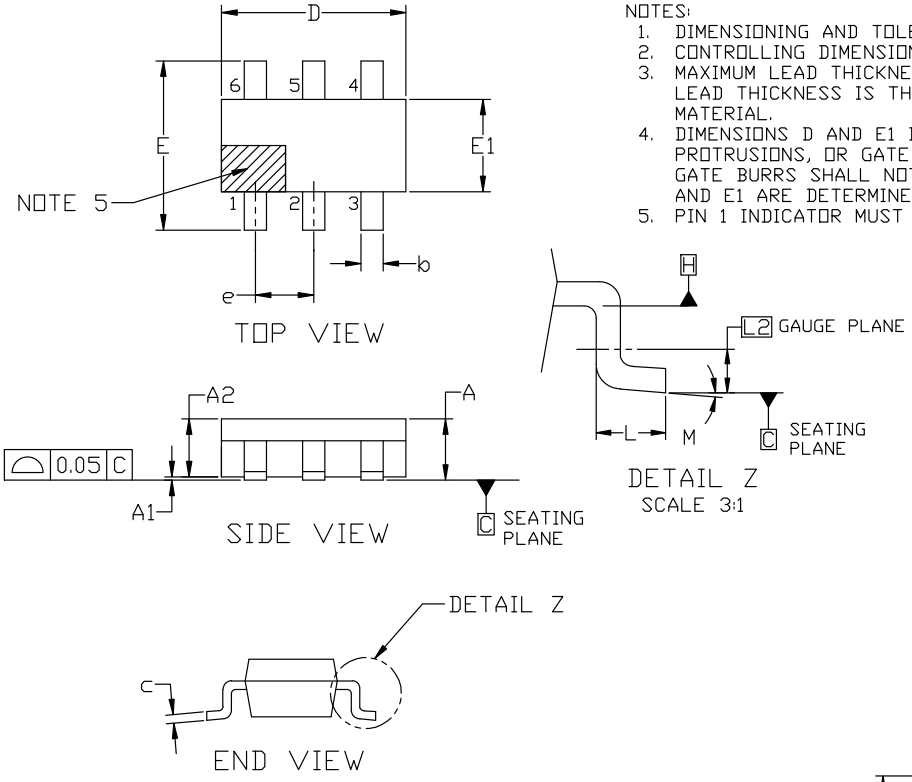
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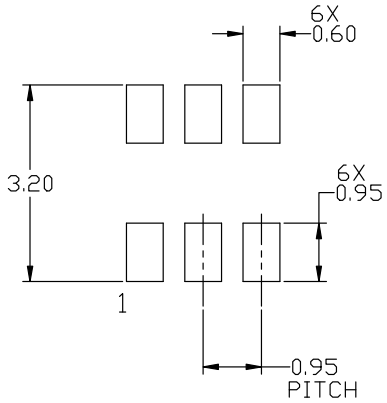
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CASE 318G
ISSUE W

DATE 26 FEB 2024



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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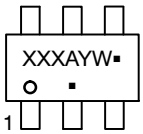
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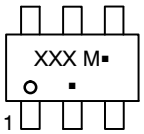
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GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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