

Features

Frequency range : 1MHz to 200MHz
 SMD seam sealing ceramic package
 Supply voltage : 1.8V, 2.5V, 3.3V
 CMOS output
 Operating Temperature : -40°C~+105°C
 Phase Jitter : 1ps(typ.)@100MHz, 3.3V
 Dimensions : 5.0 x 3.2 x 1.2 mm
 RoHS & REACH compliant, Pb-free, Halogen-free

Applications

NB, PC, Tablet, Smartphone,
 PC peripherals, IPC, Server, Storage,
 Ethernet, USB...etc.
 Audio ADC, Video,
 AI Vision Processing Unit, CPLD,
 FPGA, CPU, GPU, MCU, BMC...etc.

Electrical Characteristics

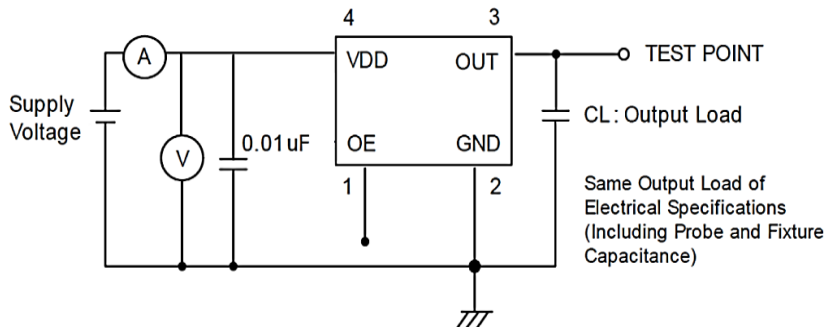
Item	7CL	Conditions
Frequency Range (F_0)	1MHz ~ 200MHz	V_{DD} @ 2.5 or 3.3V
	1MHz ~ 125MHz	V_{DD} @ 1.8V
Frequency Stability (F_{stab})	±25 ppm	-40°C ~ +85°C; Note [1]
	±50 ppm	-40°C ~ +105°C; Note [1]
Operating Temperature Range (T_{OTR})	-40°C ~ +85°C	
	-40°C ~ +105°C	
Supply Voltage (V_{DD})	1.8V, 2.5V, 3.3V	$V_{DD} \pm 10\%$
Current Consumption (I_{DD})	30 mA Max.	
Standby current (I_{DD_ST})	5 mA Max.	OE = Low
Output Type / Load (C_L)	CMOS / 15 pF	
Output Voltage High (V_{OH})	90% V_{DD} Min.	V_{DD} @ 2.5 or 3.3V
	($V_{DD} - 0.4V$) Min.	V_{DD} @ 1.8V
Output Voltage Low (V_{OL})	10% V_{DD} Max.	V_{DD} @ 2.5 or 3.3V
	0.4V Max.	V_{DD} @ 1.8V
Rise & Fall Time (T_r / T_f)	5 ns Max.	10% ~ 90% of V_{DD} level
Duty Cycle	45% ~ 55%	
Start-up Time	10 ms Max.	To 90% of final amplitude
Enable Voltage High (V_{IH}), Logic "1"	70% V_{DD} Min.	Enable control @ Pin 1
Enable Voltage Low (V_{IL}), Logic "0"	30% V_{DD} Max.	
Aging (F_{aging})	±3 ppm Max.	First year at 25°C
RMS Phase Jitter (PJ) ^[2] Fout range : 10MHz~40MHz @ Integrated from 12kHz~5MHz	1.2 ps Typ.	V_{DD} @ 3.3V
	1.5 ps Typ.	V_{DD} @ 2.5V
	2.0 ps Typ.	V_{DD} @ 1.8V
RMS Phase Jitter (PJ) ^[2] Fout range : 40MHz~200MHz @ Integrated from 12kHz~20MHz	1.0 ps Typ.	V_{DD} @ 3.3V
	1.1 ps Typ.	V_{DD} @ 2.5V
	1.5 ps Typ.	V_{DD} @ 1.8V

Notes:

[1] Inclusive of frequency tolerance at 25°C, variation over temperature, supply voltage variation, aging and vibration.

[2] Phase Jitter will be slightly different according to output frequency and supply voltage.

Testing diagram:

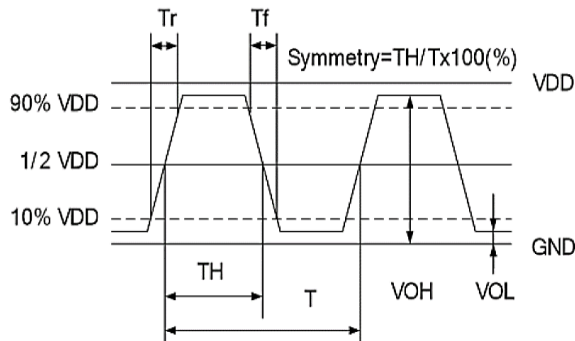


Pad 1 (OE)	Pad 3 (output)	Oscillator
High (or open)	OSC out	Normal operation
Low	High impedance	Stop oscillation

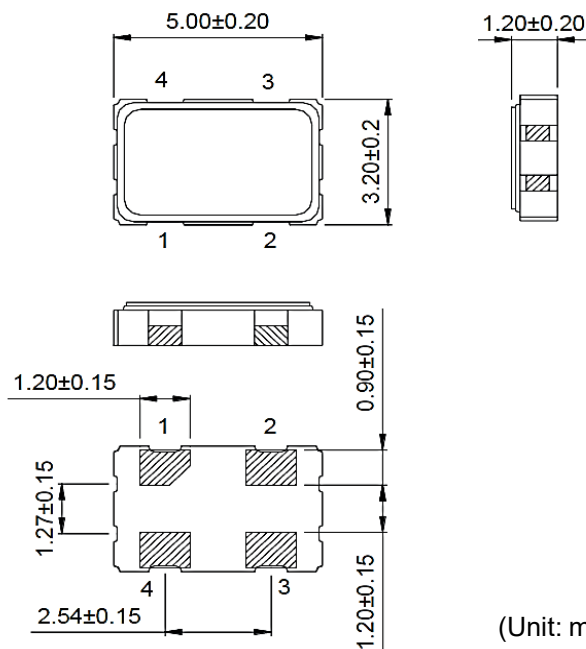
Notes: Sets CL to 15pF for simulation IC load. Customer does not need to layout it in reality circ

Waveform conditions :

Waveform measurement system should have a min. bandwidth of 5 times the frequency being testec



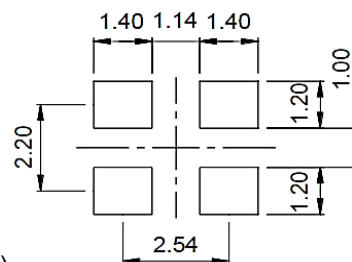
Dimensions & Recommended Footprint



PAD FUNCTION:

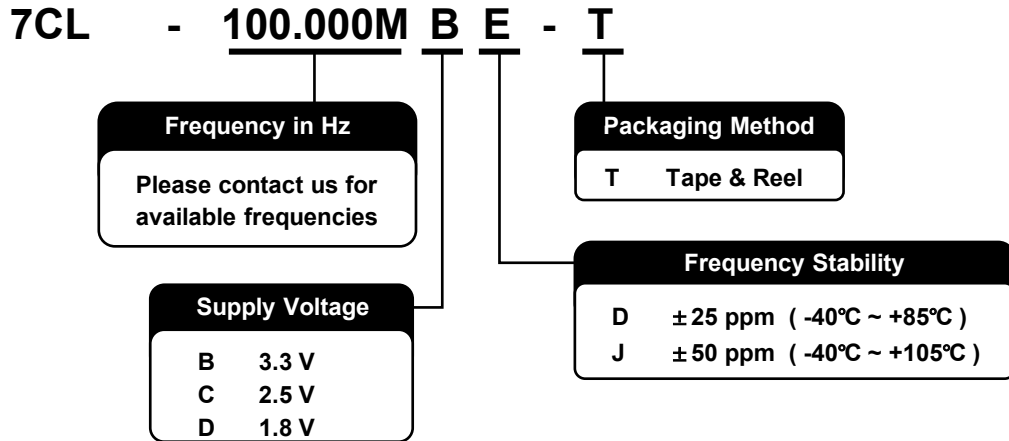
- 1: OE
- 2: GND
- 3: OUT
- 4: VDD

Suggested Layout

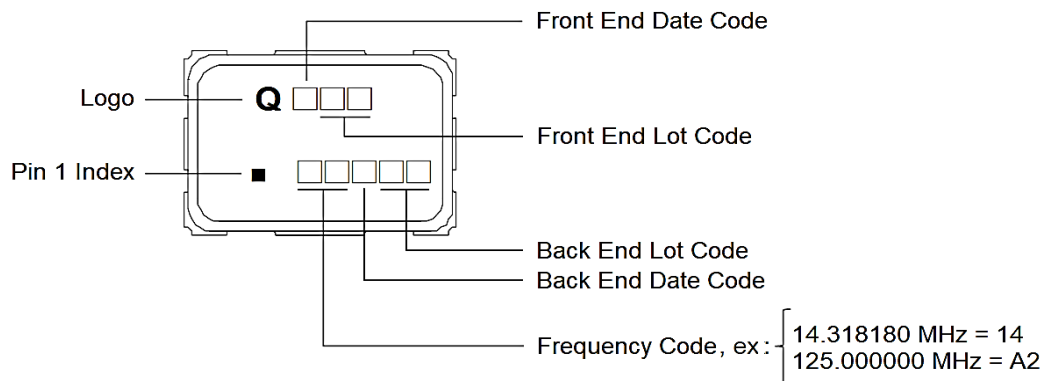


(Unit: mm)

Ordering Information



Marking

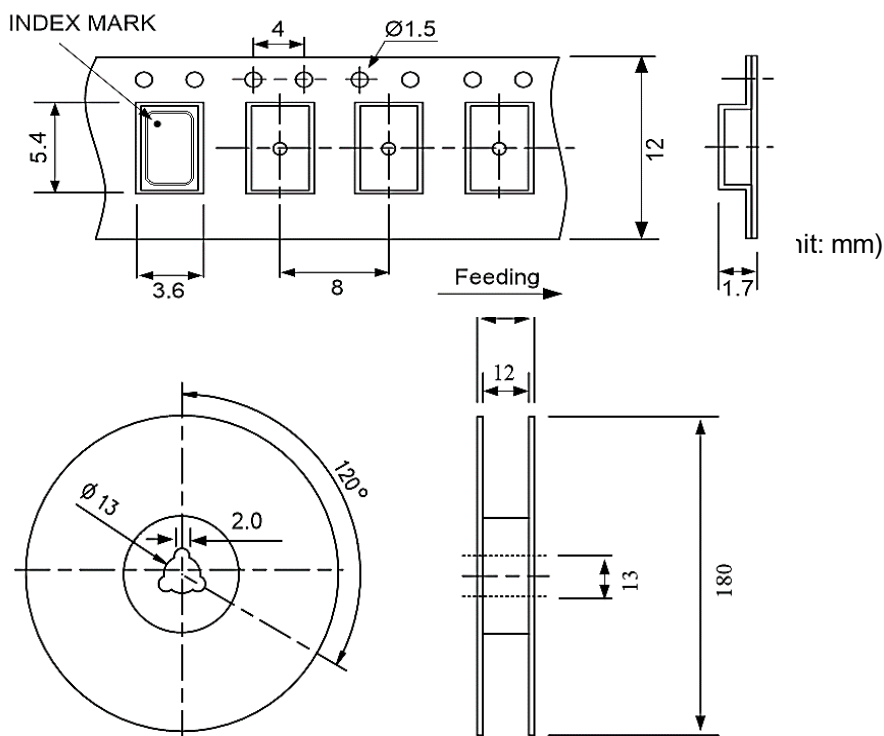


Date Code:

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
					A	B	C	D	E	F	G	H	J	K	L	M
2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z

*This date code will be cycled every four years

Packing



Reflow Profile

Solder melting point : $220^{\circ}\text{C} \pm 10^{\circ}\text{C}$, 60 sec. Min.

Peak temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$, 10 sec. Min.

