PI6CG33601C

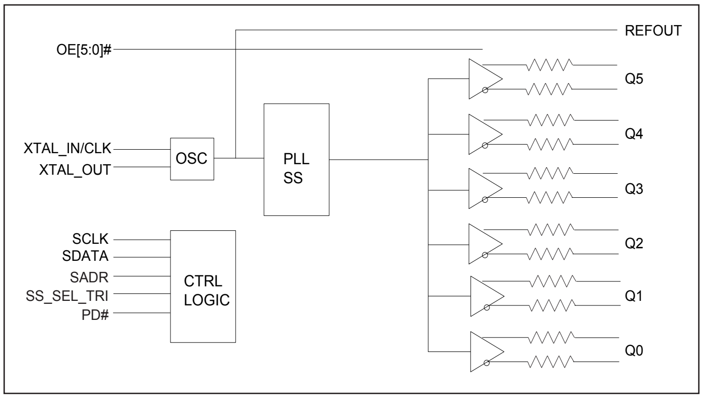
3.3V Very Low Power 6-Output PCIe Clock Generator With On-chip Termination

Description

The DIODES PI6CG33601C is a 6-output very low power PCIe Gen1/Gen2/Gen3/Gen4/Gen5/Gen6 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 24 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low noise reference for other circuitry.

It uses Diodes' proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4/Gen5/Gen6 requirements. It also provides various options such as different slew rate and amplitude through SMBUS so that users can configure the device easily to get the optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for various applications.

Block Diagram



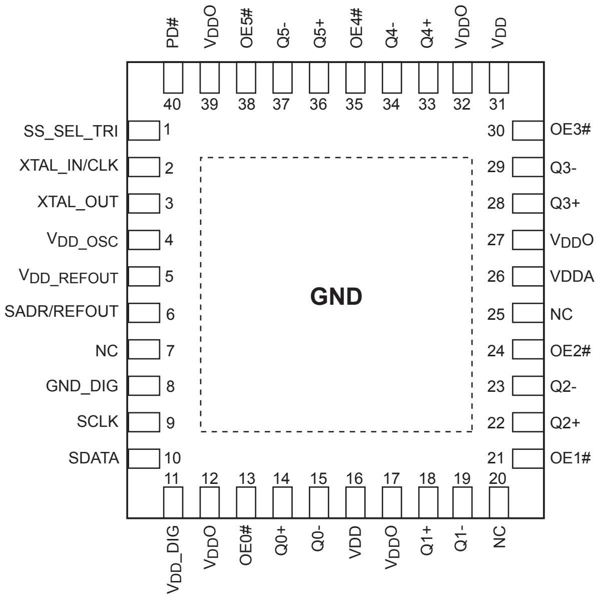
Features

- 3.3V Supply Voltage
- Crystal/CMOS input: 25 MHz
- 6 Differential low power HCSL outputs with on-chip termination
- Default Z_{OUT} = 100Ω
- Individual output enable
- Reference CMOS output
- Programmable slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Selectable 0%, -0.25% or -0.5% spread on differential outputs
- Strapping pins or SMBus for configuration
- Differential Output-To-Output Skew <50ps
- Very-Low Jitter Outputs
  - Differential Cycle-To-Cycle Jitter <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4/Gen5/Gen6 Compliant
  - CMOS REFOUT Phase Jitter
    - <0.3ps RMS, SSC off
    - <1.5ps RMS, SSC on
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 40-lead 5×5mm TQFN

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	SS_SEL_TRI	Input	Tri-level	Latched select input to select spread spectrum amount at initial power up 1 = -0.5% spread, M = Spread Off, 0 = Spread Off. This pin has both internal pull-up and pull-down. Refer to SMBUS byte_1 bit 4, 3 = '01' to get -0.25% spread.
2	XTAL_IN/CLK	Input		Crystal input or CMOS reference input
3	XTAL_OUT	Output		Crystal output
4	V_{DD}_OSC	Power		Power supply for oscillator circuitry, nominal 3.3V
5	V_{DD}_REFOUT	Power		Power supply for buffered CMOS output
6	SADR/REFOUT	Input/ Output	CMOS	Latch to select SMBus Address or LVCMOS REFOUT. This pin has an internal pull-down
7, 20, 25	NC	N/A		No Connect
8	GND_DIG	Power		Ground for digital circuitry
9	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
10	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
11	V_{DD}_DIG	Power		Power supply for digital circuitry, nominal 3.3V
12, 17, 27, 32, 39	V_{DDO}	Power		Power supply for differential outputs
13	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs

Pin #	Pin Name	Type		Description
14	Q0+	Output	HCSL	Differential true clock output
15	Q0-	Output	HCSL	Differential complementary clock output
16, 31	V_{DD}	Power		Power supply, nominal 3.3V
18	Q1+	Output	HCSL	Differential true clock output
19	Q1-	Output	HCSL	Differential complementary clock output
21	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
22	Q2+	Output	HCSL	Differential true clock output
23	Q2-	Output	HCSL	Differential complementary clock output
24	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
26	V_{DDA}	Power		Power supply for analog circuitry
28	Q3+	Output	HCSL	Differential true clock output
29	Q3-	Output	HCSL	Differential complementary clock output
30	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
33	Q4+	Output	HCSL	Differential true clock output
34	Q4-	Output	HCSL	Differential complementary clock output
35	OE4#	Input	CMOS	Active low input for enabling Q4 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
36	Q5+	Output	HCSL	Differential true clock output
37	Q5-	Output	HCSL	Differential complementary clock output
38	OE5#	Input	CMOS	Active low input for enabling Q5 pair. This pin has an internal pull-down. 1 = disable outputs, 0 = enable outputs
40	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.

Table 1. SMBus Address Selection

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101000	X
	1	1101010	X

Table 2. Power Management Table(3)

PD#	SMBus OE bit	OEn#	Qn+	Qn-	REFOUT
0	X	X	Low(1)	Low(1)	HiZ(2)
1	1	0	Running	Running	Running
1	1	1	Disabled(1)	Disabled(1)	Running
1	0	X	Disabled(1)	Disabled(1)	Disabled(4)

Note:
1. The output state is set by B11[1:0] (Low/Low default)
2. REF is Hi-Z until the 1st assertion of PD# high. After this, when PD# is low, REF is disabled. If Byte3, bit 5 = 1, then REF is running
3. Input High/ Low defined at default values for device
4. See SMBUs Byte 3, bit 4

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.. –65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx} ....–0.5V to +4.6V
Input Voltage .... –0.5V to V_{DD}+0.5V, not exceed 4.6V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) .... 2000 V
Max Junction Temperature ....+125°C

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}, V_{DDA}, V_{DD_OSC}, V_{DD_DIG},	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		1.0	3.3	3.465	V
V_{DD_REFOUT}	Reference Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DDA}	Analog Power Supply Current	All outputs active @100MHz		22	25	mA
I_{DD}	Power Supply Current	All V_{DD}, except V_{DDA} and V_{DDO}, All outputs active @100MHz		20	25	mA
I_{DDO}	Power Supply Current for Outputs(3)	All outputs active @100MHz		24	30	mA
I_{DDA_WL}	Analog Power Supply Wake-on-LAN[1] Current	Q outputs off, REF output running		0.5	1.0	mA
I_{DD_WL}	Power Supply Wake-on-LAN(1) Current	All V_{DD}, except V_{DDA} and V_{DDO}, Q outputs off, REF output running		3.0	6.0	mA
I_{DDO_WL}	Power Supply Wake-on-LAN(1) Current for Outputs	Q outputs off, REF output running		0.04	0.1	mA
I_{DDA_PD}	Analog Power Supply Power Down[2] Current	All outputs off		0.5	1.0	mA
I_{DD_PD}	Power Supply Power Down(2) Current	All outputs off		1.0	2.0	mA
I_{DDO_PD}	Power Supply Current Power Down(2) for Outputs	All outputs off		0.05	0.1	mA
T_A	Ambient Temperature	Industrial grade	–40		85	°C

Note:

1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'
3. Output drive 5 inch trace.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal pull up resistance			120		KΩ
R_{dn}	Internal pull down resistance			120		KΩ
C_{XTAL}	Internal capacitance on X_IN and X_OUT pins			8		pF
L_{PIN}	Pin inductance				7	nH

Crystal Characteristic

Parameters	Description	Min.	Typ	Max.	Units
OSCmode	Mode of Oscillation	Fundamental			
FREQ	Frequency		25		MHz
ESR(1)	Equivalent Series Resistance			50	Ω
Cload	Load Capacitance		8		pF
Cshunt	Shunt Capacitance			7	pF
	Drive Level			200	uW

Note:

1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal bus voltage		2.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.8	V
		SMBus, V_{DDSMB} < 3.3V			0.8	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			500	kHz
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

Spread Spectrum Characteristic

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{MOD}	SS Modulation Frequency	Triangular modulation	30	31.8	33	kHz

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SS_SEL_TRI	0.4V_{DD}	0.5V_{DD}	0.6V_{DD}	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	–0.3		0.25 V_{DD}	V
I_{IH}	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$			5	µA
I_{IL}	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	–5			µA
I_{IH}	Input High Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = V_{DD}$			50	µA
I_{IL}	Input Low Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = 0V$	–50			µA
V_{OH}	Output High Voltage	REFOUT, except SMBus; I_{OH} = -2mA	0.8 x V_{DD_REFOUT}			V
V_{OL}	Output Low Voltage	REFOUT, except SMBus; I_{OL} = 2mA			0.2 x V_{DD_REFOUT}	V
R_{OUT}	CMOS Output impedance			20		Ω
C_{IN}	Input Capacitance		1.5		5	pF

LVCMOS AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{INPUT}	Input Frequency	XTAL_IN/CLK		25		MHz
t_{RIN}	Input rise time	Single-ended inputs			5	ns
t_{FIN}	Input fall time	Single-ended inputs			5	ns
t_{STAB}	Clock stabilization	From Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.75	1	ms

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{OELAT}	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion		20	300	us
t_{PERIOD}	REFOUT clock period	REFOUT, assume input is at 25MHz		40		ns
f_{ACC}	REFOUT frequency accuracy(1)	REFOUT, long term accuracy to input		0		ppm
t_{SLEW}	REFOUT slew rate(1)	Byte 3 = 1F, 20% to 80% of V_{D-DREF}	0.9	1.4	2	V/ns
		Byte 3 = 5F, 20% to 80% of V_{D-DREF}	1.5	2.4	3.2	V/ns
		Byte 3 = 9F, 20% to 80% of V_{D-DREF}	2	3	3.8	V/ns
		Byte 3 = DF, 20% to 80% of V_{D-DREF}	2.3	3.2	4	V/ns
t_{DC}	REFOUT Duty Cycle(1)	$V_T = V_{DD}$ /2 V, driven by a Xtal	45	50	55	%
t_{DCDIS}	REFOUT Duty Cycle Distortion	$V_T = V_{DD}$ /2 V, driven by an external source	–2	0	+2	%
t_{JITPH}	REFOUT Phase Jitter, RMS	12kHz to 5MHz, SSC off, driven by a Xtal		70	150	ps
		12kHz to 5MHz, SSC on, driven by a Xtal		0.16	0.3	ps
t_{JITPH}	REFOUT phase jitter	12kHz to 5MHz, RMS, driven by a Xtal		0.9	1.5	ps
t_{JITN}	Noise floor	1kHz offset, driven by a Xtal		–149	–135	dBc/Hz
		10kHz offset to Nyquist, driven by a Xtal		–158	–140	dBc/Hz

Note:

1. Guaranteed by design and characterization, not 100% tested in production

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High(1)	Statistical measurement on single-ended signal using oscilloscope math function	660	784	850	mV
V_{OL}	Output Voltage Low(1)		–150		150	mV
V_{OMAX}	Output Voltage Maximum(1)	Measurement on single ended signal using absolute value		816	1150	mV
V_{OMIN}	Output Voltage Minimum(1)		–300	–42		mV
V_{OC}	Output Cross Voltage(1,2,4)		250	430	550	mV
DV_{OC}	V_{OC} Magnitude Change(1,2,5)			12	140	mV

Note:

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency			100		MHz
t_{RF}	Slew rate(1,2,3)	Scope averaging on fast setting	2.5	3.2	4	V/ns
		Scope averaging on slow setting	2.2	3	3.7	V/ns
Dt_{RF}	Slew rate matching(1,2,4)	Scope averaging on		7	15	%
t_{DC}	Duty Cycle(1,2)	Measured differentially, PLL Mode	45	50	55	%
t_{SKEW}	Output Skew(1,2)	Averaging on, V_T = 50%		20	50	ps
tj_{c-c}	Cycle to cycle jitter(1,2)			20	50	ps

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within ±150mV window.
4. It is measured using a ±75mV window centered on the average cross point.

PCIe Common Clock (CC) Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Integrated phase jitter (RMS)	PCIe 1.0		20	30	86	ps (pkpk)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0.1	0.2	3	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz); (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0.4	0.5	3.1	ps
		PCIe 3.0 (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)		0.15	0.2	1	ps
		PCIe 4.0 (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)		0.15	0.2	0.5	ps
		PCIe 5.0		0.05	0.06	0.15	ps
		PCIe 6.0		0.03	0.04	0.1	ps

PCIe Independent Reference Clock Architecture Jitter

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Integrated phase jitter (RMS)	PCIe 3.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)		0.15	0.25		ps
		PCIe 4.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR = 10MHz)		0.15	0.25		ps
		PCIe 5.0 SRIS		0.04	0.07		ps
		PCIe 6.0 SRIS		0.03	0.05		ps

Differential Output Clock Periods - Spread Spectrum Disabled

Center Freq. MHz	Measurement Window							Units
	1 clock	1 µs	0.1 s	0.1 s	0.1 s	1 µs	1 clock	
	-c2c jitter AbsPer Min	-SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns

Differential Output Clock Periods - Spread Spectrum Enabled

Center Freq. MHz	Measurement Window							Units
	1 clock	1 µs	0.1 s	0.1 s	0.1 s	1 µs	1 clock	
	-c2c jitter AbsPer Min	-SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

Note:

1. Guaranteed by design and characterization—not 100% tested in production.
2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25MHz.

SMBus Serial Data Interface

PI6CG33601C is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	SADR	0	1/0

Note: SMBus address is latched on SADR pin

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q5_OE	Q5 output enable	RW	1	See B11[1:0]	Pin Control
6	Q4_OE	Q4 output enable	RW	1		Pin Control
5	Reserved			0		
4	Q3_OE	Q3 output enable	RW	1		Pin Control
3	Q2_OE	Q2 output enable	RW	1		Pin Control
2	Q1_OE	Q1 output enable	RW	1		Pin Control
1	Reserved			0		
0	Q0_OE	Q0 output enable	RW	1		Pin Control

Note:

1. A low on these bits will override the OE# pins and force the differential outputs to the state indicated by B11[1:0] (Low/ Low default)

Byte 1: SS Spread Spectrum and Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SSENRB1	SS Enable Readback Bit1	R	Latch	'00' for SS_SEL_TRI = '0', '10' for SS_SEL_TRI = 'M' '11' for SS_SEL_TRI = '1'	
6	SSENRB0	SS Enable Readback Bit0	R	Latch		
5	SSEN_SWCTR	Enable SW control of SS	RW	0	Values in B1[7:6] control SS amount	Values in B1[4:3] control SS amount
4	SSENSW1	SS enable SW control Bit1	RW[1]	0	'00' = SS off, '01' = -0.25% SS, '10' = SS off, '11' = -0.5% SS	
3	SSENSW0	SS enable SW control Bit0	RW[1]	0		
2	Reserved			1		
1	Amplitude1	Control output amplitude	RW	1	'00' = 0.6V, '01' = 0.68V, '10' = 0.75V, '11' = 0.85V	
0	Amplitude0		RW	0		

Note:

1. Spread must be selected OFF or ON with the hardware latch pin. These bits should not be used to turn spread ON or OFF after power up. These bits can be used to change the spread amount, and B1[5] must be set to a 1 for these bits to have any effect on the part. If These bits are used to turn spread OFF or ON, the system will need to be reset.

Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SLEWRATECTR_Q5	Control slew rate of Q5	RW	1	Slow setting	Fast setting
6	SLEWRATECTR_Q4	Control slew rate of Q4	RW	1	Slow setting	Fast setting
5	Reserved			1		
4	SLEWRATECTR_Q3	Control slew rate of Q3	RW	1	Slow setting	Fast setting
3	SLEWRATECTR_Q2	Control slew rate of Q2	RW	1	Slow setting	Fast setting
2	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
1	Reserved			1		
0	SLEWRATECTR_Q0	Control slew rate of Q0	RW	1	Slow setting	Fast setting

Byte 3: REF Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	REFSLEWRATE	Slew rate control for REF	RW	0	'00' = 1.4V/ns '01' = 2.4V/ns, '10' = 3V/ns, '11' = 3.2V/ns	
6			RW	1		
5	REF_PDSTATE	Wake-on-Lan enable for REF	RW	0	REF = Disabled in PD state[1]	REF = running in PD state
4	REF_OE	Output enable for REF	RW	1	REF = Disabled[1]	REF = running
3	Reserved			1		
2	Reserved			1		
1	Reserved			1		
0	Reserved			1		

Note:

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'=HiZ, '10'=Low, '11'=High

Byte 4: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved			0x40		

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	Rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID2		R	0		
1	PVID1		R	1		
0	PVID0		R	1		

Byte 6: Device Type/Device ID Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB, '10' = Reserved, '11' = NZDB	
6	DTYPE0		R	0		
5	DID5	Device ID	R	0	000110 binary, 06Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	1		
1	DID1		R	1		
0	DID0		R	0		

Byte 7: Byte Count Register						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Byte 8 and 9: Reserved						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7:0	Reserved			B8: 0x36 B90x00		

Byte 10: PD Restore						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	Reserved			0		
6	PD Restore	PD Restore to default configuration	RW	1	Clear PD Config	Keep PD Config
5:0	Reserved			0		

Byte 11: Stop Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:2	Reserved			0		
1	STP1	True/ Compliment DIF Output Disable Sate	RW	0	00 = Low/Low	10 = High/ Low
0	STP0		RW	0	01 = HiZ/HiZ	11 = Low/ High

Byte 12: Impedance Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q2_Zout1	Q2 Zout	RW	10	00 = Reserved 01 = 85Ω 10 = 100Ω 11 = Reserved	
6	Q2_Zout0	Q2 Zout	RW			
5	Q1_Zout1	Q1 Zout	RW			
4	Q1_Zout0	Q1 Zout	RW			
3	Reserved					
2	Reserved					
1	Q0_Zout1	Q0 Zout	RW			
0	Q0_Zout0	Q0 Zout	RW			

Byte 13: Impedance Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q5_Zout1	Q5 Zout	RW	10	00 = Reserved 01 = 85Ω 10 = 100Ω 11 = Reserved	
6	Q5_Zout0	Q5 Zout	RW			
5	Q4_Zout1	Q4 Zout	RW			
4	Q4_Zout0	Q4 Zout	RW			
3	Reserved					
2	Reserved					
1	Q3_Zout1	Q3 Zout	RW			
0	Q3_Zout0	Q3 Zout	RW			

Byte 14: OE Termination Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	OE2_term1	OE2 Pull up or down	RW	0	00 = None	10 = Pullup
6	OE2_term0	OE2 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down
5	OE1_term1	OE1 Pull up or down	RW	0	00 = None	10 = Pullup
4	OE1_term0	OE1 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down
3	Reserved			0		
2	Reserved			1		
1	OE0_term1	OE0 Pull up or down	RW	0	00 = None	10 = Pullup
0	OE0_term0	OE0 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down

Byte 15: OE Termination Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	OE5_term1	OE5 Pull up or down	RW	0	00 = None	10 = Pullup
6	OE5_term0	OE5 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down
5	OE4_term1	OE4 Pull up or down	RW	0	00 = None	10 = Pullup
4	OE4_term0	OE4 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down
3	Reserved			0		
2	Reserved			1		
1	OE3_term1	OE3 Pull up or down	RW	0	00 = None	10 = Pullup
0	OE3_term0	OE3 Pull up or down	RW	1	01 = Pull-down	11 = Pullup and Down

Byte 16: Power Good Termination Control

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:2	Reserved			0x00		
1	PWRGD_PD1	Clock Power Good and Power Down Pull up or Pull down	RW	1	00 = None	10 = Pullup
0	PWRGD_PD0		RW	0	01 = Pull-down	11 = Pullup and Down

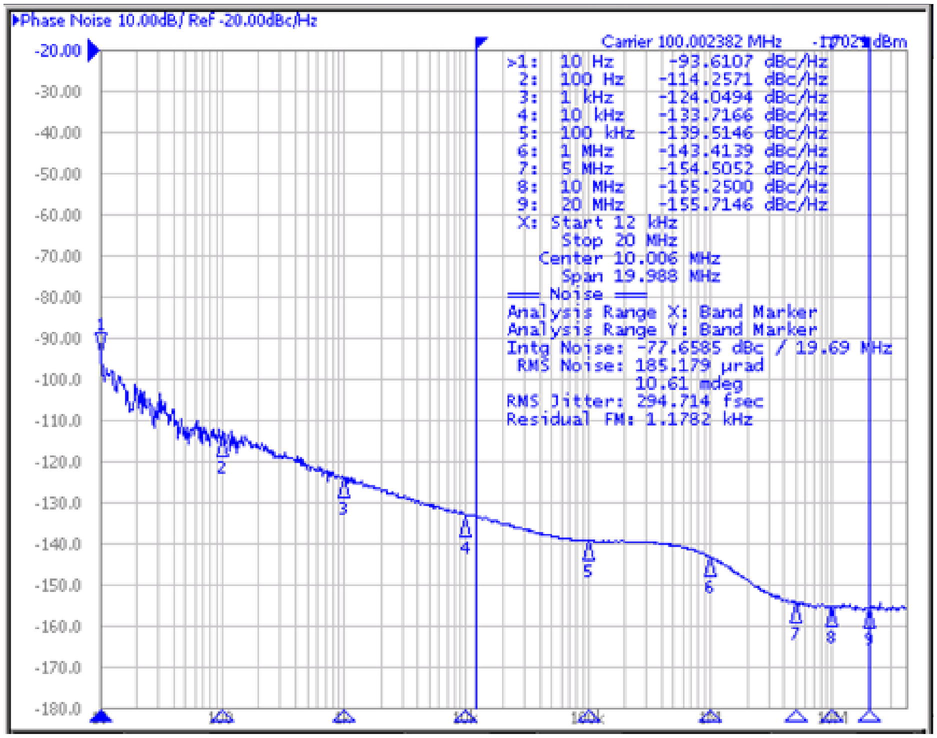
Byte 17: Reserved

Byte 18: Enable Pin Control						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7	OE5_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High
6	OE4_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High
5	Reserved			0		
4	OE3_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High
3	OE2_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High
2	OE1_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High
1	Reserved			0		
0	OE0_Enable	Sets Enable High or Low	RW	0	Enable = Low	Enable = High

Byte 19: Power Down Pin Control						
Bit	**Control Function**	**Description**	**Type**	**Power Up Condition**	**0**	**1**
7:1	Reserved			0		
0	PWRGD_PD	PWRGD_PD Active via Pull up or Pull down	RW	0	Power Down = Low	Power Down = High

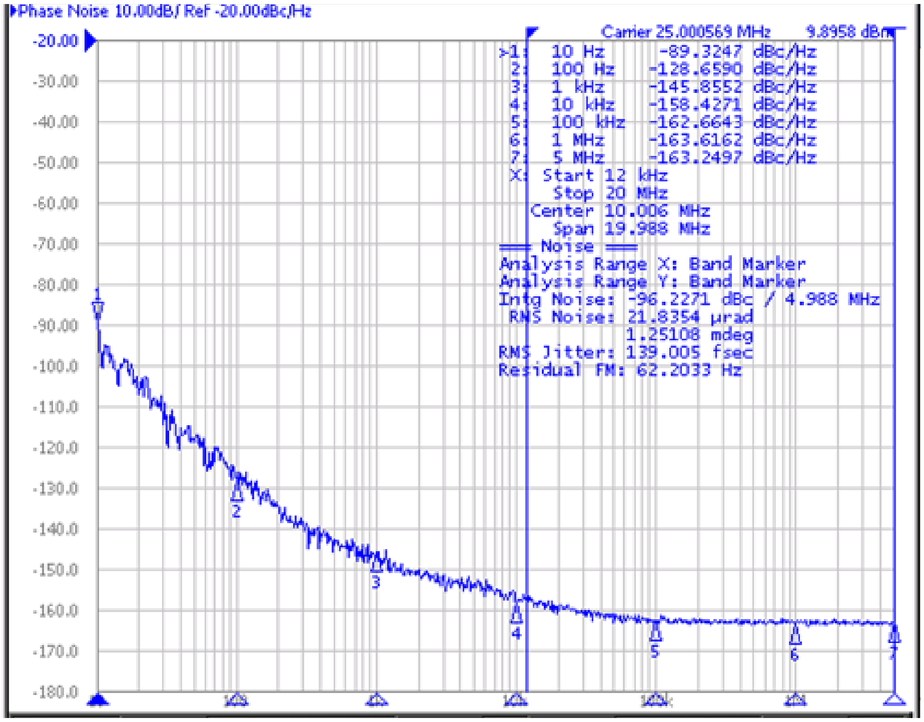
Plots

100MHz HCSL Clock (12k to 20MHz)



```
Phase Noise 10.00dB/ Ref -20.00dBc/Hz
                         Carrier 100.002382 MHz   -1.702[illegible] dBm
>1:  10 Hz     -93.6107 dBc/Hz
 2:  100 Hz   -114.2571 dBc/Hz
 3:  1 kHz    -124.0494 dBc/Hz
 4:  10 kHz   -133.7166 dBc/Hz
 5:  100 kHz  -139.5146 dBc/Hz
 6:  1 MHz    -143.4139 dBc/Hz
 7:  5 MHz    -154.5052 dBc/Hz
 8:  10 MHz   -155.2500 dBc/Hz
 9:  20 MHz   -155.7146 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -77.6585 dBc / 19.69 MHz
 RMS Noise: 185.179 µrad
            10.61 mdeg
RMS Jitter: 294.714 fsec
Residual FM: 1.1782 kHz
```

25MHz CMOS Clock



```
Phase Noise 10.00dB/ Ref -20.00dBc/Hz
                         Carrier 25.000569 MHz   9.8958 dBm
>1:  10 Hz     -89.3247 dBc/Hz
 2:  100 Hz   -128.6590 dBc/Hz
 3:  1 kHz    -145.8552 dBc/Hz
 4:  10 kHz   -158.4271 dBc/Hz
 5:  100 kHz  -162.6643 dBc/Hz
 6:  1 MHz    -163.6162 dBc/Hz
 7:  5 MHz    -163.2497 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -96.2271 dBc / 4.988 MHz
 RMS Noise: 21.8354 µrad
            1.25108 mdeg
RMS Jitter: 139.005 fsec
Residual FM: 62.2033 Hz
```

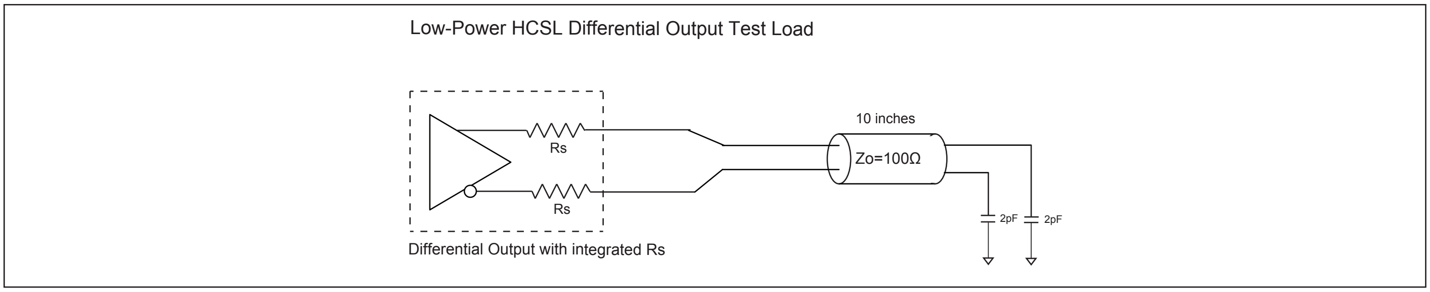


Figure 1. Low Power HCSL Test Circuit

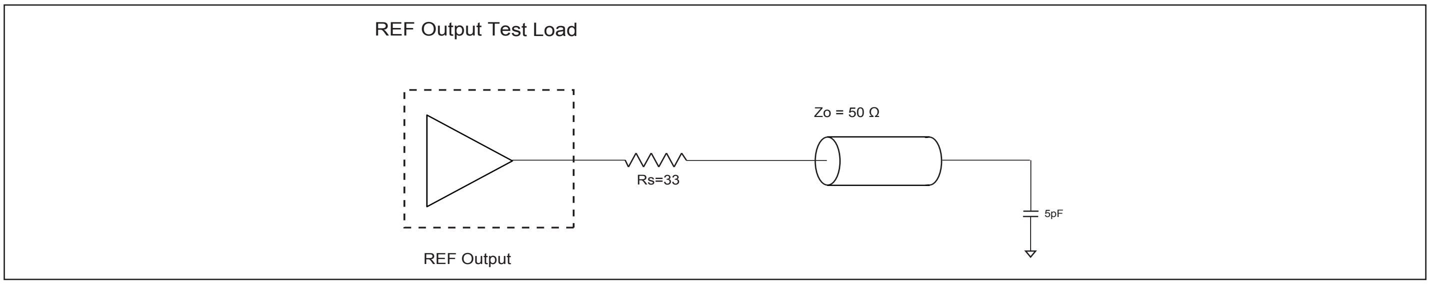


Figure 2. CMOS REF Test Circuit

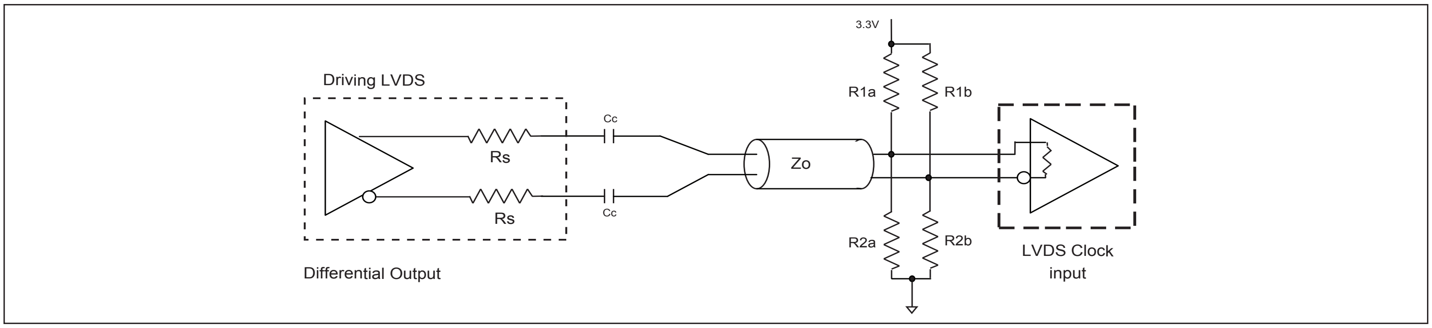


Figure 3. Differential Output driving LVDS

Table 3. Alternate Differential Output Terminations

Component	Receiver with Termination	Receiver without Termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5,600	75	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

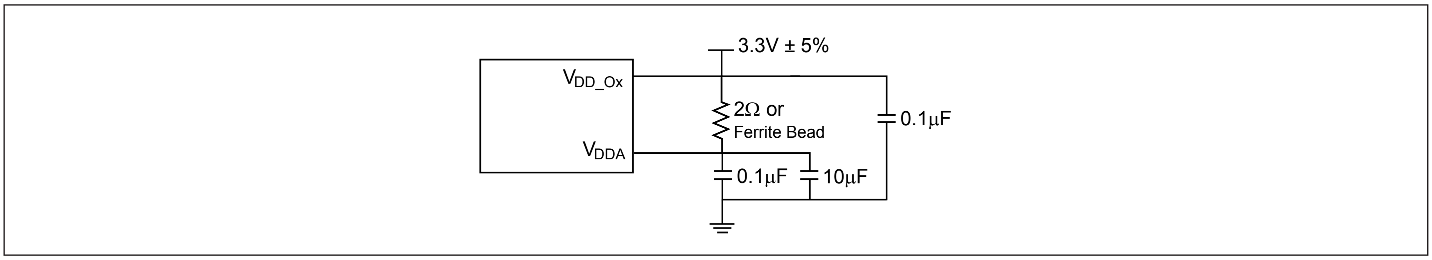
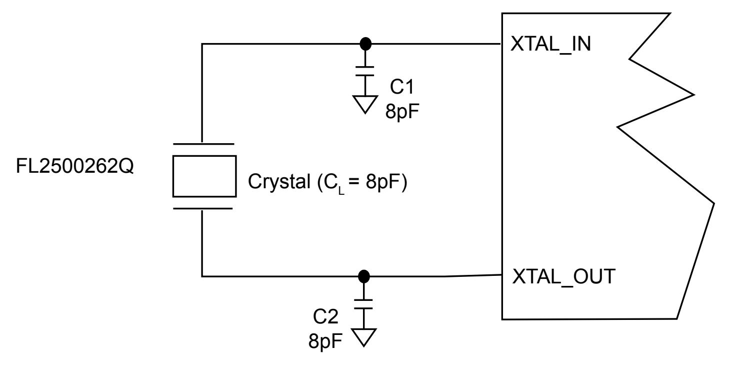


Figure 4. Power Supply Filter

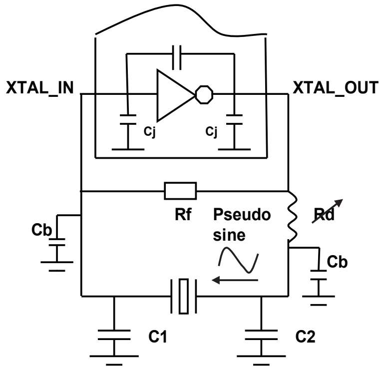
Crystal Circuit Connection

The following diagram shows PI6CG33601C crystal circuit connection with a parallel crystal. For the CL = 8pF crystal, it is suggested to use C1 = 8pF, C2 = 8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit



Crystal Capacitor Calculation



CL= crystal spec. loading cap.

Cj = chip in/output cap. (3~5pF)

Cb = PCB trace/via cap. (2~4pF)

C1, C2 = load cap. components

Rd = drive level res. (100Ω)

Final choose/trim C1=C2=2 *CL - (Cb +Cj) for the target +/-ppm
Example: C1=C2=2*(18pF) – (4pF+5pF)=27pF

Recommended Crystal Specification

Diodes Recommends:

a) FL2500217, SMD 3.2x2.5(4P), 25MHz, CL=8pF, +/-20ppm, https://www.diodes.com/assets/Datasheets/FL.pdf
b) FH2500016, SMD 2.5x2.0(4P), 25MHz, CL=8pF, +/-30ppm, https://www.diodes.com/assets/Datasheets/FH.pdf
c) FW2500031, SMD 2.0x1.6(4P), 25MHz, CL=8pF, +/-30ppm, https://www.diodes.com/assets/Datasheets/FW.pdf
d) US2500003, SMD 1.6x1.2(4P), 25MHz, CL=12pF, +/-30ppm, https://www.diodes.com/assets/Datasheets/US.pdf

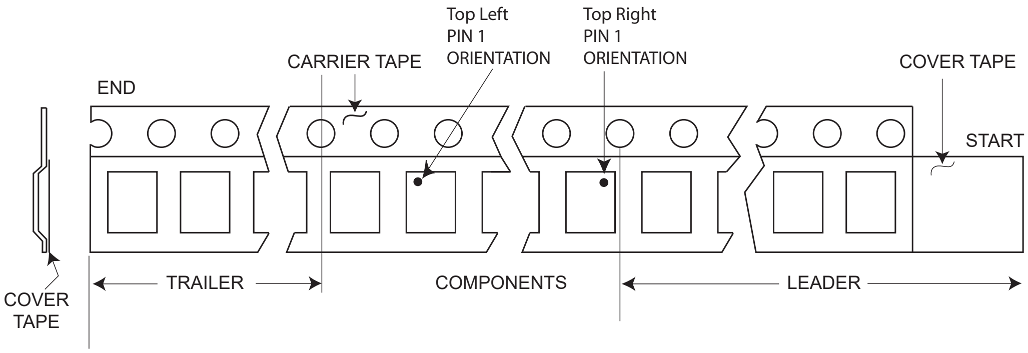
Table 4. Thermal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
θ_{JA}	Thermal Resistance Junction to Ambient	Still air			29.91	°C/W
θ_{JC}	Thermal Resistance Junction to Case				15.92	°C/W

Part Marking

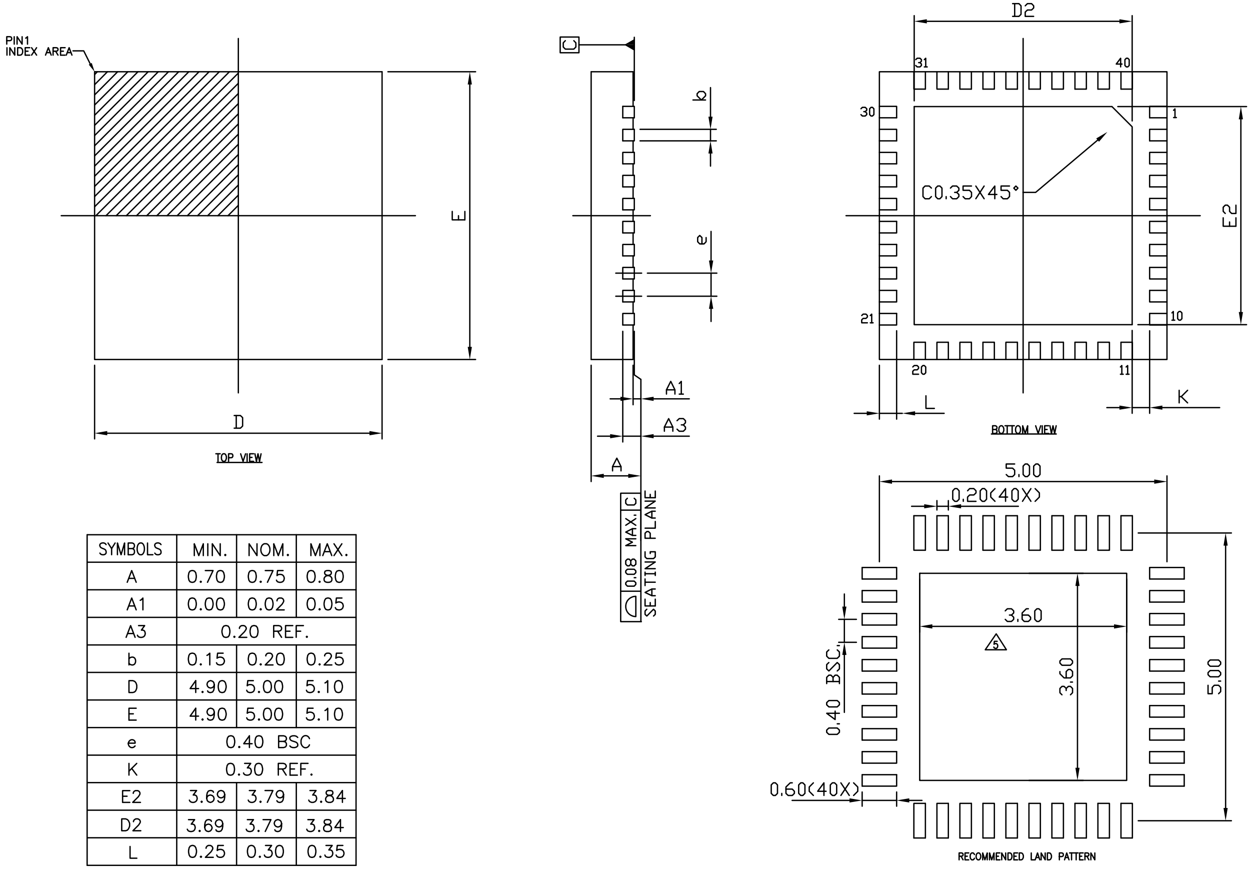
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Package Information



Packaging Mechanical

40-TQFN (ZLA)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.40 BSC		
K	0.30 REF.		
E2	3.69	3.79	3.84
D2	3.69	3.79	3.84
L	0.25	0.30	0.35

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED).

Enabling Serial Connectivity

DATE: 03/14/15

DESCRIPTION: 40-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZLA (ZLA40)

DOCUMENT CONTROL #: PD-2195 **REVISION: --**

15-0019

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Pin 1 Location
PI6CG33601CZLAIEX	ZLA	40-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Right Corner
PI6CG33601CZLAIEX-13R	ZLA	40-Contact, Very Thin Quad Flat No-Lead (TQFN)	Top Left Corner

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel
6. For packaging details, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

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