

## Features

- Non-volatile Flash Memory
- Fast Read access Time = 120 ns.
- Flash Electrical Chip-Erase
  - 3 Second Typical Chip-Erase
- Quick Programming Algorithm
  - 10  $\mu$ s Typical Byte-Program
  - 12.5 Second Chip-Program
- 12.0 V  $\pm$ 5% VPP chip erase
- 100,000 Erase/Program Cycles
- 10 year data retention
- CMOS Low Power Consumption
  - 10 mA Typical Active Current
  - 50  $\mu$ A Typical Standby Current
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Great Noise Immunity Features
  - $\pm$ 10% VCC Tolerance
- -40°C to +85°C operation – Industrial
- Safely abort Erase or Program sequence at any time including Integrated Program/Erase Stop Timer
- Protection against inadvertent programming during power up.
- JEDEC-Standard Pinouts
  - 32-Pin Plastic Dip
  - 32-Lead PLCC
  - 32-Lead TSOP

## General Description

The Tekmos TK28F020 is a high speed 2M CMOS non-volatile flash memory arranged as 256K x 8. (262,144 x 8 bits) It is electrically erasable and reprogrammable. It is well suited for use in applications where codes are changed after the initial programming, during manufacture, final test or after sale. Memory contents can be changed in a test fixture, in a PROM programmer, or in system.

The TK28F020 is manufactured to allow for low power consumption and immunity to noise. The device is designed to withstand 100,000 program/erase cycles without losing data integrity. Data retention is at least 10 years.

Standby current maximum is 100  $\mu$ A providing significant power saving when the device is deselected. Access time of 120 ns provides zero wait state performance compatible with many microcontrollers and microprocessors. Electrical erasure of the entire memory is typically achieved in less than 5 seconds. 12 volt programming and erase voltage makes it compatible with similar devices.

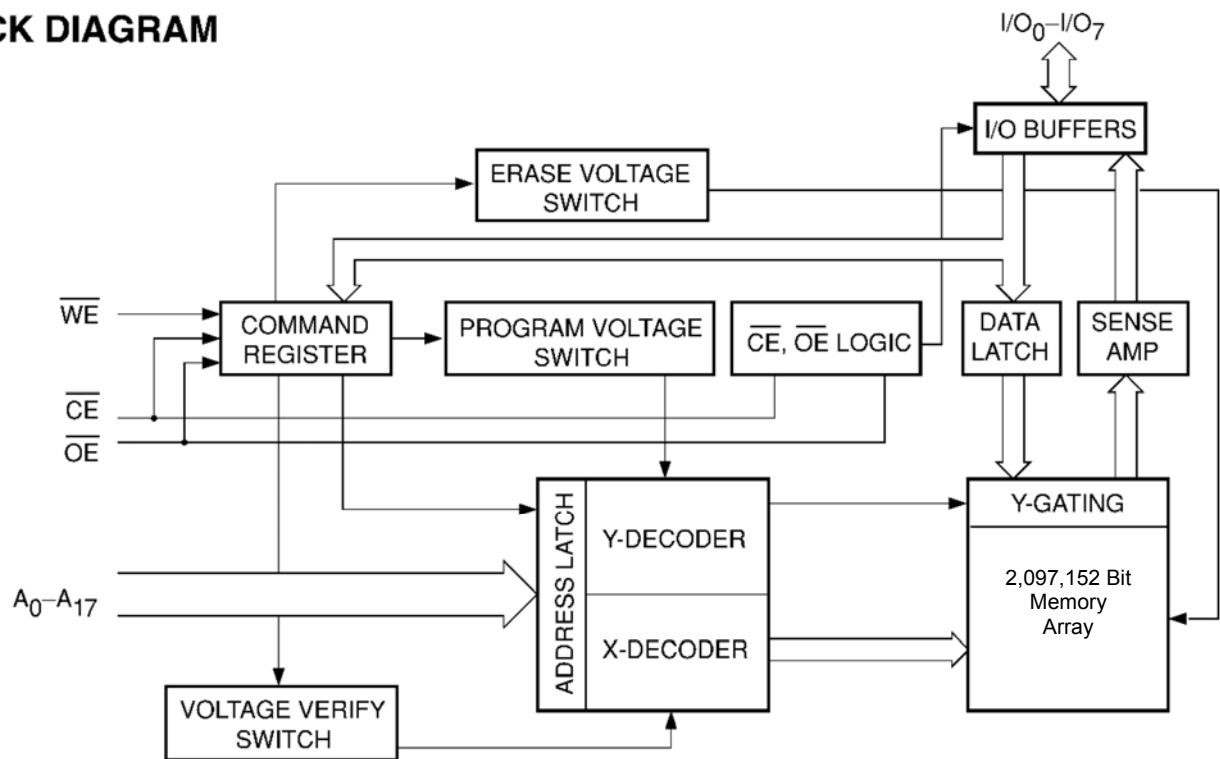
The erase procedure has a two-step process that ensures against accidental erasure of the contents of the memory. The erase command is actually written twice before it is executed. An integrated stop feature allows for automatic timing control eliminating the need for a maximum erase timing specification.

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. The abort/reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

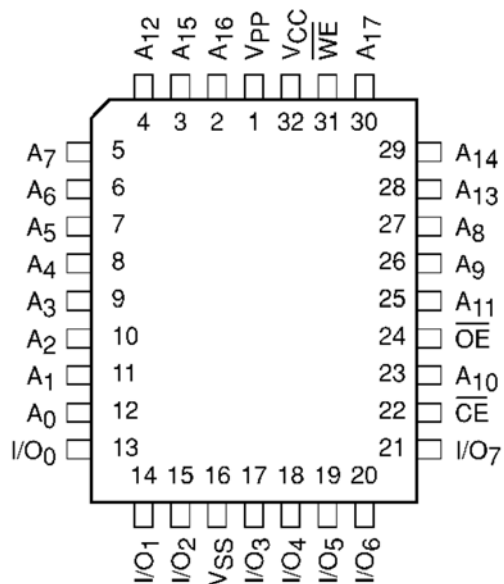
Protection against inadvertent programming during power up is provided. VPP and VCC may be powered up in any order, no sequencing is required.

The TK28F020 is offered in 32-Pin Plastic DIP, 32-Lead PLCC and 32-Lead TSOP packages. Conforming to JEDEC standards, it is pin for pin compatible with standard EPROM and EEPROM devices. The TK28F020 is often used as a drop in replacement in systems originally designed for other manufacturer's 28F020 devices.

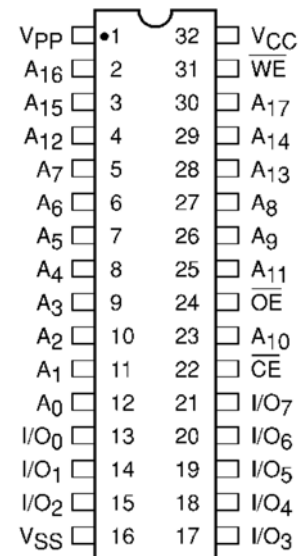
## BLOCK DIAGRAM



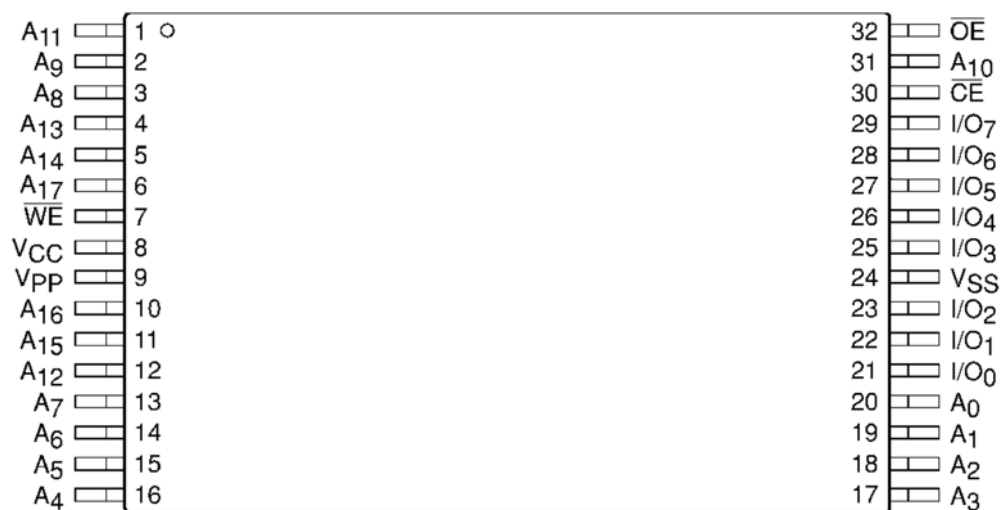
## Pin Configurations



PLCC Package



PDIP Package



TSOP

## Pin Functions

DIP/ PCC Pin #	TSOP Pin #	Pin Name	Type	Function	DIP/ PCC Pin #	TSOP Pin #	Pin Name	Type	Function
1	9	V <sub>PP</sub>	Input	Program Erase Voltage Supply	17	25	I/O 3	Input	Data Input/ Output
2	10	A <sub>16</sub>	Input	Address memory	18	26	I/O 4	Input	Data Input/ Output
3	11	A <sub>15</sub>	Input	Address memory	19	27	I/O 5	Input	Data Input/ Output
4	12	A <sub>12</sub>	Input	Address memory	20	28	I/O 6	Input	Data Input/ Output
5	13	A <sub>7</sub>	Input	Address memory	21	29	I/O 7	Input	Data Input/ Output
6	14	A <sub>6</sub>	Input	Address memory	22	30	CE	Input	Chip Enable
7	15	A <sub>5</sub>	Input	Address memory	23	31	A <sub>10</sub>	Input	Address memory
8	16	A <sub>4</sub>	Input	Address memory	24	32	OE	Input	Output Enable
9	17	A <sub>3</sub>	Input	Address memory	25	1	A <sub>11</sub>	Input	Address memory
10	18	A <sub>2</sub>	Input	Address memory	26	2	A <sub>9</sub>	Input	Address memory
11	19	A <sub>1</sub>	Input	Address memory	27	3	A <sub>8</sub>	Input	Address memory
12	20	A <sub>0</sub>	Input	Address memory	28	4	A <sub>13</sub>	Input	Address memory
13	21	I/O 0	I/O	Data Input/ Output	29	5	A <sub>14</sub>	Input	Data Input/ Output
14	22	I/O 1	I/O	Data Input/ Output	30	6	A <sub>17</sub>	Input	Address Memory
15	23	I/O 2	I/O	Data Input/ Output	31	7	WE	Input	Data Input/ Output
16	24	V <sub>SS</sub>	Supply	Ground	32	8	V <sub>CC</sub>	Supply	Voltage Supply

## Absolute Maximum Ratings\*

Temperature Under Bias	-50°C to +95°C
Storage Temperature	-55°C to 150°C
Voltage on Any Pin with Respect to Ground <sup>(1)</sup>	-2.0V to $V_{CC} + 2.0V$
Voltage on Pin A <sub>9</sub> with Respect to Ground <sup>(1)</sup>	-2.0V to +13.5V
V <sub>PP</sub> with Respect to Ground during Program/Erase <sup>(1)</sup>	-2.0V to +14.0V
Package Power Dissipation Capability ( $T_A = 25^\circ\text{C}$ )	1.0 W
Lead Soldering Temperature (10 seconds)	300°C
Output Short Circuit Current <sup>(2)</sup>	100 mA

## Reliability Characteristics

Symbol	Parameter	Min	Max	Units	Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)(5)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

### CAPACITANCE $T_A = 25^\circ\text{C}$ , $f = 1.0\text{ MHz}$

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C <sub>IN</sub> <sup>(3)</sup>	Input Pin Capacitance		6	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub> <sup>(3)</sup>	Output Pin Capacitance		10	pF	V <sub>OUT</sub> = 0V
C <sub>VPP</sub> <sup>(3)</sup>	V <sub>PP</sub> Supply Capacitance		25	pF	V <sub>PP</sub> = 0V

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

#### Other Notes:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is  $V_{CC} + 0.5V$ , which may overshoot to  $V_{CC} + 2.0V$  for periods of less than 20ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to  $V_{CC} + 1V$ .
- (5) Pins A<sub>9</sub> and V<sub>pp</sub> are tested to the

## D.C. Operating Characteristics

( $V_{CC} = +5V \pm 10\%$ , unless otherwise specified)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
$I_{LI}$	Input Leakage Current		$\pm 1$	$\mu A$	$V_{IN} = V_{CC}$ or $V_{SS}$ $V_{CC} = 5.5V$ , $OE = V_{IH}$
$I_{LO}$	Output Leakage Current		$\pm 1$	$\mu A$	$V_{OUT} = V_{CC}$ or $V_{SS}$ , $V_{CC} = 5.5V$ , $OE = V_{IH}$
$I_{SB1}$	$V_{CC}$ Standby Current CMOS		100	$\mu A$	$CE = V_{CC} \pm 0.5V$ , $V_{CC} = 5.5V$
$I_{SB2}$	$V_{CC}$ Standby Current TTL		1	mA	$\overline{CE} = V_{IH}$ , $V_{CC} = 5.5V$
$I_{CC1}$	$V_{CC}$ Active Read Current		30	mA	$V_{CC} = 5.5V$ , $\overline{CE} = V_{IL}$ , $I_{OUT} = 0mA$ , $f = 6 MHz$
$I_{CC2}^{(1)}$	$V_{CC}$ Programming Current		15	mA	$V_{CC} = 5.5V$ , Programming in Progress
$I_{CC3}$	$V_{CC}$ Erase Current		15	mA	$V_{CC} = 5.5V$ , Erase in Progress
$I_{CC4}$	$V_{CC}$ Prog./Erase Verify Current		15	mA	$V_{CC} = 5.5V$ , Program or Erase Verify in Progress
$I_{PPS}$	$V_{PP}$ Standby Current		$\pm 10$	$\mu A$	$V_{PP} = V_{PPL}$
$I_{PP1}$	$V_{PP}$ Read Current		200	$\mu A$	$V_{PP} = V_{PPH}$
$I_{PP2}^{(1)}$	$V_{PP}$ Programming Current		30	mA	$V_{PP} = V_{PPH}$ , Programming in Progress
$I_{PP3}^{(1)}$	$V_{PP}$ Erase Current		30	mA	$V_{PP} = V_{PPH}$ , Erase in Progress
$I_{PP4}^{(1)}$	$V_{PP}$ Prog./Erase Verify Current		5	mA	$V_{PP} = V_{PPH}$ , Program or Erase Verify in Progress
$V_{IL}$	Input Low Level TTL	-0.5	0.8	V	
$V_{ILC}$	Input Low Level CMOS	-0.5	0.8	V	
$V_{OL}$	Output Low Level		0.45	V	$I_{OL} = 5.8mA$ , $V_{CC} = 4.5V$
$V_{IH}$	Input High Level TTL	2	$V_{CC} + 0.5$	V	
$V_{IHC}$	Input High Level CMOS	$V_{CC} \cdot 0.7$	$V_{CC} + 0.5$	V	
$V_{OH1}$	Output High Level TTL	2.4		V	$I_{OH} = -2.5mA$ , $V_{CC} = 4.5V$
$V_{OH2}$	Output High Level CMOS	$V_{CC} - 0.4$		V	$I_{OH} = -400\mu A$ , $V_{CC} = 4.5V$
$V_{ID}$	A9 Signature Voltage	11.4	13	V	$A_9 = V_{ID}$
$I_{ID}^{(1)}$	A9 Signature Current		200	$\mu A$	
$V_{LO}$	$V_{CC}$ Erase/Prog. Lockout Voltage	2.5		V	

Note: (1) This parameter is tested initially and after a design or process change that affects the parameter.

## SUPPLY CHARACTERISTICS

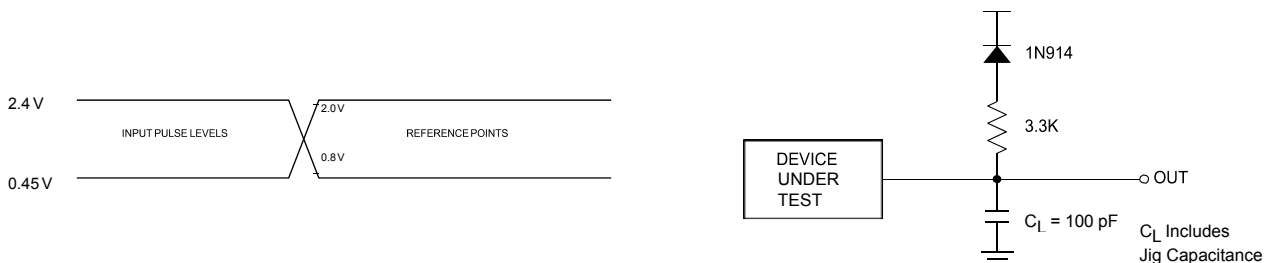
Symbol	Parameter	Limits		Unit
		Min	Max.	
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage	4.5	5.5	V
V <sub>PPL</sub>	V <sub>PP</sub> During Read Operations	0	V <sub>CC</sub> +0.5	V
V <sub>PPH</sub>	V <sub>PP</sub> During Read/Erase/Program	11.4	12.6	V

### A.C. CHARACTERISTICS, Read Operation

V<sub>CC</sub> = +5V ±10%, unless otherwise specified. Temperature -40°C to +85°C, unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	Min	Max	Unit
t <sub>AVAV</sub>	t <sub>RC</sub>	Read Cycle Time	120		ns
t <sub>ELQV</sub>	t <sub>CE</sub>	$\overline{CE}$ Access Time		120	ns
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Access Time		120	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	$\overline{OE}$ Access Time		50	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Output Hold from Address $\overline{OE}/\overline{CE}$ Change	0		ns
t <sub>GLQX</sub>	t <sub>OLZ</sub> <sup>(1)(6)</sup>	$\overline{OE}$ to Output in Low-Z	0		ns
t <sub>ELZX</sub>	t <sub>LZ</sub> <sup>(1)(6)</sup>	$\overline{CE}$ to Output in Low-Z	0		ns
t <sub>GHQZ</sub>	t <sub>DF</sub> <sup>(1)(2)</sup>	$\overline{OE}$ High to Output High-Z		20	ns
t <sub>EHQZ</sub>	t <sub>DF</sub> <sup>(1)(2)</sup>	$\overline{CE}$ High to Output High-Z		30	ns
t <sub>WHGL</sub> <sup>(1)</sup>		Write Recovery Time Before Read	6		μs

**Figure 1. A.C. Testing Input / Output Waveforms (3)(4)(5)**



<sup>51</sup>This parameter is tested initially and after a design or process change that affects the parameter.

(1) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.

(2) Input Rise and Fall Times (10% to 90%) < 10 ns.

- (3) Input Pulse Levels = 0.45V and 2.4V. For High Speed Input Pulse Levels 0.0V and 3.0V.  
 (4) Input and Output Timing Reference = 0.8V and 2.0V. For High Speed Input and Output Timing Reference = 1.5V.  
 (5) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.  
 (6) For load and reference points, see Fig. 1

### A.C. CHARACTERISTICS, Program/Erase Operation

$V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

JEDEC Symbol	Standard Symbol	Parameter	Min	Typ	Max	Unit
$t_{AVAV}$	$t_{WC}$	Write Cycle Time	120			ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0			ns
$t_{WLAX}$	$t_{AH}$	Address Hold Time	40			ns
$t_{DVWH}$	$t_{DS}$	Data Setup Time	40			ns
$t_{WHDX}$	$t_{DH}$	Data Hold Time	10			ns
$t_{ELWL}$	$t_{CS}$	$\overline{CE}$ Setup Time	0			ns
$t_{WHEH}$	$t_{CH}$	$\overline{CE}$ Hold Time	0			ns
$t_{WLWH}$	$t_{WP}$	$\overline{WE}$ Pulse Width	40			ns
$t_{WHWL}$	$t_{WPH}$	$\overline{WE}$ High Pulse Width	20			ns
$t_{WHWH1}^{(2)}$	-	Program Pulse Width	10			$\mu s$
$t_{WHWH}^{(2)}$	-	Erase Pulse Width	9.5			ms
$t_{WHGL}$	-	Write Recovery Time Before	6			$\mu s$
$t_{GHWL}$	-	Read Recovery Time Before	0			$\mu s$
$t_{VPEL}$	-	$V_{PP}$ Setup Time to $\overline{CE}$	100			ns

### Erase and Programming Performance <sup>(1)</sup>

Parameter	Min	Typ	Max	Unit
Chip Erase Time (3)		3	10	Sec
Chip Program Time (3)(4)		2	12.5	Sec

Note:

- (1) Please refer to Supply characteristics for the value of  $V_{PPH}$  and  $V_{PPL}$ . The  $V_{PP}$  supply can be either hardwired or switched. If  $V_{PP}$  is switched,  $V_{PPL}$  can be ground, less than  $V_{CC} + 2.0V$  or a no connect with a resistor tied to ground.  
 (2) Program and Erase operations are controlled by internal stop timers.  
 (3) 'Typicals' are not guaranteed, but based on characterization data. Data taken at 25°C, 12.0V  $V_{PP}$ .  
 (4) Minimum byte programming time (excluding system overhead) is 16  $\mu s$  (10  $\mu s$  program + 6  $\mu s$  write recovery), while maximum is 400  $\mu s$ / byte (16  $\mu s$  x 25 loops). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.

## Function Table <sup>(1)</sup>

Mode	Pins					Notes
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$V_{\text{PP}}$	I/O	
Read	$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{PPL}}$	D <sub>OUT</sub>	
Output Disable	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IH}}$	X	High-Z	
Standby	$V_{\text{IH}}$	X	X	$V_{\text{PPL}}$	High-Z	
Signature (MFG)	$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	X	31H	$A_0 = V_{\text{IL}}, A_9 = 12\text{V}$
Signature (Device)	$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	X	B4H	$A_0 = V_{\text{IH}}, A_9 = 12\text{V}$
Program/Erase	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IL}}$	$V_{\text{PPH}}$	D <sub>IN</sub>	See Command Table
Write Cycle	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IL}}$	$V_{\text{PPH}}$	D <sub>IN</sub>	During Write Cycle
Read Cycle	$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{PPH}}$	D <sub>OUT</sub>	During Write Cycle

## Write Command Table

Commands are written into the command register in one or two write cycles. The command register can be altered only when  $V_{\text{PP}}$  is high and the instruction byte is latched on the rising edge of  $\overline{\text{WE}}$ . Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	Pins						
	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D <sub>IN</sub>	Operation	Address	D <sub>IN</sub>	D <sub>OUT</sub>
Set Read	Write	X	00H	Read	A <sub>IN</sub>		D <sub>OUT</sub>
Read Sig. (MFG)	Write	X	90H	Read	00		31H
Read Sig. (Device)	Write	X	90H	Read	01		B4H
Erase	Write	X	20H	Write	X	20H	
Erase Verify	Write	A <sub>IN</sub>	A0H	Read	X		D <sub>OUT</sub>
Program	Write	X	40H	Write	A <sub>IN</sub>	D <sub>IN</sub>	
Program Verify	Write	X	C0H	Read	X		D <sub>OUT</sub>
Reset	Write	X	FFH	Write	X	FFH	

Note:

(1) Logic Levels: X = Logic 'Do not care' ( $V_{\text{IH}}$ ,  $V_{\text{IL}}$ ,  $V_{\text{PPL}}$ ,  $V_{\text{PPH}}$ )



## WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

### Read Mode

The device can be put into a standard READ mode by initiating a write cycle with 00H on the data bus. The subsequent read cycles will be performed similar to a standard EPROM or EEPROM Read.

### Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register while keeping  $V_{PP}$  high. A read cycle from address 0000H with  $\overline{CE}$  and  $\overline{OE}$  low (and  $\overline{WE}$  high) will output the device signature.

Tekmos Code = 0011 0100 (34H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O<sub>0</sub> to I/O<sub>7</sub>.

28F020 Code = 1011 0100 (B4H)

**Figure 4. A.C. Timing for Erase Operation**

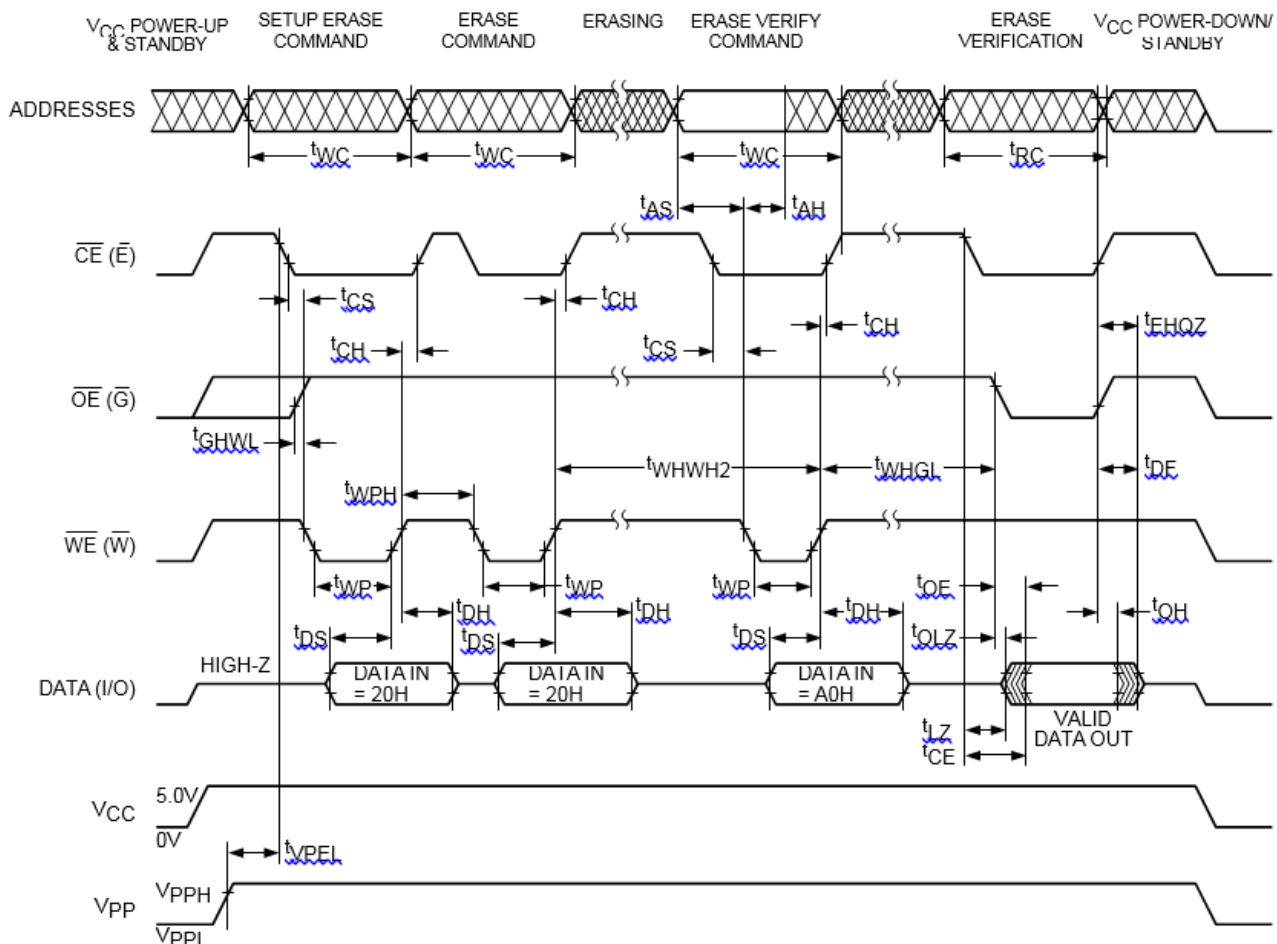
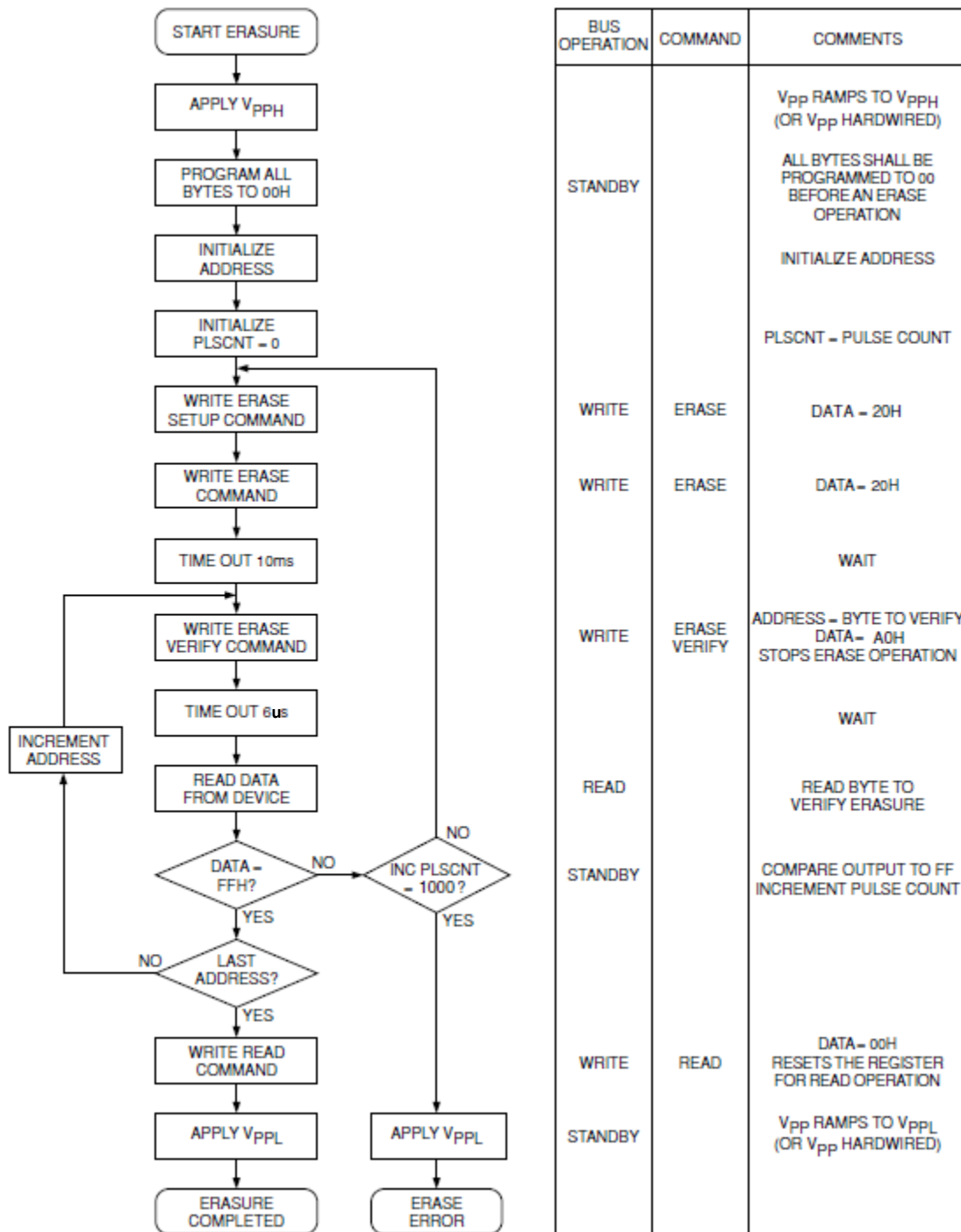


Figure 5. Chip Erase Algorithm<sup>(1)</sup>


Note:

(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device

## Erase Mode

During the first Write cycle, the command 20H is written into the command register. In order to commence the erase operation, the identical command of 20H has to be written again into the register. This two-step process ensures against accidental erasure of the memory contents. The final erase cycle will be stopped at the rising edge of  $\overline{WE}$ , at which time the Erase Verify command (A0H) is sent to the command register. During this cycle, the address to be verified is sent to the address bus and latched when  $\overline{WE}$  goes low. An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum erase timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

## Erase-Verify Mode

The Erase-Verify operation is performed on every byte after each erase pulse to verify that the bits have been erased.

## Programming Mode

The programming operation is initiated using the programming algorithm of Figure 7. During the first write cycle, the command 40H is written into the command register. During the second write cycle, the address of the memory location to be programmed is latched on the falling edge of  $\overline{WE}$ , while the data is latched on the rising edge of  $\overline{WE}$ . The program operation terminates with the next rising edge of  $\overline{WE}$ . An integrated stop timer allows for automatic timing control over this operation, eliminating the need for a maximum program timing specification. Refer to AC Characteristics (Program/Erase) for specific timing parameters.

**Figure 6. A.C. Timing for Programming Operation**

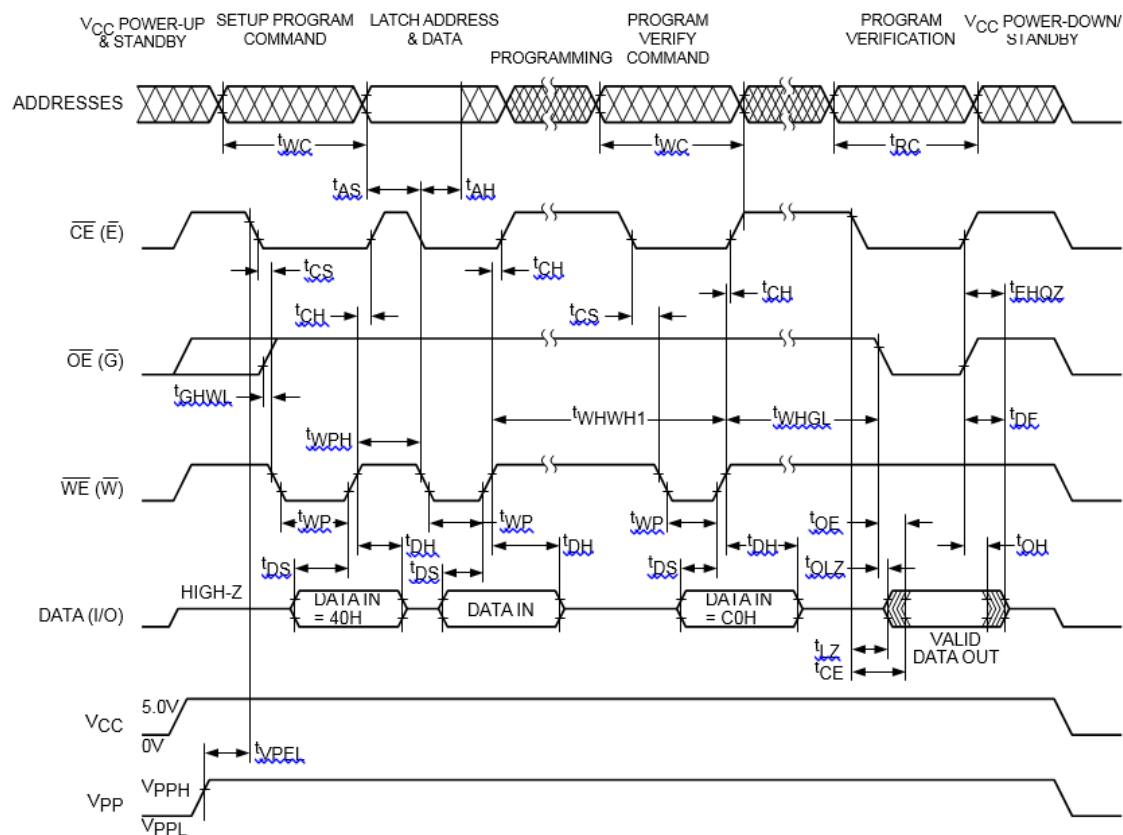
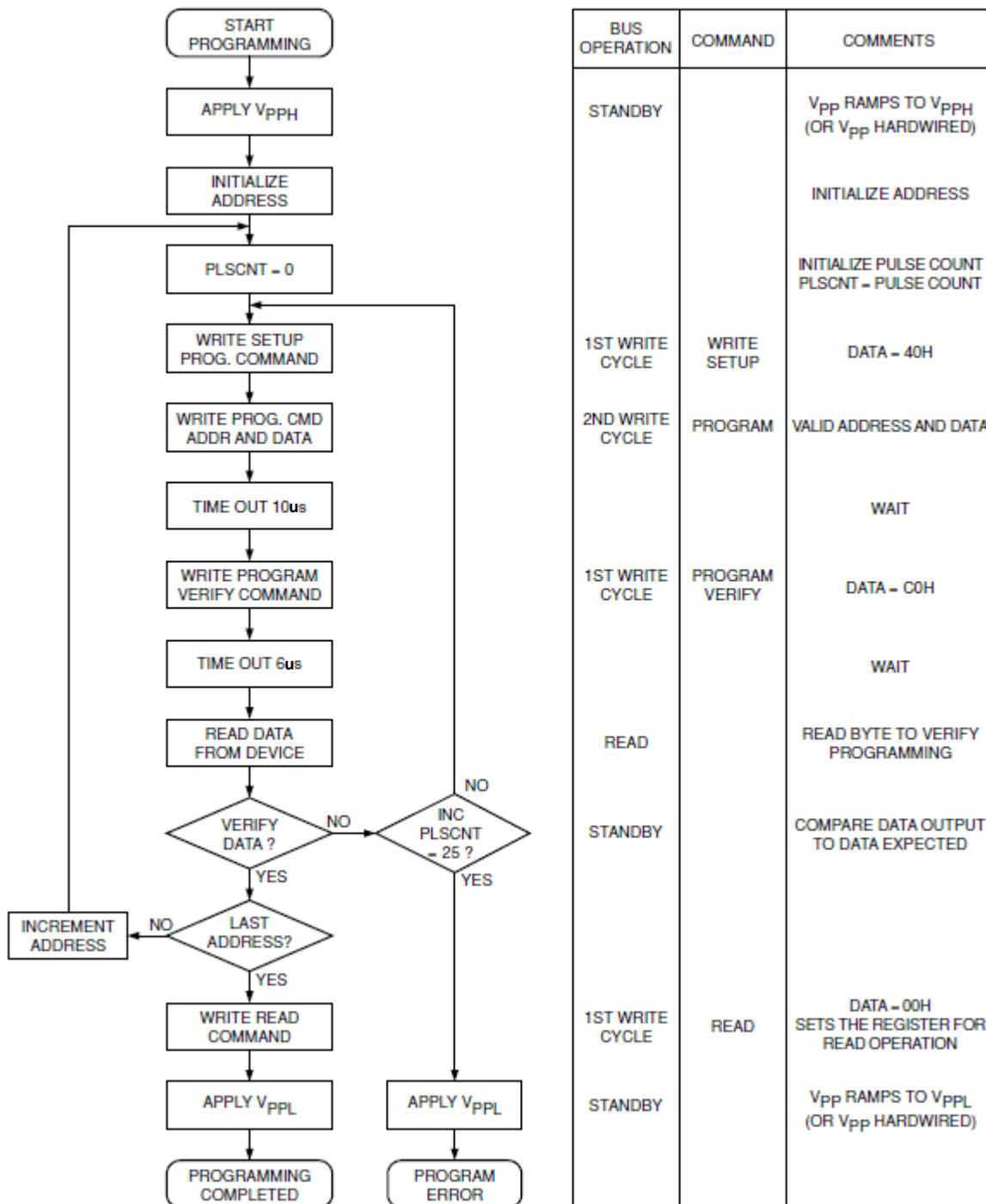


Figure 7. Programming Algorithm<sup>(1)</sup>


Note:

(1) The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device

## Program-Verify Mode

A Program-Verify cycle is performed to ensure that all bits have been correctly programmed following each byte programming operation. The specific address is already latched from the write cycle just completed, and stays latched until the verify is completed. The Program-Verify operation is initiated by writing C0H into the command register. An internal reference generates the necessary high voltages so that the user does not need to modify  $V_{CC}$ . Refer to AC Characteristics (Program/Erase) for specific timing parameters.

## Abort/Reset

An Abort/Reset command is available to allow the user to safely abort an erase or program sequence. Two consecutive program cycles with FFH on the data bus will abort an erase or a program operation. The abort/ reset operation can interrupt at any time in a program or erase operation and the device is reset to the Read Mode.

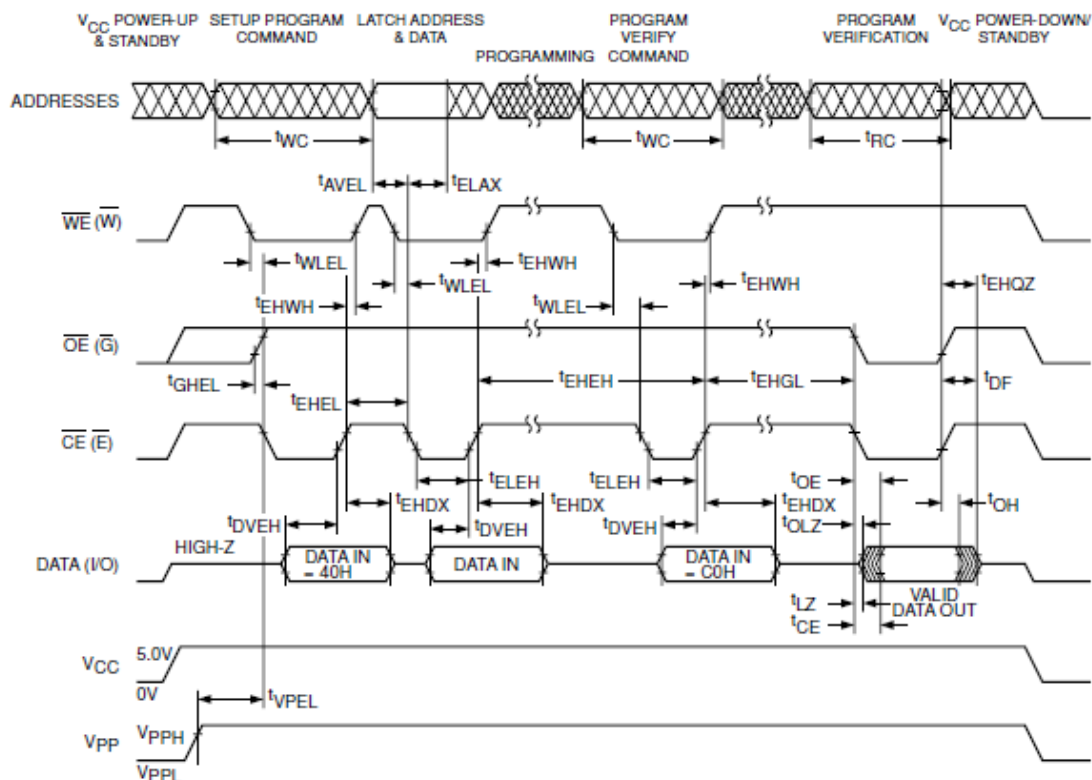
## POWER UP/DOWN PROTECTION

The TK28F020 offers protection against inadvertent programming during  $V_{PP}$  and  $V_{CC}$  power transitions. When powering up the device there is no power-on sequencing necessary. In other words,  $V_{PP}$  and  $V_{CC}$  may power up in any order. Additionally  $V_{PP}$  may be hardwired to  $V_{PPH}$  independent of the state of  $V_{CC}$  and any power up/down cycling. The internal command register of the TK28F020 is reset to the Read Mode on power up.

## POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1  $\mu\text{F}$  ceramic capacitor between  $V_{CC}$  and  $V_{SS}$  and  $V_{PP}$  and  $V_{SS}$ . These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

**Figure 8. Alternate A.C. Timing for Program Operation**



## Ordering Information

Package	Temperature	Speed	Order Number
32 Pin PLCC	-40°C to +85°C	120 ns	TK28F020NI-120
32 Pin PDIP	-40°C to +85°C	120 ns	TK28F020PI-120
32 Pin TSOP	-40°C to +85°C	120 ns	TK28F020TI-120

Note: An earlier data sheet described the 120 ns part as the TK28F020NI-12. This was a typo, and the correct suffix is -120. The -120 is an Intel naming convention, while the -12 is a Catalyst naming convention. Tekmos follows the Intel convention for speed classification.

## Contact Information

The TK28F020 can be ordered directly from Tekmos:

512-342-9871 phone  
Sales@Tekmos.com  
www.Tekmos.com

## Revision History

Date	Revision	Description
1/08/15	1.0	Initial Release
9/24/15	2.0	Specification Data Added
1/27/17	2.1	Ordering Information for 90ns added,
4/11/17	2.2	Correct pin numbering. Make military part a -95 speed
11/16/17	2.3	Add PDIP and TSOP package, Remove -90 and -95 parts. Correct typos

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