TEXAS INSTRUMENTS
TPS2384
SLUS634F – NOVEMBER 2004 – REVISED JANUARY 2022

TPS2384 Quad Integrated Power Sourcing Equipment Power Manager

1 Features

- Quad-port power management with integrated switches and sense resistors
- Compliant to IEEE 802.3af standard
- Operates from a single 48-V input supply
- Individual port 15-bit A/D
- Auto, semi-auto and power management operating modes
- Controlled current ramps for reduced EMI and charging of PD's bulk capacitance
- I^2C clock and oscillator watchdog timers
- Overtemperature protection
- DC and DC modulated disconnect
- Supports legacy detection for non-compliant PDs
- Supports AC disconnect
- High-speed 400-kHz I^2C interface
- Comprehensive power management software available
- Operating temperature range –40°C to 125°C

2 Applications

- Ethernet enterprise switches
- Ethernet hubs
- SOHO hubs
- Ethernet mid-spans
- PSE injectors

3 Description

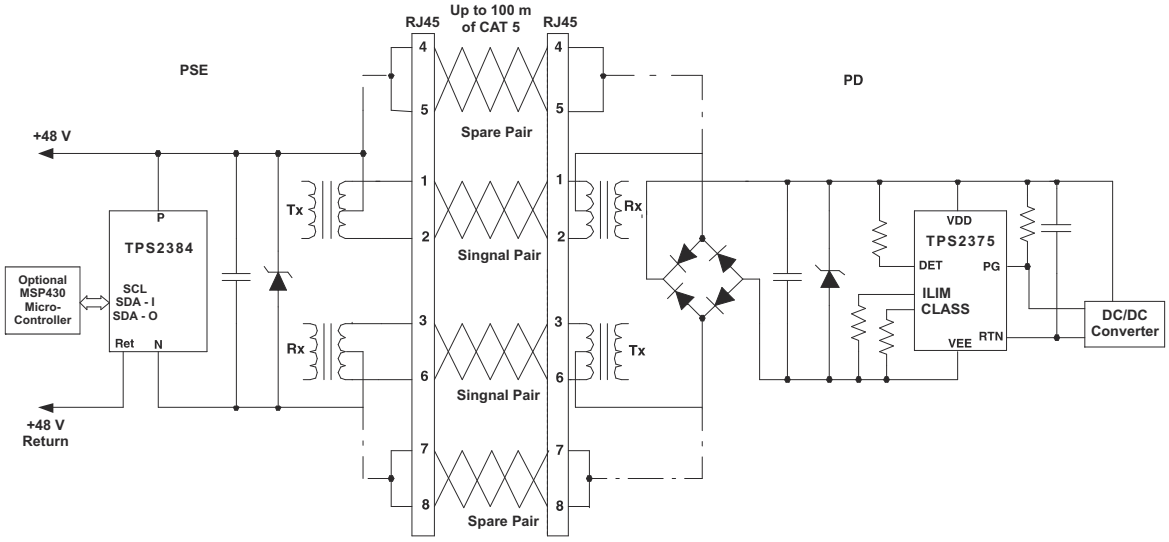
The TPS2384 is a quad-port power sourcing equipment power manager (PSEPM) and is compliant to the Power-over-Ethernet (PoE) IEEE 802.3af standard. The TPS2384 operates from a single 48-V supply and over a wide temperature range (–40°C to 125°C). The integrated output eliminates two external components per port (FET and sense resistor) and survives 100-V transients. Four individual 15-bit A/D converters are used to measure port resistance, voltage, current and die temperature making PSE solutions simple and robust. The TPS2384 comes with a comprehensive software solution to meet the most demanding applications which can serve as a core for all PoE system designs.

TheTPS2384 is available in either 64-pin PowerPAD™ down (PAP) or 64-pin PowerPAD™ up (PJD) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2384	HTQFP (64)	10.0mm x 10.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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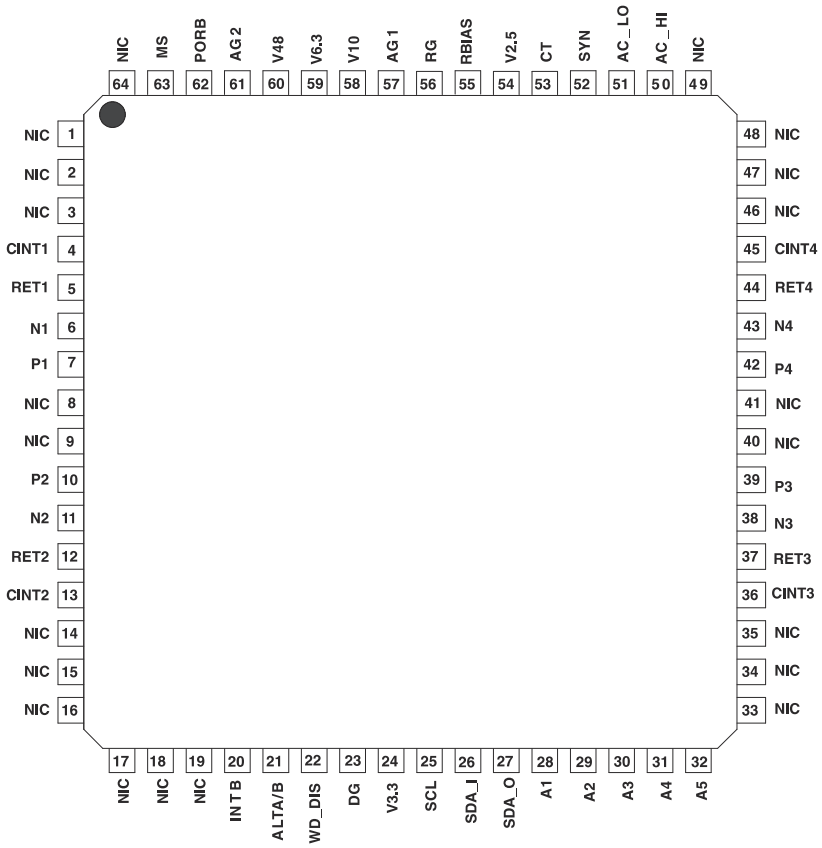
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2015) to Revision F (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed all instances of legacy terminology to controller and target where I^2C is mentioned	1
• Changed human-body model value from ±1500 V to ±1000 V	7
• Changed "Classification voltage loop control" MIN value from 15 V to 15.5 V in the *Electrical Characteristics* table	7
• Changed "Classification current limit" MIN value from 50 mA to 51 mA in the *Electrical Characteristics* table	7
• Added "R" for Read Only to Bit 7 Discovery Status in *Figure 8-23*	38

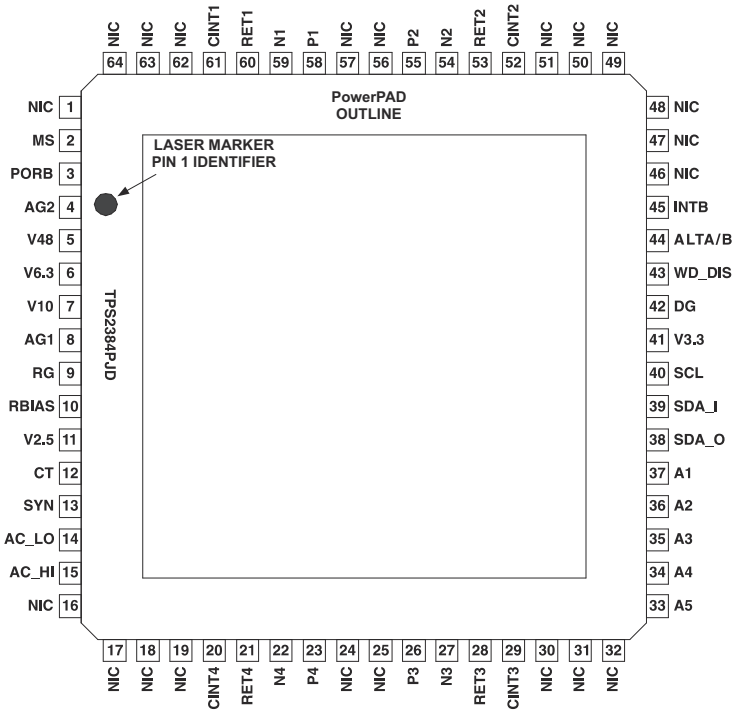
Changes from Revision D (March 2007) to Revision E (March 2015)	Page
• Added *ESD Rating* table, *Thermal Information* table *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout section*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed text in the description of pins A1-A5 From: "connecting to chip ground" To: "connecting to digital ground"	3
• Changed the first 5 rows in the Digital I^2C DC Spec3ifications of the *Electrical Characteristics*	7
• Added values for Discovery1,2 A/D conversion time in *Timing Requirements* TYP = 18, MAX = 22 ms	9
• Changed text in the *Auto Mode* From: "please contact the factory for additional application information." To: "refer to (SLUZ014)"	15
• Changed text in *Start/Stop* from "and not used by the TPS2384." To: (See Note (1) in Table 8-1)	32
• Changed text in the first sentence of *Chip Address*	32
• Added Note (1) to Table 8-1	33
• Changed text in Note 2 of Table 8-5 From: "Consult factory for Alternative B,." To: "refer to (SLUZ014) "for Alternative B,."	36
• Changed text in Note 2 of Table 8-7 From: "Consult factory for Alternative B,." To: "refer to (SLUZ014) "for Alternative B,."	37
• Changed the connections to pins 50 and 51 in Figure 9-2	44

5 Pin Configuration and Functions



A. NIC = No internal connection. Pins are floating.
B. NIC pins can be tied to the ground plane for improved thermal characteristics and to prevent noise injection from unused pins.
C. NIC pins next to CINT pins must be tied to ground to prevent noise injection into A/D converter.

Figure 5-1. PAP Package 64-Pin HTQFP Top View



A. NIC = No internal connection. Pins are floating.
B. NIC pins can be tied to the ground plane for improved thermal characteristics and to prevent noise injection from unused pins.
C. NIC pins next to CINT pins must be tied to ground to prevent noise injection into A/D converter.

Figure 5-2. PJD Package 64-Pin HTQFP Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	PAP	PDJ		
Power and Ground				
V48	60	5	I	48-V input to the device. This supply can have a range of 44 to 57 V. This pin must be decoupled with a 0.1-µF capacitor from V48 to AG1 placed as close to the device as possible.
V10	58	7	O	10-V analog supply. The 10-V reference is generated internally and connects to the main internal analog power bus. A 0.1-µF de-coupling capacitor must terminate as close to this node and the AG1 pin as possible. Do not use for an external supply.
V6.3	59	6	O	6.3-V analog supply. A 0.1-µF de-coupling capacitor must terminate as close to this pin and the AG1 pin as possible. Do not use for an external supply.
V3.3	24	41	O	3.3-V logic supply. The 3.3-V supply is generated internally and connects to the internal logic power bus. A 0.1-µF de-coupling capacitor must terminate as close to this node and the DG pin as possible. This output can be used as a low current supply to external logic.
V2.5	54	11	O	2.5-V reference supply. The V2.5 is generated internally and connects to the internal reference power bus. This pin must not be tied to any external supplies. A 0.1-µF de-coupling capacitor must terminate as close to this node and the RG pin as possible. Do not use for an external supply.
AG1	57	8	GND	Analog ground 1. This is the analog ground of the V6.3, V10 and V48 power systems. This pin must be externally tied to the common copper 48-V return plane. This pin must carry the low side of three de-coupling capacitors tied to V48, V10 and V6.3.
AG2	61	4	GND	Analog ground 2. This pin is the analog ground which ties to the substrate and ESD structures of the device. this pin must be externally tied to the common copper 48-V return plane. AG1 and AG2 must be tied together directly for the best noise immunity.
DG	23	42	GND	Digital ground. This pin connects to the internal logic ground bus. this pin must be externally tied to the common copper 48-V return plane.
RG	56	9	GND	Reference ground. This pin is a precision sense of the external ground plane. The integration capacitor (CINT) and the biasing resistor (RBIAS pin) must be tied to this ground. This ground must also be used to form a printed wiring board ground guard ring around the active node of the integration capacitor (CINT). It must tie to common copper 48-V return plane.
Port Analog Signal				
P1	7	58	I	Port Positive. 48-V load sense pin. Terminal voltage is monitored and controlled differentially with respect to each Port N pin. Optionally, if the application warrants, this high-side path can be protected with the use of a self-resetting poly fuse.
P2	10	55	I	
P3	39	26	I	
P4	42	23	I	
N1	6	59	I	Port negative. 48-V load return pin. The low side of the load is switched and protected by internal circuitry that limits the current.
N2	11	54	I	
N3	38	27	I	
N4	43	22	I	
RET1	5	60	I	48-V return pin
RET2	12	53	I	
RET3	37	28	I	
RET4	44	21	I	
CINT1	4	61	I	Integration capacitor This capacitor is used for the ramp A/D converter signal integration. Connect A 0.027- µF capacitor from this pin to RG. To minimize errors use a polycarbonate, poly-polypropylene, polystyrene or teflon capacitor type to prevent leakage. Other types of capacitors can be used with increased conversion error.
CINT2	13	52	I	
CINT3	36	29	I	
CINT4	45	20	I	

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	PAP	PDJ		
Analog Signals				
CT	53	12	I	This is a dual-purpose pin. When tied to an external capacitor this pin sets the internal clock. When the CT pin is grounded the SYN pin turns from a output to an input (see SYN pin description). The timing capacitor and the resistor on the RBIAS pin sets the internal clock frequency of the device. This internal clock is used for the internal state machine, integrating A/D counters, POR time out, faults and delay timers of each port. Using a 220-pF capacitor for CT and a 124-kΩ resistor for RBIAS sets the internal clock to 245 kHz and ensure IEEE 802.3af compliance along with maximizing the rejection of 60-Hz line frequency noise from A/D measurements.
RBIAS	55	10	I	Bias set resistor. This resistor sets all precision bias currents within the chip. This pin regulates to 1.25 V (V2.5/2) when a resistor is connected between RBIAS and RG. This voltage and RBIAS generate a current which is replicated and used throughout the chip. This resistor also works in conjunction with the capacitors on CT and CINT to set internal timing values. The RBIAS resistor must be connected RG. RBIAS is a high impedance input and care must be taken to avoid signal injection from the SYN pin or I^2C signals.
SYN	52	13	I/O	This is a dual purpose pin. When the CT pin is connected to a timing capacitor this output pin is a 0-V to 3.3-V pulse of the internal clock which can be used to drive other TPS2384 SYN pins for elimination of a timing capacitor. When the CT pin is grounded this pin becomes an input pin that can be driven from a controller TPS2384 or any other clock generator signal.
AC_LO	51	14	O	Totem-pole output pin for AC Disconnect excitation.
AC_HI	50	15	O	Totem-pole output pin for AC Disconnect excitation.
Digital Signals				
SCL	25	40	I	Serial clock input pin for the I^2C interface.
SDA_I	26	39	I	Serial data input pin for the I^2C interface. When tied to the SDA_O pin, this connection becomes the standard bi-directional serial data line (SDA)
SDA_O	27	38	O	Serial data open drain output for the I^2C interface. When tied to the SDA_I pin, this connection becomes the standard bi-directional serial data line (SDA). This pin is an open drain output that can directly drive opto-coupler.
WD_DIS	22	43	I	The WD_DIS pin disables the watchdog timer function when connected to 3.3 V. The pin has internal 50-kΩ resistor to digital ground. The watchdog timer monitors the I^2C clock pin (SCL) and the internal oscillator activity in power management mode and only the internal oscillator activity in auto mode.
INTB	20	45	O	This pin is an open-drain output that goes low if a fault condition occurs on any of the 4 ports.
ALTA/B	21	44	I	When this input is set to logic low there is no back-off time after a discovery failure. When this pin set to a logic high there is a back-off time (approximately 2 seconds) before initiating another discovery cycle. This pin has an internal 50-kΩ resistor pulldown to digital ground.
A1	28	37	I	Address 1 through 5. These pins are the I^2C address select inputs. Select the appropriate binary address on these pins by connecting to digital ground for a logic low or tying to the V3.3 pin for a logic high. Each address line has an internal current source pulldown to digital ground.
A2	29	36	I	
A3	30	35	I	
A4	31	34	I	
A5	32	33	I	
MS	63	2	I	The MS pin selects either the auto mode (MS low) or the power management mode, PMM, (MS high). This pin can be held low for controller-less standalone applications. When MS is low and the POR timing cycle is complete the chip sequentially *Discovers, Classifies and Powers on* each port. When MS is set high the ports are controlled by register setting via the I^2C bus. The MS pin has an internal 50-kΩ resistor pulldown to analog ground.
PORB	62	3	I	This pin can be used to override the internal POR. When held low, the I^2C interface, all the state machines, and registers are held in reset. When all internal and external supplies are within specification, and this pin is set to a logic high level, the POR delay begins. The I^2C interface and registers become active within 70 µs of this event and communications to read or preset registers can begin. The reset delay for the remainder of the chip then extinguishes in 1 second. This pin has an internal 50-kΩ resistor pulldown to analog ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
	V10 current sourced	100	100	µA
	V3.3 current sourced	5	5	mA
	Applied voltage on CINT#, CT, RBIAS	–0.5 to 10	10	V
	Applied voltage on SCL_I, SDA_I, SDA_O, INTB, A1, A2, A3, A4, A5, MS, PORB, WD_DIS, ALT_A/B, AC_LO, AC_HI	–0.5	6	
	Applied voltage on V48, P#, N#	–0.5	80	
T_J	Junction operating temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{DD}	Input voltage, V48	44	48	57	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PAP [HTQFP] 64 PINS	PJD [HTQFP] 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.9	30.1(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.4	0.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	7.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.8	7.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) $R_{\theta JA}$ varies with the heat sink used. Data modeled using 15 mm x 15 mm x 5 mm copper block heat sink.

6.5 Electrical Characteristics

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply					
V48 quiescent current	Off mode (all ports)	4	9	12	mA
V48 quiescent current	Powered mode (all ports)		10	14	
V10, internal analog supply	I_{LOAD} = 0	9.75	10.5	11.5	V
V3.3, internal digital supply	I_{LOAD} = 0 to 3 mA	3	3.3	3.7	

6.5 Electrical Characteristics (continued)

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V3.3 short circuit current	V = 0	3		12	mA
V6.3, internal supply	I_{LOAD} = 0	5	6.3	7	V
V2.5, internal reference supply	I_{LOAD} = 0	2.46	2.5	2.54	V
Input UVLO			26	32	V
Internal POR time out(I^2C)	After all supplies are good I^2C activity is valid		8		Clock Pulses
Internal POR time out (Port)	After all supplies are good Port active to I^2C commands		66000		Clock Pulses
Port Discovery					
Port off #P to #N input resistance		400	600		kΩ
Discovery open circuit voltage			22	30	V
Discovery 1 voltage loop control	70 µA < I_{PORT} < 3 mA	2.8	4.4		V
Discovery 2 voltage loop control	70 µA < I_{PORT} < 3 mA		8.8	10	V
Discovery current limit	P = N = 48 V	3	4	5	mA
Auto-mode discovery resistance acceptance Band		19		26.5	kΩ
Auto-mode discovery resistance low end rejection		0		15	kΩ
Auto-mode discovery resistance high end rejection		33			kΩ
Discovery1,2 A/D conversion scale factor	100 µA < I_{PORT} < 3 mA	5.30	6.10	6.75	count/µA
Port Classification					
Classification voltage loop control	100 µA < I_{PORT} < 50 mA	15.5	17.5	20	V
Classification current limit	P = N = 48 V	51	60	100	mA
Class 0 to 1 detection threshold		5.5	6.5	7.5	mA
Class 1 to 2 detection threshold		13	14.5	16	mA
Class 2 to 3 detection threshold		21	23	25	mA
Class 3 to 4 detection threshold		31	33	35	mA
Class 4 to 0 detection threshold		45	48	51	mA
Classification A/D conversion scale factor		375	424	475	Count/ mA
Port Legacy Detection					
Legacy current limit	P = N = 48 V	2.6	3.5	4.3	mA
Legacy voltage A/D conversion scale factor	100 mV < V_{PORT} < 17.5 V	1365	1400	1445	Count/V
Port Powered Mode					
Port on resistance	20 mA < I_{PORT} < 300 mA		1.3	1.8	Ω
Over current threshold (I_{CUT})	R_{BIAS} = 124 kΩ, C_T = 220 pF, –25 ≤ T_J ≤ 105	350	375	400	mA
Output current limit (I_{LIM})	R_{BIAS} = 124 kΩ, C_T = 220 pF, –25 ≤ T_J ≤ 105		425	450	mA
Disconnect timer current threshold	R_{BIAS} = 124 kΩ, C_T = 220 pF		7.5	10	mA
Port output UV		42.0	42.7	44.0	V
Port output OV		54	55	56	V
Port current A/D conversion scale factor	20 mA < I_{PORT} < 56 V	31	36.41	40	Count/ mA
Port voltage A/D conversion scale factor	45 V < V_{PORT} < 56 V	335	353	370	Count/V
Port temperature A/D conversion		(17500 - counts)/16			°C
Port Disable Mode					
Port N voltage	P = 48 V	47			V

6.5 Electrical Characteristics (continued)

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC LO and AC HI Specification					
AC_LO, AC_HI – low output voltage		0		0.5	V
AC_LO – high output voltage		3.0		5.0	
AC_HI – high output voltage		5.0		7.0	
Digital I²C DC Specifications					
SCL logic low input threshold (V_{IL})		0.5			V
SDA_I logic low input threshold (V_{IL})		1.25			V
SCL, SDA_I logic high input threshold (V_{IH})				1.75	V
A1–A5 ,WD_DIS, ALTA/B, MS, PORB logic input threshold			1.5		V
MS, PORB input hysteresis			150		V
WD_DIS,ALTA/B, MS, PORB input pulldown resistance	Input voltage 0.5 to 3 V		50		kΩ
A1–A5 pulldown current			10		µA
SDA_O logic high leakage	Drain = 5 V		100		nA
SDA_O logic low	I_{SINK} = 10 mA		200		mV
INTB logic high leakage	Drain = 6 V		10		µA
INTB logic low	I_{SINK} = 10 mA		200		mV

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Port Discovery					
Discovery1,2 A/D conversion time	I_{PORT}= 120 µA		18	22	ms
Port Classification					
Classification A/D conversion time	I_{PORT} = 50 mA		18	22	ms
Port Legacy Detection					
Legacy A/D conversion time	0 V < V_{PORT} < 15 V		18	22	ms
Port Powered Mode					
t_{MPDO}, disconnect detection time	R_{BIAS} = 124 kΩ, C_T = 220 pF, I_{LOAD} < current threshold	300		400	ms
Over current time out (T_{OVLD})	R_{BIAS} = 124 kΩ, C_T = 220 pF	50		75	ms
Short circuit time out (T_{LIM})	R_{BIAS} = 124 kΩ, C_T = 220 pF	50		75	
Turn-off delay from UV/OV faults	R_{BIAS} = 124 kΩ, C_T = 220 pF, After port enabled and ramped up		3		
Port current A/D conversion time	I_{PORT} < 300 mA		18	22	ms
Port voltage A/D conversion time	45 V < V_{PORT} < 56 V		18	22	ms
Digital I²C Timing					
SCL clock frequency, f_{SCL}		0		400	kHz
Pulse duration, t_{HIGH}	SCL high	0.6			µs
Pulse duration, t_{LOW}	SCL low	1.3			
Rise time, SCL and SDA, t_r				0.300	
Fall time, SCL and SDA, t_f				0.300	
Setup time, SDA to SCL, $t_{SU;DAT}$		0.250			
Hold time, SCL to SDA, $t_{HD;DAT}$		0.300		0.900	
Bus free time between start and stop, t_{BUF}		1.3			
Setup time, SCL to start condition, $t_{SU;STA}$		0.6			
Hold time, start condition to SCL, $t_{HD;STA}$		0.6			
Setup time, SCL to stop condition, $t_{SU;STO}$		0.6			

6.7 Typical Characteristics

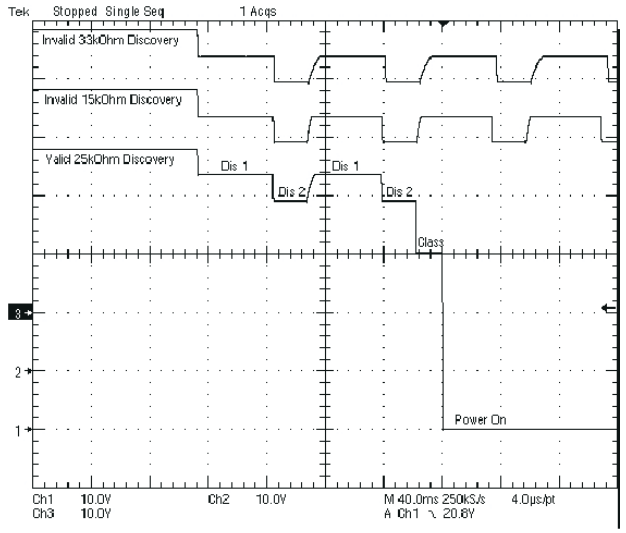


Figure 6-1. Invalid (33 kΩ and 15 kΩ) and Valid Discovery (25 kΩ)

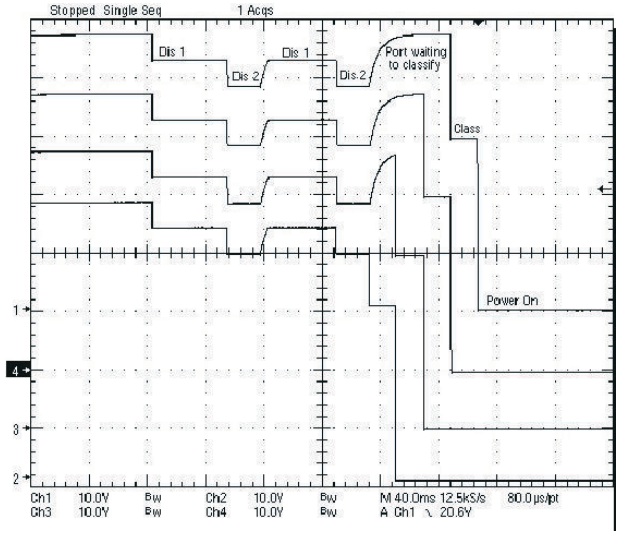


Figure 6-2. Four Port Discovery, Class, Power On

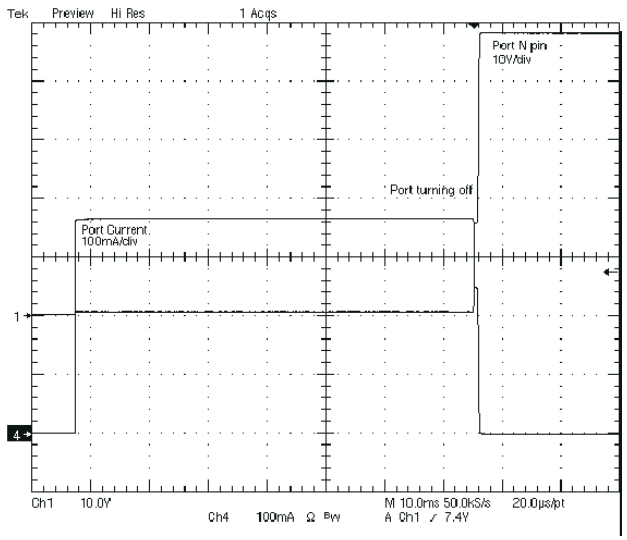


Figure 6-3. Port Overcurrent Response

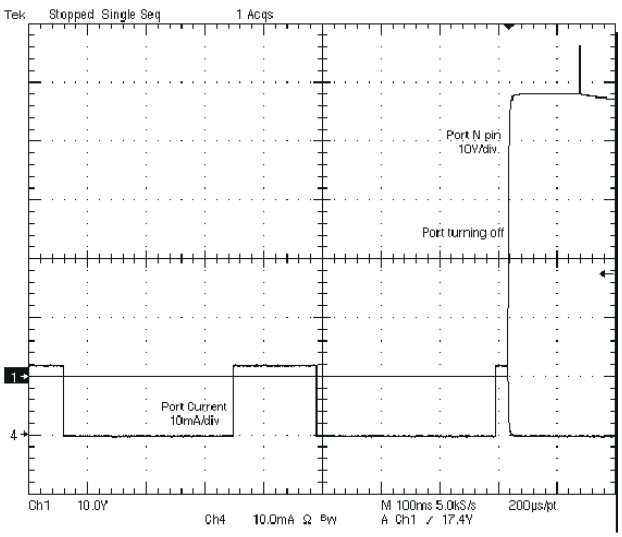
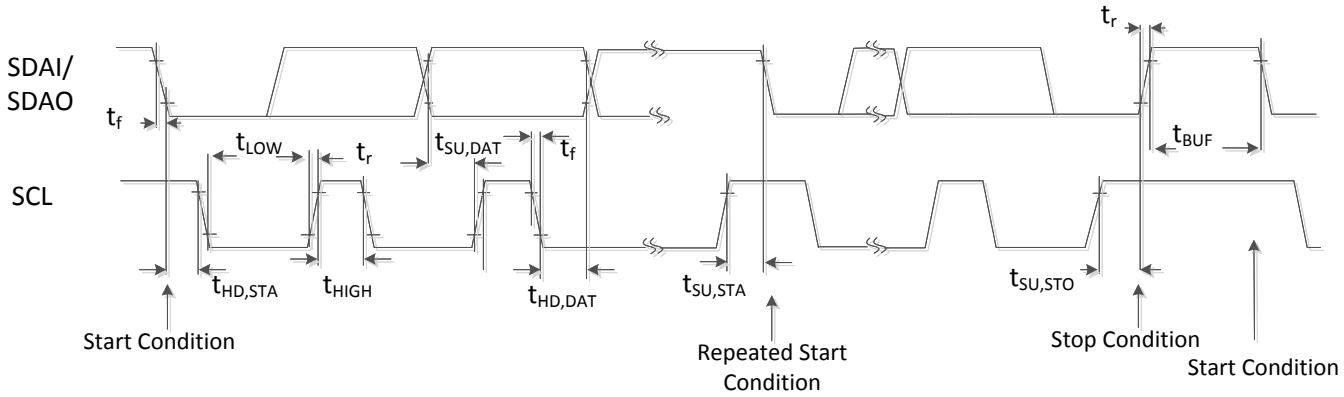


Figure 6-4. Port Undercurrent Response in DC Disconnect

7 Parameter Measurement Information



8 Detailed Description

8.1 Overview

The TPS2384 has three internal supply buses (10 V, 6.3 V and 3.3 V) generated from the 48-V input supply. These supplies are used to bias all internal digital and analog circuitry. Each supply has been brought out separately for proper bypassing to insure high performance. The digital supply (3.3 V) is available for powering external loads up to 2 mA. For more demanding loads TI highly recommends to use external buffers to prevent system degradation. When the TPS2384 is initially powered up an internal Power-on-Reset (POR) circuit resets all registers and sets all ports to the off state to ensure that the device is powered up in a known safe operating state.

The TPS2384 has three modes of operation: auto mode (AM), semi-auto mode (SAM), and power management mode (PMM).

- In auto mode the TPS2384 performs discovery, classification and delivery of power autonomously to a compliant PD without the need of a micro-controller.
- In semi-auto mode the TPS2384 operates in auto mode but users can access the contents of all read status registers and A/D registers through the I^2C serial interface. All write control registers are active except for D0 through D3 of Port Control register 1 (Address 0010) for limited port control. The semi-auto mode allows the TPS2384 to detect valid PDs without micro-controller intervention but adds a flexibility to perform power management activities.
- Power management mode (with a micro-controller) allows users additional capabilities of discovering non-compliant (legacy) PDs, performing AC Disconnect and advanced power management system control that are based on real time port voltages and currents. All functions in this mode are programmed and controlled through read and write registers over the I^2C interface. This feature allows users complete freedom in detecting and powering devices. A comprehensive software package is available that mates the power of the TPS2384 with the MSP430 micro-controller.

TPS2384 integrated output stage provides port power and low-side control. The internal low-side circuitry is designed with internal current sensing so there are no external resistors required. The output design ensures the power switches operate in the fully enhanced mode for low power dissipation.

The I^2C interface allows easy application of opto-coupler circuitry to maintain Ethernet port isolation when a ground based micro-controller is required. The TPS2384 five address pins (A1–A5) allow the device to be addressed at one of 31 possible I^2C addresses. Per-port write registers separately control each port state (discovery, classification, legacy, power up, and so on) while the read registers contain status information of the entire process along with parametric values of discovery, classification, and real-time port operating current, voltage and die temperature.

The proprietary 15-bit integrating A/D converter is designed to meet the harsh environment where the PSEPM resides. The converter is set for maximum rejection of power line noise allowing it to make accurate measurements of line currents during discovery, classification and power delivery for reliable power management decisions.

8.2 Functional Block Diagrams

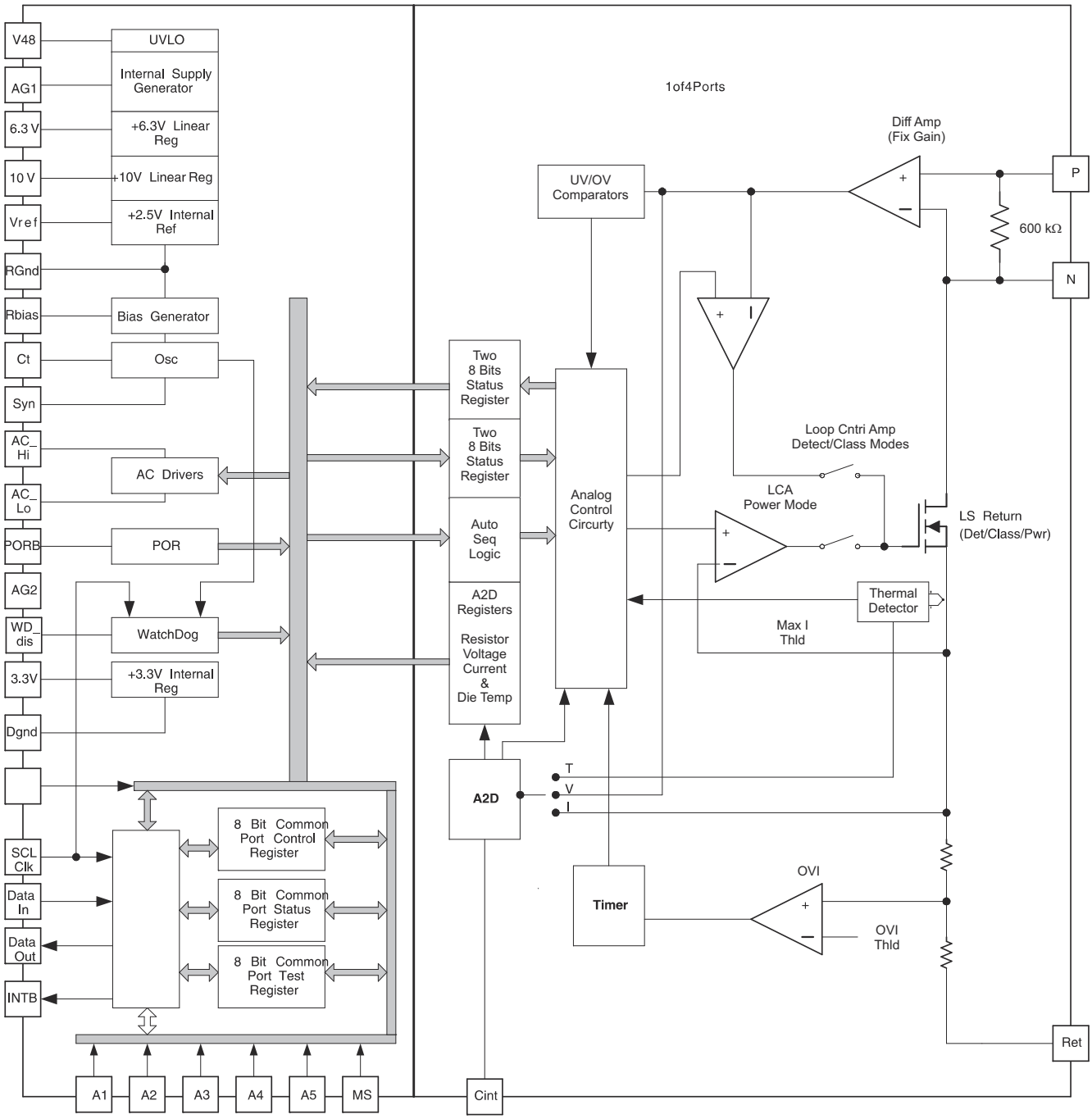
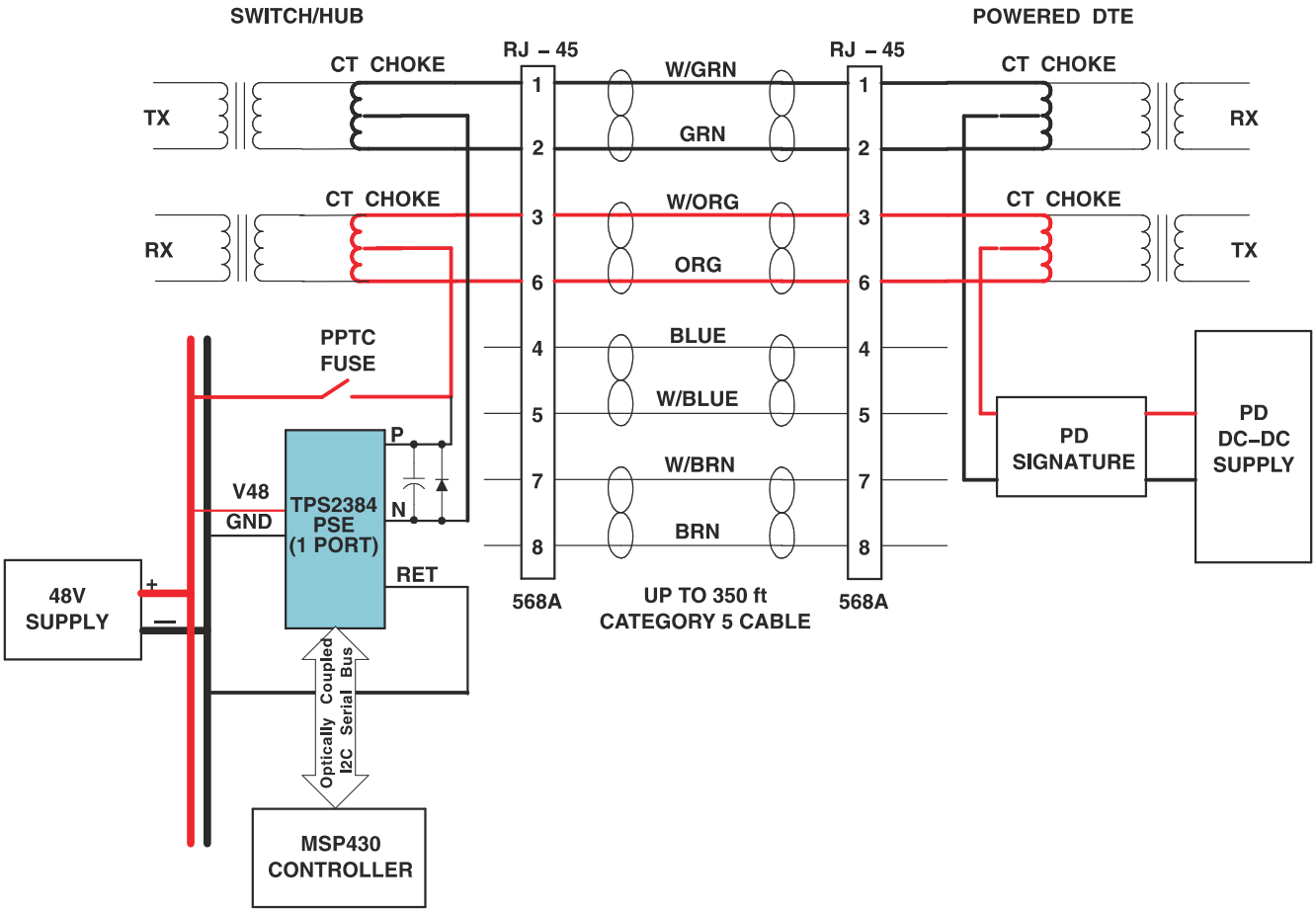


Figure 8-1. Single Port Block Diagram



A fuse can be required to provide additional protection if isolation is lost or the low-side current sense fails.

Figure 8-2. System Block Diagram

8.3 Feature Description

8.3.1 PMM Faults

PMM faults are the same as those shown in the *AM Faults and INTB Output* section. In PM mode, the port under and overvoltage and undercurrent faults can be disabled by writing to the control bits in the appropriate register. Monitoring for these fault conditions is enabled by default after device POR or other reset operation. The enable state of these features can be toggled by writing to the corresponding control bit as defined below and in Table 8-4 and Table 8-5.

The PMM faults are:

- Port under and overvoltage faults (disable through Common Control register 0001b, bit D2)
- Overcurrent fault (cannot be disabled)
- Undercurrent (DC Disconnect) fault (disable through Port Control register 0010b, bit D4)
- Thermal shutdown (TSD) fault (cannot be disabled)
- Watchdog fault (disable via WD_DIS pin)

Any one of these faults causes the port to shutdown. After a fault has occurred the port can not be repowered until a Disable function is sent. The Disable function clears the fault latch and the fault register.

INTB pin operation is essentially the same in PMM as in AM, with the following exceptions:

- For load undercurrent to generate a fault shutdown and status indication, the condition of load current less than the threshold must be detected by the continuous sample (C_SAMPLE) function (0111b).
- In PMM only, a Watchdog timer fault also asserts INTB.

8.3.2 Watchdog Timer

TPS2384 has two watchdog timers. One monitors the I^2C clock and the other monitors the internal clock. When auto mode is selected and the watchdog timer has not been disabled only the internal clock is monitored. When in power management mode and the watchdog timer has not been disabled then both the I^2C and internal clocks are monitored. If there is no I^2C clock activity for approximately two seconds then all ports are disabled. There are three means to enable ports after a I^2C clock fault and they are:

1. Hard power reset
2. PORB pulse
3. Writing a software reset to the Common Control register

In both auto mode and power management mode if the internal oscillator is lost for more than 20 ms all ports are disabled.

Loss of these signals is considered catastrophic because the system loses its ability to talk to each port. Therefore the watchdog timers disabling all ports protects the system.

This function can be easily over ridden by setting the WD_DIS pin high.

8.4 Device Functional Modes

8.4.1 Auto Mode

Auto mode (AM, MS = 0) operation is the basic approach for applying power to IEEE compliant PDs. When AM has been selected the TPS2384 automatically performs the following functions:

- Discovery of IEEE 802.3af compliant powered devices (PDs)
- Classification
- Power delivery
- Port over and undervoltage detection
- Port over current detection (350 mA < I_{PORT} < 400 mA
- Port maximum current limit (400 mA < I_{PORT} < 450 mA)
- DC Disconnect (5 mA < I_{PORT} < 10 mA)
- Thermal shutdown protection (TSD), (T_J > 150°C)
- Internal oscillator watchdog

In AM the contents of all read registers are available through the I^2C interface. In addition, all control registers except for the function bits can be written. This fact supports a semi-auto mode where the TPS2384 auto detects compliant PDs while a host can access the A/D registers and class information and then implement power management (including turning a port off, responding to faults, and so forth).

The write registers that are still active in AM are:

- All ports disable – Common Control register 0001b
- Over and undervoltage faults – Common Control register 0001b
- Software reset – Common Control register 0001b
- Disconnect disable – Port Control 1 register 0010b
- Discovery fault disable – Port Control 1 register 0010b
- Port enable – Port Control 2 register 0011b

For Alternative B, semi-auto mode implementations which manipulate the all Ports Disable or Port Enable bits, refer to *TPS2384 Power Sourcing Equipment Power Manager Device Errata*.

8.4.2 Auto Mode Functional Description

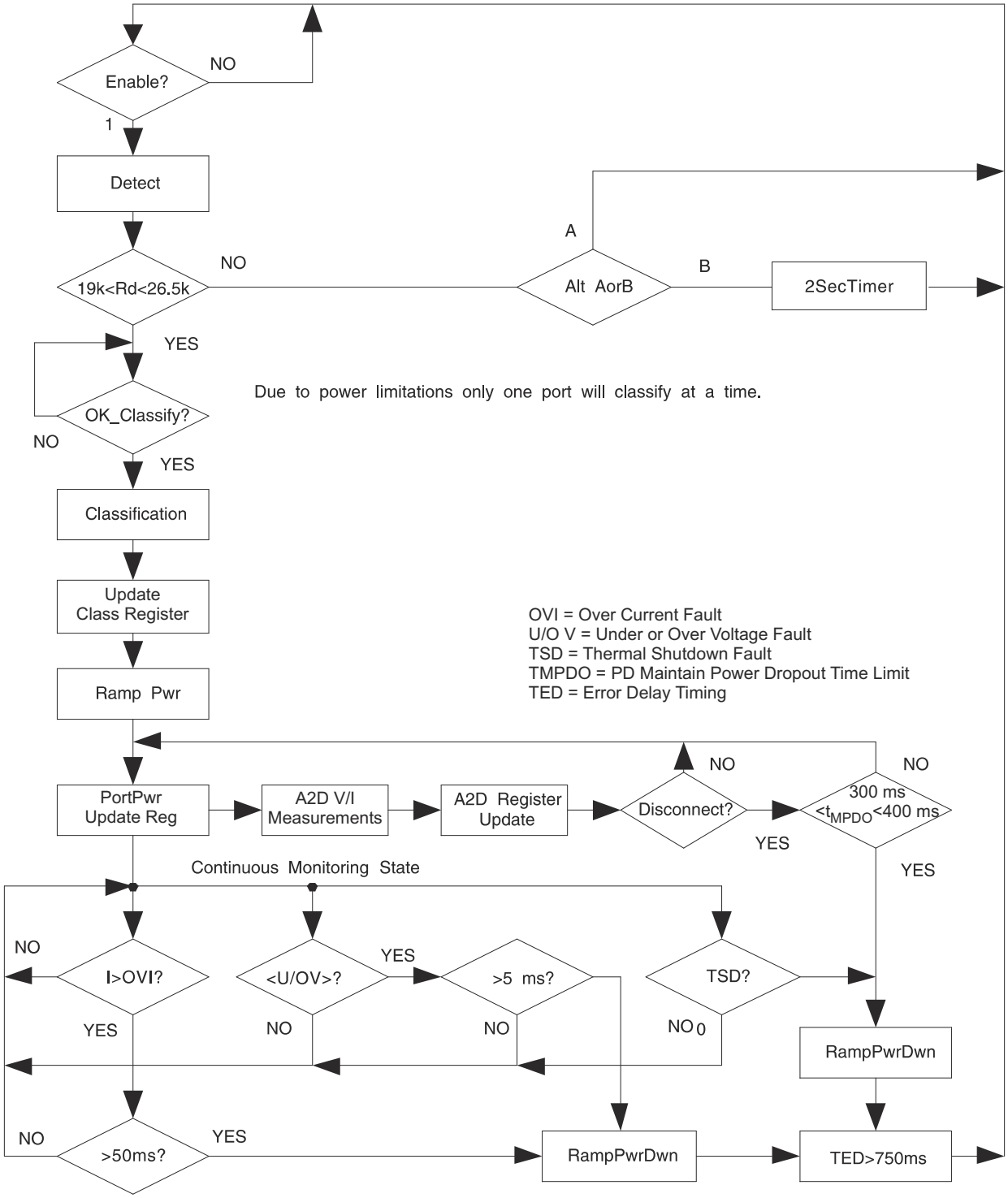


Figure 8-3. The Basic Flow for Auto Mode

8.4.2.1 AM Discovery

The TPS2384 uses a four-point measurment technique using two low level probe signals (typically 4.4 V and 8.8 V) during the discovery process to determine whether a valid PD is present. The use of a multipoint detection method for the PD resistor measurement allows accurate detection even when series steering diodes

are present. The low level probe voltages also prevent damage to non-802.3 devices. When a valid PD has been detected the TPS2384 moves to classification. If a valid PD has not been detected the TPS2384 continues to cycle through the discovery process. The waveform in Figure 8-4 shows typical N-pin waveforms for the discovery of a valid PD and the failure to discovery due to a discovery resistor of 15 kΩ and 33 kΩ.

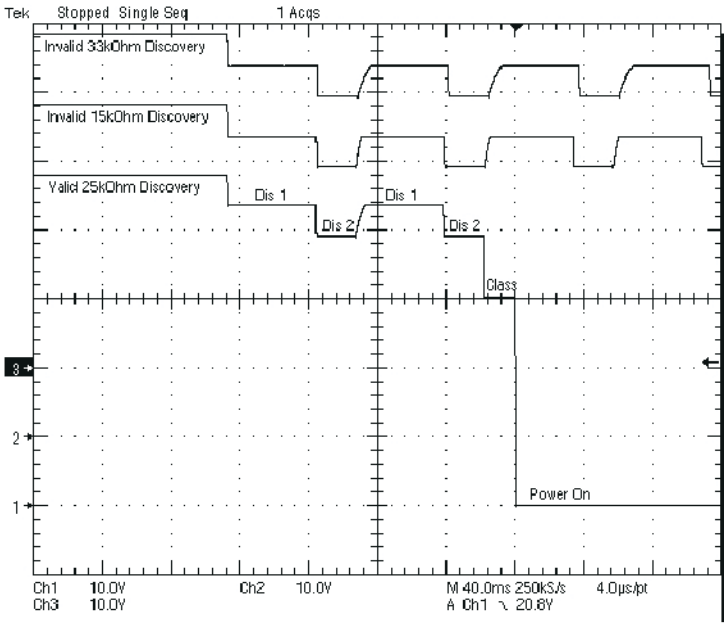


Figure 8-4. Invalid (33 kΩ and 15 kΩ) and Valid Discovery (25 kΩ)

8.4.2.2 AM Classification

After a successful discovery of a valid PD, the TPS2384 enters the classification function that identifies the power level based on the PD's current signature. The classification current level is measured at a reduced terminal voltage of 17.5 V. During classification the power dissipation can be at its highest; therefore, to prevent overtemperature shutdown in auto mode, only one port classifies at a time. When multiple ports successfully discover and proceed to classification at the same time the auto sequencer processes each request separately allowing only one port to enter classification. Figure 8-5 shows all four ports successfully detecting a valid PD at the same time and then the classification of each port occurring separately.

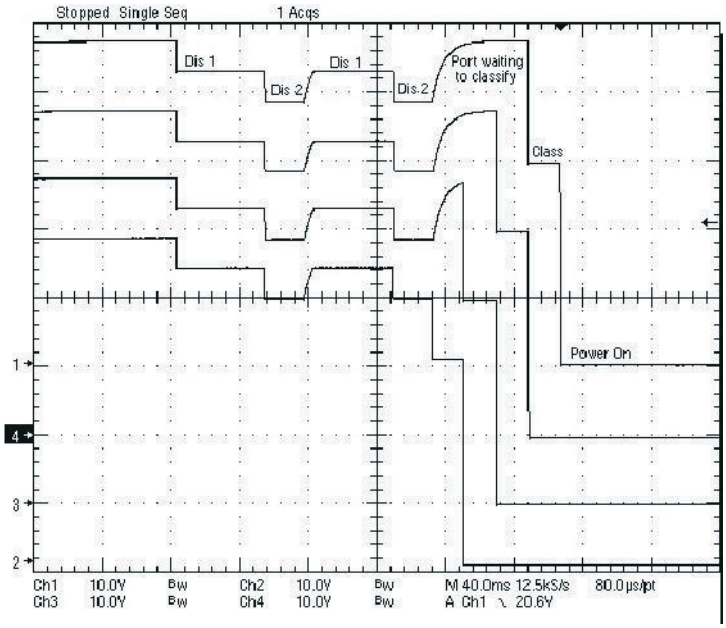


Figure 8-5. Four Port Discovery, Class, Power On

Upon completion of classification, the port classification register is updated. In AM mode, this information is not used but for semi-auto mode the class information can be used for power management. Figure 8-6 shows actual class currents and the class assignment which were stored in the register. These assignments are compliant with the IEEE 802.3af Standard

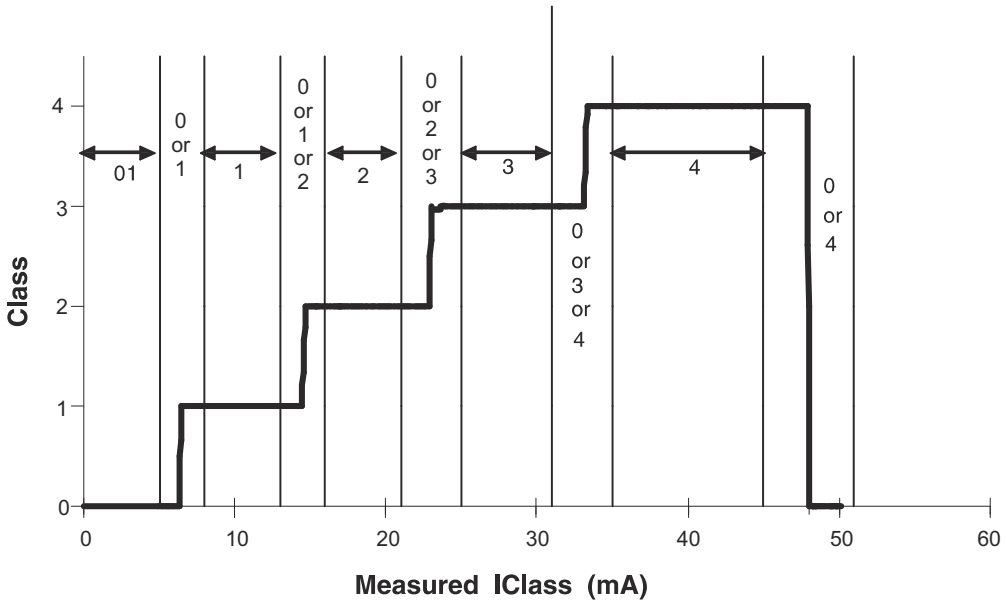


Figure 8-6. Class Current and Class Assignments

8.4.2.3 AM Power Delivery

After successful discovery and classification of a valid PD, the power is delivered by controlling the current to the PD until its current requirements are met or until the internal current limit is reached (approximately 425 mA). The power switch is fully enhanced after 500 µs. Figure 8-7 shows the voltage and the current that is being applied to the PD during power up and reaching the PD load of 250 mA.

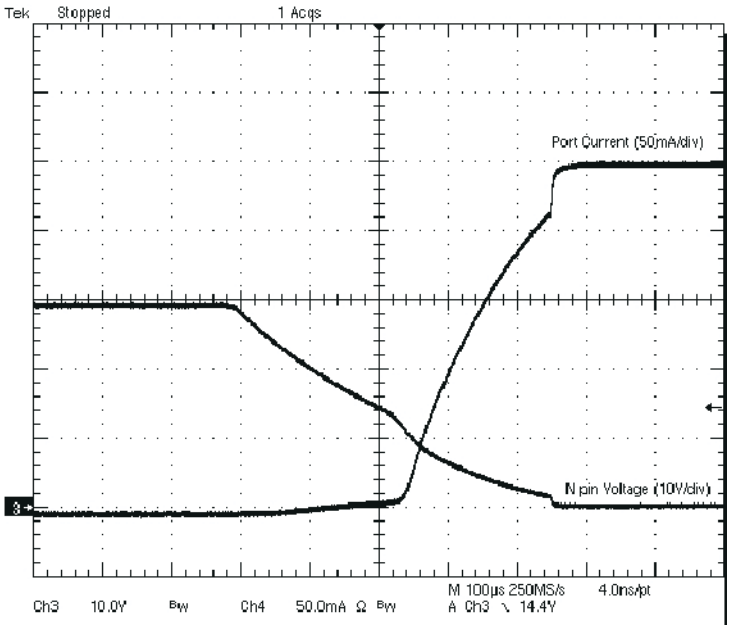


Figure 8-7. Port Power Delivery Voltage and Current

After power has been applied to the PD, the TPS2384 automatically enters the current and voltage sample mode. The sample mode performs 31 current measurements and 1 voltage measurement. Each measurement takes approximately 18 ms to complete. The port remains powered and the current and voltage measurement cycle continues until a fault condition occurs. The current and voltage measurements are both stored in the A/D current and voltage registers and can be accessed through the I^2C pins. This feature allows power management in the AM if it is desired.

8.4.3 AM Faults and INTB Output

AM faults are:

- Port under and overvoltage faults
- Overcurrent faults
- Undercurrent (DC Disconnect) fault
- Thermal shutdown (TSD) fault
- Watchdog timer faults (disabled through WD_DIS pin)

Any one of the first four fault conditions listed above causes the port to shut down, and a 3-bit fault code to be latched into the affected port's Status Read 1 register (addr = 0100b). Watchdog faults cause all four ports to shut down. Faulted ports are temporarily disabled after a fault has been detected and latched.

The INTB pin is an open-drain, active-low output which is asserted if a fault condition occurs on any of the four ports. This indication is asserted for any of the port faults which result in a code displayed in the port status register (the faults listed in Table 8-8). In auto mode, the fault latch, the status register fault bits, and consequently, INTB assertion, are cleared by expiration of the 750-ms TED timer.

8.4.4 Over and Undervoltage Fault

Over and under voltage faults are only processed after port power up has completed (voltage/power ramp to PD is done). The TPS2384 measures the voltage between the P and N pin and if this voltage drops below

the undervoltage threshold (typically 43 V) or increases above the overvoltage threshold (typically 55 V) the voltage timer is turned on. When the voltage timer reaches its time-out limit that is set between 2 ms to 5 ms the corresponding port is turned off and the UV/OV fault code generated in the Port Status 1 register. If the over and undervoltage condition is removed prior to the voltage timer reaching its limit, the timer is reset and waits for the next event. Figure 8-8 shows a voltage fault lasting for more then 2 ms that has caused the port to shutdown.

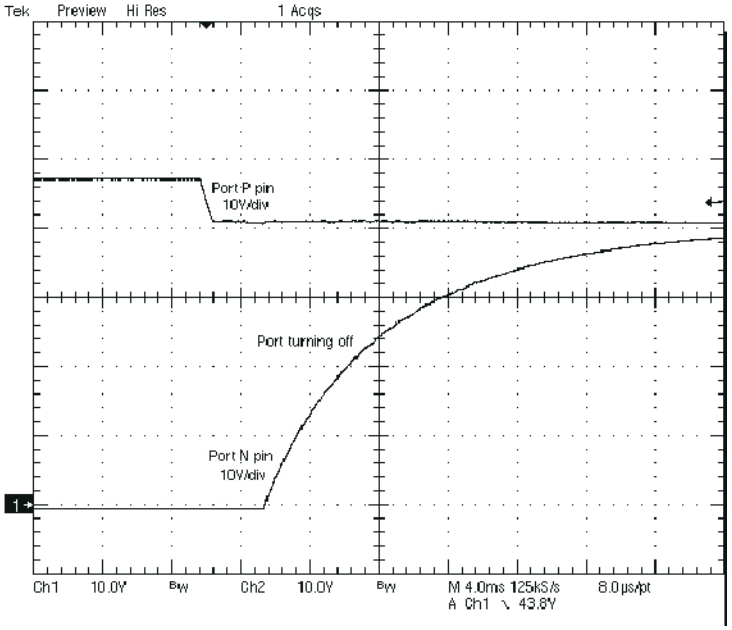


Figure 8-8. Port Turn OFF due to Undervoltage Fault

8.4.5 Over Current or Current Limit Faults

Overcurrent or current limit faults are conditions when the load current that is being sensed trips either the I_{CUT} comparator (350 mA to 400 mA) or the I_{LIM} comparator (400 mA to 450 mA) and turns on the current fault timer. When the overcurrent timer reaches its time out limit that is set between 50 ms to 75 ms the corresponding port is turned off and the over current fault code generated in the Port Status 1 register. If the overcurrent condition goes away prior to the overcurrent timer reaching its limit, the timer is reset and waits for the next event. Figure 8-9 shows an overcurrent fault lasting more than 50 ms that has caused the port to shut off.

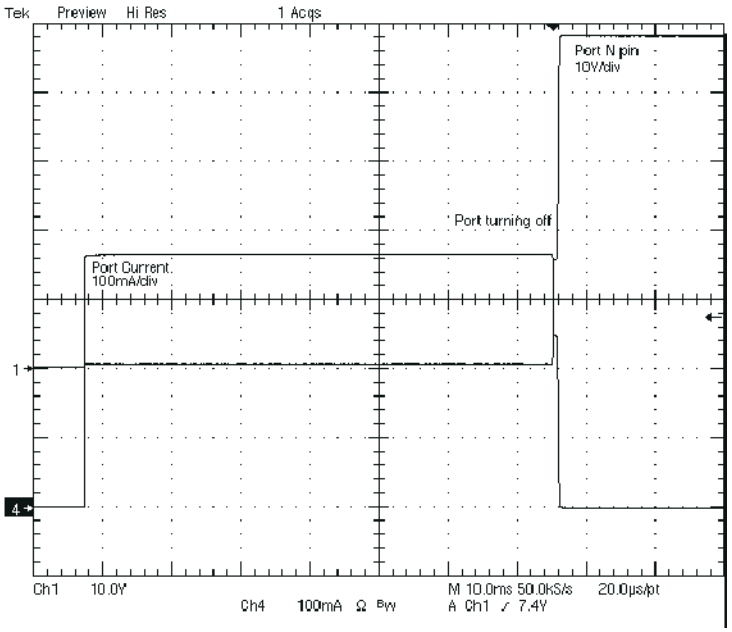


Figure 8-9. Port Overcurrent Response

8.4.6 Undercurrent Fault (DC Modulated Disconnect)

Undercurrent fault (dc modulated disconnect) is a condition when the load current that is being measured drops below 7.5 mA and turns on the disconnect timer. If the disconnect timer reaches its time out limit that is set between 300 ms to 400 ms, the corresponding port is turned off and the load disconnect fault code is generated in the Port Status 1 register. If the undercurrent condition goes away prior to the disconnect timer reaching its limit the timer is reset and the port remains powered.

Figure 8-10 shows DC Disconnect event. In this setup, the load current was set right above the 7.5-mA threshold. The duty cycle of the load was then adjusted until the off period exceeded the disconnect time out, causing turn-off of the port. The time-out period was > 300 ms.

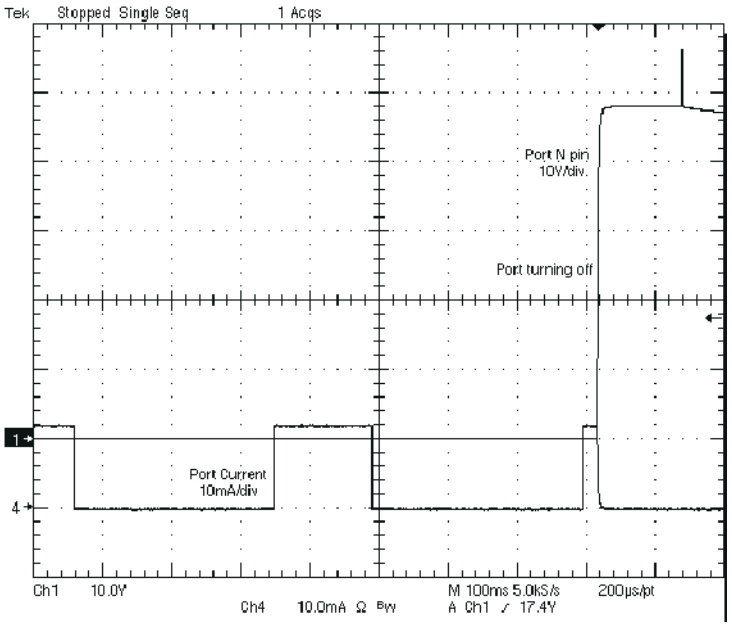


Figure 8-10. Port Undercurrent Response in DC Disconnect

8.4.7 Power Management Mode (PMM)

Power management mode (PMM) has been designed to work efficiently with simple low-cost microcontrollers such as those in the MSP430 family.

The power management mode uses 13 self-contained functions to completely control the device operation. Simply write and read through the I^2C pins and wait for the function done bit to be set. If an A/D measurement was performed during the function, the results can be accessed by going to the read mode and addressing the proper register. Refer to Figure 8-11 for more detail.

8.4.7.1 13 PMM Functions

- **Disable:** Disable the port and reset all functions.
- **Discovery 1:** Enable the Discovery 1 condition which applies a 4.4 V across the PD and measure and store the resulting current.
- **Discovery 2:** Enable the Discovery 2 condition which applies a 8.8 V across the PD and measure and store the resulting current.
- **V Sample:** Measure the voltage between the P and N pins and store the result in the A/D voltage register.
- **Legacy:** Enable the 3.5-mA current source for measuring capacitance and measure the voltage across the P and N terminals and store the result in the A/D voltage register.
- **Classify:** Enable the classification condition which applies 17.7 V across the PD and measure and store the resulting current.
- **Rup Pwr:** Turn on the output switch while controlling the current being delivered to the PD until the PD current needs are met or the max current is reached.
- **C Sample:** Continuous cycle of 31 current measurements and 1 voltage measurement. After each measurement the contents of the appropriate register are updated.
- **Rdwn:** Turn off the output switch while controlling current until output current reaches 0 mA.
- **AC LO:** Turns on low side output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **AC HI:** Turns on high side output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **ISample:** Measure the current and store the result in the A/D current register.
- **TSample:** Measure the internal die temperature and store the result in the A/D temperature register.

Conversion times for A/D measurements performed as part of the functions listed above are generally as shown in the typical values in the Electrical Characteristics table. However, conversion time is somewhat dependant on the magnitude of the input signal being measured. Power management mode applications must take precautions to test the A/D DONE bit (MSB of the high byte) of the pertinent results register before accepting or using the returned value. A logic 1 at this bit location indicates the conversion is complete. Also, after an A/D conversion is in process on a given port, subsequent function calls to that port must wait until the currently executing conversion is complete. Commands written prior to completion can cause the results of the initial conversion to be written to the register of the subsequent function.

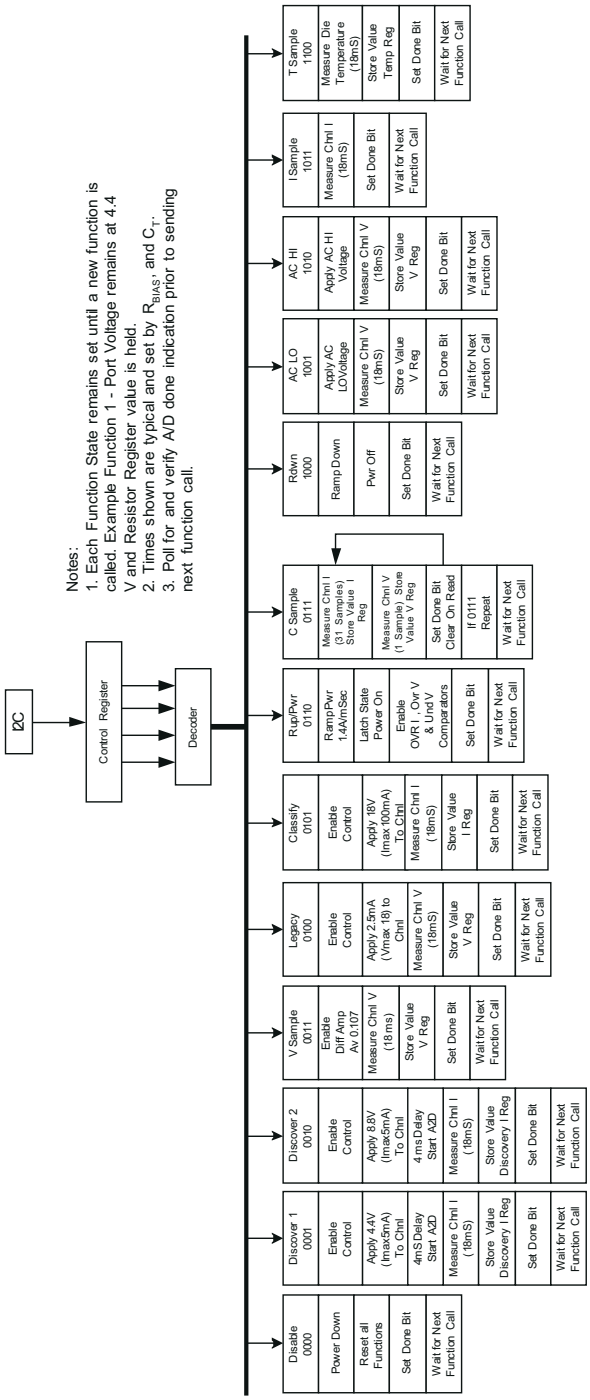


Figure 8-11. Device Process Function Flow

8.4.8 PMM Discovery 1

PMM Discovery 1 function waveforms for the N and CINT pins are shown in Figure 8-12. The measurement is being performed using 25-kΩ impedance between the P and N pin. The Discovery 1 voltage is allowed to settle for approximately 5 ms before the A/D begins integrating. The voltage on the CINT pin shows the A/D cycle. There are four distinct regions to any A/D cycle: precharge (to a known starting voltage), charge, coarse discharge, and fine discharge. CINT pin is very high impedance therefore extreme care must be taken to avoid any noise or leakage affecting this pin. For the measurements where CINT voltage is shown a buffer was used to prevent performance degradation. The A/D measurement time is approximately 18 ms. The entire Discovery 1 function takes approximately 22 ms to complete. At the end of the A/D cycle the Discovery 1 current is stored in the Discovery Current Register and the function done bit is set. The applied Discovery 1 voltage level remains until a new function is called. The data for this measurement remains stored in the Discovery Current Register until another Discovery 1 or 2 function is called.

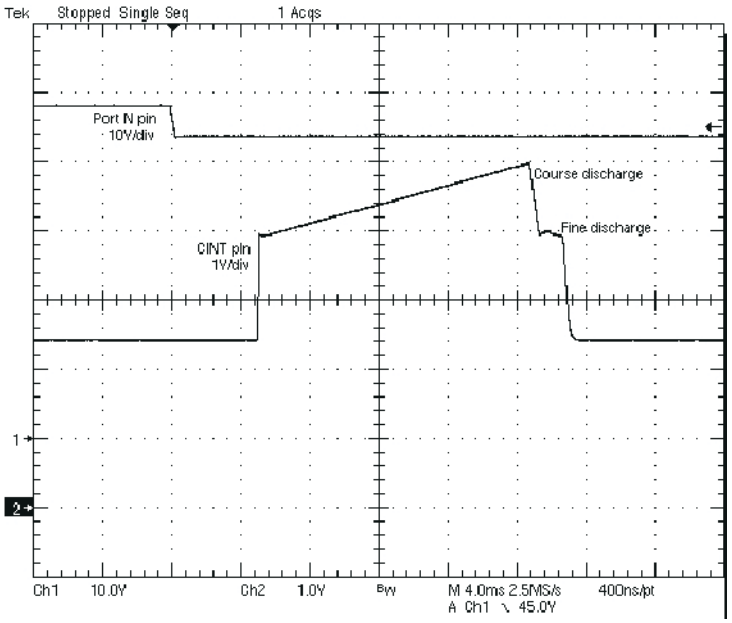


Figure 8-12. Discovery 1 Function Waveforms

8.4.9 PMM Discovery 2

PMM Discovery 2 function waveforms for the N and CINT pins are shown in Figure 8-13. Again the measurement is being performed using 25 kΩ impedance between the P and N pin. The Discovery 2 function was called after a Discovery 1 function so the voltage ramps from 4.4 V to 8.8 V below the P pin. The Discovery 2 voltage is given 5 ms to settle before the A/D begins to integrate. At the end of the A/D cycle the Discovery 2 current is stored in the Port Discovery Current Register and the function done bit is set. The applied Discovery 2 voltage level remains until a new function is called. The data for this measurement remains stored in the Discovery Current Register until another Discovery 1 or 2 function is called.

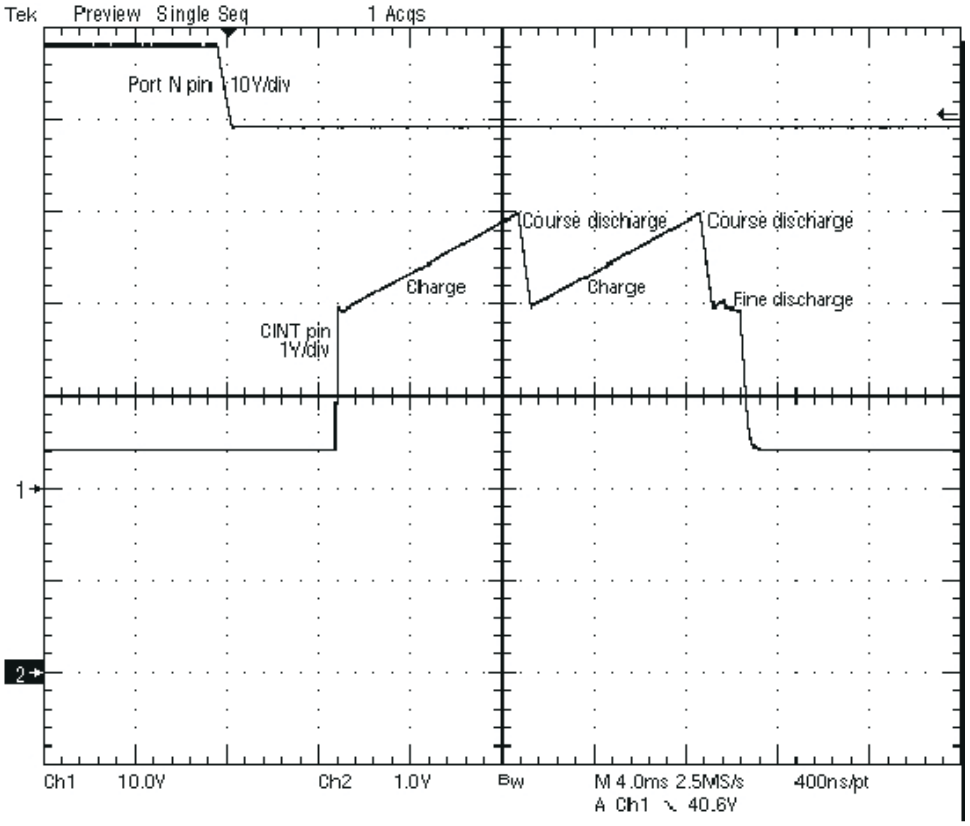


Figure 8-13. Discovery 2 Function Waveforms

8.4.10 PMM Classification

PMM Classification function looks similar to Discovery 1 and 2 except that the voltage between the P and N pins regulates to approximately 17.5 V. At the end of the A/D cycle the classification current is stored in the Port Current Register and the done bit is set. The applied classification level remains until a new function is called. The data for this measurement remains stored in the Port Current Register until either the Classify or Sample function is called.

As indicated in the flow diagram of Figure 8-3, the TPS2384 in AM only performs classification at one port at a time. Similarly, PMM applications must take care to ensure that only one port per device is put into the classification mode at any one time to limit power dissipation in the package.

8.4.11 PMM Legacy

PMM Legacy function is used to detect PDs that are non compliant. Legacy detection uses a current source (typically 3.5 mA) as a test current while the A/D measures the average voltage for approximately 18 ms. The waveform shown in Figure 8-14 is the Legacy function charging a 10-µF capacitor. The capacitance charges to a value that is no greater than 20 V below the P port voltage. As the capacitor is charging the A/D is accumulating counts in the voltage A/D register. Figure 8-15 shows the relationship between port capacitance and the number of counts. A user can characterize non-compliant PD's signatures and use the Legacy function to recognize these devices.

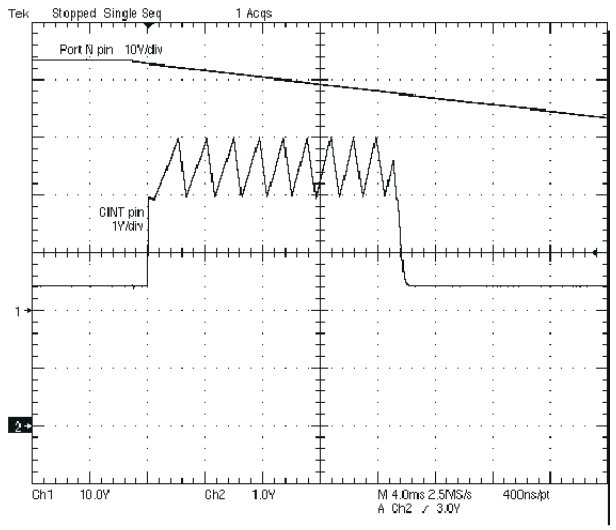


Figure 8-14. Legacy Detection Function Waveforms

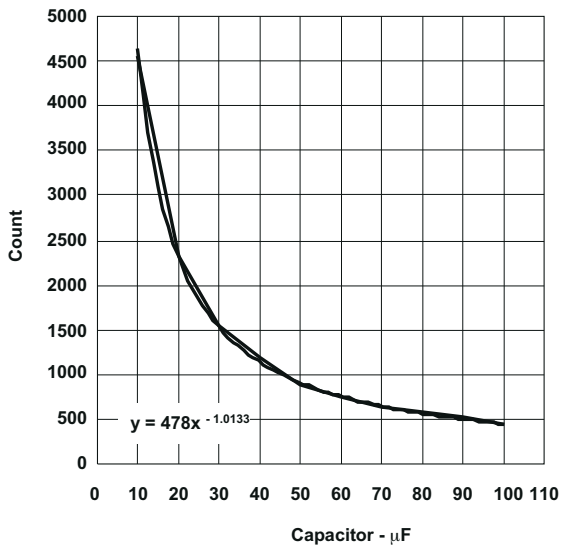


Figure 8-15. A/D Counts vs Legacy Port Capacitance

8.4.12 PMM Rup Pwr

PMM Rup Pwr function turns on the port power by ramping up the current that is being delivered to the load in a controlled fashion. The output current ramps from 0 mA to I_{LIM} (typically 425 mA) in approximately 500 µs. Figure 8-16 shows the output voltage and current turning on for a 250-mA load.

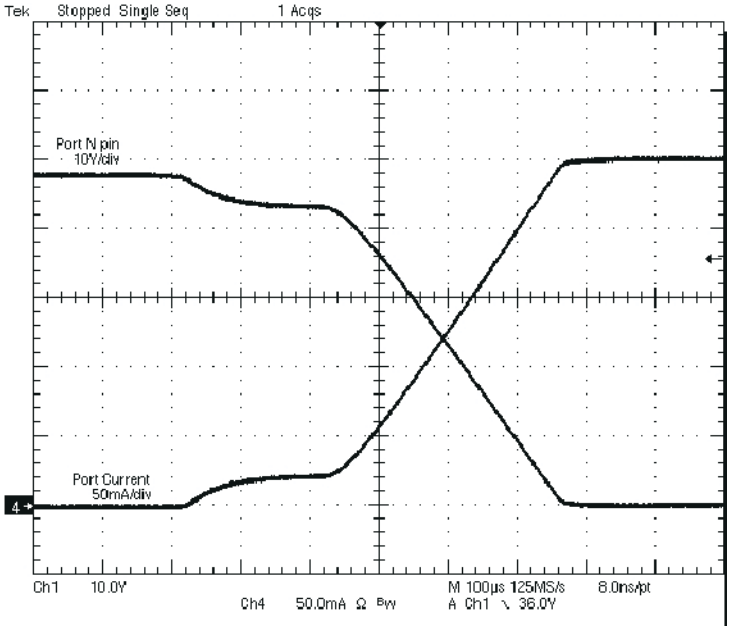


Figure 8-16. Rup Pwr Function Waveforms

8.4.13 PMM R_{DWN}

PMM R_{DWN} function turns off the port power by ramping down the current in a controlled fashion. The output current ramps from I_{LIM} (typically 425 mA) to 0 mA in approximately 300 µs. Figure 8-17 shows the output voltage and current shutting down for a 250-mA load.

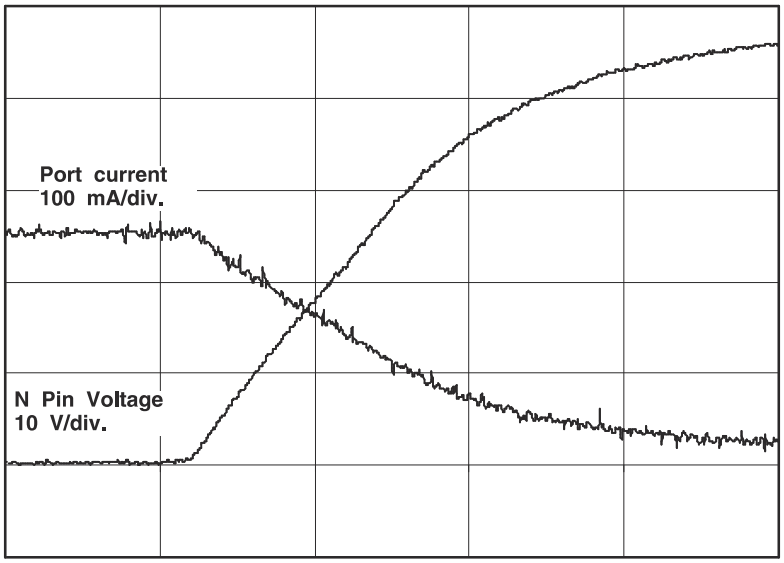


Figure 8-17. Rdwn Function Waveforms

8.5 Programming

8.5.1 I²C Interface Description

The serial interface used in the TPS2384 is a standard 2-wire I²C target architecture. The standard SDA line of the I²C architecture is broken out into independent input and output data paths. This feature simplifies earth grounded controller applications that require opto-isolators to keep the 48-V return of the Ethernet power system floating. For applications where opto-isolation is not required, the bidirectional property of the SDA line can be restored by connecting SDA_I to SDA_O. The SCL line is a unidirectional input only line as the TPS2384 is always accessed as a target device and it never controls the bus.

Data transfers that require a data-flow reversal on the SDA line are 4-byte operations. This occurs during a TPS2384 port read cycle where a target address byte is sent, followed by a port/register address byte write. A second target address byte is sent followed by the data byte read using the port/register setup from the second byte in the sequence.

The I²C interface and the port read write registers are held in active reset until all input voltages are within specifications (V10, V6.3, V3.3 and V2.5) and the internal POR timer has timed out (see electrical specifications).

The I²C read cycle consists of the following steps 1 through 14 and is shown in Figure 8-18:

1. Start Sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Stop
8. Start
9. Device address field
10. Read
11. Acknowledge
12. Data Transfer
13. Acknowledge
14. Stop

Data write transfers to the TPS2384 do not require a data-flow reversal and as such only a 3-byte operation is required. The sequence in this case is to send a target device address byte, followed by a write of the port/register address followed by a write of the data byte for the addressed port.

The I²C write cycle consists of the following steps 1 through 9 and is also shown in Figure 8-18:

1. Start Sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Data for TPS2384
8. Acknowledge
9. Stop

8.5.2 Start and Stop

The high-to-low transition of SDA_I while SCL is high defines the start condition. The low to high transition of SDA_I while SCL is high defines the stop condition. The controller device initiates all start and stop conditions.

The first serial packet is enclosed within start and stop bits, consists of a 7-bit address field, read and write bit, and the acknowledge bit. The acknowledge bit is always generated by the device receiving the address or data field. Five of the seven address bits are used by the TPS2384. The value of the sixth and seventh bit is ignored. (See Note (1) in Table 8-1)

8.5.3 Chip Address

The address field of the TPS2384 is 8 bits long and contains 5 bits of device address select, a read/write bit, and two spare bits per Table 8-1. The five device address select bits follow this plan. These bits are compared against the hard-wired state of the corresponding device address select pins (A1–A5). When the field contents are equivalent to the pin logic states, the device is addressed. These bits are followed by LSB bit, which is used to set the read or write condition (1 for read and 0 for write). Following a start condition and an address field, the TPS2384 responds with an acknowledge by pulling the SDA_O line low during the 9th clock cycle if the address field is equivalent to the value programmed by the pins. The SDA_O line remains a stable low while the 9th clock pulse is high.

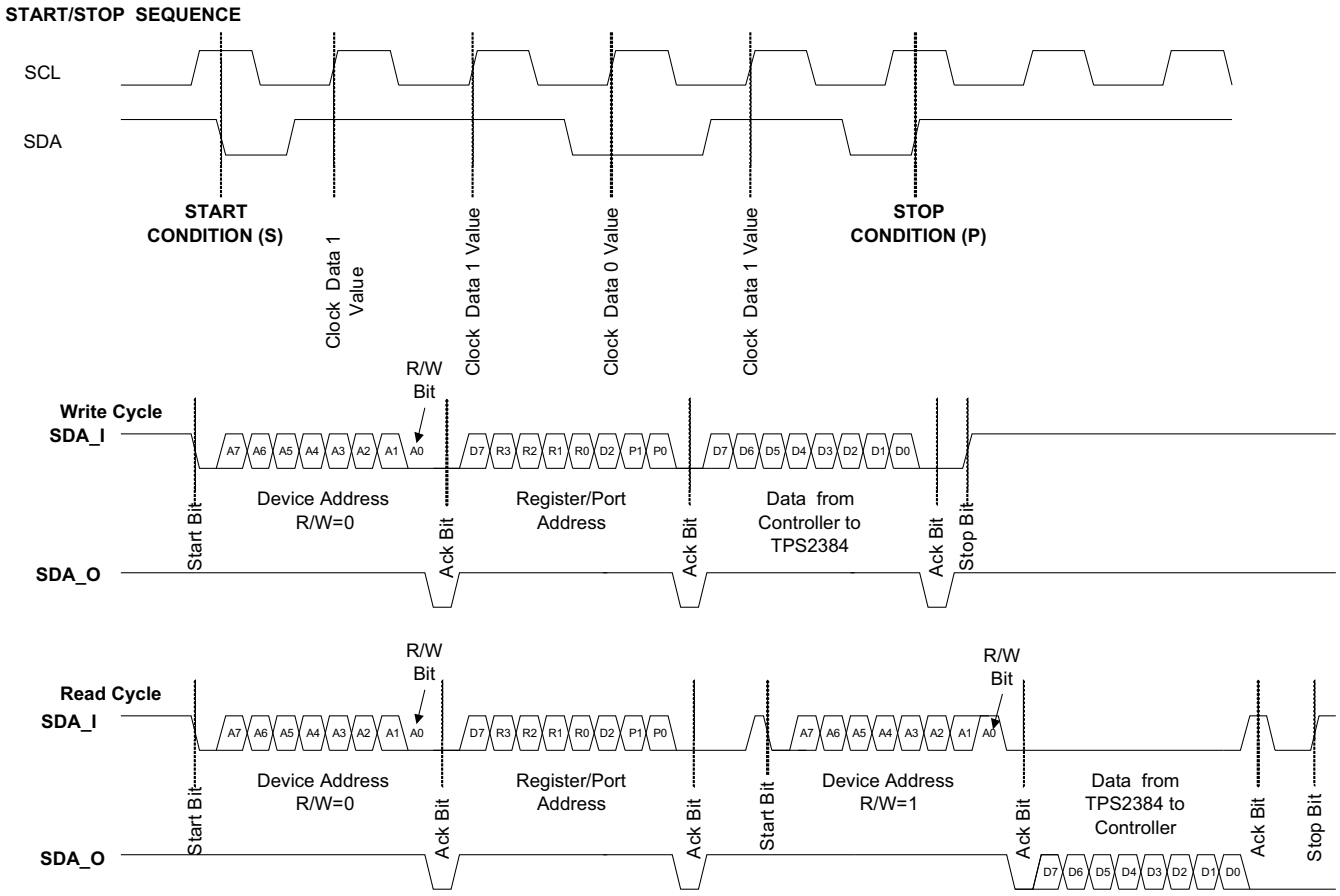


Figure 8-18. I²C Read and Write Cycles

8.5.4 Chip Addressing

Table 8-1 shows the bit assignments during the addressing cycle.

Table 8-1. Address Selection Field

BIT	FUNCTION
A7	Future expansion (value not compared) (1)
A6	Future expansion (value not compared) (1)
A5	Device address. Compared with pin A5.
A4	Device address. Compared with pin A4.
A3	Device address. Compared with pin A3.
A2	Device address. Compared with pin A2.
A1	Device address LSB. Compared with pin A1.
A0	Read/Write

(1) TPS2384 acknowledges four target address values for each setting of A5–A1 (A7,A6 = 00, 01, 10, 11). Target devices sharing the bus with TPS2384must use unique A5-A1 values not matching those of the TPS2384.

8.5.5 Data Write Cycle

For a data write sequence, after the Port/Register address cycle, the TPS2384 accepts the eight bits of data as defined in the tables below. The data is latched into the previously selectedWrite Register, and the TPS2384 generates a data acknowledge pulse by pulling the SDA_O line low for one clock cycle. Common register functions act on all ports simultaneously. Per port registers are specific to the target port only.

To reset the interface, the host or controller subsequently generates a stop bit by releasing the SDA_I line during the clock-high portion of an SCL pulse.

8.5.6 Port and Register Cycle

After the chip address cycle, the TPS2384 accepts eight bits of port and register select data as defined in Table 8-2. The SCL line high-to-low transition after the eighth data bit then latches the selection of the appropriate internal register for the follow-on data read or write operation. After latching the eight-bit data field, the TPS2384 pulls the SDA_O line low for one clock cycle, for the acknowledge pulse.

8.5.7 Data Read Cycle

For a data read sequence, after the register acknowledge bit, the controller device generates a stop condition. This action is followed by a second start condition, and retransmitting the device address as described in chip address above. For this cycle, however, the R/W bit is set to a 1 to signal the read operation. The TPS2384 again responds with an acknowledge pulse. The address acknowledge is then followed by sequentially presenting each of the eight data bits on the SDA_O line (MSB first), to be read by the host device on the rising edges of SCL. After eight bits are transmitted, the host acknowledges by pulling the SDA_I line high for one clock pulse. The completed data transfer is terminated with the host generating a stop condition.

8.6 Register Maps

8.6.1 Register/Port Addressing Map

Figure 8-17. Register/Port Addressing Map

7	6	5	4	3	2	1	0
Unused	Register select MSB	Register select Bit 2	Register select Bit 1	Register select LSB	Unused	Port address MSB	Port address LSB
	R/W	R/W	R/W	R/W		R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-2. Register/Port Addressing Map

Bit	Field	Type	Reset	Description
D7	Unused		0	0
D6	Register select MSB	R/W	0000	0000 = Common Read — Port fault status, chip ID and rev. 0001 = Common Control Write — Software reset, ports disable and AC Disc. 0010 = Port Control Write 1 — Function calls; misc. fault disables 0011 = Port Control Write 2 — Port enable; A/D control 0100 = Port Status Read 1 — Fault status; device Class info. 0101 = Port Status Read 2 — Function and other status 0110 = Discovery Current – Lower Bits — A/D resistance results 0111 = Discovery Current – Upper Bits — A/D resistance results 1000 = Voltage – Lower Bits – A/D voltage results 1001 = Voltage – Upper Bits — A/D voltage results 1010 = Current – Lower Bits — A/D current results 1011 = Current – Upper Bits — A/D current results 1100 = Temperature – Lower Bits — A/D temperature results 1101 = Temperature – Upper Bits — A/D temperature results 1110 = unused 1111 = Common Write – Test mode selections — timer disables, discovery control, etc.
D5	Register select Bit 2	R/W		
D4	Register select Bit 1	R/W		
D3	Register select LSB	R/W		
D2	Unused		0	0
D1	Port address MSB	R/W	00	00 = port 1 01 = port 2 10 = port 3 11 = port 4
D0	Port address LSB	R/W		

8.6.2 Common Read, Register Select

Figure 8-18. Common Read, Register Select = 0000

7	6	5	4	3	2	1	0
Port 4 general Fault status	Port 3 general Fault status	Port 2 general Fault status	Port 1 general Fault status	Chip rev		Chip ID	
	R	R	R	R		R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-3. Common Read, Register Select = 0000

Bit	Field	Type	Reset	Description
D7	Port 4 general Fault status	R	0	0 = no fault 1 = port fault(1) (2)
D6	Port 3 general Fault status	R	0	0 = no fault 1 = port fault(1) (2)
		R	0	0 = no fault 1 = port fault (1) (2)
D5	Port 2 general Fault status	R	0	0 = no fault 1 = port fault (1) (2)
D4	Port 1 general Fault status	R		
D3	Chip rev	R	Varies	00 = rev -- 01 = rev 1 10 = rev 2 11 = rev 3
D2				
D1	Chip ID	R	10	00 = TPS23841 01= future use 10 = TPS2384 11 = reserved
D0				

(1) PMM faults cleared by Disable function.
(2) AM faults cleared by TED timer.

8.6.3 Common Write, Register Select = 1111 (Test Register)

Figure 8-19. Common Write, Register Select = 1111 (Test Register)

7	6	5	4	3	2	1	0
Unused	Thermal shutdown test	POR disable	Discovery timers	Discovery 1 and 2	DC Disconnect timer	TED timer	Unused
	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-4. Common Write, Register Select = 1111 (Test Register)(1)

Bit	Field	Type	Reset	Description
D7	Unused		0	0
D6	Thermal shutdown test	R/W	0	0 = normal operation 1 = force TSD condition (all ports off)
D5	POR disable	R/W	0	0 = normal POR timing 1 = force POR to a non-reset state
D4	Discovery timers	R/W	0	0 = normal (4-ms Discovery 1 and Discovery 2) 1 = timers disable
D3	Discovery 1 and 2	R/W	0	0 = normal operation 1 = all 4-port Discovery 1 and Discovery 2 – halt
D2	DC Disconnect timer	R/W	0	0 = DC Disconnect timer between 300 ms to 400 ms for loads less than 5 mA (IEEE standard) 1 = DC Disconnect timer 0 ms for loads less than 5 mA
D1	TED timer	R/W	0	0 = normal operation 1 = 750-ms TED timer disable
D0	Unused		0	0

(1) Test mode select; not intended for end--application use.

8.6.4 Common Control Write, Register Select = 0001

Figure 8-20. Common Control Write, Register Select = 0001

7	6	5	4	3	2	1	0
Unused	Unused	Thermal shutdown	AC high	AC low	Port over/under voltage faults	All ports disable	Software RESET
		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-5. Common Control Write, Register Select = 0001

Bit	Field	Type	Reset	Description
D7	Unused		0	0
D6	Unused		0	0
D5	Thermal shutdown fault(1)	R/W	0	0 = active 1 = disable
D4	AC high	R/W	0	0 = off 1 = AC_HI driver on
D3	AC low	R/W	0	0 = off 1 = AC_LO driver on
D2	Port over/under voltage faults	R/W	0	0 = active 1 = disable
D1	All ports disable(2)	R/W	0	0 = normal operation 1 = all ports shut down (no ramp)
D0	Software RESET	R/W	0	0 = normal operation 1 = reset all circuits and start a POR timing cycle

(1) Register 0001, bit D5 operation inhibited after device probe.
(2) Refer to (SLUZ014) for Alternative B, semi-auto mode implementations which write to bit D1.

8.6.5 Port Control Write 1, Register Select = 0010 (One Per Port)

Figure 8-21. Port Control Write 1, Register Select = 0010 (One Per Port)

7	6	5	4	3	2	1	0
Unused	Unused	Discovery fault disable	DC Disconnect disable	Function Bit 3	Function Bit 2	Function Bit 1	Function Bit 0
		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-6. Port Control Write 1, Register Select = 0010 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Unused		0	0
D6	Unused		0	0
D5	Discovery fault disable	R/W	0	0 = normal operation 1 = disable internal discovery fault limits (19 kΩ to 29.5 kΩ)
D4	DC Disconnect disable	R/W	0	0 = DC Disconnect active 1 = DC Disconnect disable (for AC Disconnect)
D3	Function Bit 3	R/W	0000	0000 = Disable function (power down and reset all functions) 0001 = Discovery 1 function 0010 = Discovery 2 function 0011 = port voltage sample function (V sample) 0100 = legacy detection function 0101 = classification function 0110 = ramp up/power function (rup pwr) 0111 = continuous sample function (C sample) 1000 = ramp power down function (Rdwn) 1001 = ac low 1010 = ac high 1011 = port current sample function (I sample) 1100 = die temperature sample function (T sample) 1101 = spare 1110 = spare 1111 = spare
D2	Function Bit 2	R/W		
D1	Function Bit 1	R/W		
D0	Function Bit 0	R/W		

8.6.6 Port Control Write 2, Register Select = 0011 (One Per Port)

Figure 8-22. Port Control Write 2, Register Select = 0011 (One Per Port)

7	6	5	4	3	2	1	0
Unused	Unused	Unused	Port Enable	A/D Start	A/D Abort	Unused	Unused
			R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-7. Port Control Write 2, Register Select = 0011 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Unused		0	0
D6	Unused		0	0
D5	Unused		0	0
D4	Port Enable(1)	R/W	0	0 = normal 1 = port disable
D3	A/D Start	R/W	0	0 = normal 1 = start A/D (self clearing)
D2	A/D Abort	R/W	0	0 = normal 1 = abort
D1	Unused		0	0
D0	Unused		0	0

(1) Refer to (SLUZ014) for Alternative B, semi-auto mode implementations which write to bit D4.

8.6.7 Port Status Read 1, Register Select = 0100 (One Per Port)

Figure 8-23. Port Status Read 1, Register Select = 0100 (One Per Port)

7	6	5	4	3	2	1	0
Discovery Status	Function Done Bit	Port Class			Fault status (MSB)	Fault status	Fault status (LSB)
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-8. Port Status Read 1, Register Select = 0100 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Discovery Status	R	0	0 = normal 1 = discovery fail
D6	Function Done Bit	R	0	0 = normal 1 = function complete (self clearing by a new function write)
D5	Port Class	R	000	000 = class 0 001 = class 1 010 = class 2 011 = class 3 100 = class 4
D4	Port Class	R		
D3	Port Class	R		
D2	Fault status (MSB)	R	000	000 = no faults 001 = UV/OV fault 010 = thermal shutdown fault (TSD) 011 = overload current > 50-ms fault 100 = load disconnect 101 = reserved for future 110 = reserved for future 111 = reserved for future
D1	Fault status	R		
D0	Fault status (LSB)	R		

8.6.8 Port Status Read 2, Register Select = 0101 (One Per Port)

Figure 8-24. Port Status Read 2, Register Select = 0101 (One Per Port)

7	6	5	4	3	2	1	0
Unused	Unused	Unused	Watch dog timer	A/D status	Function status (MSB)	Function status	Function status (LSB)
			R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-9. Port Status Read 2, Register Select = 0101 (One Per Port)

Bit	Field	Type	Reset	Description
D7			0	0
D6	Unused		0	0
D5	Unused		0	0
D4	Watch dog timer	R	0	0 = not active 1 = active
D3	A/D status	R	0	0 = not active 1 = active (conversion in process)
D2	Function status (MSB)	R	000	000 = disabled 001 = searching 010 = power delivery 011 = fault 100 = test 101 = other fault 110 = undefined 111 = undefined
D1	Function status	R		
D0	Function status (LSB)	R		

8.6.9 A/D Results Registers (Discovery Current, Voltage, Current and Temperature)

8.6.9.1 Discovery Current — Lower Bits, Register Select = 0110 (One Per Port)

Figure 8-25. Discovery Current — Lower Bits, Register Select = 0110 (One Per Port)

7	6	5	4	3	2	1	0
A/D bit 7	A/D bit 6	A/D bit 5	A/D bit 4	A/D bit 3	A/D bit 2	A/D bit 1	A/D bit 0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-10. Discovery Current — Lower Bits, Register Select = 0110 (One Per Port)

Bit	Field	Type	Reset	Description
D7	A/D bit 7	R	0	A/D lower bits
D6	A/D bit 6	R		
D5	A/D bit 5	R		
D4	A/D bit 4	R		
D3	A/D bit 3	R		
D2	A/D bit 2	R		
D1	A/D bit 1	R		
D0	A/D bit 0	R		

8.6.9.2 Discovery Current — Upper Bits, Register Select = 0111 (One Per Port)

Figure 8-26. Discovery Current — Upper Bits, Register Select = 0111 (One Per Port)

7	6	5	4	3	2	1	0
Resistor measurement complete	A/D bit 14	A/D bit 13	A/D bit 12	A/D bit 11	A/D bit 10	A/D bit 9	A/D bit 8
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-11. Discovery Current — Upper Bits, Register Select = 0111 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Resistor measurement complete	R	0	0 = measurement active (bit set low at the start of Discovery 1 or Discovery 2) 1 = measurement complete (bit set high after A/D is completed during Discovery 1 or Discovery 2)
D6	A/D bit 14	R	0	A/D upper bits
D5	A/D bit 13	R		
D4	A/D bit 12	R		
D3	A/D bit 11	R		
D2	A/D bit 10	R		
D1	A/D bit 9	R		
D0	A/D bit 8	R		

8.6.9.3 Voltage — Lower Bits, Register Select = 1000 (One Per Port)

Figure 8-27. Voltage — Lower Bits, Register Select = 1000 (One Per Port)

7	6	5	4	3	2	1	0
A/D bit 7	A/D bit 6	A/D bit 5	A/D bit 4	A/D bit 3	A/D bit 2	A/D bit 1	A/D bit 0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-12. Voltage — Lower Bits, Register Select = 1000 (One Per Port)

Bit	Field	Type	Reset	Description
D7	A/D bit 7	R	0	A/D lower bits
D6	A/D bit 6	R		
D5	A/D bit 5	R		
D4	A/D bit 4	R		
D3	A/D bit 3	R		
D2	A/D bit 2	R		
D1	A/D bit 1	R		
D0	A/D bit 0	R		

8.6.9.4 Voltage — Upper Bits, Register Select = 1001 (One Per Port)

Figure 8-28. Voltage — Upper Bits, Register Select = 1001 (One Per Port)

7	6	5	4	3	2	1	0
Voltage measurement complete	A/D bit 14	A/D bit 13	A/D bit 12	A/D bit 11	A/D bit 10	A/D bit 9	A/D bit 8
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-13. Voltage — Upper Bits, Register Select = 1001 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Voltage measurement complete	R	0	0 = measurement active (bit set low when A/D begins a voltage measurement) 1 = measurement complete (bit set high after A/D has completed a voltage measurement)
D6	A/D bit 14	R	0	A/D upper bits
D5	A/D bit 13	R		
D4	A/D bit 12	R		
D3	A/D bit 11	R		
D2	A/D bit 10	R		
D1	A/D bit 9	R		
D0	A/D bit 8	R		

8.6.9.5 Current — Lower Bits, Register Select = 1010 (One Per Port)

Figure 8-29. Current — Lower Bits, Register Select = 1010 (One Per Port)

7	6	5	4	3	2	1	0
A/D bit 7	A/D bit 6	A/D bit 5	A/D bit 4	A/D bit 3	A/D bit 2	A/D bit 1	A/D bit 0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-14. Current — Lower Bits, Register Select = 1010 (One Per Port)

Bit	Field	Type	Reset	Description
D7	A/D bit 7	R	0	A/D lower bits
D6	A/D bit 6	R		
D5	A/D bit 5	R		
D4	A/D bit 4	R		
D3	A/D bit 3	R		
D2	A/D bit 2	R		
D1	A/D bit 1	R		
D0	A/D bit 0	R		

8.6.9.6 Current — Upper Bits, Register Select = 1011 (One Per Port)

Figure 8-30. Current — Upper Bits, Register Select = 1011 (One Per Port)

7	6	5	4	3	2	1	0
Current measurement complete	A/D bit 14	A/D bit 13	A/D bit 12	A/D bit 11	A/D bit 10	A/D bit 9	A/D bit 8
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-15. Current — Upper Bits, Register Select = 1011 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Current measurement complete	R	0	0 = measurement active (bit set low when A/D begins a current measurement) 1 = measurement complete (bit set high after A/D has completed a current measurement)
D6	A/D bit 14	R	0	
D5	A/D bit 13	R		
D4	A/D bit 12	R		
D3	A/D bit 11	R		
D2	A/D bit 10	R		
D1	A/D bit 9	R		
D0	A/D bit 8	R		

8.6.9.7 Temperature — Lower Bits, Register Select = 1100 (One Per Port)

Figure 8-31. Temperature — Lower Bits, Register Select = 1100 (One Per Port)

7	6	5	4	3	2	1	0
A/D bit 7	A/D bit 6	A/D bit 5	A/D bit 4	A/D bit 3	A/D bit 2	A/D bit 1	A/D bit 0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-16. Temperature — Lower Bits, Register Select = 1100 (One Per Port)

Bit	Field	Type	Reset	Description
D7	A/D bit 7	R	0	A/D lower bits
D6	A/D bit 6	R	0	
D5	A/D bit 5	R	0	
D4	A/D bit 4	R	0	
D3	A/D bit 3	R	0	
D2	A/D bit 2	R	0	
D1	A/D bit 1	R	0	
D0	A/D bit 0	R	0	

8.6.9.8 Temperature — Upper Bits, Register Select = 1101 (One Per Port)

Figure 8-32. Temperature — Upper Bits, Register Select = 1101 (One Per Port)

7	6	5	4	3	2	1	0
Temperature measurement complete	A/D bit 14	A/D bit 13	A/D bit 12	A/D bit 11	A/D bit 10	A/D bit9	A/D bit 8
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8-17. Temperature — Upper Bits, Register Select = 1101 (One Per Port)

Bit	Field	Type	Reset	Description
D7	Temperature measurement complete	R	0	0 = measurement active (bit set low when A/D begins a temperature measurement) 1 = measurement complete (bit set high after A/D has completed a temperature measurement)
D6	A/D bit 14	R	0	A/D upper bits
D5	A/D bit 13	R		
D4	A/D bit 12	R		
D3	A/D bit 11	R		
D2	A/D bit 10	R		
D1	A/D bit 9	R		
D0	A/D bit 8	R		

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS2384 is a quad-port PSEPM that can be used in simple, low port count, automatic or high port count micro-controller managed applications.

9.1.1 AC Disconnect Drive Circuit Detail

TPS2384 AC_HI and AC_LO can be used with the port generator drive circuit shown in Figure 9-1 for up to 16 ports. Detailed component specifications can be found in the TPS2384EVM User Guide (*TPS2384 Evaluation Module* user's guide).

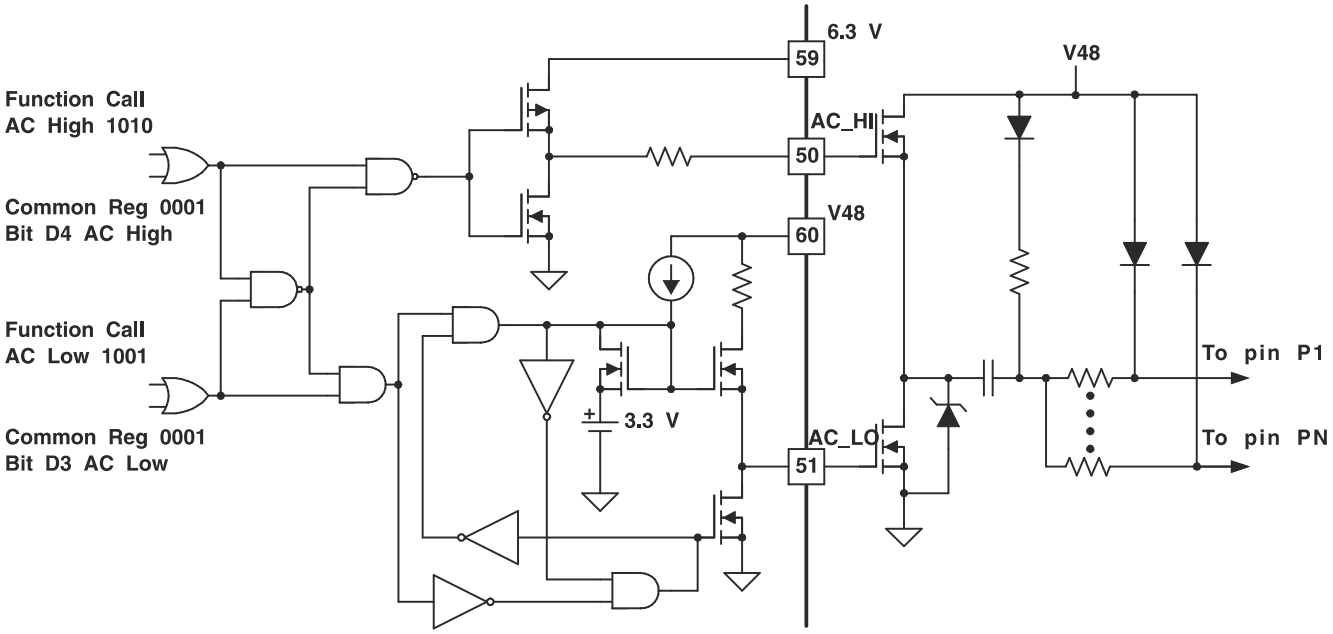


Figure 9-1. AC_HI and LOW Without External FET Configurations

9.1.2 Connection of Unused Ports and Pins

The TPS2384 can be used on applications needing only 1 to 4 ports. For unused ports follow the guidelines shown in *Opto-Isolator Selection Guidelines: TPS2384 I 2C Interface* application note.

9.1.3 Opto-isolator Interface

The TPS2384 can be used in applications requiring digital isolation of the I^2C signals. The detailed design procedure and component selection can be found in *Opto-Isolator Selection Guidelines: TPS2384 I 2C Interface* application note.

9.1.4 Port Protection from Electrical Transients

Detailed design procedure and component selection for electrical transient protection of ports can be found in *Electrical Transient Immunity for Power-Over-Ethernet* application note.

9.2 Typical Application

This section provides a typical application example for a four port PSE system. The detailed schematic for a basic 4 PORT (PMM) isolated configuration with AC Disconnect is shown in Figure 9-2 (PAP pinout shown).

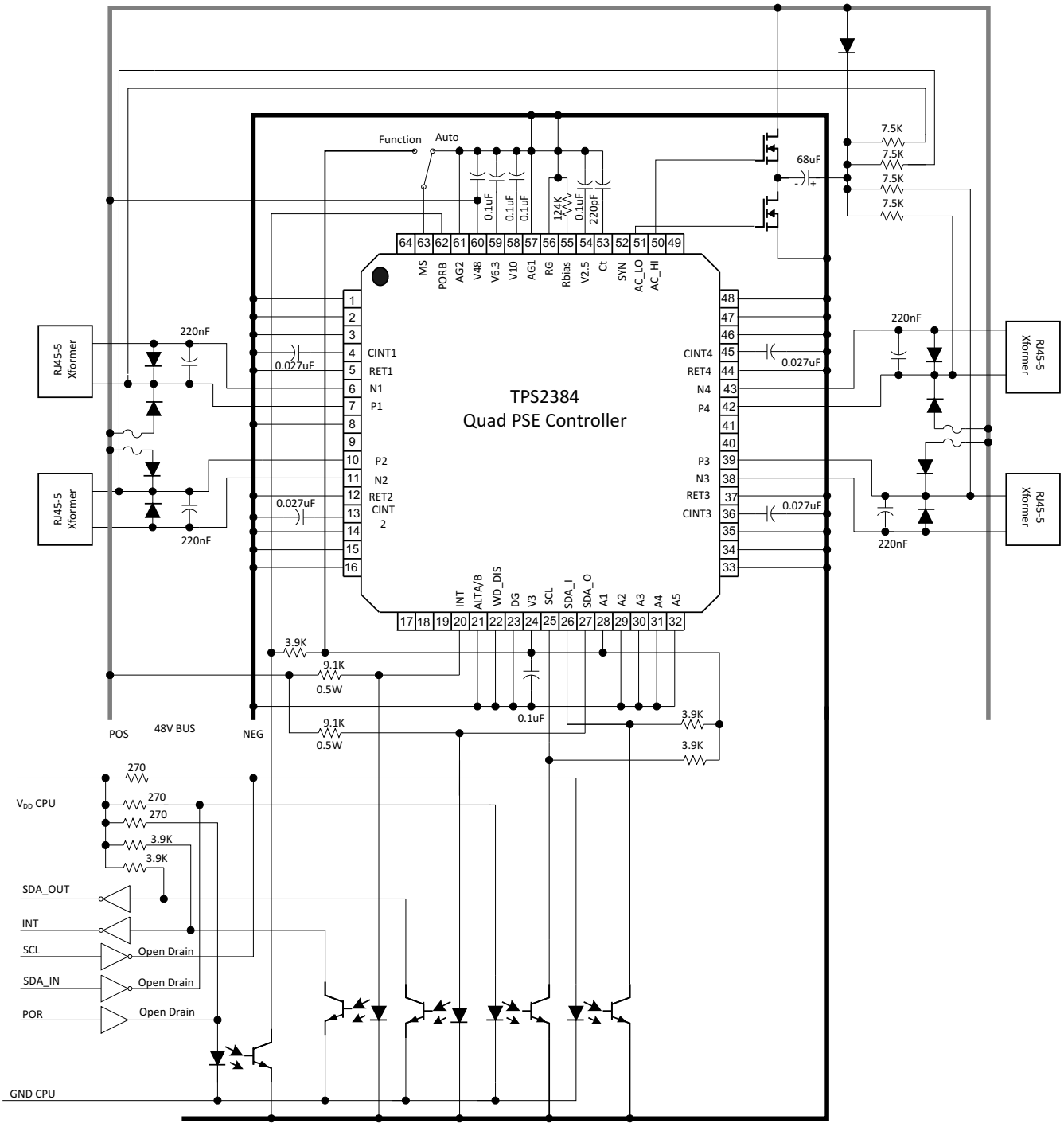


Figure 9-2. Basic 4 PORT (PMM) Isolated Configuration with AC Disconnect

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input voltage	48 V ±3 V
Input current	1.52 A ±0.1 A (fully loaded ports)
Number of ports	4
Other requirements	AC Disconnect Detection

9.2.2 Detailed Design Procedure

9.2.2.1 Power Pin Bypass Capacitors

- V48: Connect a 0.1-µF, 100-V, X7R ceramic capacitor from V48 to AG1 as close to the device as possible.
- V10: Connect a 0.1-µF, 25-V, X7R ceramic capacitor from V10 to AG1 as close to the device as possible.
- V6.3: Connect a 0.1-µF, 10-V, X7R ceramic capacitor from V6.3 to AG1 as close to the device as possible.
- V3.3: Connect a 0.1-µF, 10-V, X7R ceramic capacitor from V3.3 to DG as close to the device as possible.
- V2.5: Connect a 0.1-µF, 10-V, X7R ceramic capacitor from V2.5 to RG as close to the device as possible.

9.2.2.2 Per Port Components

- Port capacitor: Connect a 220 nF–470 nF, 100-V, X7R ceramic capacitor from Px to Nx.
- Fuse: The port fuse must be a slow blow type rated for at least 60 VDC and 1 A. A resettable Polyfuse can also be used.
- Protection Diodes: The port TVS must be rated for the expected port surge environment. The TVS must have a minimum reverse standoff voltage of 58 V and a maximum clamping voltage of 95 V at the expected peak surge current. The negative clamp diode must be rated for V_R = 100-V minimum and be able to survive the expected negative surge current. Low forward voltage drop at the rated current is essential.
- Integration capacitor: Connect a 0.027-µF, 16-V minimum, polycarbonate, poly-polypropylene, polystyrene, teflon, or other low leakage capacitor from CINTx to RG as close to the device as possible.

9.2.2.3 Bias and Timing

- Bias resistor: Connect a 124-kΩ, 1/16W, 1% chip resistor from RBIAS to RG as close to the device as possible.
- Timing Capacitor: Connect a 220-pF, 25-V, COG, 2% ceramic capacitor from CT to RG as close to the device as possible.

9.2.3 Application Curves

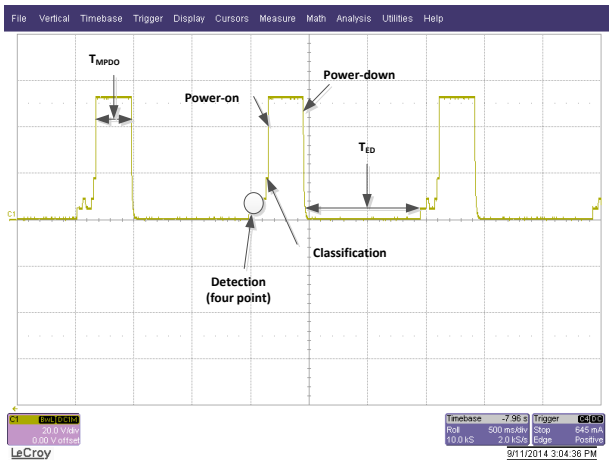


Figure 9-3. Good Detect, Class, Power On, Followed by Undercurrent Disconnect

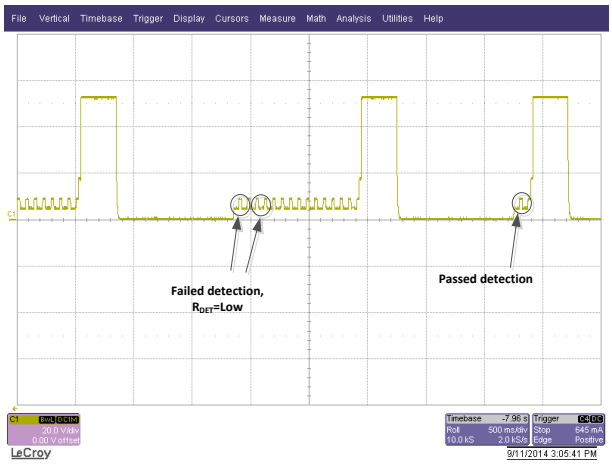


Figure 9-4. Marginal Detect, Class, Power On Followed by Undercurrent Disconnect

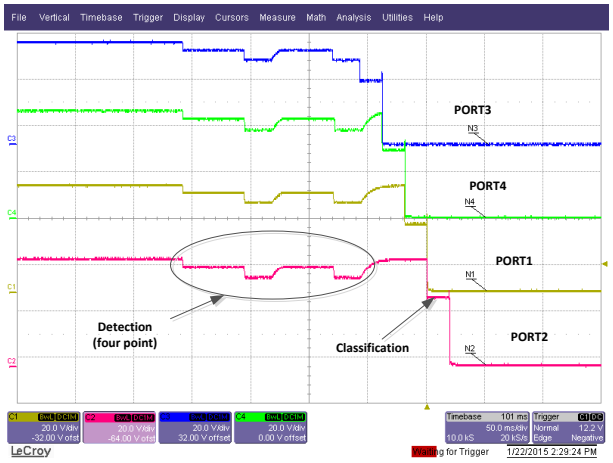


Figure 9-5. Four Port Power-on Sequence After TPS2384 POR Pin De-assertion

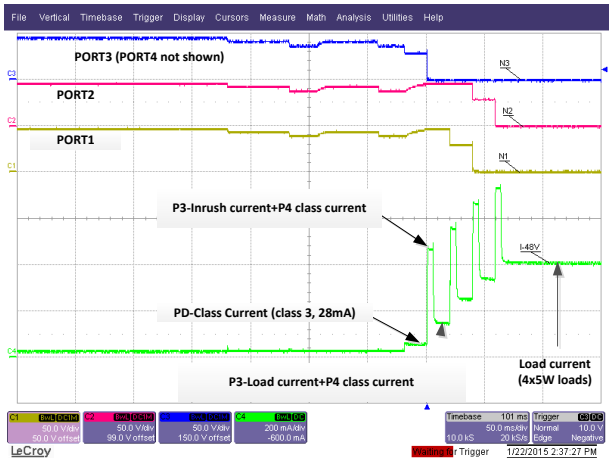


Figure 9-6. 48-V Supply Current During Four Port Startup Sequence (After POR Pin De-assertion)

10 Power Supply Recommendations

The recommended V48 supply voltage requirement is 44 V to 57 V. A power supply with a nominal 48-V output can support type 1 PD requirements. The output current required from the V48 supply depends on the number of ports required in the system. ICUT for a type 1 port is 375 mA ±25 mA. Size the V48 supply accordingly for the number of ports to be supported.

The V3.3 digital supply can be used externally for light loads less than 3 mA.

11 Layout

11.1 Layout Guidelines

11.1.1 Local Circuits

- V48: Place the V48 capacitor from V48 to AG1 as close to the device as possible.
- V10: Place the V10 capacitor from V10 to AG1 as close to the device as possible.
- V6.3: Place the V6.3 capacitor from V6.3 to AG1 as close to the device as possible.
- V3.3: Place the V3.3 capacitor from V3.3 to DG as close to the device as possible.
- V2.5: Place the V2.5 capacitor from V2.5 to RG as close to the device as possible.
- RBIAS: Place the RBIAS resistor from RBIAS to RG on PCB topside as close to the device as possible.
- CT: Place the CT capacitor from CT to RG on PCB topside as close to the device as possible.
- CINTx: Place the CINTx capacitors from CINTx to RG on PCB topside as close to the device as possible.

11.1.2 System Protection Circuits

These circuits include the per-port capacitor, fuse, protection diodes, common mode filtering (ferrite beads or chokes), Bob Smith terminations and AC disconnect generator components. Detailed layout and placement guidelines can be found in *Electrical Transient Immunity for Power-Over-Ethernet* application note.

11.2 Layout Example

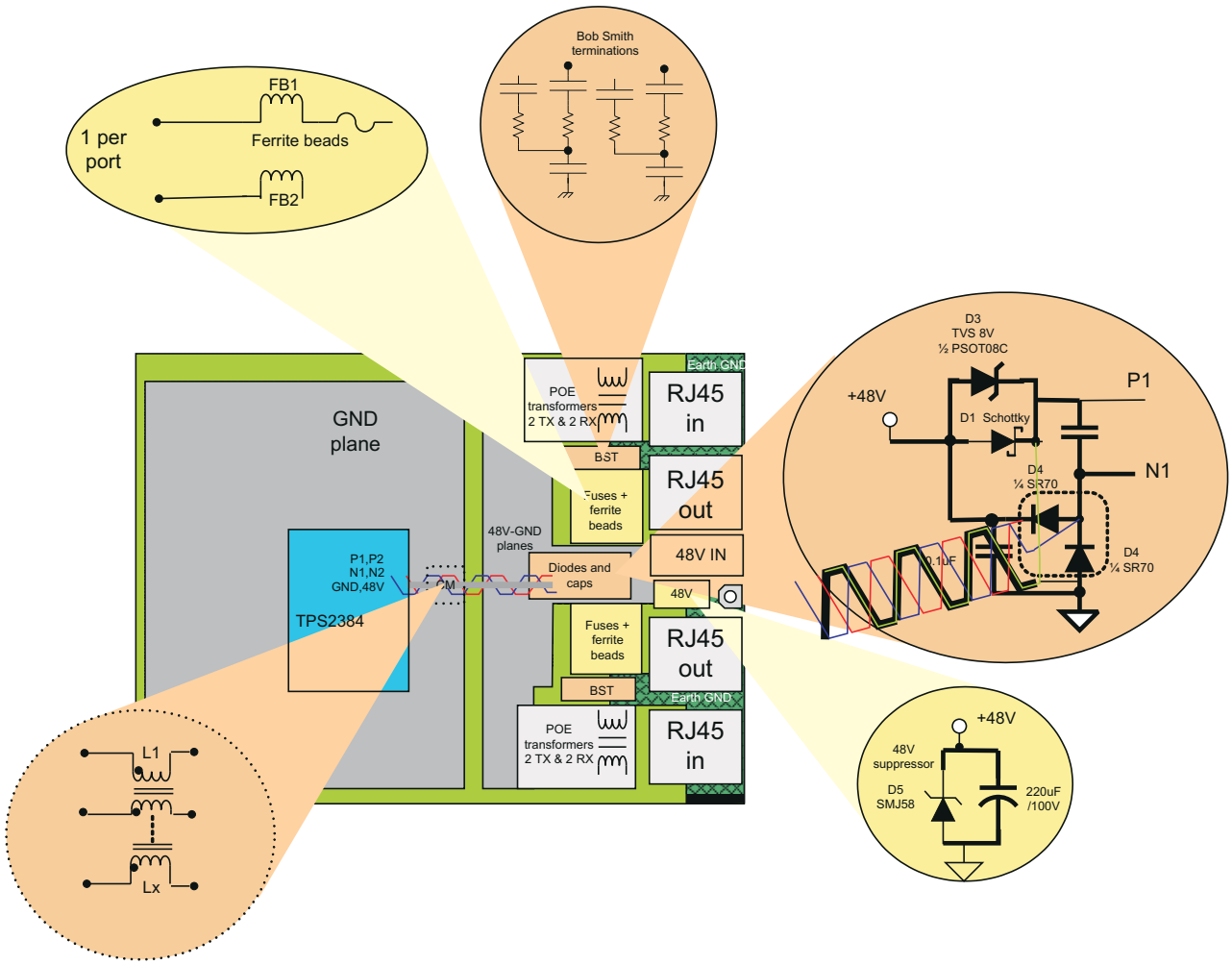


Figure 11-1. Layout

11.3 Thermal Consideration

Ensure proper thermal management of TPS2384 by following the example board layout guidelines provided in the *Mechanical, Packaging, and Orderable Information* section.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *Opto-Isolator Selection Guidelines: TPS2384 I 2C Interface* application note

Texas Instruments, *Proper Termination of Unused Port Connections* application note

Texas Instruments, *Electrical Transient Immunity for Power-Over-Ethernet* application note

Texas Instruments, *TPS2384 Power Sourcing Equipment Power Manager Device Errata* errata

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2384PAP	ACTIVE	HTQFP	PAP	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2384PAP	Samples
TPS2384PAPG4	ACTIVE	HTQFP	PAP	64	160	TBD	Call TI	Call TI	-40 to 125		Samples
TPS2384PAPR	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2384PAP	Samples
TPS2384PAPRG4	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2384PAP	Samples
TPS2384PJD	ACTIVE	HTQFP	PJD	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2384PJD	Samples
TPS2384PJDR	ACTIVE	HTQFP	PJD	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS2384PJD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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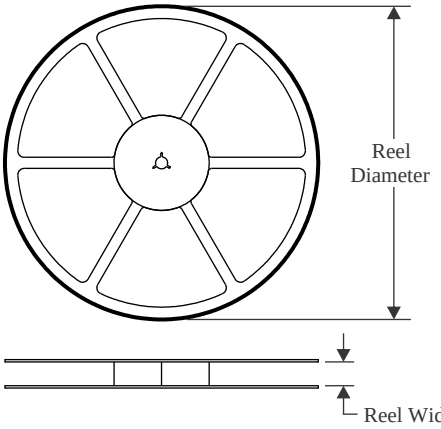
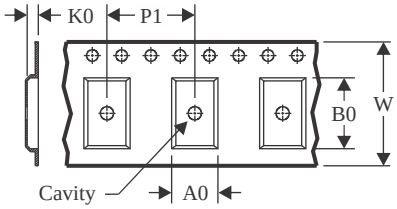
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

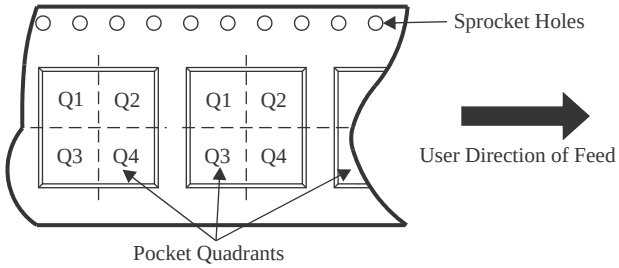


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

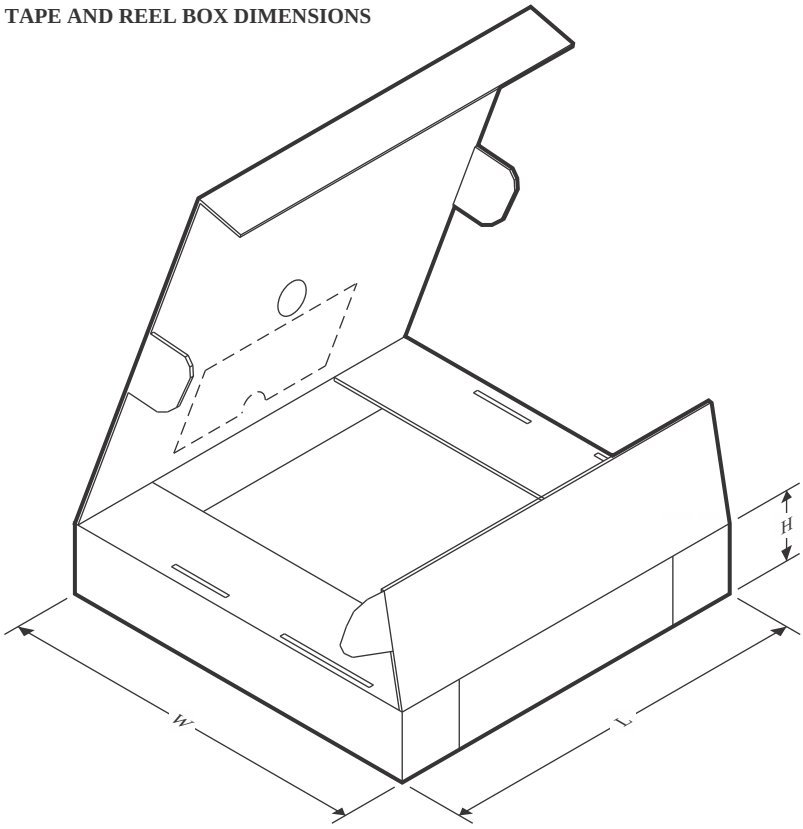
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2384PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
TPS2384PJDR	HTQFP	PJD	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

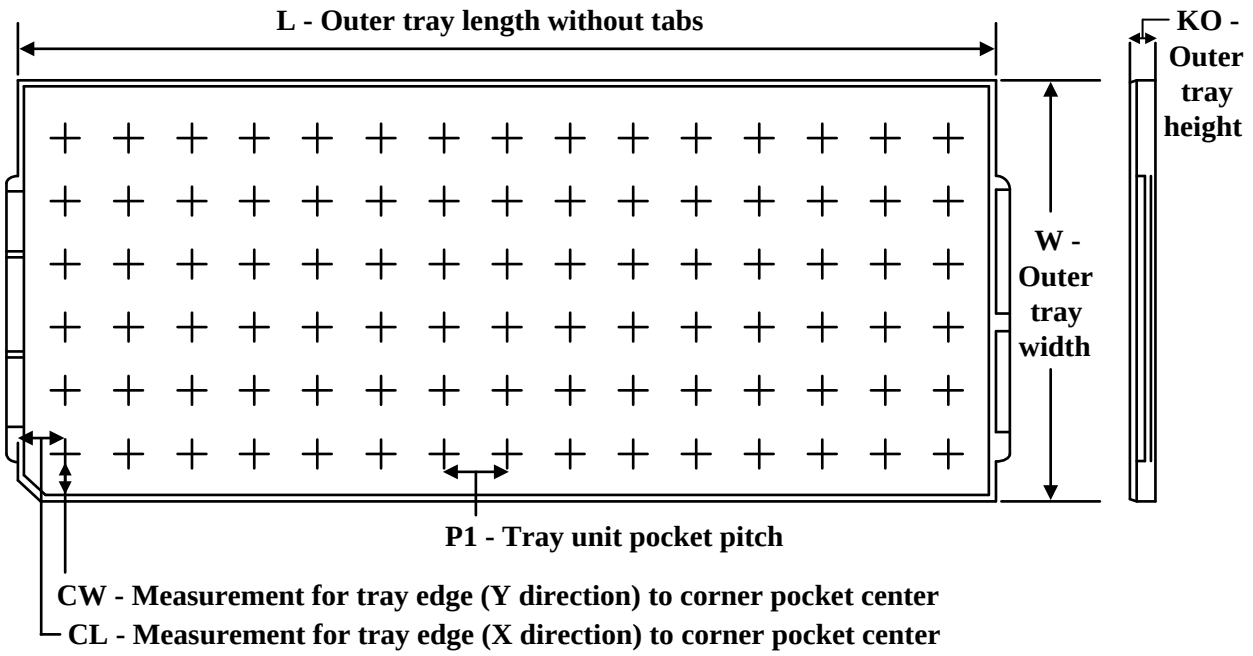
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2384PAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0
TPS2384PJDR	HTQFP	PJD	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS2384PAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TPS2384PJD	PJD	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

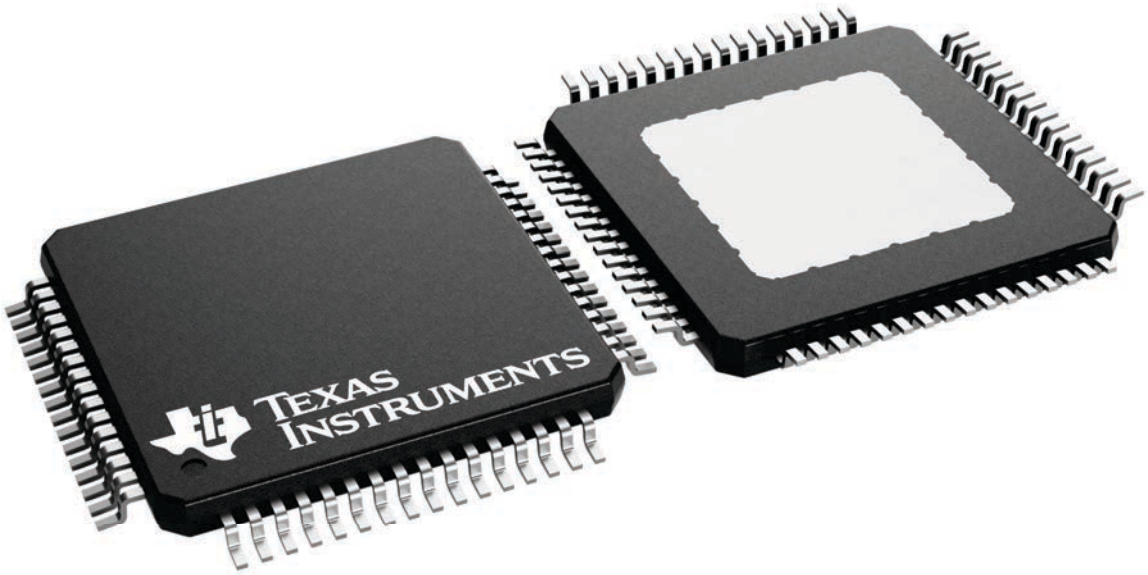
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



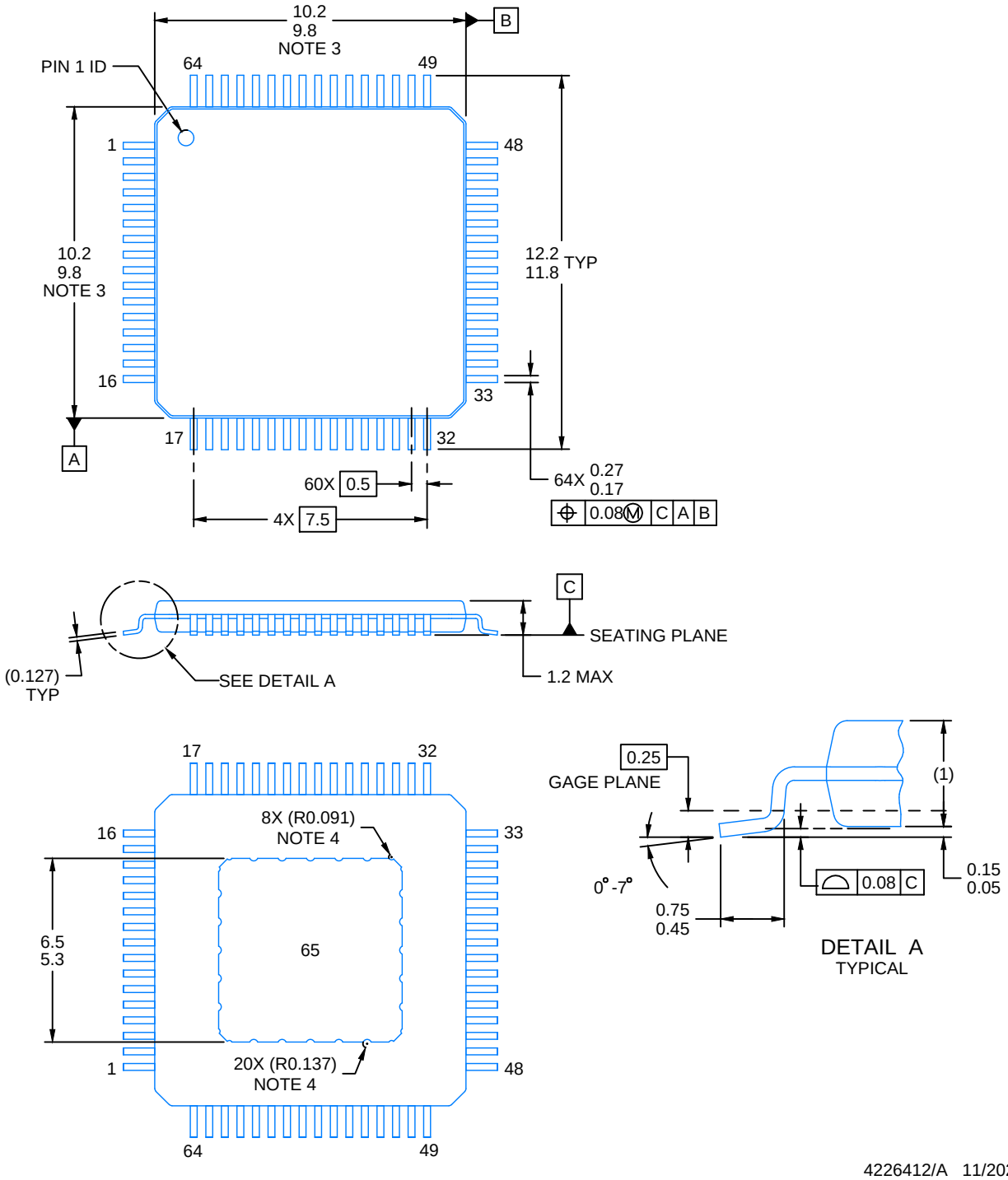
4226442/A

PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

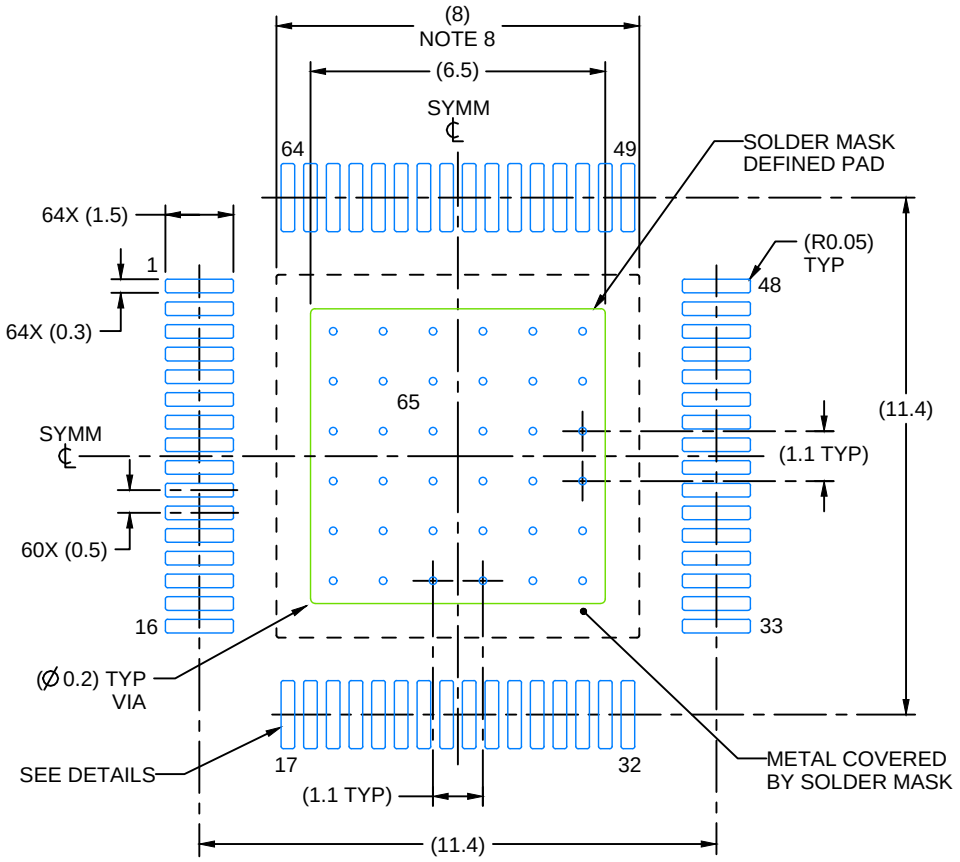
PLASTIC QUAD FLATPACK



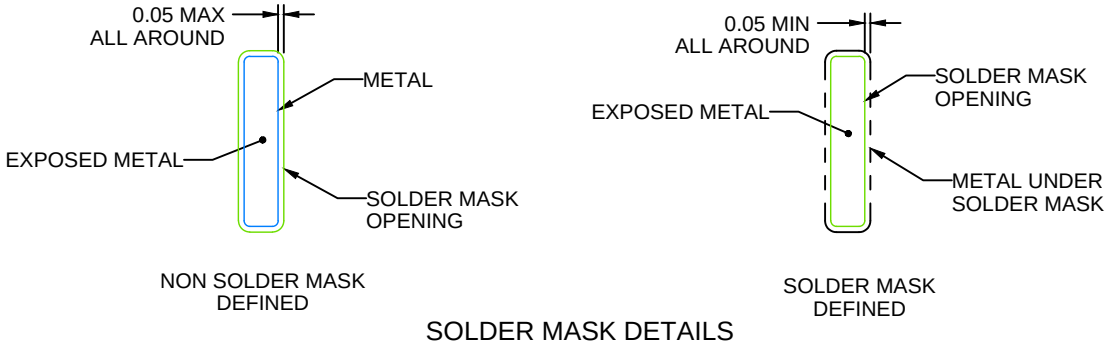
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

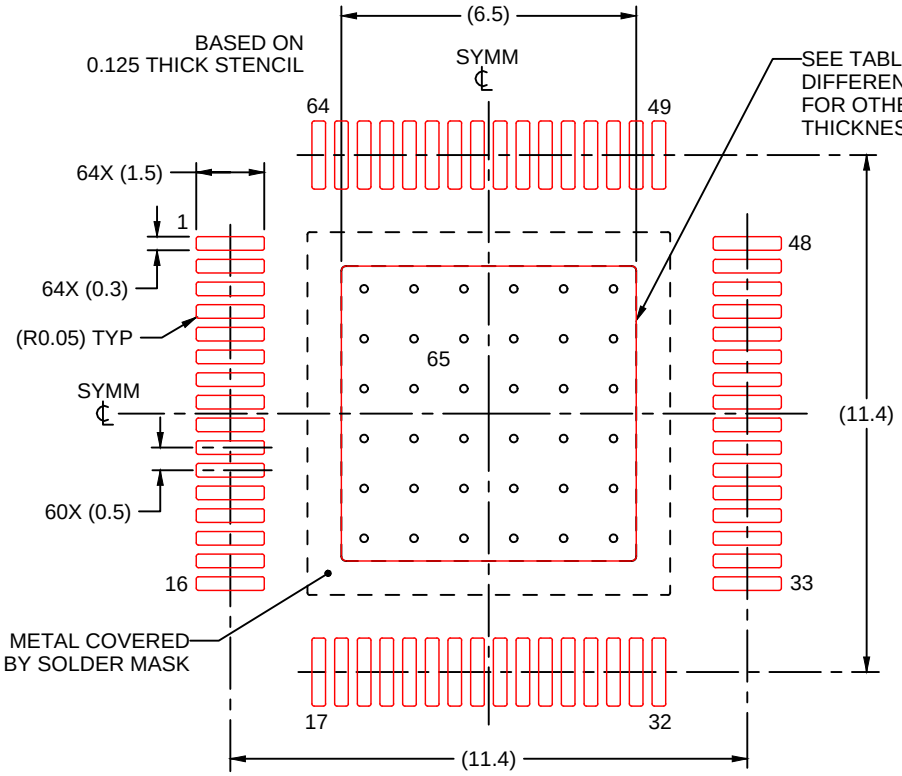


SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

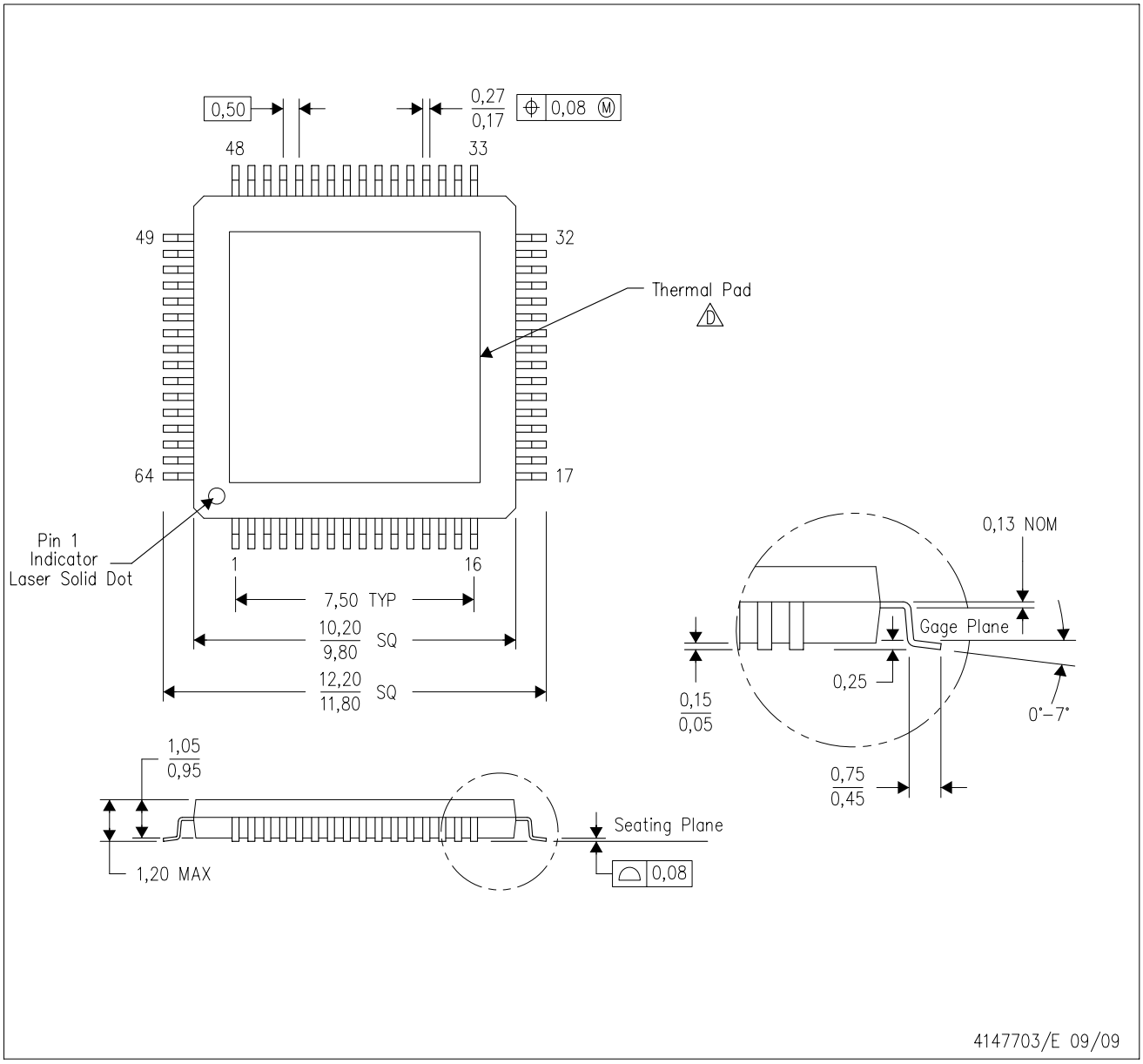
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

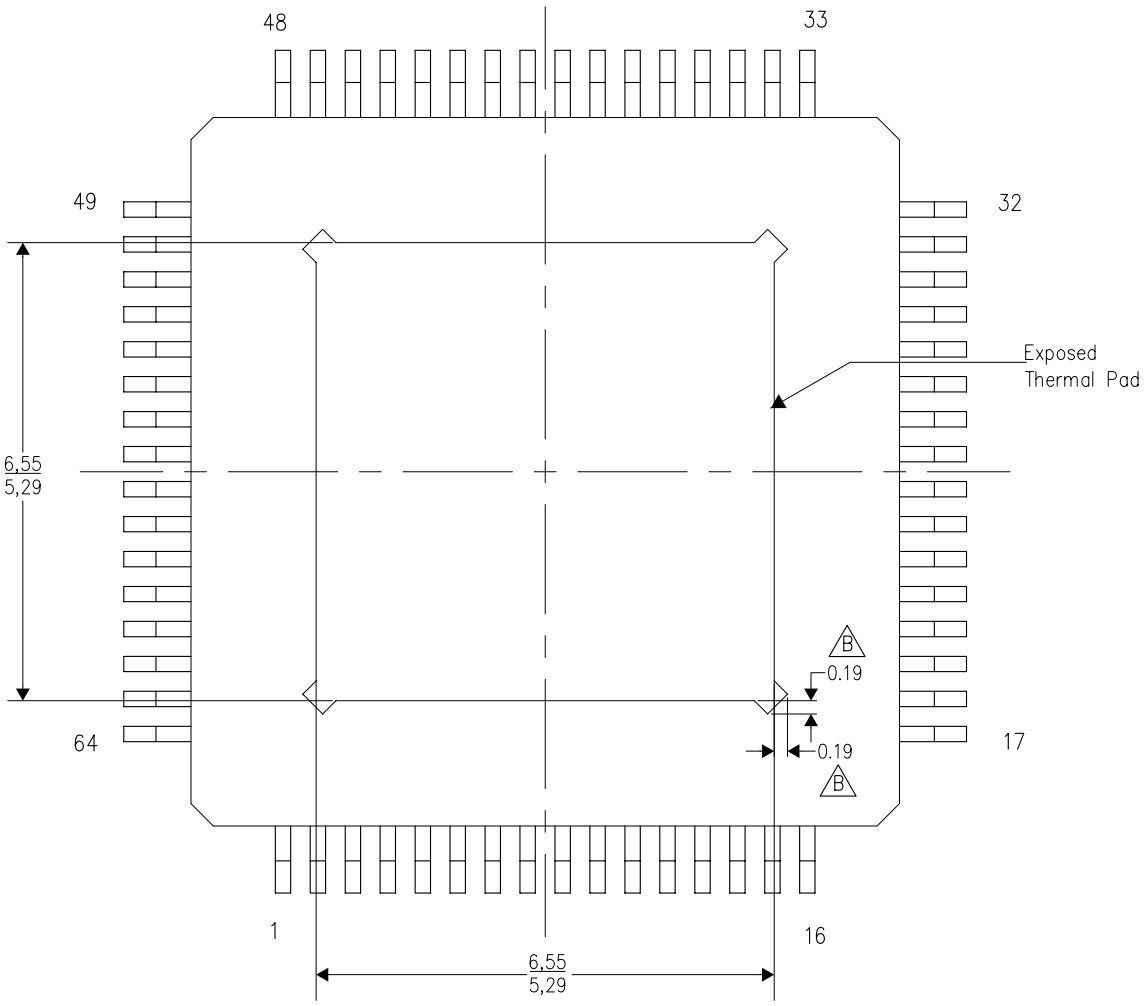
PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

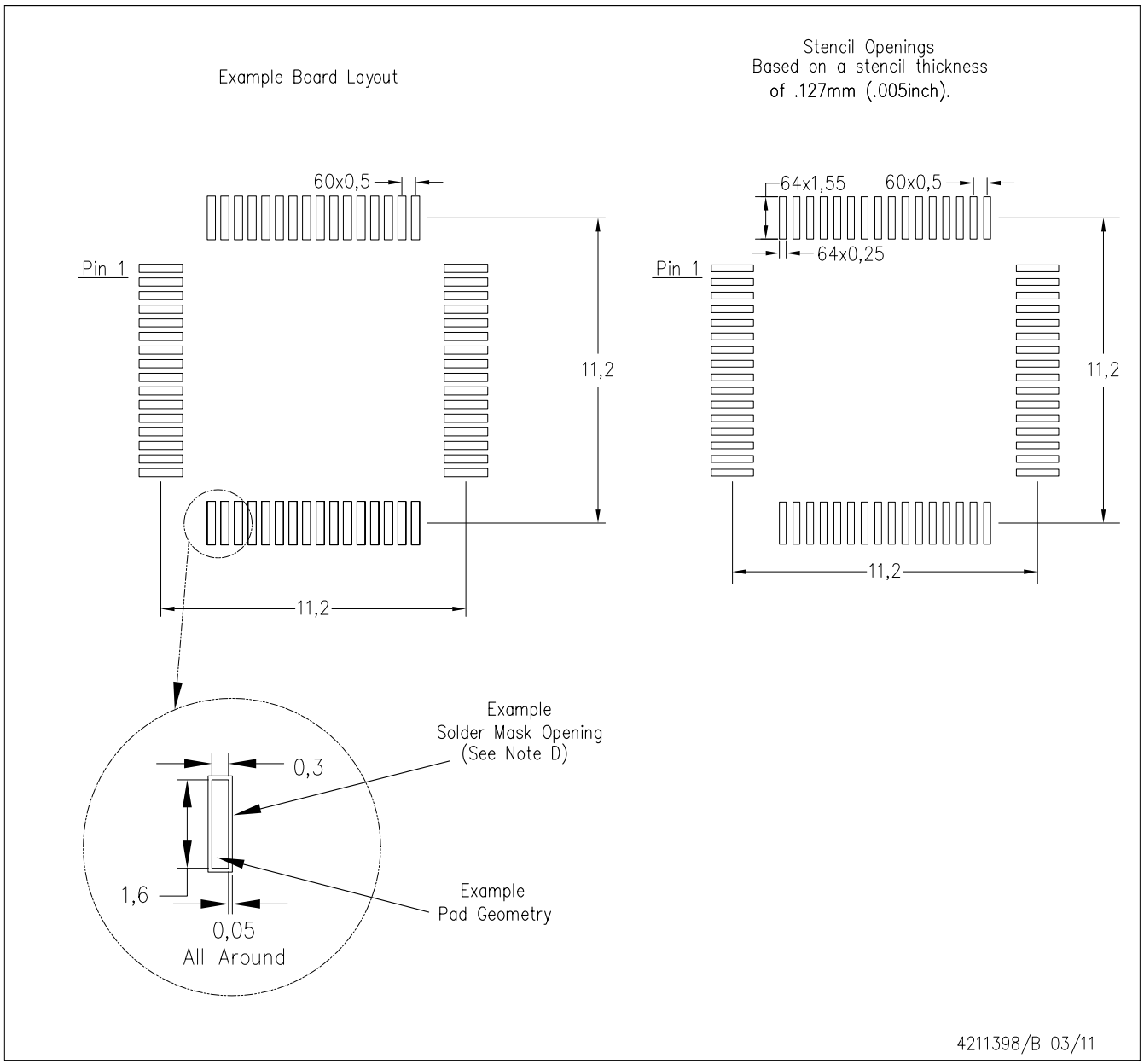
Exposed Thermal Pad Dimensions 4206330–4/B 10/10

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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