# RX66N Group
Renesas MCUs

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120-MHz 32-bit RX MCU, on-chip double-precision FPU, 698 CoreMark, up to 4-MB flash memory (supportive of the dual bank function), 1-MB SRAM, various communications interfaces including Ethernet MAC, SD host interface, quad SPI, and CAN, 12-bit A/D converter, RTC, Encryption functions (optional), Serial sound interface, CMOS camera interface, Graphic-LCD controller, 2D drawing engine

## Features

### ■ 32-bit RXv3 CPU core
- Maximum operating frequency: 120 MHz
  Capable of 698 CoreMark in operation at 120 MHz
- Double-precision 64-bit IEEE-754 floating point
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

### ■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- RTC is capable of operation from a dedicated power supply.
- Four low-power modes

### ■ On-chip code flash memory
- Supports versions with up to 4 Mbytes of ROM
- Read cycle of 8.3 ns in operation at 120-MHz with no access wait cycles
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

### ■ On-chip data flash memory
- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

### ■ On-chip SRAM
- 1 Mbyte of SRAM (no wait states)
- 32 Kbytes of RAM with ECC (single error correction/double error detection)
- 8 Kbytes of standby RAM (backup on deep software standby)

### ■ Data transfer
- DMACAa: 8 channels
- DTCb: 1 channel
- EXDMAC: 2 channels
- DMAC for the Ethernet controller: 1 channel

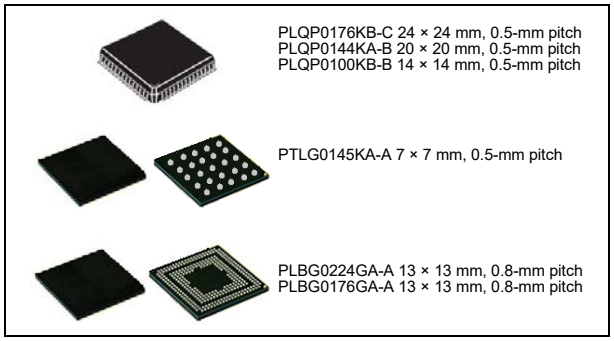
### ■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

### ■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- PLL for specific purposes
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

### ■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture function
  (for capturing times in response to event-signal input)

### ■ Independent watchdog timer
- 120-kHz clock operation

### ■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function can protect values in important registers against overwriting.




### ■ Various communications interfaces
- Ethernet MAC (1 channel)
- PHY layer (1 channel) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 3 channels)
- SCIj and SCIh with multiple functionalities (up to 8 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I$^2$C, and extended serial mode.
- SCIi with 16-byte transmission and reception FIFOs (up to 5 channels)
- I$^2$C bus interface for transfer at up to 1 Mbps (3 channels)
- Four-wire QSPI (1 channel) in addition to RSPIc (3 channels)
- Parallel data capture unit (PDC) for the CMOS camera interface (except for 100-pin products)
- Graphic-LCD controller (GLCDC)
- 2D drawing engine (DRW2D)
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- MMCIF with 1-, 4-, or 8-bit transfer bus width

### ■ External address space
- Buses for full-speed data transfer (max. operating frequency of 80 MHz)
- 8 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

### ■ Up to 29 extended-function timers
- 32-bit GPTW (4 channels)
- 16-bit TPUa (6 channels), MTU3a (9 channels)
- 8-bit TMRa (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

### ■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 21 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

### ■ 12-bit D/A converter: 2 channels

### ■ Temperature sensor for measuring temperature within the chip

### ■ Encryption functions (optional)
- AES (key lengths: 128, 192, and 256 bits)
- Trusted Secure IP (TSIP)

### ■ Up to 182 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

### ■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C



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# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.
Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package and the capacity of the code flash memory. For details, refer to Table 1.2, Comparison of Functions for Different Packages.

**Table 1.1 Outline of Specifications (1/11)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | • Maximum operating frequency: 120 MHz<br>• 32-bit RX CPU (RXv3)<br>• Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>• Address space: 4-Gbyte linear<br>• Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Ten 32-bit registers<br>Accumulator: Two 72-bit registers<br>• 113 instructions<br>Instructions installed as standard: 111<br>Basic instructions: 77<br>Single-precision floating-point operation instructions: 11<br>DSP instructions: 23<br>Instructions for register bank save function: 2<br>• Addressing modes: 11<br>• Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>• On-chip 32-bit multiplier: 32 × 32 → 64 bits<br>• On-chip divider: 32 / 32 → 32 bits<br>• Barrel shifter: 32 bits |
| | FPU | • Single-precision floating-point numbers (32 bits) and double-precision floating-point numbers (64 bits)<br>• Data types and floating-point exceptions in conformance with the IEEE754 standard |
| | Double-precision floating point coprocessor | • Double-precision floating-point register set<br>Double-precision floating-point data registers: 16, each with 64-bit width<br>Double-precision floating-point control registers: Four, each with 32-bit width<br>• Double-precision floating-point processing instructions: 21<br>• Notifying the interrupt controller of double-precision floating-point exceptions |
| | Register bank save function | • Fast collective saving and restoration of the values of CPU registers<br>• 16 save register banks |



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**Table 1.1 Outline of Specifications (2/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Memory | Code flash memory | • Capacity: 2 Mbytes/4 Mbytes<br>• ROM cache: 8 Kbytes<br>• Up to 120 MHz, no-wait access<br>• On-board programming: Four types<br>• Off-board programming (parallel programmer mode)<br>• Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized.<br>• A dual-bank structure allows programming during reading or exchanging the start-up areas |
| | Data flash memory | • Capacity: 32 Kbytes<br>• Programming/erasing: 100,000 times |
| | Unique ID | • 16-byte unique ID for each device |
| | RAM | • Capacity: 512 Kbytes<br>• Up to 120 MHz, no-wait access |
| | Expansion RAM | • Capacity: 512 Kbytes<br>• Up to 120 MHz, no-wait access |
| | ECC RAM | • Capacity: 32 Kbytes<br>• Up to 120 MHz, one-wait cycle access<br>• SEC-DED (single-bit error correction and double-bit error detection) |
| | Standby RAM | • Capacity: 8 Kbytes<br>• Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access |
| Operating modes | | • Operating modes by the mode-setting pins at the time of release from the reset state<br>Single-chip mode<br>Boot mode (for the SCI interface)<br>Boot mode (for the USB interface)<br>Boot mode (for the FINE interface)<br>• Selection of operating mode by register setting<br>Single-chip mode<br>On-chip ROM disabled extended mode<br>On-chip ROM enabled extended mode<br>• Endian selectable |
| Clock | Clock generation circuit | • Main clock oscillator, sub-clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer (two circuits), and IWDT-dedicated on-chip oscillator<br>• The peripheral module clocks can be set to frequencies above that of the system clock.<br>• Main-clock oscillation stoppage detection<br>• Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz<br>Peripheral modules of MTU, RSPI, SCIi, ETHERC, PMGI, EDMAC, GPTW, GLCDC, and DRW2D, run in synchronization with PCLKA, which operates at up to 120 MHz.<br>Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz<br>ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz<br>ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz<br>Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz<br>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 80 MHz<br>• The high-speed on-chip oscillator (HOCO) can be obtained through frequency-multiplication of the PLL or PPLL reference clock<br>• External clock input frequency: 30 MHz (max)<br>• Clock output function |



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**Table 1.1 Outline of Specifications (3/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Reset | | Nine types of reset<br>• RES# pin reset: Generated when the RES# pin is driven low.<br>• Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises.<br>• Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby.<br>• Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs.<br>• Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs.<br>• Software reset: Generated by register setting. |
| Power-on reset | | • If the RES# pin is at the high level when power is supplied, an internal reset is generated.<br>After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled. |
| Voltage detection circuit (LVDA) | | Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt.<br>• Voltage detection circuit 0<br>Capable of generating an internal reset<br>The option-setting memory can be used to select enabling or disabling of the reset.<br>Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V)<br>• Voltage detection circuits 1 and 2<br>Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V)<br>Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency)<br>Capable of generating an internal reset<br>• Two types of timing are selectable for release from reset<br>An internal interrupt can be requested.<br>• Detection of voltage rising above and falling below thresholds is selectable.<br>• Maskable or non-maskable interrupt is selectable<br>Voltage detection monitoring<br>Event linking |
| Low power consumption | Low power consumption function | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| | Battery backup function | • When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating. |
| Interrupt | Interrupt controller (ICUD) | • Number of interrupt vectors: 256<br>• External interrupts: 16 (pins IRQ0 to IRQ15)<br>• Software interrupts: 2 sources<br>• Non-maskable interrupts: 8 sources<br>• Sixteen levels specifiable for the order of priority<br>• Method of interrupt source selection:<br>The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 161 sources.) |
| External bus extension | | • The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings.<br>Capacity of each area: 16 Mbytes (CS0 to CS7)<br>A chip-select signal (CS0# to CS7#) can be output for each area.<br>Each area is specifiable as an 8-, 16-, or 32-bit bus space.<br>The data arrangement in each area is selectable as little or big endian (only for data).<br>• SDRAM interface connectable<br>• Bus format: Separate bus, multiplex bus<br>• Wait control<br>• Write buffer facility |



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**Table 1.1 Outline of Specifications (4/11)**

| Classification | Module/Function | Description |
|---|---|---|
| DMA | DMA controller (DMACAa) | • 8 channels<br>• Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger and interrupt requests from peripheral functions |
| | EXDMA controller (EXDMACa) | • 2 channels<br>Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer<br>• Single-address transfer enabled with the EDACKn signal<br>• Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions |
| | Data transfer controller (DTCb) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Request sources: External interrupts and interrupt requests from peripheral functions<br>• Sequence transfer |
| I/O ports | Programmable I/O ports | • I/O ports for the 224-pin LFBGA<br>I/O pins: 182<br>Input pin: 1<br>Pull-up resistors: 182<br>Open-drain outputs: 182<br>5-V tolerance: 19<br>• I/O ports for the 176-pin LFBGA and 176-pin LFQFP<br>I/O pins: 136<br>Input pin: 1<br>Pull-up resistors: 136<br>Open-drain outputs: 136<br>5-V tolerance: 19<br>• I/O ports for the 145-pin TFLGA and 144-pin LFQFP<br>I/O pins: 111<br>Input pin: 1<br>Pull-up resistors: 111<br>Open-drain outputs: 111<br>5-V tolerance: 18<br>• I/O ports for the 100-pin LFQFP<br>I/O pins: 78<br>Input pin: 1<br>Pull-up resistors: 78<br>Open-drain outputs: 78<br>5-V tolerance: 17 |
| Event link controller (ELC) | | • Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions.<br>• 123 internal event signals can be freely combined for interlinked operation with connected functions.<br>• Event signals from peripheral modules can be used to change the states of output pins (of ports B and E).<br>• Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules. |



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**Table 1.1 Outline of Specifications (5/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | 16-bit timer pulse unit (TPUa) | • (16 bits × 6 channels) × 1 unit<br>• Maximum of 16 pulse-input/output possible<br>• Select from among seven or eight counter-input clock signals for each channel<br>• Input capture/output compare function<br>• Output of PWM waveforms in up to 15 phases in PWM mode<br>• Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel.<br>• PPG output trigger can be generated<br>• Capable of generating conversion start triggers for the A/D converters<br>• Digital filtering of signals from the input capture pins<br>• Event linking by the ELC |
| | Multifunction timer pulse unit (MTU3a) | • 9 channels (16 bits × 8 channels, 32 bits × 1 channel)<br>• Maximum of 28 pulse-input/output and 3 pulse-input possible<br>• Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A)<br>14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5.<br>• Input capture function<br>• 39 output compare/input capture registers<br>• Counter clear operation (synchronous clearing by compare match/input capture)<br>• Simultaneous writing to multiple timer counters (TCNT)<br>• Simultaneous register input/output by synchronous counter operation<br>• Buffered operation<br>• Support for cascade-connected operation<br>• 43 interrupt sources<br>• Automatic transfer of register data<br>• Pulse output mode<br>Toggle/PWM/complementary PWM/reset-synchronized PWM<br>• Complementary PWM output mode<br>Outputs non-overlapping waveforms for controlling 3-phase inverters<br>Automatic specification of dead times<br>PWM duty cycle: Selectable as any value from 0% to 100%<br>Delay can be applied to requests for A/D conversion.<br>Non-generation of interrupt requests at peak or trough values of counters can be selected.<br>Double buffer configuration<br>• Reset synchronous PWM mode<br>Three phases of positive and negative PWM waveforms can be output with desired duty cycles.<br>• Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2)<br>• Counter functionality for dead-time compensation<br>• Generation of triggers for A/D converter conversion<br>• A/D converter start triggers can be skipped<br>• Digital filter function for signals on the input capture and external counter clock pins<br>• PPG output trigger can be generated<br>• Event linking by the ELC |
| | Port output enable 3 (POE3a) | • Control of the high-impedance state of the MTU waveform output pins<br>• 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11#<br>• Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level)<br>• Initiation by oscillation-stoppage detection or software<br>• Additional programming of output control target pins is enabled |



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**Table 1.1 Outline of Specifications (6/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | General PWM timer (GPTW) | • 32 bits × 4 channels (GPTW0 to GPTW3)<br>• Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels<br>• Clock sources independently selectable for each channel<br>• 2 input/output pins per channel<br>• 2 output compare/input capture registers per channel<br>• For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use.<br>• In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetrically PWM waveforms.<br>• Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow)<br>• Generation of dead times in PWM operation<br>• Capable of synchronous start, stop, or clearing of counter for any channel<br>• Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison<br>• Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers<br>• Output pin disabling function by a dead time error or a short circuit detection among output pins<br>• Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion.<br>• Capable of outputting events, such as compare-match from A to F and overflow/ underflow, to ELC<br>• Capable of using noise filter of input capture |
| | Port output enable for GPTW (POEG) | • Controlling the output disable for GPTW waveform output<br>• Initiation by input level detection of GTETRG pins<br>• Initiation by output disable request from GPTW<br>• Initiation by detection of oscillation stop or by software |
| | Programmable pulse generator (PPG) | • (4 bits × 4 groups) × 2 units<br>• Pulse output with the MTU or TPU output as a trigger<br>• Maximum of 32 pulse-output possible |
| | 8-bit timers (TMR) | • (8 bits × 2 channels) × 2 units<br>• Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal<br>• Capable of output of pulse trains with desired duty cycles or of PWM signals<br>• The 2 channels of each unit can be cascaded to create a 16-bit timer<br>• Generation of triggers for A/D converter conversion<br>• Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12<br>• Event linking by the ELC |
| | Compare match timer (CMT) | • (16 bits × 2 channels) × 2 units<br>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) |
| | Compare match timer W (CMTW) | • (32 bits × 1 channel) × 2 units<br>• Compare-match, input-capture input, and output-comparison output are available.<br>• Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)<br>• Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.<br>• Event linking by the ELC |
| | Realtime clock (RTCd)*1 | • Clock sources: Main clock, sub-clock<br>• Selection of the 32-bit binary count in time count/second unit possible<br>• Clock and calendar functions<br>• Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt<br>• Battery backup operation<br>• Time-capture facility for three values<br>• Event linking by the ELC |
| | Watchdog timer (WDTA) | • 14 bits × 1 channel<br>• Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192) |



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**Table 1.1 Outline of Specifications (7/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | Independent watchdog timer (IWDTa) | • 14 bits × 1 channel<br>• Counter-input clock: IWDT-dedicated on-chip oscillator<br>• Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256<br>• Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled).<br>• Event linking by the ELC |
| Communication function | Ethernet controller (ETHERC) | • 1 channel<br>• Input and output of Ethernet/IEEE 802.3 frames<br>• Transfer at 10 or 100 Mbps<br>• Full- and half-duplex modes<br>• MII (Media Independent Interface) and RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u<br>• Detection of Magic Packets™*2 or output of a “wake-on-LAN” signal (WOL)<br>• Compliance with flow control as defined in IEEE 802.3x standards |
| | PHY management interface (PMGI) | • 1 channel<br>• This module is compliant with the MII (Media Independent Interface) as defined in the IEEE 802.3u standard.<br>• Transmission and reception of management frames through PHY-LSI chips having an MII or RMII interface is supported.<br>• Alleviates load on the CPU by shifting it to dedicated hardware<br>• The timing of management data is adjustable.<br>• Preambles can be deleted. |
| | DMA controller for ethernet controller (EDMACa) | • 1 channel<br>For ETHERC: 1 channel<br>• Alleviation of CPU load by the descriptor control method<br>• Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes |
| | USB 2.0 FS host/ function module (USBb) | • Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS<br>• One port<br>• Compliance with the USB 2.0 specification<br>• Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only)<br>• Both self-power mode and bus-power mode are supported<br>• OTG (On the Go) operation is possible (low-speed is not supported)<br>• Incorporates 2 Kbytes of RAM as a transfer buffer<br>• External pull-up and pull-down resistors are not required |



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**Table 1.1 Outline of Specifications (8/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Serial communications interfaces (SCIj, SCIi, SCIh) | • 13 channels (SCIj: 7 channels + SCIi: 5 channels + SCIh: 1 channel)<br>• SCIj, SCIi, SCIh<br>Serial communications modes: Asynchronous, clock synchronous, and smart-card interface<br>Multi-processor function<br>On-chip baud rate generator allows selection of the desired bit rate<br>Choice of LSB-first or MSB-first transfer<br>Start-bit detection: Level or edge detection is selectable.<br>Simple $I^2C$<br>Simple SPI<br>7- to 9-bit transfer mode<br>Bit rate modulation<br>Double-speed mode<br>Detecting matches of data is supported (other than for SCI12)<br>• SCIj, SCIh<br>Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12<br>Event linking by the ELC (only on channel 5)<br>• SCIh<br>Supports the serial communications protocol, which contains the start frame and information frame<br>Supports the LIN format<br>• SCIi<br>Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit |
| | $I^2C$ bus interface (RIICa) | • 3 channels (only channel 0 can be used in fast-mode plus)<br>Communication formats<br>$I^2C$ bus format/SMBus format<br>Supports the multi-master<br>Max. transfer rate: 1 Mbps (channel 0)<br>• Event linking by the ELC |
| | CAN module (CAN) | • 3 channels<br>• Compliance with the ISO11898-1 specification (standard frame and extended frame)<br>• 32 mailboxes per channel |
| | Serial peripheral interface (RSPIc) | • 3 channels<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>Transit/receive data can be swapped in byte units<br>• Buffered structure<br>Double buffers for both transmission and reception<br>• RSPCK can be stopped with the receive buffer full for master reception.<br>• Event linking by the ELC |
| | Quad serial peripheral interface (QSPI) | • 1 channel<br>• Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation)<br>• Programmable bit length and selectable active sense and phase of the clock signal<br>• Sequential execution of transfer<br>• LSB or MSB first is selectable |



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**Table 1.1 Outline of Specifications (9/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Extended serial sound interface (SSIE) | | • 2 channels<br>• Full-duplex transmission (only for channel 0)<br>• Various types of serial audio formatting are supported.<br>• Master and slave operations are supported.<br>• The bit-clock frequency is selectable from among 13 frequencies (1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128).<br>• Data formats with 8, 16, 18, 20, 22, 24, and 32 bits are supported.<br>• 32-stage FIFO buffers for transmission and reception<br>• Stopping or not stopping the SSILRCK signal on stopping of data transmission is selectable. |
| SD host interface (SDHI) | | • 1 channel<br>• Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s)<br>• One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses)<br>• SD specifications<br>Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported)<br>Part E1: SDIO Specification Ver. 3.00<br>• Error checking: CRC7 for commands and CRC16 for data<br>• Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, interrupt of SD buffer access<br>• DMA transfer requests: SD_BUF write and SD_BUF read<br>• Support for card detection and write protection |
| MMC host interface (MMCIF) | | • 1 channel<br>• Transfer speed: Data transfer mode (30 MB/s), backward compatible mode (25 MB/s)<br>• Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported)<br>• Interface for Multimedia Cards (MMCs)<br>• Data buses: Support for 1-, 4-, and 8-bit MMC buses<br>• Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt, interrupt of MMCIF buffer access<br>• DMA transfer requests: CE_DATA write and CE_DATA read<br>• Support for card detection, boot operation, high priority interrupt (HPI) |
| Parallel data capture unit (PDC) | | • 1 channel<br>• Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals<br>• Setting of the image size when clipping of the output for a one-frame image is required |
| Graphic-LCD controller (GLCDC) | | • 1 channel<br>• Various data formats and LCD panels are supported<br>• Superposition of 3 planes (single-color background, graphic 1, graphic 2)<br>• 32- and 16-bpp graphics data and 8-, 4-, and 1-bit CLUT data formats are supported |
| 2D drawing engine (DRW2D) | | • 1 channel<br>• Vector drawing (straight lines, triangles, and circles)<br>• Bit blitting (with support for filling, copying, stretching, and rotation)<br>• Bus master function for input and output of frame buffer data<br>32-, 16-, and 8-bit pixel graphics data are supported<br>• Bus master function for input of texture data<br>Input of texture data (32, 24, 16, 8, 4, 2, or 1 bit) are supported.<br>Run length encoding is supported<br>A CLUT is installed and index data can be converted into color data<br>• Two rendering modes are supported (register mode and display list mode)<br>• Performance counting<br>• Interrupts in response to completion of rendering and processing of the display list |



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**Table 1.1 Outline of Specifications (10/11)**

| Classification | Module/Function | Description |
|---|---|---|
| 12-bit A/D converter (S12ADFa) | | • 12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels)<br>• 12-bit resolution (switchable between 8, 10, and 12 bits)<br>• Conversion time<br>0.48 µs per channel (for 12-bit conversion)<br>0.45 µs per channel (for 10-bit conversion)<br>0.42 µs per channel (for 8-bit conversion)<br>• Operating mode<br>Scan mode (single scan mode, continuous scan mode, or 3 group scan mode)<br>Group priority control (only for 3 group scan mode)<br>• Sample-and-hold function<br>Common sample-and-hold circuit included<br>In addition, channel-dedicated sample-and-hold function (3 channels: in unit 0 only) included<br>• Sampling variable<br>Sampling time can be set up for each channel.<br>• Digital comparison<br>Method: Comparison to detect voltages above or below thresholds and window comparison<br>Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1)<br>• Double trigger mode (A/D conversion data duplicated)<br>• Detection of analog input disconnection<br>• Three ways to start A/D conversion<br>Software trigger, timer (MTU, TMR, TPU) trigger, external trigger<br>• Event linking by the ELC |
| 12-bit D/A converter (R12DAa) | | • 2 channels<br>• 12-bit resolution<br>• Output voltage: 0.2 V to AVCC1 – 0.2 V (buffered output), 0 V to AVCC1 (unbuffered output)<br>• Buffered output or unbuffered output can be selected.<br>• Event linking by the ELC |
| Temperature sensor | | • 1 channel<br>• Relative precision: ± 1°C<br>• The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1). |
| Safety | Memory protection unit (MPU) | • Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh.<br>• Minimum protection unit: 16 bytes<br>• Reading from, writing to, and enabling the execution access can be specified for each area.<br>• An access exception occurs when the detected access is not in the permitted area. |
| | Trusted Memory (TM) Function | • Programs in the TM target area in the code flash memory are protected against reading<br>• Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled. |
| | Register write protection function | • Protects important registers from being overwritten for in case a program runs out of control. |
| | CRC calculator (CRCA) | • Generation of CRC codes for 8-/32-bit data<br>8-bit data<br>Selectable from the following three polynomials<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$<br>32-bit data<br>Selectable from the following two polynomials<br>$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$,<br>$X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| | Main clock oscillation stop detection | • Main clock oscillation stop detection: Available |



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**Table 1.1 Outline of Specifications (11/11)**

| Classification | Module/Function | Description |
|---|---|---|
| Safety | Clock frequency accuracy measurement circuit (CAC) | • Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, USB clock, Ethernet-PHY external clock, and PCLKB, and generates interrupts when the setting range is exceeded. |
| | Data operation circuit (DOC) | • The function to compare, add, or subtract 16-bit data |
| Encryption function | Trusted Secure IP (TSIP)*3 | • Security algorithm<br>Common key encryption: AES (compliant with NIST FIPS PUB 197), TDES, ARC4<br>Non-common key encryption: RSA<br>• Other features<br>TRNG (true-random number generator)<br>Hash value generation: SHA1, SHA224, SHA256, MD5, GHASH<br>Prevention of the illicit copying of keys |
| Operating frequency | | Up to 120 MHz |
| Power supply voltage | | VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,<br>$V_{BATT}$ = 1.62 to 3.6 V*4 |
| Operating temperature | | D-version: –40 to +85°C<br>G-version: –40 to +105°C |
| Package | | 224-pin LFBGA (PLBG0224GA-A)<br>176-pin LFBGA (PLBG0176GA-A)<br>176-pin LFQFP (PLQP0176KB-C)<br>145-pin TFLGA (PTLG0145KA-A)<br>144-pin LFQFP (PLQP0144KA-B)<br>100-pin LFQFP (PLQP0100KB-B) |
| On-chip debugging system | | • E1 emulator (JTAG and FINE interfaces) |

Note 1. When the realtime clock is not used, initialize the registers in the time clock according to description in section 33.6.7, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.
Note 2. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 3. The product part number differs according to whether or not the MCU includes the encryption function.
Note 4. The low CL crystal unit cannot be used when the $V_{BATT}$ voltage is less than 2.0 V.



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**Table 1.2 Comparison of Functions for Different Packages (1/2)**

| Functions | | RX66N | | | |
|---|---|---|---|---|---|
| **Package** | | **224 Pins** | **176 Pins** | **144 Pins/145 Pins** | **100 Pins** |
| External bus | External bus width | 32 bits/16 bits/8 bits | | 16 bits/8 bits | |
| | SDRAM area controller | Available | | | Not available |
| DMA | DMA controller | Ch. 0 to 7 | | | |
| | Data transfer controller | Available | | | |
| | EXDMA controller | Ch. 0 and 1 | | | |
| Timers | 16-bit timer pulse unit | Ch. 0 to 5 | | | |
| | Multi-function timer pulse unit 3 | Ch. 0 to 8 | | | |
| | General PWM timer | Ch. 0 to 3 | | | |
| | Port output enable 3 | Available | | | |
| | Port output enable for GPTW | Available | | | |
| | Programmable pulse generator | Ch. 0 and 1 | | | |
| | 8-bit timers | Ch. 0 to 3 | | | |
| | Compare match timer | Ch. 0 to 3 | | | |
| | Compare match timer W | Ch. 0 and 1 | | | |
| | Realtime clock | Available | | | |
| | Watchdog timer | Available | | | |
| | Independent watchdog timer | Available | | | |
| Communication function | Ethernet controller | Ch. 0 | | | |
| | PHY management interface | Ch. 0 | | | |
| | DMA controller for the ethernet controller | Ch. 0 (ETHERC) | | | |
| | USB2.0 FS host/function module | Ch. 0 | | | |
| | Serial communications interfaces (SCIj) | Ch. 0 to 6 | | | Ch. 0 to 3, 5, and 6 |
| | Serial communications interfaces (SCIi) | Ch. 7 to 11 | | | Ch. 8 to 11 |
| | Serial communications interfaces (SCIh) | Ch. 12 | | | |
| | $I^2C$ bus interfaces | Ch. 0 to 2 | | | |
| | Serial peripheral interface | Ch. 0 to 2 | | | |
| | CAN module | Ch. 0 to 2 | | | Ch. 0 and 1 |
| | Quad serial peripheral interface | Ch. 0 | | | |
| | Expansion serial sound interface | Ch. 0 and 1 | | | |
| | SD host interface | Ch. 0 | | | |
| | Multimediacard interface | Ch. 0 | | | |
| | Parallel data capture unit | Available | | | Not available |
| Graphics | Graphic-LCD controller | Available | | | |
| | 2D drawing engine | Available | | | |
| 12-bit A/D converter | Unit 0 | AN000 to AN007 (8 channels) | | | |
| | Unit 1 | AN100 to AN120 (21 channels) | | | AN100 to AN113 (14 channels) |
| 12-bit D/A converter | | Ch. 0 and 1 | | | Ch. 1 |
| Temperature sensor | | Available | | | |
| CRC calculator | | Available | | | |
| Data operation circuit | | Available | | | |
| Clock frequency accuracy measurement circuit | | Available | | | |



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**Table 1.2 Comparison of Functions for Different Packages (2/2)**

| Functions | RX66N | | | |
|---|---|---|---|---|
| **Package** | **224 Pins** | **176 Pins** | **144 Pins/145 Pins** | **100 Pins** |
| Trusted Secure IP | Available/Not available | | | |
| Event link controller | Available | | | |



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## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1/2)**

| Group | Part No. | Package | Code Flash Memory Capacity | RAM Capacity | Data Flash Memory Capacity | Operating Frequency (Max.) | Encryption Module | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|
| RX66N (D-version) | R5F566NNDDFC | PLQP0176KB-C | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDFC | PLQP0176KB-C | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDFC | PLQP0176KB-C | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDFC | PLQP0176KB-C | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NNDDFB | PLQP0144KA-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDFB | PLQP0144KA-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDFB | PLQP0144KA-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDFB | PLQP0144KA-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NNDDFP | PLQP0100KB-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDFP | PLQP0100KB-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDFP | PLQP0100KB-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDFP | PLQP0100KB-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NNDDBD | PLBG0224GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDBD | PLBG0224GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDBD | PLBG0224GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDBD | PLBG0224GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NNDDBG | PLBG0176GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDBG | PLBG0176GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDBG | PLBG0176GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDBG | PLBG0176GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NNDDLK | PTLG0145KA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NNHDLK | PTLG0145KA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| | R5F566NDDDLK | PTLG0145KA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +85 |
| | R5F566NDHDLK | PTLG0145KA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +85 |
| RX66N (G-version) | R5F566NNDGFC | PLQP0176KB-C | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGFC | PLQP0176KB-C | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGFC | PLQP0176KB-C | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGFC | PLQP0176KB-C | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NNDGFB | PLQP0144KA-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGFB | PLQP0144KA-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGFB | PLQP0144KA-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGFB | PLQP0144KA-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NNDGFP | PLQP0100KB-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGFP | PLQP0100KB-B | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGFP | PLQP0100KB-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGFP | PLQP0100KB-B | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NNDGBD | PLBG0224GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGBD | PLBG0224GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGBD | PLBG0224GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGBD | PLBG0224GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NNDGBG | PLBG0176GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGBG | PLBG0176GA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGBG | PLBG0176GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGBG | PLBG0176GA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |



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**Table 1.3 List of Products (2/2)**

| Group | Part No. | Package | Code Flash Memory Capacity | RAM Capacity | Data Flash Memory Capacity | Operating Frequency (Max.) | Encryption Module | Operating temperature (°C) |
|---|---|---|---|---|---|---|---|---|
| RX66N (G-version) | R5F566NNDGLK | PTLG0145KA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NNHGLK | PTLG0145KA-A | 4 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |
| | R5F566NDDGLK | PTLG0145KA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Not available | –40 to +105 |
| | R5F566NDHGLK | PTLG0145KA-A | 2 Mbytes | 1 Mbyte | 32 Kbytes | 120 MHz | Available | –40 to +105 |

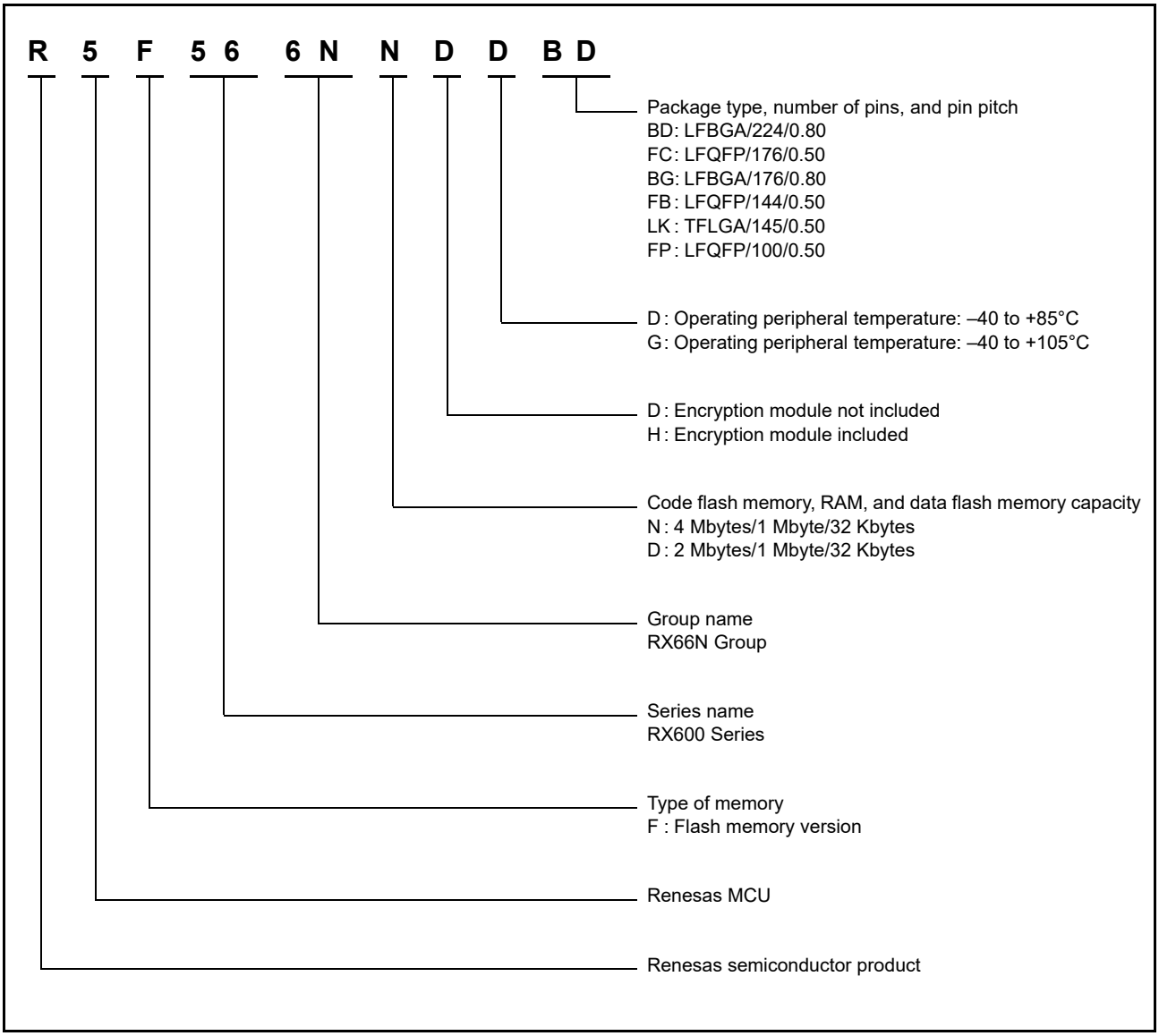


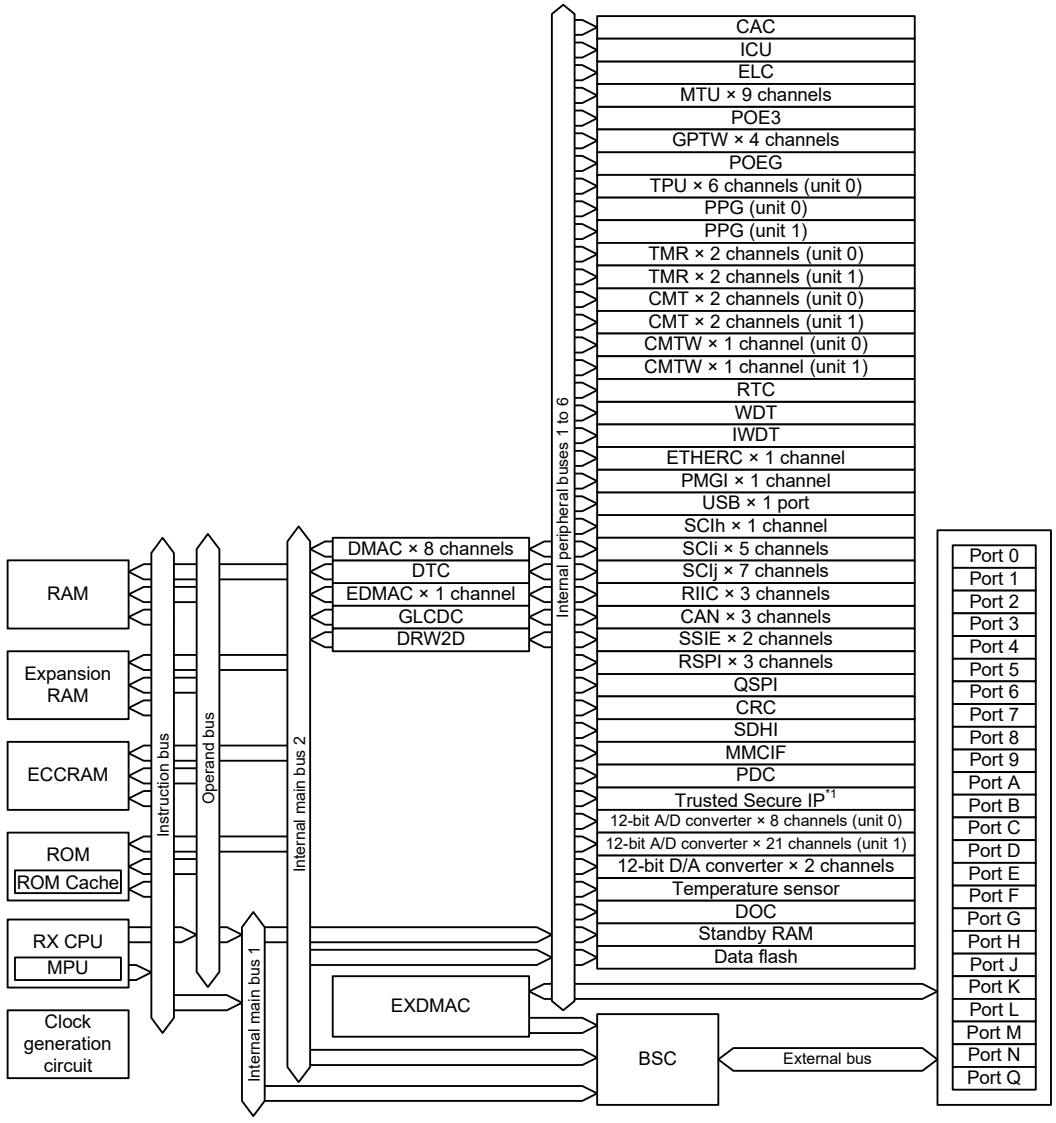

**Figure 1.1 How to Read the Product Part Number**



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## 1.3 Block Diagram

Figure 1.2 shows a block diagram.




CAC: Clock frequency accuracy measurement circuit
ICU: Interrupt controller
BSC: Bus controller
MPU: Memory protection unit
DMAC: DMA controller
EXDMAC: EXDMA controller
DTC: Data transfer controller
ELC: Event link controller
MTU: Multi-function timer pulse unit 3
POE3: Port output enable 3
GPTW: General PWM timer
POEG: GPTW port output enable
TPU: 16-bit timer pulse unit
PPG: Programmable pulse unit
TMR: 8-bit timer
CMT: Compare match timer
CMTW: Compare match timer W
RTC: Realtime clock
WDT: Watchdog timer
IWDT: Independent watchdog timer
ETHERC: Ethernet controller

EDMAC: DMA controller for the ethernet controller
PMGI: Phy management interface
USB: USB2.0 FS host/function module
SCIj, SCIi, SCIh: Serial communications interface
RIIC: I²C-bus interface
CAN: CAN module
SSIE: Serial sound interface enhanced
RSPI: Serial communications interface
QSPI: Quad serial peripheral interface
CRC: CRC calculator
SDHI: SD host interface
MMCIF: MultiMediaCard interface
PDC: Parallel data capture unit
GLCDC: Graphic LCD controller
DRW2D: 2D drawing engine
Trusted Secure IP: Trusted secure IP*1
DOC: Data operation circuit

Note 1. Optional

**Figure 1.2 Block Diagram**



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## 1.4 Pin Functions

Table 1.4 lists the pin functions.

**Table 1.4 Pin Functions (1/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Digital power supply | VCC | Input | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | Input | Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Input/output pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the SDRAM-dedicated clock. |
| | XCOUT | Output | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| | CLKOUT | Output | Clock output pin. |
| Clock frequency accuracy measurement | CACREF | Input | Reference clock input pin for the clock frequency accuracy measurement circuit |
| Operating mode control | MD | Input | Input pin for setting the operating mode. The signal level on this pin must not be changed during operation. |
| | UB | Input | USB boot mode enable pin |
| | UPSEL | Input | Selects the power supply method in USB boot mode.<br>The low level selects self-power mode and the high level selects bus power mode. |
| System control | RES# | Input | Reset signal input pin. This MCU enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | FINE interface pin |
| | TRST# | Input | On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC, TRSYNC1 | Output | These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid. |
| | TRDATA0 to TRDATA7 | Output | These pins output the trace information. |
| Address bus | A0 to A23 | Output | Output pins for the address |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |



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**Table 1.4 Pin Functions (2/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode |
| | WR0# to WR3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode |
| | BC0# to BC3# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT# | Input | Input pin for wait request signals in access to the external space |
| | CS0# to CS7# | Output | Select signals for CS areas |
| SDRAM interface | CKE | Output | SDRAM clock enable signal |
| | SDCS# | Output | SDRAM chip select signal |
| | RAS# | Output | SDRAM row address strobe signal |
| | CAS# | Output | SDRAM column address strove signal |
| | WE# | Output | SDRAM write enable pin |
| | DQM0 to DQM3 | Output | SDRAM I/O data mask enable signals |
| EXDMA controller | EDREQ0, EDREQ1 | Input | External DMA transfer request pins |
| | EDACK0, EDACK1 | Output | Single address transfer acknowledge signals |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS | Input | Maskable interrupt request pins |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins |
| | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins |
| | MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins |
| | MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D | I/O | The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Port output enable 3 | POE0#, POE4#, POE8#, POE10#, POE11# | Input | Input pins for request signals to place the MTU in the high impedance state |



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**Table 1.4 Pin Functions (3/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| General PWM timer W | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | Input pins for the external trigger signals |
| | GTIOC0A to GTIOC3A, GTIOC0B to GTIOC3B | I/O | Input capture input/output compare output/PWM output pins |
| | GTADSM0, GTADSM1 | Output | Output pins for monitoring A/D conversion start requests. |
| 16-bit timer pulse unit | TIOCA0, TIOCB0, TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | TIOCA3, TIOCB3, TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins |
| | TCLKA, TCLKB, TCLKC, TCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals |
| 8-bit timer | TMO0 to TMO3 | Output | Compare match output pins |
| | TMCI0 to TMCI3 | Input | Input pins for external clocks to be input to the counter |
| | TMRI0 to TMRI3 | Input | Input pins for the counter reset |
| Compare match timer W | TIC0 to TIC3 | Input | Input pins for CMTW |
| | TOC0 to TOC3 | Output | Output pins for CMTW |
| Serial communications interface (SCIj) | • Asynchronous mode/clock synchronous mode | | |
| | SCK0 to SCK6 | I/O | Input/output pins for the clock |
| | RXD0 to RXD6 | Input | Input pins for received data |
| | TXD0 to TXD6 | Output | Output pins for transmitted data |
| | CTS0# to CTS6# | Input | Input pins for controlling the start of transmission and reception |
| | RTS0# to RTS6# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL0 to SSCL6 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA0 to SSDA6 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK0 to SCK6 | I/O | Input/output pins for the clock |
| | SMISO0 to SMISO6 | I/O | Input/output pins for slave transmission of data |
| | SMOSI0 to SMOSI6 | I/O | Input/output pins for master transmission of data |
| | SS0# to SS6# | Input | Chip-select input pins |



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**Table 1.4 Pin Functions (4/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL12 | I/O | Input/output pin for the $I^2C$ clock |
| | SSDA12 | I/O | Input/output pin for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | SMISO12 | I/O | Input/output pin for slave transmission of data |
| | SMOSI12 | I/O | Input/output pin for master transmission of data |
| | SS12# | Input | Chip-select input pin |
| | • Extended serial mode | | |
| | RXDX12 | Input | Input pin for received data |
| | TXDX12 | Output | Output pin for transmitted data |
| | SIOX12 | I/O | Input/output pin for received or transmitted data |
| Serial communications interface (SCIi) | • Asynchronous mode/clock synchronous mode | | |
| | SCK7 to SCK11 | I/O | Input/output pins for the clock |
| | RXD7 to RXD11 | Input | Input pins for received data |
| | TXD7 to TXD11 | Output | Output pins for transmitted data |
| | CTS7# to CTS11# | Input | Input pins for controlling the start of transmission and reception |
| | RTS7# to RTS11# | Output | Output pins for controlling the start of transmission and reception |
| | • Simple $I^2C$ mode | | |
| | SSCL7 to SSCL11 | I/O | Input/output pins for the $I^2C$ clock |
| | SSDA7 to SSDA11 | I/O | Input/output pins for the $I^2C$ data |
| | • Simple SPI mode | | |
| | SCK7 to SCK11 | I/O | Input/output pins for the clock |
| | SMISO7 to SMISO11 | I/O | Input/output pins for slave transmission of data |
| | SMOSI7 to SMOSI11 | I/O | Input/output pins for master transmission of data |
| | SS7# to SS11# | Input | Chip-select input pins |
| $I^2C$ bus interface | SCL0[FM+], SCL1, SCL2, SCL2-DS | I/O | Input/output pins for clocks. Bus can be directly driven by the N-channel open drain |
| | SDA0[FM+], SDA1, SDA2, SDA2-DS | I/O | Input/output pins for data. Bus can be directly driven by the N-channel open drain |



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**Table 1.4 Pin Functions (5/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Ethernet controller | REF50CK0 | Input | 50-MHz reference clock. This pin inputs a reference signal for transmission/reception timing in RMII mode. |
| | RMII0_CRS_DV | Input | This pin indicates that there are carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode. |
| | RMII0_TXD0, RMII0_TXD1 | Output | 2-bit transmit data in RMII mode |
| | RMII0_RXD0, RMII0_RXD1 | Input | 2-bit receive data in RMII mode |
| | RMII0_TXD_EN | Output | Output pin for a data transmit enable signal in RMII mode |
| | RMII0_RX_ER | Input | This pin indicates an error has occurred during reception of data in RMII mode. |
| | ET0_CRS | Input | Carrier detection/data reception enable pin |
| | ET0_RX_DV | Input | This pin indicates that there are valid receive data on ET0_ERXD3 to ET0_ERXD0. |
| | ET0_EXOUT | Output | General-purpose external output pin |
| | ET0_LINKSTA | Input | Input link status from the PHY-LSI. |
| | ET0_ETXD0 to ET0_ETXD3 | Output | 4 bits of MII transmit data |
| | ET0_ERXD0 to ET0_ERXD3 | Input | 4 bits of MII receive data |
| | ET0_TX_EN | Output | Transmit enable pin. This pin functions as a signal indicating that transmit data are ready on ET0_ETXD3 to ET0_ETXD0. |
| | ET0_TX_ER | Output | Transmit error pin. This pin functions as a signal notifying the PHY-LSI of an error during transmission. |
| | ET0_RX_ER | Input | Receive error pin. This pin functions as a signal to recognize an error during reception. |
| | ET0_TX_CLK | Input | Transmit clock pin. This pin inputs a reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER. |
| | ET0_RX_CLK | Input | Receive clock pin. This pin inputs a reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER. |
| | ET0_COL | Input | Input collision detection signal. |
| | ET0_WOL | Output | Receive Magic packet. |
| | ET0_MDC | Output | Output reference clock signal for information transfer via ET0_MDIO. |
| | ET0_MDIO | I/O | Input or output bidirectional signal for exchange of management information between this MCU and the PHY-LSI. |
| | CLKOUT25M | Output | 25-MHz clock output pin for PHY clock input |
| PHY management interface | PMGI0_MDC | Output | Reference clock signal for information transfer by PMGI0_MDIO |
| | PMGI0_MDIO | I/O | Bi-directional signal for the exchange of management information between the PHY LSI chip and this MCU |
| USB 2.0 host/function module | VCC_USB | Input | Power supply pin |
| | VSS_USB | Input | Ground pin |
| | USB0_DP | I/O | Input or output USB transceiver D+ data. |
| | USB0_DM | I/O | Input or output USB transceiver D- data. |
| | USB0_EXICEN | Output | Connect to the OTG power IC. |
| | USB0_ID | Input | Connect to the OTG power IC. |
| | USB0_VBUSEN | Output | USB VBUS power enable pin |
| | USB0_OVRCURA/ USB0_OVRCURB | Input | USB overcurrent pins |
| | USB0_VBUS | Input | USB cable connection/disconnection detection input pin |



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**Table 1.4 Pin Functions (6/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| CAN module | CRX0, CRX1, CRX2, CRX1-DS | Input | Input pins |
| | CTX0, CTX1, CTX2 | Output | Output pins |
| Serial peripheral interface | RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B | I/O | Clock input/output pins |
| | MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B | I/O | Input or output data output from the master |
| | MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B | I/O | Input or output data output from the slave |
| | SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A/SSLC0-B | I/O | Input or output pins for slave selection |
| | SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A/SSLC1-B, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A/SSLC2-B, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A/SSLC3-B | Output | Output pins for slave selection |
| Quad serial peripheral interface | QSPCLK-A/QSPCLK-B/ QSPCLK-C | Output | QSPI clock output pins |
| | QSSL-A/QSSL-B/QSSL-C | Output | QSPI slave output pins |
| | QMO-A/QMO-B/QMO-C, QIO0-A/QIO0-B/QIO0-C | I/O | Master transmit data/data 0 |
| | QMI-A/QMI-B/QMI-C, QIO1-A/QIO1-B/QIO1-C | I/O | Master input data/data 1 |
| | QIO2-A/QIO2-B/QIO2-C, QIO3-A/QIO3-B/QIO3-C | I/O | Data 2, data 3 |
| Serial sound interface enhanced | SSIBCK0, SSIBCK1 | I/O | SSIE serial bit-clock pins |
| | SSILRCK0, SSILRCK1 | I/O | LR clock |
| | SSITXD0 | Output | Serial data output pin |
| | SSIRXD0 | Input | Serial data input pin |
| | SSIDATA1 | I/O | Serial data input/output pin |
| | AUDIO_CLK | Input | External clock pin for audio (input for an oversampling clock) |
| MMC host interface | MMC_CLK-A/MMC_CLK-B | Output | MMC clock pins |
| | MMC_CMD-A/MMC_CMD-B | I/O | Command/response pins |
| | MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B | I/O | Transmit data/receive data |
| | MMC_CD-A/MMC_CD-B | Input | Card detection pins |
| | MMC_RES#-A/MMC_RES#-B | Output | MMC reset output pins |



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**Table 1.4 Pin Functions (7/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| SD host interface | SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C/SDHI_CLK-D | Output | SD clock output pins |
| | SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C/SDHI_CMD-D | I/O | SD command output, response input signal pins |
| | SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C/SDHI_D3-D to SDHI_D0-A/SDHI_D0-B/ SDHI_D0-C/SDHI_D0-D | I/O | SD data bus pins |
| | SDHI_CD | Input | SD card detection pin |
| | SDHI_WP | Input | SD write-protect signal |
| Parallel data capture unit | PIXCLK | Input | Image transfer clock pin |
| | VSYNC | Input | Vertical synchronization signal pin |
| | HSYNC | Input | Horizontal synchronization signal pin |
| | PIXD0 to PIXD7 | Input | 8-bit image data pins |
| | PCKO | Output | Output pin for dot clock |
| Graphic-LCD controller | LCD_CLK-A, LCD_CLK-B | Output | Panel clock output pins |
| | LCD_TCON3-A/ LCD_TCON3-B to LCD_TCON0-A/ LCD_TCON0-B | Output | Control signal output pins |
| | LCD_DATA23-A/ LCD_DATA23-B to LCD_DATA0-A/ LCD_DATA0-B | Output | LCD signal output pins |
| | LCD_EXTCLK-A, LCD_EXTCLK-B | Input | Panel clock source input pins |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz/64-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins |
| 12-bit A/D converter | AN000 to AN007, AN100 to AN120 | Input | Input pins for the analog signals to be processed by the A/D converter |
| | ADTRG0#, ADTRG1# | Input | Input pins for the external trigger signals that start the A/D conversion |
| | ANEX0 | Output | Extended analog output pin |
| | ANEX1 | Input | Extended analog input pin |
| 12-bit D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | AVSS0 | Input | Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VREFH0 | Input | Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used. |
| | VREFL0 | Input | Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used. |



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**Table 1.4 Pin Functions (8/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Analog power supply | AVCC1 | Input | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | AVSS1 | Input | Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins |
| | P10 to P17 | I/O | 8-bit input/output pins |
| | P20 to P27 | I/O | 8-bit input/output pins |
| | P30 to P37 | I/O | 8-bit input/output pins (P35: input pin) |
| | P40 to P47 | I/O | 8-bit input/output pins |
| | P50 to P57 | I/O | 8-bit input/output pins |
| | P60 to P67 | I/O | 8-bit input/output pins |
| | P70 to P77 | I/O | 8-bit input/output pins |
| | P80 to P87 | I/O | 8-bit input/output pins |
| | P90 to P97 | I/O | 8-bit input/output pins |
| | PA0 to PA7 | I/O | 8-bit input/output pins |
| | PB0 to PB7 | I/O | 8-bit input/output pins |
| | PC0 to PC7 | I/O | 8-bit input/output pins |
| | PD0 to PD7 | I/O | 8-bit input/output pins |
| | PE0 to PE7 | I/O | 8-bit input/output pins |
| | PF0 to PF5 | I/O | 6-bit input/output pins |
| | PG0 to PG7 | I/O | 8-bit input/output pins |
| | PJ0 to PJ3, PJ5 | I/O | 5-bit input/output pins |
| | PH0 to PH7 | I/O | 8-bit input/output pins |
| | PK0 to PK7 | I/O | 8-bit input/output pins |
| | PL0 to PL7 | I/O | 8-bit input/output pins |
| | PM0 to PM7 | I/O | 8-bit input/output pins |
| | PN0 to PN5 | I/O | 6-bit input/output pins |
| | PQ0 to PQ7 | I/O | 8-bit input/output pins |

Note: Note the following regarding pin names. For details, refer to section 1.5, Pin Assignments.
- We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups.
  For the RSPI, QSPI, SDHI, MMC, and GLCDC interfaces, the AC portion of the electrical characteristics is measured for each group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC pin functions that have [FM+] appended to their names support fast-mode plus.



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## 1.5 Pin Assignments

### 1.5.1 224-Pin LFBGA

RX66N Group
PLBG0224GA-A (224-pin LFBGA)
(Upper Perspective View)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | P70 | PE7 | P66 | P67 | PG4 | PG7 | PA4 | PA5 | PA7 | P72 | PB4 | PB6 | PB7 | PM3 | PM5 | 15 |
| 14 | PE1 | PE4 | P65 | PG2 | PG5 | PG6 | PA3 | PA6 | PB0 | PB3 | PB2 | PC0 | PC1 | PM4 | P74 | 14 |
| 13 | P62 | PE2 | PE5 | VSS | PE6 | PG3 | PA2 | VSS | P71 | PB5 | VCC | PM7 | PM6 | PC2 | P75 | 13 |
| 12 | P61 | P63 | VSS | PE3 | VCC | PA0 | PA1 | VCC | PB1 | VSS | PN4 | PL6 | P76 | PL2 | PL4 | 12 |
| 11 | PD7 | VCC | P64 | PE0 | PQ4 | PM1 | PM0 | PL0 | PN5 | PM2 | P77 | PL5 | PK2 | PC4 | PC3 | 11 |
| 10 | PG0 | PD6 | P60 | PG1 | PQ5 | VSS | VCC | P73 | PL1 | PL3 | PL7 | PK0 | P80 | P82 | PC5 | 10 |
| 9 | PD3 | PD4 | P97 | PD5 | PQ3 | PQ6 | PN2 | PN3 | PK3 | PK1 | P81 | P83 | PC7 | VSS | PC6 | 9 |
| 8 | P96 | P95 | VCC | VSS | PQ1 | PN1 | PQ2 | PQ7 | P53*1 | P50 | P52 | P51 | VCC | P11 | P55 | 8 |
| 7 | PD2 | P94 | PD1 | P93 | PQ0 | PK6 | RES# | PJ3 | P15 | P10 | VCC | VSS | P56 | P57 | P54 | 7 |
| 6 | PD0 | VCC | P90 | P02 | PN0 | EMLE | PF5 | BSCANP | PH2 | PH1 | PJ2 | P84 | PJ1 | VSS_USB | USB0_DP | 6 |
| 5 | P92 | P91 | VSS | P01 | P07 | PK5 | PJ5 | P32 | P30 | PF0 | VCC | PJ0 | P13 | VCC_USB | USB0_DM | 5 |
| 4 | P41 | P46 | P44 | P40 | P43 | PK4 | MD/FINED | P33 | P31 | PH5 | P24 | VSS | P85 | P14 | P12 | 4 |
| 3 | VREFL0 | P42 | P05 | P03 | P00 | PF4 | VCC | P35 | PF3 | PH4 | PF1 | P25 | P86 | P20 | P16 | 3 |
| 2 | VREFH0 | AVCC0 | AVCC1 | P47 | VSS | VBATT | VSS | P34 | PF2 | PH6 | P27 | P23 | PH0 | P17 | P87 | 2 |
| 1 | NC | AVSS0 | AVSS1 | P45 | VCL | XCIN | XCOUT | XTAL | EXTAL | PH7 | PH3 | P26 | P22 | PK7 | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

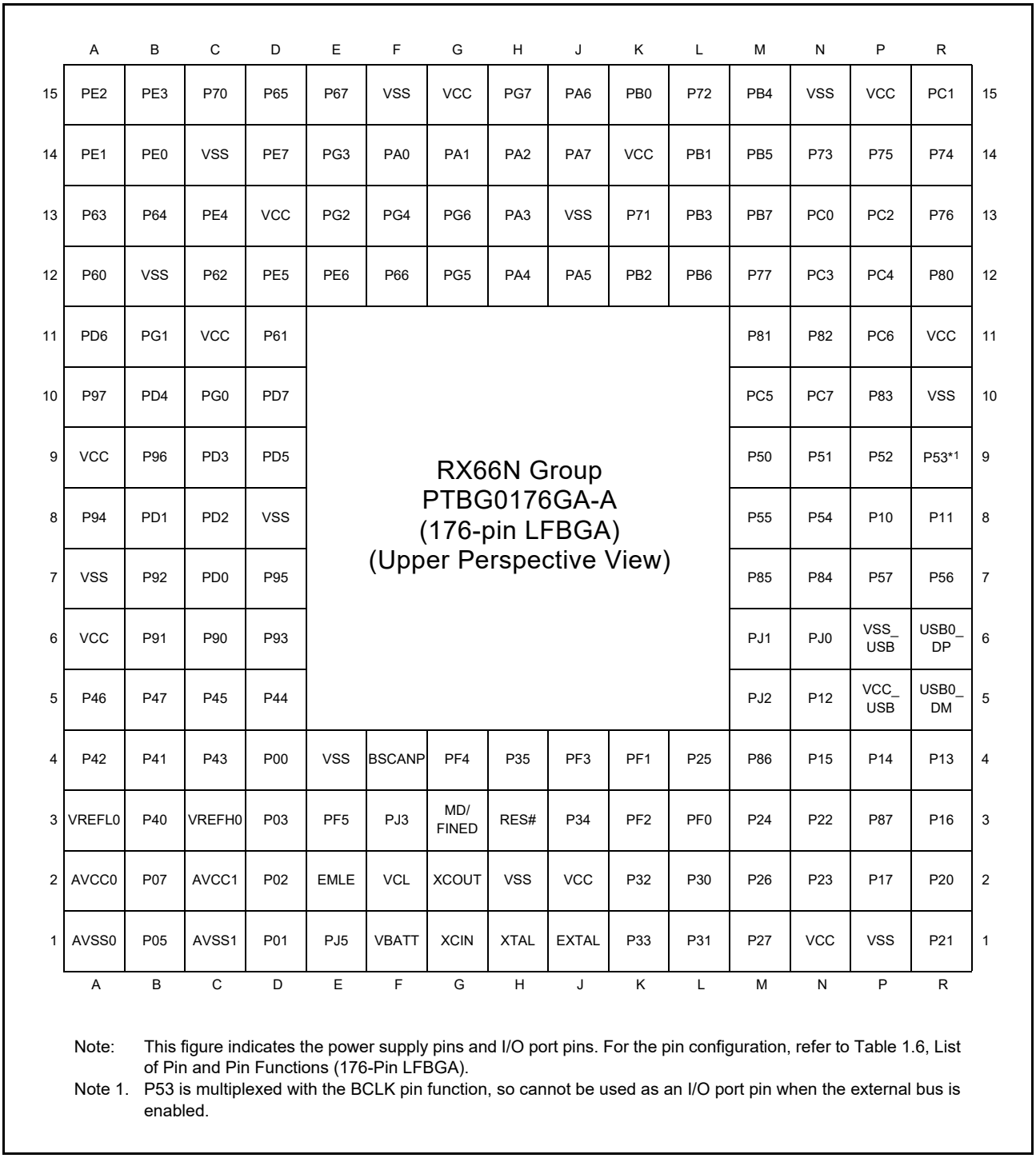
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.5, List of Pin and Pin Functions (224-Pin LFBGA).
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.3 Pin Assignment (224-Pin LFBGA)**



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## 1.5.2 176-Pin LFBGA




| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE2 | PE3 | P70 | P65 | P67 | VSS | VCC | PG7 | PA6 | PB0 | P72 | PB4 | VSS | VCC | PC1 | 15 |
| 14 | PE1 | PE0 | VSS | PE7 | PG3 | PA0 | PA1 | PA2 | PA7 | VCC | PB1 | PB5 | P73 | P75 | P74 | 14 |
| 13 | P63 | P64 | PE4 | VCC | PG2 | PG4 | PG6 | PA3 | VSS | P71 | PB3 | PB7 | PC0 | PC2 | P76 | 13 |
| 12 | P60 | VSS | P62 | PE5 | PE6 | P66 | PG5 | PA4 | PA5 | PB2 | PB6 | P77 | PC3 | PC4 | P80 | 12 |
| 11 | PD6 | PG1 | VCC | P61 | | | | | | | | P81 | P82 | PC6 | VCC | 11 |
| 10 | P97 | PD4 | PG0 | PD7 | | | | | | | | PC5 | PC7 | P83 | VSS | 10 |
| 9 | VCC | P96 | PD3 | PD5 | | | | | | | | P50 | P51 | P52 | P53*1 | 9 |
| 8 | P94 | PD1 | PD2 | VSS | | | | | | | | P55 | P54 | P10 | P11 | 8 |
| 7 | VSS | P92 | PD0 | P95 | | | | | | | | P85 | P84 | P57 | P56 | 7 |
| 6 | VCC | P91 | P90 | P93 | | | | | | | | PJ1 | PJ0 | VSS_ USB | USB0_ DP | 6 |
| 5 | P46 | P47 | P45 | P44 | | | | | | | | PJ2 | P12 | VCC_ USB | USB0_ DM | 5 |
| 4 | P42 | P41 | P43 | P00 | VSS | BSCANP | PF4 | P35 | PF3 | PF1 | P25 | P86 | P15 | P14 | P13 | 4 |
| 3 | VREFL0 | P40 | VREFH0 | P03 | PF5 | PJ3 | MD/ FINED | RES# | P34 | PF2 | PF0 | P24 | P22 | P87 | P16 | 3 |
| 2 | AVCC0 | P07 | AVCC1 | P02 | EMLE | VCL | XCOUT | VSS | VCC | P32 | P30 | P26 | P23 | P17 | P20 | 2 |
| 1 | AVSS0 | P05 | AVSS1 | P01 | PJ5 | VBATT | XCIN | XTAL | EXTAL | P33 | P31 | P27 | VCC | VSS | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.6, List of Pin and Pin Functions (176-Pin LFBGA).

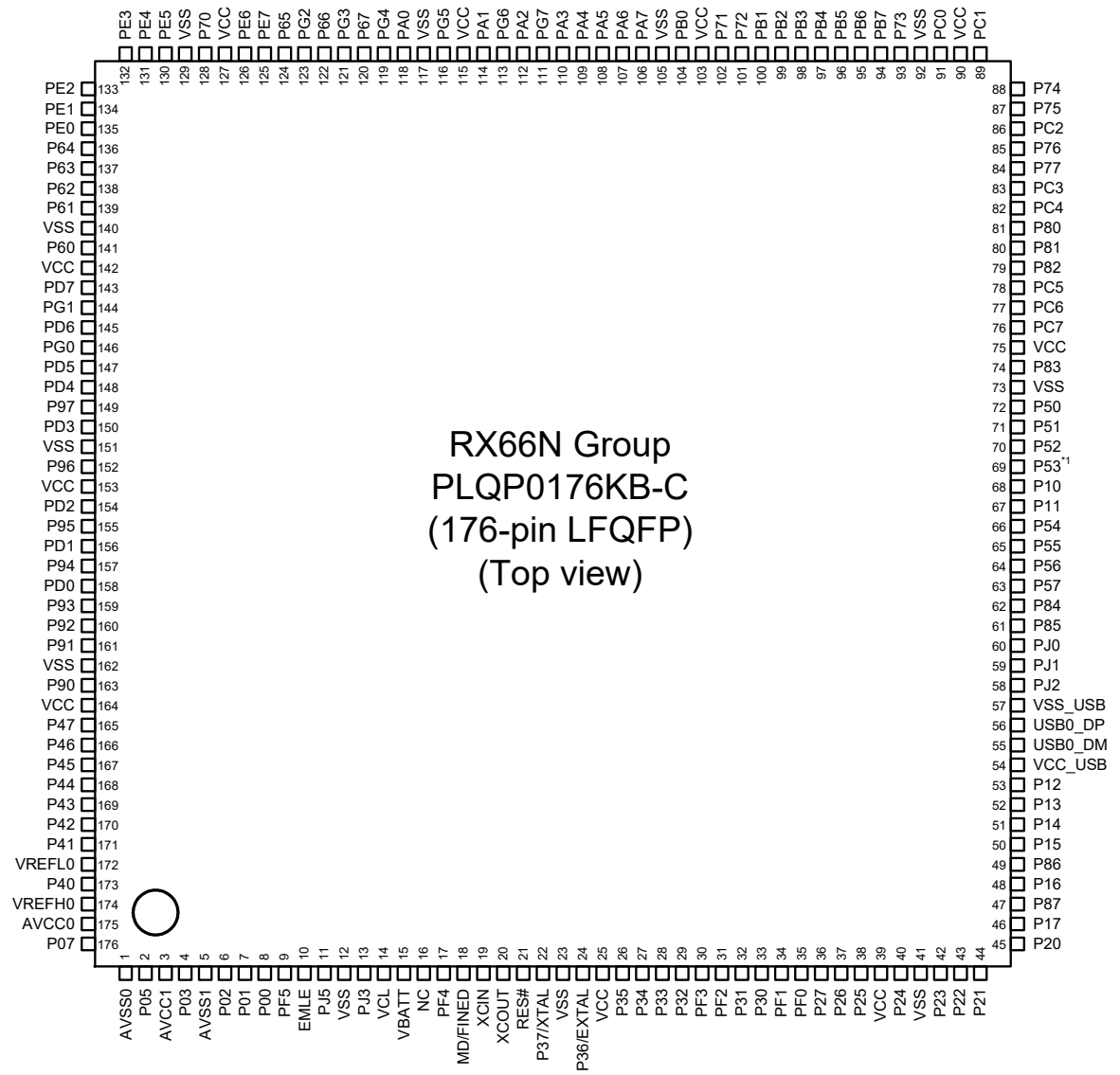
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.4 Pin Assignment (176-Pin LFBGA)**



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### 1.5.3 176-Pin LFQFP




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.7, List of Pin and Pin Functions (176-Pin LFQFP).

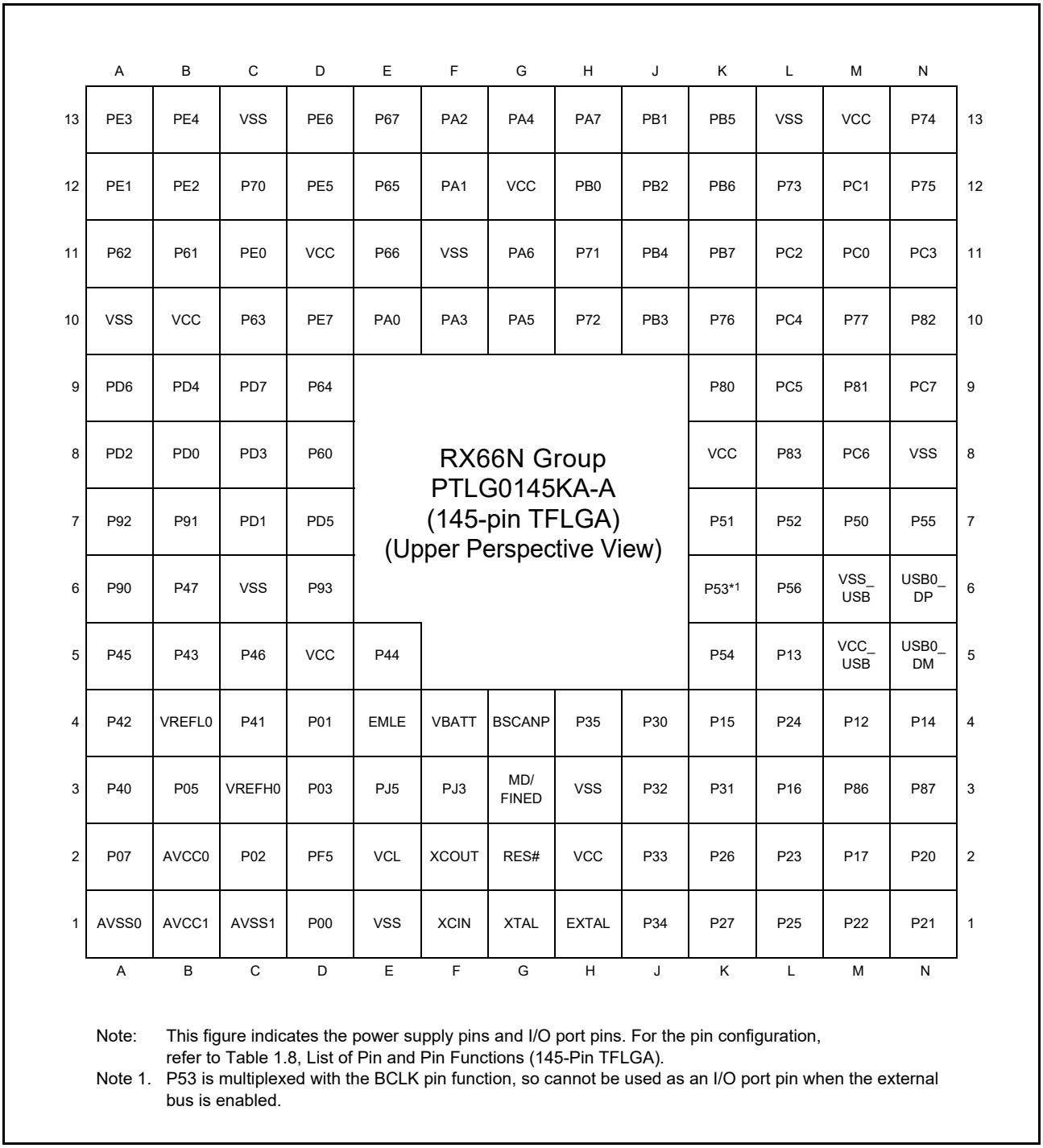
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.5 Pin Assignment (176-Pin LFQFP)**



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## 1.5.4 145-Pin TFLGA




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.8, List of Pin and Pin Functions (145-Pin TFLGA).

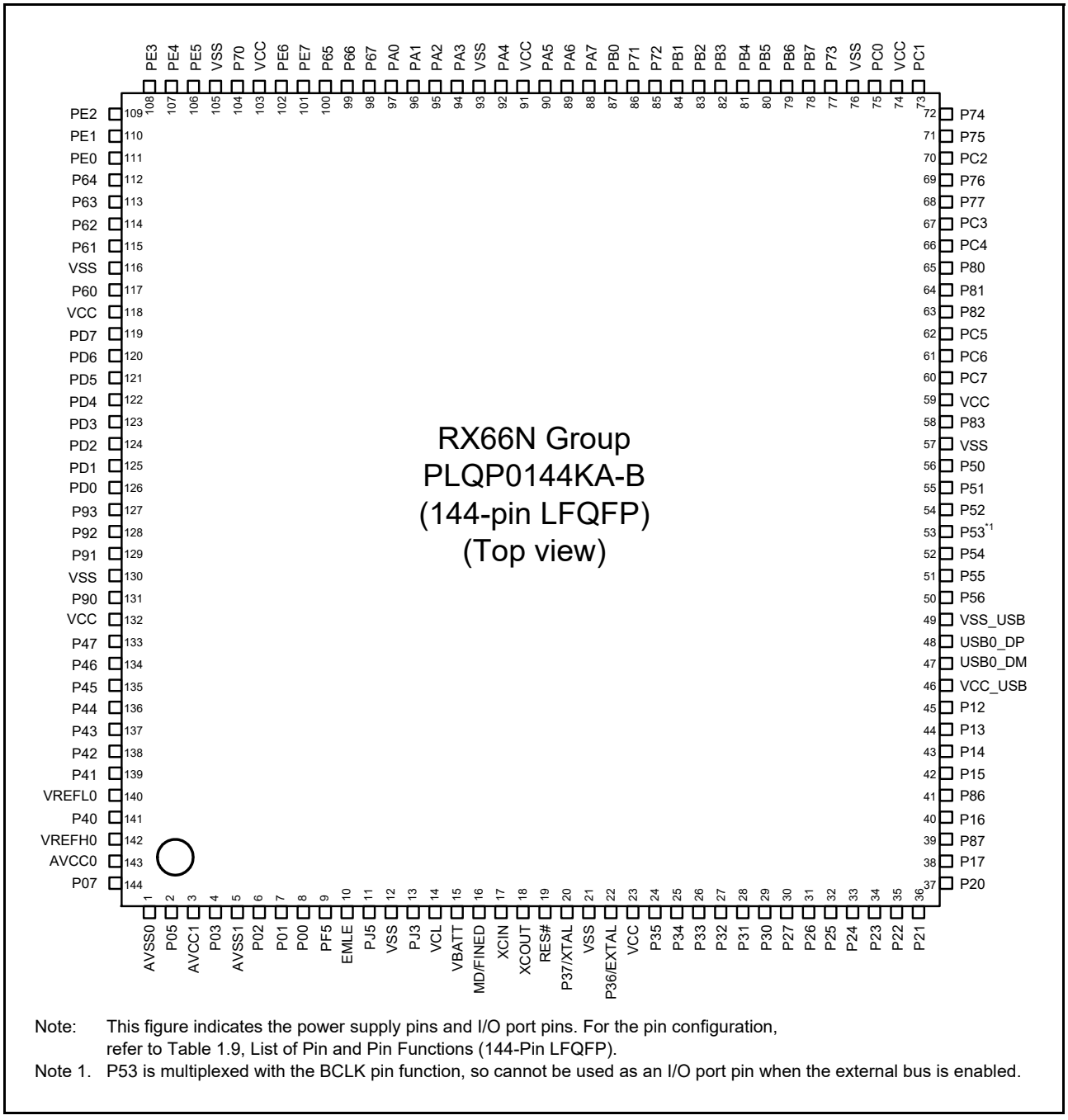
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.6 Pin Assignment (145-Pin TFLGA)**



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### 1.5.5 144-Pin LFQFP




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.9, List of Pin and Pin Functions (144-Pin LFQFP).

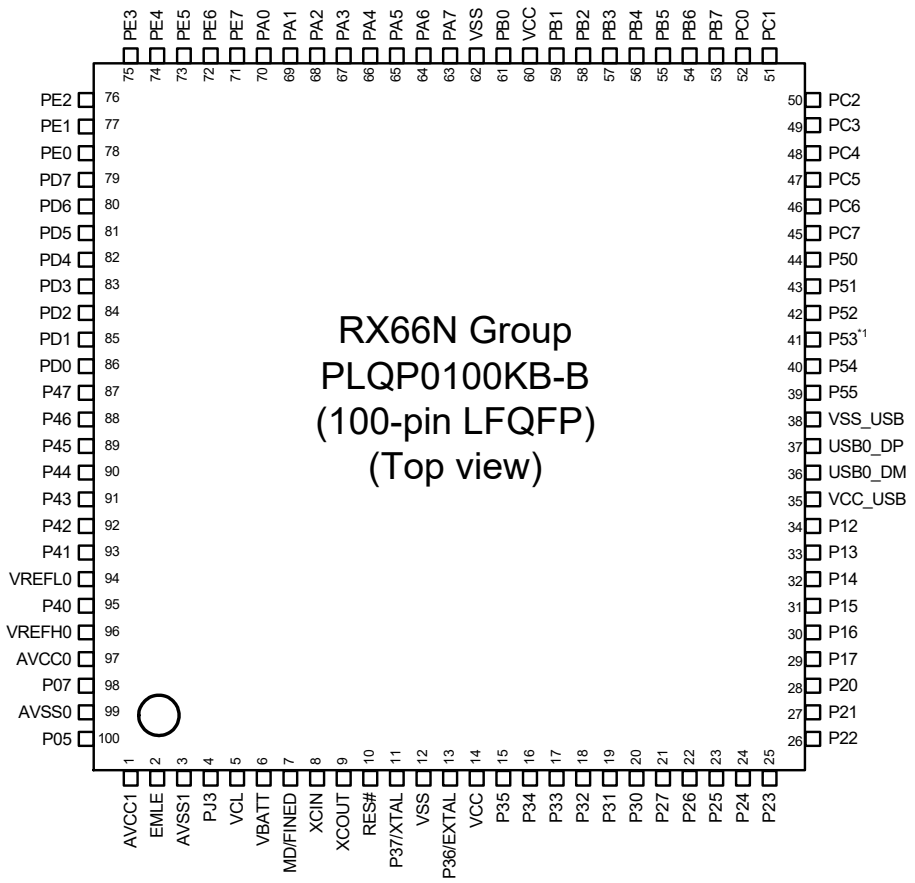
Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.7 Pin Assignment (144-Pin LFQFP)**



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### 1.5.6 100-Pin LFQFP




Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.10, List of Pin and Pin Functions (100-Pin LFQFP).

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

**Figure 1.8 Pin Assignment (100-Pin LFQFP)**



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## 1.6 List of Pin and Pin Functions

### 1.6.1 224-Pin LFBGA

**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (1/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| A1 | NC | | | | | | | | | | |
| A2 | VREFH0 | | | | | | | | | | |
| A3 | VREFL0 | | | | | | | | | | |
| A4 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| A5 | | P92 | D18/A18 | POE4# | | RXD7/ SMISO7/ SSCL7 | | | | | AN116 |
| A6 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXT CLK-B | IRQ0 | AN108 |
| A7 | | PD2 | D2[A2/D2] | MTIOC4D/ TIC2 | GTIOC0B | MISOC-A/ CRX0 | | QIO2-B/ SDHI_D2-B/ MMC_D2-B | LCD_DAT A22-B | IRQ2 | AN110 |
| A8 | TRDATA5 | P96 | D22/A22 | | | | | | | | |
| A9 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/ SDHI_D3-B/ MMC_D3-B | LCD_DAT A21-B | IRQ3 | AN111 |
| A10 | TRDATA6 | PG0 | D24 | | | | | | | | |
| A11 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | SSLC3-A | | QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B | LCD_DAT A17-B | IRQ7 | AN107 |
| A12 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | | | |
| A13 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | | | |
| A14 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | GTIOC1B | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B | | MMC_D5-B | LCD_DAT A15-B | | ANEX1 |
| A15 | | P70 | SDCLK | | | | | | | | |
| B1 | AVSS0 | | | | | | | | | | |
| B2 | AVCC0 | | | | | | | | | | |
| B3 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| B4 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| B5 | | P91 | D17/A17 | | | SCK7 | | | | | AN115 |
| B6 | VCC | | | | | | | | | | |
| B7 | | P94 | D20/A20 | | | | | | | | |
| B8 | TRDATA4 | P95 | D21/A21 | | | | | | | | |
| B9 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | | SSLC0-A | | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DAT A20-B | IRQ4 | AN112 |
| B10 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B | LCD_DAT A18-B | IRQ6 | AN106 |
| B11 | VCC | | | | | | | | | | |
| B12 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (2/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| B13 | | PE2 | D10[A10/D10]/D2[A2/D2] | MTIOC4A/PO23/TIC3 | GTIOC0B | RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| B14 | | PE4 | D12[A12/D12]/D4[A4/D4] | MTIOC4D/MTIOC1A/PO28 | GTIOC1A | SSLB0-B | ET0_ERXD2 | | LCD_DATA12-B | | AN102 |
| B15 | | PE7 | D15[A15/D15]/D7[A7/D7] | MTIOC6A/TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| C1 | AVSS1 | | | | | | | | | | |
| C2 | AVCC1 | | | | | | | | | | |
| C3 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |
| C4 | | P44 | | | | | | | | IRQ12-DS | AN004 |
| C5 | VSS | | | | | | | | | | |
| C6 | | P90 | D16/A16 | | | TXD7/SMOSI7/SSDA7 | | | | | AN114 |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B/POE0# | GTIOC1A | MOSIC-A/CTX0 | | | LCD_DATA23-B | IRQ1 | AN109 |
| C8 | VCC | | | | | | | | | | |
| C9 | TRSYNC1 | P97 | D23/A23 | | | | | | | | |
| C10 | | P60 | CS0# | | | | | | | | |
| C11 | | P64 | WE#/D3[A3/D3]/CS4# | | | | | | | | |
| C12 | VSS | | | | | | | | | | |
| C13 | | PE5 | D13[A13/D13]/D5[A5/D5] | MTIOC4C/MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_CLK/REF50CK0 | | LCD_DATA11-B | IRQ5 | AN103 |
| C14 | | P65 | CKE/CS5# | | | | | | | | |
| C15 | | P66 | DQM0/CS6# | MTIOC7D | GTIOC2B | CTX2 | | | | | |
| D1 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| D2 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| D3 | | P03 | | | | SSIDATA1 | | | | IRQ11 | DA0 |
| D4 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| D5 | | P01 | | TMCI0 | | RXD6/SMISO6/SSCL6/SSIBCK0 | | QIO3-C | | IRQ9 | AN119 |
| D6 | | P02 | | TMCI1 | | SCK6/SSIBCK1 | | | | IRQ10 | AN120 |
| D7 | | P93 | D19/A19 | POE0# | | CTS7#/RTS7#/SS7# | | | | | AN117 |
| D8 | VSS | | | | | | | | | | |
| D9 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/MTCLKA/POE10# | | SSLC1-A | | QSPCLK-B/SDHI_CLK-B/MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| D10 | TRDATA7 | PG1 | D25 | | | | | | | | |
| D11 | | PE0 | D8[A8/D8]/D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| D12 | | PE3 | D11[A11/D11]/D3[A3/D3] | MTIOC4B/PO26/TOC3/POE8# | GTIOC2A | CTS12#/RTS12#/SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| D13 | VSS | | | | | | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (3/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| D14 | TRDATA0 | PG2 | D26 | | | | | | | | |
| D15 | | P67 | DQM1/ CS7# | MTIOC7C | GTIOC1B | CRX2 | | | | IRQ15 | |
| E1 | VCL | | | | | | | | | | |
| E2 | VSS | | | | | | | | | | |
| E3 | | P00 | | TMRI0 | | TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK | | QIO2-C | | IRQ8 | AN118 |
| E4 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| E5 | | P07 | | | | | | | | IRQ15 | ADTRG0# |
| E6 | | PN0 | | | | | | | | | |
| E7 | | PQ0 | | | | SCK11 | | | | | |
| E8 | | PQ1 | | | | SMISO11/ SSCL11/ RXD11 | | | | | |
| E9 | | PQ3 | | | | RTS11#/ CTS11#/ SS11# | | | | | |
| E10 | | PQ5 | | | | | | | | | |
| E11 | | PQ4 | | | | | | | | | |
| E12 | VCC | | | | | | | | | | |
| E13 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/ TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/ MMC_CD-B | LCD_DAT A10-B | IRQ6 | AN104 |
| E14 | TRCLK | PG5 | D29 | | | | | | | | |
| E15 | TRSYNC | PG4 | D28 | | | | | | | | |
| F1 | XCIN | | | | | | | | | | |
| F2 | VBATT | | | | | | | | | | |
| F3 | TRST# | PF4 | | | | | | | | | |
| F4 | | PK4 | | | GTADSM0 | SSLB1 | ET0_ERXD 2 | | | | |
| F5 | | PK5 | | | GTADSM1 | SSLB2 | ET0_ERXD 3 | | | | |
| F6 | EMLE | | | | | | | | | | |
| F7 | | PK6 | | | GTIOC1A | SSLB3 | | | | | |
| F8 | | PN1 | | | | | | | | | |
| F9 | | PQ6 | | | | | | | | | |
| F10 | VSS | | | | | | | | | | |
| F11 | | PM1 | | TOC3 | GTETRGB | SMISO10/ SSCL10/ RXD10 | | SDHI_CMD-D/ QSSL-A | | | |
| F12 | | PA0 | DQM2/ BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_E N/ RMII0_TXD _EN | | LCD_DAT A8-B | | |
| F13 | TRDATA1 | PG3 | D27 | | | | | | | | |
| F14 | TRDATA2 | PG6 | D30 | | | | | | | | |
| F15 | TRDATA3 | PG7 | D31 | | | | | | | | |
| G1 | XCOUT | | | | | | | | | | |
| G2 | VSS | | | | | | | | | | |
| G3 | VCC | | | | | | | | | | |
| G4 | MD/FINED | | | | | | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (4/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| G5 | | PJ5 | | POE8# | | CTS2#/ RTS2#/ SS2#/ SSIRXD0 | | QMI-C/QIO1-C | | | |
| G6 | | PF5 | WAIT# | | | SSILRCK0 | | | | IRQ4 | |
| G7 | RES# | | | | | | | | | | |
| G8 | | PQ2 | | | | SMOSI11/ SSDA11/ TXD11 | | | | | |
| G9 | | PN2 | | | | | | | | | |
| G10 | VCC | | | | | | | | | | |
| G11 | | PM0 | | TIC3 | GTETRGA | SCK10 | | SDHI_CLK-D/ QSPCLK-A | | | |
| G12 | | PA1 | DQM3/A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DATA7-B | IRQ11 | |
| G13 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DATA6-B | | |
| G14 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO / PMGI0_MDIO | | LCD_DATA5-B | IRQ6-DS | |
| G15 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MDC | | LCD_DATA4-B | IRQ5-DS | |
| H1 | XTAL | P37 | | | | | | | | | |
| H2 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| H3 | UPSEL | P35 | | | | | | | | NMI | |
| H4 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | PCKO | | IRQ3-DS | |
| H5 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN | | VSYNC | | IRQ2-DS | |
| H6 | BSCANP | | | | | | | | | | |
| H7 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | QMO-C/QIO0-C | | | |
| H8 | | PQ7 | | | | | | | | | |
| H9 | | PN3 | | | | | | | | | |
| H10 | | P73 | CS3# | PO16 | | | ET0_WOL | | LCD_EXTCLK-A | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (5/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| H11 | | PL0 | | TIC2 | GTETRGA | SCK9/ RSPCKC | ET0_ERXD 0/ RMII0_RX D0 | | | | |
| H12 | VCC | | | | | | | | | | |
| H13 | VSS | | | | | | | | | | |
| H14 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOU T | | LCD_DAT A2-B | | |
| H15 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINK STA | | LCD_DAT A3-B | | |
| J1 | EXTAL | P36 | | | | | | | | | |
| J2 | TDI | PF2 | | | | RXD1/ SMISO1/ SSCL1 | | | | | |
| J3 | TMS | PF3 | | | | | | | | | |
| J4 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |
| J5 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| J6 | | PH2 | | | GTETRG C | SMOSI7/ SSDA7/ TXD7/MISOA | | | | | |
| J7 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/CRX1-DS/ SSILRCK1 | | PIXD0 | | IRQ5 | |
| J8 | | P53*1 | BCLK | | | | | | | | |
| J9 | | PK3 | | | GTETRG D | RTS8#/ CTS8#/ SS8#/SSLB0 | ET0_TX_E R | | | | |
| J10 | | PL1 | | TOC2 | GTETRGB | SMISO9/ SSCL9/ RXD9/ MOSIC | ET0_ERXD 1/ RMII0_RX D1 | | | | |
| J11 | | PN5 | | | | | | QSSL-C | | | |
| J12 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6 | ET0_ERXD 0/ RMII0_RX D0 | | LCD_TCO N3-B | IRQ4-DS | |
| J13 | | P71 | A18/CS1# | | | | ET0_MDIO / PMGI0_MD IO | | | | |
| J14 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6 | ET0_ERXD 1/ RMII0_RX D1 | | LCD_DAT A0-B | IRQ12 | |
| J15 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DAT A1-B | | |
| K1 | CLKOUT2 5M | PH7 | | | GTIOC0B | | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (6/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| K2 | CLKOUT | PH6 | | | GTIOC0A | SSLA3 | | | | | |
| K3 | | PH4 | | | GTADSM0 | SSLA1 | | | | | |
| K4 | | PH5 | | | GTADSM1 | SSLA2 | | | | | |
| K5 | TDO | PF0 | | | | TXD1/ SMOSI1/ SSDA1 | | | | | |
| K6 | | PH1 | | TOC0 | GTETRGB | SMISO7/ SSCL7/ RXD7/ MOSIA | | | | | |
| K7 | | P10 | ALE | MTIC5W/ TMRI3 | | | | | | IRQ0 | |
| K8 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |
| K9 | | PK1 | | TOC1 | GTETRGB | SMISO8/ SSCL8/ RXD8/ MOSIB | ET0_COL | | | | |
| K10 | | PL3 | | | GTETRGD | RTS9#/ CTS9#/ SS9#/SSLC0 | ET0_RX_CLK/ REF50CK0 | | | | |
| K11 | | PM2 | | | GTETRGC | SMOSI10/ SSDA10/ TXD10 | | SDHI_D0-D/ QMO-A/QIO0-A | | | |
| K12 | VSS | | | | | | | | | | |
| K13 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD0/ RMII0_TXD0 | | LCD_CLK-B | | |
| K14 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK4/SCK6 | ET0_RX_ER/ RMII0_RX_ER | | LCD_TCON1-B | | |
| K15 | | P72 | A19/CS2# | | | | ET0_MDC/ PMGI0_MDC | | LCD_DATA23-A | | |
| L1 | | PH3 | | | GTETRGD | RTS7#/ CTS7#/ SS7#/SSLA0 | | | | | |
| L2 | | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| L3 | TCK | PF1 | | | | SCK1 | | | | | |
| L4 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUSEN/SSIBCK1 | | SDHI_WP/ PIXCLK | | | |
| L5 | VCC | | | | | | | | | | |
| L6 | CLKOUT25M | PJ2 | | | | TXD8/ SMOSI8/ SSDA8/ SSLC3-B | | | LCD_TCON2-A | | |
| L7 | VCC | | | | | | | | | | |
| L8 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (7/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| L9 | | P81 | EDACK0 | MTIOC3D/ PO27 | GTIOC0B | SMISO10/ SSCL10/ RXD10 | ET0_ETXD0/ RMII0_TXD0 | QIO3-A/ SDHI_CD/ MMC_D3-A | LCD_DATA13-A | | |
| L10 | | PL7 | | | GTIOC2B | | ET0_MDIO/ PMGI0_MDIO | | | | |
| L11 | | P77 | CS7# | PO23 | | SMOSI11/ SSDA11/ TXD11 | ET0_RX_ER/ RMII0_RX_ER | QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A | LCD_DATA17-A | | |
| L12 | | PN4 | | | | | | QSPCLK-C | | | |
| L13 | VCC | | | | | | | | | | |
| L14 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/SS6# | ET0_RX_CLK/ REF50CK0 | | LCD_TCON2-B | | |
| L15 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_EN/ RMII0_TXD_EN | | LCD_TCON0-B | | |
| M1 | | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |
| M2 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | SDHI_D1-C/ PIXD7 | | | |
| M3 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | SDHI_CD/ HSYNC | | | ADTRG0# |
| M4 | VSS | | | | | | | | | | |
| M5 | | PJ0 | | MTIOC6B | | SCK8/ SSLC1-B | | | LCD_DATA0-A | | |
| M6 | | P84 | | MTIOC6D | | | | | LCD_DATA2-A | | |
| M7 | VSS | | | | | | | | | | |
| M8 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |
| M9 | | P83 | EDACK1 | MTIOC4C | GTIOC0A | SCK10/ SS10#/ CTS10# | ET0_CRS/ RMII0_CRS_DV | | LCD_DATA8-A | | |
| M10 | | PK0 | | TIC1 | GTETRGA | SCK8/ RSPCKB | ET0_MDC/ PMGI0_MDC | | | | |
| M11 | | PL5 | | | GTADSM1 | SSLC2 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| M12 | | PL6 | | | GTIOC2A | SSLC3 | ET0_TX_EN/ RMII0_TXD_EN | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (8/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| M13 | | PM7 | | | GTIOC3B | | ET0_CRS/ RMII0_CRS_DV | SDHI_WP | | | |
| M14 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |
| M15 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| N1 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRCURB/ AUDIO_CLK | | SDHI_D0-C/ PIXD6 | | | |
| N2 | | PH0 | | TIC0 | GTETRGA | SCK7/ RSPCKA | | | | | |
| N3 | | P86 | | MTIOC4D/ TIOCA0 | GTIOC2B | SMISO10/ SSCL10/ RXD10 | | PIXD1 | | | |
| N4 | | P85 | | MTIOC6C/ TIOCC0 | | | | | LCD_DATA1-A | | |
| N5 | | P13 | WR2#/BC2# | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | LCD_TCON0-A | IRQ3 | ADTRG1# |
| N6 | | PJ1 | | MTIOC6A | | RXD8/ SMISO8/ SSCL8/ SSLC2-B | | | LCD_TCON3-A | | |
| N7 | CLKOUT25M | P56 | EDACK1 | MTIOC3C/ TIOCA1 | | SCK7/ RSPCKC-B | | | LCD_DATA4-A | | |
| N8 | VCC | | | | | | | | | | |
| N9 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| N10 | | P80 | EDREQ0 | MTIOC3B/ PO26 | | SCK10/ RTS10# | ET0_TX_EN/ RMII0_TXD_EN | QIO2-A/ SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| N11 | | PK2 | | | GTETRGC | SMOSI8/ SSDA8/ TXD8/MISOB | ET0_RX_DV | | | | |
| N12 | | P76 | CS6# | PO22 | | SMISO11/ SSCL11/ RXD11 | ET0_RX_CLK/ REF50CK0 | QSSL-A/ SDHI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| N13 | | PM6 | | | GTIOC3A | | ET0_TX_CLK | SDHI_CD | | | |
| N14 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD2 | | LCD_DATA22-A | IRQ12 | |
| N15 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CRS_DV | | | | |
| P1 | | PK7 | | | GTIOC1B | | | | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (9/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| P2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | SDHI_D3-C/ PIXD3 | | IRQ7 | ADTRG1# |
| P3 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0 | | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| P4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRGD | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | LCD_CLK-A | IRQ4 | |
| P5 | VCC_USB | | | | | | | | | | |
| P6 | VSS_USB | | | | | | | | | | |
| P7 | | P57 | | | | RXD7/ SMISO7/ SSCL7/ SSLC0-B | | | LCD_DATA3-A | | |
| P8 | | P11 | | MTIC5V/ TMCI3 | | SCK2 | | | LCD_DATA7-A | IRQ1 | |
| P9 | VSS | | | | | | | | | | |
| P10 | | P82 | EDREQ1 | MTIOC4A/ PO28 | GTIOC2A | SMOSI10/ SSDA10/ TXD10 | ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | LCD_DATA12-A | | |
| P11 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |
| P12 | | PL2 | | | GTETRGC | SMOSI9/ SSDA9/ TXD9/ MISOC | ET0_RX_ER/ RMII0_RX_ER | | | | |
| P13 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | SDHI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| P14 | | PM4 | | | GTADSM0 | | ET0_ETXD2 | SDHI_D2-D/ QIO2-A | | | |
| P15 | | PM3 | | | GTETRGD | RTS10#/ CTS10#/ SS10# | | SDHI_D1-D/ QMI-A/QIO1-A | | | |
| R1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SSILRCK0 | | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| R2 | | P87 | | MTIOC4C/ TIOCA2 | GTIOC1B | SMOSI10/ SSDA10/ TXD10 | | SDHI_D2-C/ PIXD2 | | | |



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**Table 1.5 List of Pin and Pin Functions (224-Pin LFBGA) (10/10)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 224-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| R3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | | IRQ6 | ADTRG0# |
| R4 | | P12 | WR3#/BC3# | MTIC5U/ TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | LCD_TCON1-A | IRQ2 | |
| R5 | | | | | | USB0_DM | | | | | |
| R6 | | | | | | USB0_DP | | | | | |
| R7 | | P54 | D1[A1/D1]/ EDACK0/ ALE | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1 | ET0_LINKSTA | | LCD_DATA6-A | | |
| R8 | | P55 | D0[A0/D0]/ EDREQ0/ WAIT# | MTIOC4D/ TMO3 | | TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1 | ET0_EXOUT | | LCD_DATA5-A | IRQ10 | |
| R9 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| R10 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD2 | MMC_D5-A | LCD_DATA11-A | | |
| R11 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_ER | QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| R12 | | PL4 | | | GTADSM0 | SSLC1 | ET0_ETXD0/ RMII0_TXD0 | | | | |
| R13 | | P75 | CS5# | PO20 | | SCK11/ RTS11# | ET0_ERXD0/ RMII0_RXD0 | SDHI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| R14 | | P74 | A20/CS4# | PO19 | | SS11#/ CTS11# | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA21-A | | |
| R15 | | PM5 | | | GTADSM1 | | ET0_ETXD3 | SDHI_D3-D/ QIO3-A | | | |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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## 1.6.2 176-Pin LFBGA

**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (1/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| A1 | AVSS0 | | | | | | | | | | |
| A2 | AVCC0 | | | | | | | | | | |
| A3 | VREFL0 | | | | | | | | | | |
| A4 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| A5 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| A6 | VCC | | | | | | | | | | |
| A7 | VSS | | | | | | | | | | |
| A8 | | P94 | D20/A20 | | | | | | | | |
| A9 | VCC | | | | | | | | | | |
| A10 | TRSYNC1 | P97 | D23/A23 | | | | | | | | |
| A11 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| A12 | | P60 | CS0# | | | | | | | | |
| A13 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | | | |
| A14 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | GTIOC1B | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B | | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| A15 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | GTIOC0B | RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| B1 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |
| B2 | | P07 | | | | | | | | IRQ15 | ADTRG0# |
| B3 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| B4 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| B5 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| B6 | | P91 | D17/A17 | | | SCK7 | | | | | AN115 |
| B7 | | P92 | D18/A18 | POE4# | | RXD7/ SMISO7/ SSCL7 | | | | | AN116 |
| B8 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | GTIOC1A | MOSIC-A/ CTX0 | | | LCD_DATA23-B | IRQ1 | AN109 |
| B9 | TRDATA5 | P96 | D22/A22 | | | | | | | | |
| B10 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | | SSLC0-A | | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| B11 | TRDATA7 | PG1 | D25 | | | | | | | | |
| B12 | VSS | | | | | | | | | | |
| B13 | | P64 | WE#/D3[A3/ D3]/CS4# | | | | | | | | |
| B14 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/ SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| B15 | | PE3 | D11[A11/ D11]/D3[A3/ D3] | MTIOC4B/ PO26/TOC3/ POE8# | GTIOC2A | CTS12#/ RTS12#/ SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| C1 | AVSS1 | | | | | | | | | | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (2/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| C2 | AVCC1 | | | | | | | | | | |
| C3 | VREFH0 | | | | | | | | | | |
| C4 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| C5 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| C6 | | P90 | D16/A16 | | | TXD7/ SMOSI7/ SSDA7 | | | | | AN114 |
| C7 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXT CLK-B | IRQ0 | AN108 |
| C8 | | PD2 | D2[A2/D2] | MTIOC4D/ TIC2 | GTIOC0B | MISOC-A/ CRX0 | | QIO2-B/ SDHI_D2-B/ MMC_D2-B | LCD_DAT A22-B | IRQ2 | AN110 |
| C9 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/ SDHI_D3-B/ MMC_D3-B | LCD_DAT A21-B | IRQ3 | AN111 |
| C10 | TRDATA6 | PG0 | D24 | | | | | | | | |
| C11 | VCC | | | | | | | | | | |
| C12 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | | | |
| C13 | | PE4 | D12[A12/ D12]/D4[A4/ D4] | MTIOC4D/ MTIOC1A/ PO28 | GTIOC1A | SSLB0-B | ET0_ERXD 2 | | LCD_DAT A12-B | | AN102 |
| C14 | VSS | | | | | | | | | | |
| C15 | | P70 | SDCLK | | | | | | | | |
| D1 | | P01 | | TMCI0 | | RXD6/ SMISO6/ SSCL6/ SSIBCK0 | | | | IRQ9 | AN119 |
| D2 | | P02 | | TMCI1 | | SCK6/ SSIBCK1 | | | | IRQ10 | AN120 |
| D3 | | P03 | | | | SSIDATA1 | | | | IRQ11 | DA0 |
| D4 | | P00 | | TMRI0 | | TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK | | | | IRQ8 | AN118 |
| D5 | | P44 | | | | | | | | IRQ12-DS | AN004 |
| D6 | | P93 | D19/A19 | POE0# | | CTS7#/ RTS7#/SS7# | | | | | AN117 |
| D7 | TRDATA4 | P95 | D21/A21 | | | | | | | | |
| D8 | VSS | | | | | | | | | | |
| D9 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ MTCLKA/ POE10# | | SSLC1-A | | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DAT A19-B | IRQ5 | AN113 |
| D10 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | SSLC3-A | | QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B | LCD_DAT A17-B | IRQ7 | AN107 |
| D11 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | | | |
| D12 | | PE5 | D13[A13/ D13]/D5[A5/ D5] | MTIOC4C/ MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_C LK/ REF50CK0 | | LCD_DAT A11-B | IRQ5 | AN103 |
| D13 | VCC | | | | | | | | | | |
| D14 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/ MMC_RES#-B | LCD_DAT A9-B | IRQ7 | AN105 |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (3/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| D15 | | P65 | CKE/CS5# | | | | | | | | |
| E1 | | PJ5 | | POE8# | | CTS2#/ RTS2#/ SS2#/ SSIRXD0 | | | | | |
| E2 | EMLE | | | | | | | | | | |
| E3 | | PF5 | WAIT# | | | SSILRCK0 | | | | IRQ4 | |
| E4 | VSS | | | | | | | | | | |
| E12 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/ TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/ MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| E13 | TRDATA0 | PG2 | D26 | | | | | | | | |
| E14 | TRDATA1 | PG3 | D27 | | | | | | | | |
| E15 | | P67 | DQM1/ CS7# | MTIOC7C | GTIOC1B | CRX2 | | | | IRQ15 | |
| F1 | VBATT | | | | | | | | | | |
| F2 | VCL | | | | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | | | | |
| F4 | BSCANP | | | | | | | | | | |
| F12 | | P66 | DQM0/ CS6# | MTIOC7D | GTIOC2B | CTX2 | | | | | |
| F13 | TRSYNC | PG4 | D28 | | | | | | | | |
| F14 | | PA0 | DQM2/ BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_EN/ RMII0_TXD_EN | | LCD_DATA8-B | | |
| F15 | VSS | | | | | | | | | | |
| G1 | XCIN | | | | | | | | | | |
| G2 | XCOUT | | | | | | | | | | |
| G3 | MD/FINED | | | | | | | | | | |
| G4 | TRST# | PF4 | | | | | | | | | |
| G12 | TRCLK | PG5 | D29 | | | | | | | | |
| G13 | TRDATA2 | PG6 | D30 | | | | | | | | |
| G14 | | PA1 | DQM3/A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DATA7-B | IRQ11 | |
| G15 | VCC | | | | | | | | | | |
| H1 | XTAL | P37 | | | | | | | | | |
| H2 | VSS | | | | | | | | | | |
| H3 | RES# | | | | | | | | | | |
| H4 | UPSEL | P35 | | | | | | | | NMI | |
| H12 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MDC | | LCD_DATA4-B | IRQ5-DS | |
| H13 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO/ PMGI0_MDIO | | LCD_DATA5-B | IRQ6-DS | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (4/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| H14 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DATA6-B | | |
| H15 | TRDATA3 | PG7 | D31 | | | | | | | | |
| J1 | EXTAL | P36 | | | | | | | | | |
| J2 | VCC | | | | | | | | | | |
| J3 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| J4 | TMS | PF3 | | | | | | | | | |
| J12 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINKSTA | | LCD_DATA3-B | | |
| J13 | VSS | | | | | | | | | | |
| J14 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DATA1-B | | |
| J15 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOUT | | LCD_DATA2-B | | |
| K1 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | PCKO | | IRQ3-DS | |
| K2 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN | | VSYNC | | IRQ2-DS | |
| K3 | TDI | PF2 | | | | RXD1/ SMISO1/ SSCL1 | | | | | |
| K4 | TCK | PF1 | | | | SCK1 | | | | | |
| K12 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/SS6# | ET0_RX_CLK/ REF50CK0 | | LCD_TCON2-B | | |
| K13 | | P71 | A18/CS1# | | | | ET0_MDIO/ PMGI0_MDIO | | | | |
| K14 | VCC | | | | | | | | | | |
| K15 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6 | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA0-B | IRQ12 | |
| L1 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (5/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| L2 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| L3 | TDO | PF0 | | | | TXD1/ SMOSI1/ SSDA1 | | | | | |
| L4 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | SDHI_CD/ HSYNC | | | ADTRG0# |
| L12 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| L13 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK4/SCK6 | ET0_RX_ER/ RMII0_RX_ER | | LCD_TCON1-B | | |
| L14 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6 | ET0_ERXD0/ RMII0_RXD0 | | LCD_TCON3-B | IRQ4-DS | |
| L15 | | P72 | A19/CS2# | | | | ET0_MDC/ PMGI0_MDC | | LCD_DATA23-A | | |
| M1 | | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| M2 | | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |
| M3 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUSEN/SSIBCK1 | | SDHI_WP/ PIXCLK | | | |
| M4 | | P86 | | MTIOC4D/ TIOCA0 | GTIOC2B | SMISO10/ SSCL10/ RXD10 | | PIXD1 | | | |
| M5 | CLKOUT25M | PJ2 | | | | TXD8/ SMOSI8/ SSDA8/ SSLC3-B | | | LCD_TCON2-A | | |
| M6 | | PJ1 | | MTIOC6A | | RXD8/ SMISO8/ SSCL8/ SSLC2-B | | | LCD_TCON3-A | | |
| M7 | | P85 | | MTIOC6C/ TIOCC0 | | | | | LCD_DATA1-A | | |
| M8 | | P55 | D0[A0/D0]/ EDREQ0/ WAIT# | MTIOC4D/ TMO3 | | TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1 | ET0_EXOUT | | LCD_DATA5-A | IRQ10 | |
| M9 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (6/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| M10 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD 2 | MMC_D5-A | LCD_DAT A11-A | | |
| M11 | | P81 | EDACK0 | MTIOC3D/ PO27 | GTIOC0B | SMISO10/ SSCL10/ RXD10 | ET0_ETXD 0/ RMII0_TXD 0 | QIO3-A/ SDHI_CD/ MMC_D3-A | LCD_DAT A13-A | | |
| M12 | | P77 | CS7# | PO23 | | SMOSI11/ SSDA11/ TXD11 | ET0_RX_E R/ RMII0_RX_ ER | QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A | LCD_DAT A17-A | | |
| M13 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CR S_DV | | | | |
| M14 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD 0/ RMII0_TXD 0 | | LCD_CLK-B | | |
| M15 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_E N/ RMII0_TXD _EN | | LCD_TCO N0-B | | |
| N1 | VCC | | | | | | | | | | |
| N2 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | SDHI_D1-C/ PIXD7 | | | |
| N3 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRC URB/ AUDIO_CLK | | SDHI_D0-C/ PIXD6 | | | |
| N4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/CRX1-DS/ SSILRCK1 | | PIXD0 | | IRQ5 | |
| N5 | | P12 | WR3#/BC3# | MTIC5U/ TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | LCD_TCO N1-A | IRQ2 | |
| N6 | | PJ0 | | MTIOC6B | | SCK8/ SSLC1-B | | | LCD_DAT A0-A | | |
| N7 | | P84 | | MTIOC6D | | | | | LCD_DAT A2-A | | |
| N8 | | P54 | D1[A1/D1]/ EDACK0/ ALE | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1 | ET0_LINK STA | | LCD_DAT A6-A | | |
| N9 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (7/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| N10 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| N11 | | P82 | EDREQ1 | MTIOC4A/ PO28 | GTIOC2A | SMOSI10/ SSDA10/ TXD10 | ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | LCD_DATA12-A | | |
| N12 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_ER | QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| N13 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |
| N14 | | P73 | CS3# | PO16 | | | ET0_WOL | | LCD_EXTCLK-A | | |
| N15 | VSS | | | | | | | | | | |
| P1 | VSS | | | | | | | | | | |
| P2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | SDHI_D3-C/ PIXD3 | | IRQ7 | ADTRG1# |
| P3 | | P87 | | MTIOC4C/ TIOCA2 | GTIOC1B | SMOSI10/ SSDA10/ TXD10 | | SDHI_D2-C/ PIXD2 | | | |
| P4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRGD | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | LCD_CLK-A | IRQ4 | |
| P5 | VCC_USB | | | | | | | | | | |
| P6 | VSS_USB | | | | | | | | | | |
| P7 | | P57 | | | | RXD7/ SMISO7/ SSCL7/ SSLC0-B | | | LCD_DATA3-A | | |
| P8 | | P10 | ALE | MTIC5W/ TMRI3 | | | | | | IRQ0 | |
| P9 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |
| P10 | | P83 | EDACK1 | MTIOC4C | GTIOC0A | SCK10/ SS10#/ CTS10# | ET0_CRS/ RMII0_CRS_DV | | LCD_DATA8-A | | |
| P11 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| P12 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |



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**Table 1.6 List of Pin and Pin Functions (176-Pin LFBGA) (8/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFBGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| P13 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | SDHI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| P14 | | P75 | CS5# | PO20 | | SCK11/ RTS11# | ET0_ERXD0/ RMII0_RXD0 | SDHI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| P15 | VCC | | | | | | | | | | |
| R1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXICEN/ SSILRCK0 | | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| R2 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0 | | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| R3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | | IRQ6 | ADTRG0# |
| R4 | | P13 | WR2#/BC2# | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | LCD_TCON0-A | IRQ3 | ADTRG1# |
| R5 | | | | | | USB0_DM | | | | | |
| R6 | | | | | | USB0_DP | | | | | |
| R7 | CLKOUT25M | P56 | EDACK1 | MTIOC3C/ TIOCA1 | | SCK7/ RSPCKC-B | | | LCD_DATA4-A | | |
| R8 | | P11 | | MTIC5V/ TMCI3 | | SCK2 | | | LCD_DATA7-A | IRQ1 | |
| R9 | | P53*1 | BCLK | | | | | | | | |
| R10 | VSS | | | | | | | | | | |
| R11 | VCC | | | | | | | | | | |
| R12 | | P80 | EDREQ0 | MTIOC3B/ PO26 | | SCK10/ RTS10# | ET0_TX_EN/ RMII0_TXD_EN | QIO2-A/ SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| R13 | | P76 | CS6# | PO22 | | SMISO11/ SSCL11/ RXD11 | ET0_RX_CLK/ REF50CK0 | QSSL-A/ SDHI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| R14 | | P74 | A20/CS4# | PO19 | | SS11#/ CTS11# | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA21-A | | |
| R15 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD2 | | LCD_DATA22-A | IRQ12 | |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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## 1.6.3 176-Pin LFQFP

**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (1/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 1 | AVSS0 | | | | | | | | | | |
| 2 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |
| 3 | AVCC1 | | | | | | | | | | |
| 4 | | P03 | | | | SSIDATA1 | | | | IRQ11 | DA0 |
| 5 | AVSS1 | | | | | | | | | | |
| 6 | | P02 | | TMCI1 | | SCK6/ SSIBCK1 | | | | IRQ10 | AN120 |
| 7 | | P01 | | TMCI0 | | RXD6/ SMISO6/ SSCL6/ SSIBCK0 | | | | IRQ9 | AN119 |
| 8 | | P00 | | TMRI0 | | TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK | | | | IRQ8 | AN118 |
| 9 | | PF5 | WAIT# | | | SSILRCK0 | | | | IRQ4 | |
| 10 | EMLE | | | | | | | | | | |
| 11 | | PJ5 | | POE8# | | CTS2#/ RTS2#/ SS2#/ SSIRXD0 | | | | | |
| 12 | VSS | | | | | | | | | | |
| 13 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | | | | |
| 14 | VCL | | | | | | | | | | |
| 15 | VBATT | | | | | | | | | | |
| 16 | NC | | | | | | | | | | |
| 17 | TRST# | PF4 | | | | | | | | | |
| 18 | MD/FINED | | | | | | | | | | |
| 19 | XCIN | | | | | | | | | | |
| 20 | XCOUT | | | | | | | | | | |
| 21 | RES# | | | | | | | | | | |
| 22 | XTAL | P37 | | | | | | | | | |
| 23 | VSS | | | | | | | | | | |
| 24 | EXTAL | P36 | | | | | | | | | |
| 25 | VCC | | | | | | | | | | |
| 26 | UPSEL | P35 | | | | | | | | NMI | |
| 27 | | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| 28 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | PCKO | | IRQ3-DS | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (2/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 29 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUS EN | | VSYNC | | IRQ2-DS | |
| 30 | TMS | PF3 | | | | | | | | | |
| 31 | TDI | PF2 | | | | RXD1/ SMISO1/ SSCL1 | | | | | |
| 32 | | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |
| 33 | | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| 34 | TCK | PF1 | | | | SCK1 | | | | | |
| 35 | TDO | PF0 | | | | TXD1/ SMOSI1/ SSDA1 | | | | | |
| 36 | | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| 37 | | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |
| 38 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | SDHI_CD/ HSYNC | | | ADTRG0# |
| 39 | VCC | | | | | | | | | | |
| 40 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUS EN/SSIBCK1 | | SDHI_WP/ PIXCLK | | | |
| 41 | VSS | | | | | | | | | | |
| 42 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | SDHI_D1-C/ PIXD7 | | | |
| 43 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRC URB/ AUDIO_CLK | | SDHI_D0-C/ PIXD6 | | | |
| 44 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXIC EN/ SSILRCK0 | | SDHI_CLK-C/ PIXD5 | | IRQ9 | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (3/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 45 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0 | | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| 46 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | SDHI_D3-C/ PIXD3 | | IRQ7 | ADTRG1# |
| 47 | | P87 | | MTIOC4C/ TIOCA2 | GTIOC1B | SMOSI10/ SSDA10/ TXD10 | | SDHI_D2-C/ PIXD2 | | | |
| 48 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | | IRQ6 | ADTRG0# |
| 49 | | P86 | | MTIOC4D/ TIOCA0 | GTIOC2B | SMISO10/ SSCL10/ RXD10 | | PIXD1 | | | |
| 50 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/CRX1-DS/ SSILRCK1 | | PIXD0 | | IRQ5 | |
| 51 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRGD | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | LCD_CLK-A | IRQ4 | |
| 52 | | P13 | WR2#/BC2# | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | LCD_TCON0-A | IRQ3 | ADTRG1# |
| 53 | | P12 | WR3#/BC3# | MTIC5U/ TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | LCD_TCON1-A | IRQ2 | |
| 54 | VCC_USB | | | | | | | | | | |
| 55 | | | | | | USB0_DM | | | | | |
| 56 | | | | | | USB0_DP | | | | | |
| 57 | VSS_USB | | | | | | | | | | |
| 58 | CLKOUT25M | PJ2 | | | | TXD8/ SMOSI8/ SSDA8/ SSLC3-B | | | LCD_TCON2-A | | |
| 59 | | PJ1 | | MTIOC6A | | RXD8/ SMISO8/ SSCL8/ SSLC2-B | | | LCD_TCON3-A | | |
| 60 | | PJ0 | | MTIOC6B | | SCK8/ SSLC1-B | | | LCD_DATA0-A | | |
| 61 | | P85 | | MTIOC6C/ TIOCC0 | | | | | LCD_DATA1-A | | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (4/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 62 | | P84 | | MTIOC6D | | | | | LCD_DATA2-A | | |
| 63 | | P57 | | | | RXD7/ SMISO7/ SSCL7/ SSLC0-B | | | LCD_DATA3-A | | |
| 64 | CLKOUT25M | P56 | EDACK1 | MTIOC3C/ TIOCA1 | | SCK7/ RSPCKC-B | | | LCD_DATA4-A | | |
| 65 | | P55 | D0[A0/D0]/ EDREQ0/ WAIT# | MTIOC4D/ TMO3 | | TXD7/ SMOSI7/ SSDA7/ MISOC-B/ CRX1 | ET0_EXOUT | | LCD_DATA5-A | IRQ10 | |
| 66 | | P54 | D1[A1/D1]/ EDACK0/ ALE | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/ MOSIC-B/ CTX1 | ET0_LINKSTA | | LCD_DATA6-A | | |
| 67 | | P11 | | MTIC5V/ TMCI3 | | SCK2 | | | LCD_DATA7-A | IRQ1 | |
| 68 | | P10 | ALE | MTIC5W/ TMRI3 | | | | | | IRQ0 | |
| 69 | | P53*1 | BCLK | | | | | | | | |
| 70 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |
| 71 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |
| 72 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |
| 73 | VSS | | | | | | | | | | |
| 74 | | P83 | EDACK1 | MTIOC4C | GTIOC0A | SCK10/ SS10#/ CTS10# | ET0_CRS/ RMII0_CRS_DV | | LCD_DATA8-A | | |
| 75 | VCC | | | | | | | | | | |
| 76 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | MMC_D7-A | LCD_DATA9-A | IRQ14 | |
| 77 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | MMC_D6-A | LCD_DATA10-A | IRQ13 | |
| 78 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD2 | MMC_D5-A | LCD_DATA11-A | | |
| 79 | | P82 | EDREQ1 | MTIOC4A/ PO28 | GTIOC2A | SMOSI10/ SSDA10/ TXD10 | ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | LCD_DATA12-A | | |
| 80 | | P81 | EDACK0 | MTIOC3D/ PO27 | GTIOC0B | SMISO10/ SSCL10/ RXD10 | ET0_ETXD0/ RMII0_TXD0 | QIO3-A/ SDHI_CD/ MMC_D3-A | LCD_DATA13-A | | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (5/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 81 | | P80 | EDREQ0 | MTIOC3B/ PO26 | | SCK10/ RTS10# | ET0_TX_EN/ RMII0_TXD_EN | QIO2-A/ SDHI_WP/ MMC_D2-A | LCD_DATA14-A | | |
| 82 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | QMI-A/QIO1-A/SDHI_D1-A/ MMC_D1-A | LCD_DATA15-A | | |
| 83 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_ER | QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A | LCD_DATA16-A | | |
| 84 | | P77 | CS7# | PO23 | | SMOSI11/ SSDA11/ TXD11 | ET0_RX_ER/ RMII0_RX_ER | QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A | LCD_DATA17-A | | |
| 85 | | P76 | CS6# | PO22 | | SMISO11/ SSCL11/ RXD11 | ET0_RX_CLK/ REF50CK0 | QSSL-A/ SDHI_CMD-A/ MMC_CMD-A | LCD_DATA18-A | | |
| 86 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | SDHI_D3-A/ MMC_CD-A | LCD_DATA19-A | | |
| 87 | | P75 | CS5# | PO20 | | SCK11/ RTS11# | ET0_ERXD0/ RMII0_RXD0 | SDHI_D2-A/ MMC_RES#-A | LCD_DATA20-A | | |
| 88 | | P74 | A20/CS4# | PO19 | | SS11#/ CTS11# | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA21-A | | |
| 89 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD2 | | LCD_DATA22-A | IRQ12 | |
| 90 | VCC | | | | | | | | | | |
| 91 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |
| 92 | VSS | | | | | | | | | | |
| 93 | | P73 | CS3# | PO16 | | | ET0_WOL | | LCD_EXTCLK-A | | |
| 94 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CRS_DV | | | | |
| 95 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| 96 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD0/ RMII0_TXD0 | | LCD_CLK-B | | |
| 97 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_EN/ RMII0_TXD_EN | | LCD_TCON0-B | | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (6/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 98 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK4/SCK6 | ET0_RX_ER/ RMII0_RX_ER | | LCD_TCON1-B | | |
| 99 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/SS6# | ET0_RX_CLK/ REF50CK0 | | LCD_TCON2-B | | |
| 100 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6 | ET0_ERXD0/ RMII0_RXD0 | | LCD_TCON3-B | IRQ4-DS | |
| 101 | | P72 | A19/CS2# | | | | ET0_MDC/ PMGI0_MDC | | LCD_DATA23-A | | |
| 102 | | P71 | A18/CS1# | | | | ET0_MDIO/ PMGI0_MDIO | | | | |
| 103 | VCC | | | | | | | | | | |
| 104 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6 | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA0-B | IRQ12 | |
| 105 | VSS | | | | | | | | | | |
| 106 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DATA1-B | | |
| 107 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOUT | | LCD_DATA2-B | | |
| 108 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINKSTA | | LCD_DATA3-B | | |
| 109 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MDC | | LCD_DATA4-B | IRQ5-DS | |
| 110 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO/ PMGI0_MDIO | | LCD_DATA5-B | IRQ6-DS | |
| 111 | TRDATA3 | PG7 | D31 | | | | | | | | |
| 112 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DATA6-B | | |
| 113 | TRDATA2 | PG6 | D30 | | | | | | | | |
| 114 | | PA1 | DQM3/A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DATA7-B | IRQ11 | |
| 115 | VCC | | | | | | | | | | |
| 116 | TRCLK | PG5 | D29 | | | | | | | | |
| 117 | VSS | | | | | | | | | | |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (7/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 118 | | PA0 | DQM2/ BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_EN/ RMII0_TXD_EN | | LCD_DATA8-B | | |
| 119 | TRSYNC | PG4 | D28 | | | | | | | | |
| 120 | | P67 | DQM1/ CS7# | MTIOC7C | GTIOC1B | CRX2 | | | | IRQ15 | |
| 121 | TRDATA1 | PG3 | D27 | | | | | | | | |
| 122 | | P66 | DQM0/ CS6# | MTIOC7D | GTIOC2B | CTX2 | | | | | |
| 123 | TRDATA0 | PG2 | D26 | | | | | | | | |
| 124 | | P65 | CKE/CS5# | | | | | | | | |
| 125 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| 126 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/ TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/ MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| 127 | VCC | | | | | | | | | | |
| 128 | | P70 | SDCLK | | | | | | | | |
| 129 | VSS | | | | | | | | | | |
| 130 | | PE5 | D13[A13/ D13]/D5[A5/ D5] | MTIOC4C/ MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_CLK/ REF50CK0 | | LCD_DATA11-B | IRQ5 | AN103 |
| 131 | | PE4 | D12[A12/ D12]/D4[A4/ D4] | MTIOC4D/ MTIOC1A/ PO28 | GTIOC1A | SSLB0-B | ET0_ERXD2 | | LCD_DATA12-B | | AN102 |
| 132 | | PE3 | D11[A11/ D11]/D3[A3/ D3] | MTIOC4B/ PO26/TOC3/ POE8# | GTIOC2A | CTS12#/ RTS12#/ SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| 133 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | GTIOC0B | RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| 134 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | GTIOC1B | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B | | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| 135 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/ SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| 136 | | P64 | WE#/D3[A3/ D3]/CS4# | | | | | | | | |
| 137 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | | | |
| 138 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | | | |
| 139 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | | | |
| 140 | VSS | | | | | | | | | | |
| 141 | | P60 | CS0# | | | | | | | | |
| 142 | VCC | | | | | | | | | | |
| 143 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | SSLC3-A | | QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B | IRQ7 | AN107 |



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**Table 1.7 List of Pin and Pin Functions (176-Pin LFQFP) (8/8)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 176-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 144 | TRDATA7 | PG1 | D25 | | | | | | | | |
| 145 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| 146 | TRDATA6 | PG0 | D24 | | | | | | | | |
| 147 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ MTCLKA/ POE10# | | SSLC1-A | | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| 148 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | | SSLC0-A | | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| 149 | TRSYNC1 | P97 | D23/A23 | | | | | | | | |
| 150 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/ SDHI_D3-B/ MMC_D3-B | LCD_DATA21-B | IRQ3 | AN111 |
| 151 | VSS | | | | | | | | | | |
| 152 | TRDATA5 | P96 | D22/A22 | | | | | | | | |
| 153 | VCC | | | | | | | | | | |
| 154 | | PD2 | D2[A2/D2] | MTIOC4D/ TIC2 | GTIOC0B | MISOC-A/ CRX0 | | QIO2-B/ SDHI_D2-B/ MMC_D2-B | LCD_DATA22-B | IRQ2 | AN110 |
| 155 | TRDATA4 | P95 | D21/A21 | | | | | | | | |
| 156 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | GTIOC1A | MOSIC-A/ CTX0 | | | LCD_DATA23-B | IRQ1 | AN109 |
| 157 | | P94 | D20/A20 | | | | | | | | |
| 158 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXTCLK-B | IRQ0 | AN108 |
| 159 | | P93 | D19/A19 | POE0# | | CTS7#/ RTS7#/SS7# | | | | | AN117 |
| 160 | | P92 | D18/A18 | POE4# | | RXD7/ SMISO7/ SSCL7 | | | | | AN116 |
| 161 | | P91 | D17/A17 | | | SCK7 | | | | | AN115 |
| 162 | VSS | | | | | | | | | | |
| 163 | | P90 | D16/A16 | | | TXD7/ SMOSI7/ SSDA7 | | | | | AN114 |
| 164 | VCC | | | | | | | | | | |
| 165 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| 166 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| 167 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| 168 | | P44 | | | | | | | | IRQ12-DS | AN004 |
| 169 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| 170 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| 171 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| 172 | VREFL0 | | | | | | | | | | |
| 173 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| 174 | VREFH0 | | | | | | | | | | |
| 175 | AVCC0 | | | | | | | | | | |
| 176 | | P07 | | | | | | | | IRQ15 | ADTRG0# |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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## 1.6.4 145-Pin TFLGA

**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (1/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| A1 | AVSS0 | | | | | | | | | | |
| A2 | | P07 | | | | | | | | IRQ15 | ADTRG0# |
| A3 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| A4 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| A5 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| A6 | | P90 | A16 | | | TXD7/ SMOSI7/ SSDA7 | | | | | AN114 |
| A7 | | P92 | A18 | POE4# | | RXD7/ SMISO7/ SSCL7 | | | | | AN116 |
| A8 | | PD2 | D2[A2/D2] | MTIOC4D/ TIC2 | GTIOC0B | MISOC-A/ CRX0 | | QIO2-B/ SDHI_D2-B/ MMC_D2-B | LCD_DATA22-B | IRQ2 | AN110 |
| A9 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| A10 | VSS | | | | | | | | | | |
| A11 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | | | |
| A12 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | GTIOC1B | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B | | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| A13 | | PE3 | D11[A11/ D11]/D3[A3/ D3] | MTIOC4B/ PO26/TOC3/ POE8# | GTIOC2A | CTS12#/ RTS12#/ SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| B1 | AVCC1 | | | | | | | | | | |
| B2 | AVCC0 | | | | | | | | | | |
| B3 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |
| B4 | VREFL0 | | | | | | | | | | |
| B5 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| B6 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| B7 | | P91 | A17 | | | SCK7 | | | | | AN115 |
| B8 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXTCLK-B | IRQ0 | AN108 |
| B9 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | | SSLC0-A | | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| B10 | VCC | | | | | | | | | | |
| B11 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | | | |
| B12 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | GTIOC0B | RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| B13 | | PE4 | D12[A12/ D12]/D4[A4/ D4] | MTIOC4D/ MTIOC1A/ PO28 | GTIOC1A | SSLB0-B | ET0_ERXD2 | | LCD_DATA12-B | | AN102 |
| C1 | AVSS1 | | | | | | | | | | |
| C2 | | P02 | | TMCI1 | | SCK6/ SSIBCK1 | | | | IRQ10 | AN120 |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (2/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| C3 | VREFH0 | | | | | | | | | | |
| C4 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| C5 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| C6 | VSS | | | | | | | | | | |
| C7 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | GTIOC1A | MOSIC-A/ CTX0 | | | LCD_DATA23-B | IRQ1 | AN109 |
| C8 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/ SDHI_D3-B/ MMC_D3-B | LCD_DATA21-B | IRQ3 | AN111 |
| C9 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | SSLC3-A | | QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B | LCD_DATA17-B | IRQ7 | AN107 |
| C10 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | | | |
| C11 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/ SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| C12 | | P70 | SDCLK | | | | | | | | |
| C13 | VSS | | | | | | | | | | |
| D1 | | P00 | | TMRI0 | | TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK | | | | IRQ8 | AN118 |
| D2 | | PF5 | WAIT# | | | SSILRCK0 | | | | IRQ4 | |
| D3 | | P03 | | | | SSIDATA1 | | | | IRQ11 | DA0 |
| D4 | | P01 | | TMCI0 | | RXD6/ SMISO6/ SSCL6/ SSIBCK0 | | | | IRQ9 | AN119 |
| D5 | VCC | | | | | | | | | | |
| D6 | | P93 | A19 | POE0# | | CTS7#/ RTS7#/SS7# | | | | | AN117 |
| D7 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ MTCLKA/ POE10# | | SSLC1-A | | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| D8 | | P60 | CS0# | | | | | | | | |
| D9 | | P64 | WE#/ D3[A3/D3]/ CS4# | | | | | | | | |
| D10 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| D11 | VCC | | | | | | | | | | |
| D12 | | PE5 | D13[A13/ D13]/D5[A5/ D5] | MTIOC4C/ MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_CLK/ REF50CK0 | | LCD_DATA11-B | IRQ5 | AN103 |
| D13 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/ TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/ MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| E1 | VSS | | | | | | | | | | |
| E2 | VCL | | | | | | | | | | |
| E3 | | PJ5 | | POE8# | | CTS2#/ RTS2#/ SS2#/ SSIRXD0 | | | | | |
| E4 | EMLE | | | | | | | | | | |
| E5 | | P44 | | | | | | | | IRQ12-DS | AN004 |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (3/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| E10 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_EN/ RMII0_TXD_EN | | LCD_DATA8-B | | |
| E11 | | P66 | DQM0/ CS6# | MTIOC7D | GTIOC2B | CTX2 | | | | | |
| E12 | | P65 | CKE/CS5# | | | | | | | | |
| E13 | | P67 | DQM1/ CS7# | MTIOC7C | GTIOC1B | CRX2 | | | | IRQ15 | |
| F1 | XCIN | | | | | | | | | | |
| F2 | XCOUT | | | | | | | | | | |
| F3 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | | | | |
| F4 | VBATT | | | | | | | | | | |
| F10 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO/ PMGI0_MDIO | | LCD_DATA5-B | IRQ6-DS | |
| F11 | VSS | | | | | | | | | | |
| F12 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DATA7-B | IRQ11 | |
| F13 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DATA6-B | | |
| G1 | XTAL | P37 | | | | | | | | | |
| G2 | RES# | | | | | | | | | | |
| G3 | MD/FINED | | | | | | | | | | |
| G4 | BSCANP | | | | | | | | | | |
| G10 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINKSTA | | LCD_DATA3-B | | |
| G11 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOUT | | LCD_DATA2-B | | |
| G12 | VCC | | | | | | | | | | |
| G13 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MDC | | LCD_DATA4-B | IRQ5-DS | |
| H1 | EXTAL | P36 | | | | | | | | | |
| H2 | VCC | | | | | | | | | | |
| H3 | VSS | | | | | | | | | | |
| H4 | UPSEL | P35 | | | | | | | | NMI | |
| H10 | | P72 | A19/CS2# | | | | ET0_MDC/ PMGI0_MDC | | | | |
| H11 | | P71 | A18/CS1# | | | | ET0_MDIO/ PMGI0_MDIO | | | | |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (4/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| H12 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6 | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA0-B | IRQ12 | |
| H13 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DATA1-B | | |
| J1 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| J2 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | PCKO | | IRQ3-DS | |
| J3 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN | | VSYNC | | IRQ2-DS | |
| J4 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| J10 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK4/SCK6 | ET0_RX_ER/ RMII0_RX_ER | | LCD_TCON1-B | | |
| J11 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_EN/ RMII0_TXD_EN | | LCD_TCON0-B | | |
| J12 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/SS6# | ET0_RX_CLK/ REF50CK0 | | LCD_TCON2-B | | |
| J13 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6 | ET0_ERXD0/ RMII0_RXD0 | | LCD_TCON3-B | IRQ4-DS | |
| K1 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| K2 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |
| K3 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |
| K4 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/CRX1-DS/ SSILRCK1 | | PIXD0 | | IRQ5 | |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (5/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| K5 | TRDATA2 | P54 | ALE/ D1[A1/D1]/ EDACK0 | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/CTX1 | ET0_LINK STA | | | | |
| K6 | | P53*1 | BCLK | | | | | | | | |
| K7 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |
| K8 | VCC | | | | | | | | | | |
| K9 | TRDATA0 | P80 | EDREQ0 | MTIOC3B/ PO26 | | SCK10/ RTS10# | ET0_TX_EN/ RMII0_TXD_EN | QIO2-A/ SDHI_WP/ MMC_D2-A | | | |
| K10 | TRDATA6 | P76 | CS6# | PO22 | | SMISO11/ SSCL11/ RXD11 | ET0_RX_CLK/ REF50CK0 | QSSL-A/ SDHI_CMD-A/ MMC_CMD-A | | | |
| K11 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CRS_DV | | | | |
| K12 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| K13 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD0/ RMII0_TXD0 | | LCD_CLK-B | | |
| L1 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | SDHI_CD/ HSYNC | | | ADTRG0# |
| L2 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | SDHI_D1-C/ PIXD7 | | | |
| L3 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | | IRQ6 | ADTRG0# |
| L4 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUSEN/SSIBCK1 | | SDHI_WP/ PIXCLK | | | |
| L5 | | P13 | | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | | IRQ3 | ADTRG1# |
| L6 | CLKOUT25M | P56 | EDACK1 | MTIOC3C/ TIOCA1 | | SCK7 | | | | | |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (6/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| L7 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |
| L8 | TRCLK | P83 | EDACK1 | MTIOC4C | GTIOC0A | SCK10/ SS10#/ CTS10# | ET0_CRS/ RMII0_CRS_DV | | | | |
| L9 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD2 | MMC_D5-A | | | |
| L10 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | QMI-A/ QIO1-A/ SDHI_D1-A/ MMC_D1-A | | | |
| L11 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | SDHI_D3-A/ MMC_CD-A | | | |
| L12 | TRDATA4 | P73 | CS3# | PO16 | | | ET0_WOL | | | | |
| L13 | VSS | | | | | | | | | | |
| M1 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRCURB/ AUDIO_CLK | | SDHI_D0-C/ PIXD6 | | | |
| M2 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | SDHI_D3-C/ PIXD3 | | IRQ7 | ADTRG1# |
| M3 | | P86 | | MTIOC4D/ TIOCA0 | GTIOC2B | SMISO10/ SSCL10/ RXD10 | | PIXD1 | | | |
| M4 | | P12 | | TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | | IRQ2 | |
| M5 | VCC_USB | | | | | | | | | | |
| M6 | VSS_USB | | | | | | | | | | |
| M7 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |
| M8 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | MMC_D6-A | | IRQ13 | |
| M9 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ PO27 | GTIOC0B | SMISO10/ SSCL10/ RXD10 | ET0_ETXD0/ RMII0_TXD0 | QIO3-A/ SDHI_CD/ MMC_D3-A | | | |
| M10 | TRDATA7 | P77 | CS7# | PO23 | | SMOSI11/ SSDA11/ TXD11 | ET0_RX_ER/ RMII0_RX_ER | QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A | | | |
| M11 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |



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**Table 1.8 List of Pin and Pin Functions (145-Pin TFLGA) (7/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 145-Pin TFLGA | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| M12 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD 2 | | | IRQ12 | |
| M13 | VCC | | | | | | | | | | |
| N1 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXIC EN/ SSILRCK0 | | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| N2 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0 | | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| N3 | | P87 | | MTIOC4C/ TIOCA2 | GTIOC1B | SMOSI10/ SSDA10/ TXD10 | | SDHI_D2-C/ PIXD2 | | | |
| N4 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRG D | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRC URA | | | | IRQ4 | |
| N5 | | | | | | USB0_DM | | | | | |
| N6 | | | | | | USB0_DP | | | | | |
| N7 | TRDATA3 | P55 | D0[A0/D0]/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | | TXD7/ SMOSI7/ SSDA7/ CRX1 | ET0_EXOU T | | | IRQ10 | |
| N8 | VSS | | | | | | | | | | |
| N9 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | MMC_D7-A | | IRQ14 | |
| N10 | TRSYNC | P82 | EDREQ1 | MTIOC4A/ PO28 | GTIOC2A | SMOSI10/ SSDA10/ TXD10 | ET0_ETXD 1/ RMII0_TXD 1 | MMC_D4-A | | | |
| N11 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_E R | QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A | | | |
| N12 | TRSYNC1 | P75 | CS5# | PO20 | | SCK11/ RTS11# | ET0_ERXD 0/ RMII0_RX D0 | SDHI_D2-A/ MMC_RES#-A | | | |
| N13 | TRDATA5 | P74 | A20/CS4# | PO19 | | SS11#/ CTS11# | ET0_ERXD 1/ RMII0_RX D1 | | | | |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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## 1.6.5 144-Pin LFQFP

**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (1/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 1 | AVSS0 | | | | | | | | | | |
| 2 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |
| 3 | AVCC1 | | | | | | | | | | |
| 4 | | P03 | | | | SSIDATA1 | | | | IRQ11 | DA0 |
| 5 | AVSS1 | | | | | | | | | | |
| 6 | | P02 | | TMCI1 | | SCK6/ SSIBCK1 | | | | IRQ10 | AN120 |
| 7 | | P01 | | TMCI0 | | RXD6/ SMISO6/ SSCL6/ SSIBCK0 | | | | IRQ9 | AN119 |
| 8 | | P00 | | TMRI0 | | TXD6/ SMOSI6/ SSDA6/ AUDIO_CLK | | | | IRQ8 | AN118 |
| 9 | | PF5 | WAIT# | | | SSILRCK0 | | | | IRQ4 | |
| 10 | EMLE | | | | | | | | | | |
| 11 | | PJ5 | | POE8# | | CTS2#/ RTS2#/ SS2#/ SSIRXD0 | | | | | |
| 12 | VSS | | | | | | | | | | |
| 13 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | | | | |
| 14 | VCL | | | | | | | | | | |
| 15 | VBATT | | | | | | | | | | |
| 16 | MD/FINED | | | | | | | | | | |
| 17 | XCIN | | | | | | | | | | |
| 18 | XCOUT | | | | | | | | | | |
| 19 | RES# | | | | | | | | | | |
| 20 | XTAL | P37 | | | | | | | | | |
| 21 | VSS | | | | | | | | | | |
| 22 | EXTAL | P36 | | | | | | | | | |
| 23 | VCC | | | | | | | | | | |
| 24 | UPSEL | P35 | | | | | | | | NMI | |
| 25 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| 26 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | PCKO | | IRQ3-DS | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (2/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 27 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUS EN | | VSYNC | | IRQ2-DS | |
| 28 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |
| 29 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| 30 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| 31 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |
| 32 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | SDHI_CD/ HSYNC | | | ADTRG0# |
| 33 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUS EN/SSIBCK1 | | SDHI_WP/ PIXCLK | | | |
| 34 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | SDHI_D1-C/ PIXD7 | | | |
| 35 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRC URB/ AUDIO_CLK | | SDHI_D0-C/ PIXD6 | | | |
| 36 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ SCL1/ USB0_EXIC EN/ SSILRCK0 | | SDHI_CLK-C/ PIXD5 | | IRQ9 | |
| 37 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ SDA1/ USB0_ID/ SSIRXD0 | | SDHI_CMD-C/ PIXD4 | | IRQ8 | |
| 38 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | SDHI_D3-C/ PIXD3 | | IRQ7 | ADTRG1# |
| 39 | | P87 | | MTIOC4C/ TIOCA2 | GTIOC1B | SMOSI10/ SSDA10/ TXD10 | | SDHI_D2-C/ PIXD2 | | | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (3/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 40 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUSEN/ USB0_VBUS/ USB0_OVRCURB | | | | IRQ6 | ADTRG0# |
| 41 | | P86 | | MTIOC4D/ TIOCA0 | GTIOC2B | SMISO10/ SSCL10/ RXD10 | | PIXD1 | | | |
| 42 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/CRX1-DS/ SSILRCK1 | | PIXD0 | | IRQ5 | |
| 43 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRGD | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRCURA | | | | IRQ4 | |
| 44 | | P13 | | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | | IRQ3 | ADTRG1# |
| 45 | | P12 | | TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | | IRQ2 | |
| 46 | VCC_USB | | | | | | | | | | |
| 47 | | | | | | USB0_DM | | | | | |
| 48 | | | | | | USB0_DP | | | | | |
| 49 | VSS_USB | | | | | | | | | | |
| 50 | CLKOUT25M | P56 | EDACK1 | MTIOC3C/ TIOCA1 | | SCK7 | | | | | |
| 51 | TRDATA3 | P55 | D0[A0/D0]/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | | TXD7/ SMOSI7/ SSDA7/ CRX1 | ET0_EXOUT | | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/D1[A1/D1]/ EDACK0 | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/CTX1 | ET0_LINKSTA | | | | |
| 53 | | P53*1 | BCLK | | | | | | | | |
| 54 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |
| 55 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |
| 56 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |
| 57 | VSS | | | | | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C | GTIOC0A | SCK10/ SS10#/ CTS10# | ET0_CRS/ RMII0_CRS_DV | | | | |
| 59 | VCC | | | | | | | | | | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (4/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 60 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | MMC_D7-A | | IRQ14 | |
| 61 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | MMC_D6-A | | IRQ13 | |
| 62 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD2 | MMC_D5-A | | | |
| 63 | TRSYNC | P82 | EDREQ1 | MTIOC4A/ PO28 | GTIOC2A | SMOSI10/ SSDA10/ TXD10 | ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | | | |
| 64 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ PO27 | GTIOC0B | SMISO10/ SSCL10/ RXD10 | ET0_ETXD0/ RMII0_TXD0 | QIO3-A/ SDHI_CD/ MMC_D3-A | | | |
| 65 | TRDATA0 | P80 | EDREQ0 | MTIOC3B/ PO26 | | SCK10/ RTS10# | ET0_TX_EN/ RMII0_TXD_EN | QIO2-A/ SDHI_WP/ MMC_D2-A | | | |
| 66 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | QMI-A/ QIO1-A/ SDHI_D1-A/ MMC_D1-A | | | |
| 67 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_ER | QMO-A/QIO0-A/SDHI_D0-A/ MMC_D0-A | | | |
| 68 | TRDATA7 | P77 | CS7# | PO23 | | SMOSI11/ SSDA11/ TXD11 | ET0_RX_ER/ RMII0_RX_ER | QSPCLK-A/ SDHI_CLK-A/ MMC_CLK-A | | | |
| 69 | TRDATA6 | P76 | CS6# | PO22 | | SMISO11/ SSCL11/ RXD11 | ET0_RX_CLK/ REF50CK0 | QSSL-A/ SDHI_CMD-A/ MMC_CMD-A | | | |
| 70 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | SDHI_D3-A/ MMC_CD-A | | | |
| 71 | TRSYNC1 | P75 | CS5# | PO20 | | SCK11/ RTS11# | ET0_ERXD0/ RMII0_RXD0 | SDHI_D2-A/ MMC_RES#-A | | | |
| 72 | TRDATA5 | P74 | A20/CS4# | PO19 | | SS11#/ CTS11# | ET0_ERXD1/ RMII0_RXD1 | | | | |
| 73 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD2 | | | IRQ12 | |
| 74 | VCC | | | | | | | | | | |
| 75 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |
| 76 | VSS | | | | | | | | | | |
| 77 | TRDATA4 | P73 | CS3# | PO16 | | | ET0_WOL | | | | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (5/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 78 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CRS_DV | | | | |
| 79 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD1/ RMII0_TXD1 | | | | |
| 80 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD0/ RMII0_TXD0 | | LCD_CLK-B | | |
| 81 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_EN/ RMII0_TXD_EN | | LCD_TCON0-B | | |
| 82 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK4/SCK6 | ET0_RX_ER/ RMII0_RX_ER | | LCD_TCON1-B | | |
| 83 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS4#/ RTS4#/ SS4#/ CTS6#/ RTS6#/SS6# | ET0_RX_CLK/ REF50CK0 | | LCD_TCON2-B | | |
| 84 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD4/ SMOSI4/ SSDA4/ TXD6/ SMOSI6/ SSDA6 | ET0_ERXD0/ RMII0_RXD0 | | LCD_TCON3-B | IRQ4-DS | |
| 85 | | P72 | A19/CS2# | | | | ET0_MDC/ PMGI0_MDC | | | | |
| 86 | | P71 | A18/CS1# | | | | ET0_MDIO/ PMGI0_MDIO | | | | |
| 87 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD4/ SMISO4/ SSCL4/ RXD6/ SMISO6/ SSCL6 | ET0_ERXD1/ RMII0_RXD1 | | LCD_DATA0-B | IRQ12 | |
| 88 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DATA1-B | | |
| 89 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOUT | | LCD_DATA2-B | | |
| 90 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINKSTA | | LCD_DATA3-B | | |
| 91 | VCC | | | | | | | | | | |
| 92 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MDC | | LCD_DATA4-B | IRQ5-DS | |
| 93 | VSS | | | | | | | | | | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (6/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 94 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO / PMGI0_MDIO | | LCD_DATA5-B | IRQ6-DS | |
| 95 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DATA6-B | | |
| 96 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DATA7-B | IRQ11 | |
| 97 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_EN/ RMII0_TXD_EN | | LCD_DATA8-B | | |
| 98 | | P67 | DQM1/ CS7# | MTIOC7C | GTIOC1B | CRX2 | | | | IRQ15 | |
| 99 | | P66 | DQM0/ CS6# | MTIOC7D | GTIOC2B | CTX2 | | | | | |
| 100 | | P65 | CKE/CS5# | | | | | | | | |
| 101 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/ MMC_RES#-B | LCD_DATA9-B | IRQ7 | AN105 |
| 102 | | PE6 | D14[A14/ D14]/D6[A6/ D6] | MTIOC6C/ TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/ MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| 103 | VCC | | | | | | | | | | |
| 104 | | P70 | SDCLK | | | | | | | | |
| 105 | VSS | | | | | | | | | | |
| 106 | | PE5 | D13[A13/ D13]/D5[A5/ D5] | MTIOC4C/ MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_CLK/ REF50CK0 | | LCD_DATA11-B | IRQ5 | AN103 |
| 107 | | PE4 | D12[A12/ D12]/D4[A4/ D4] | MTIOC4D/ MTIOC1A/ PO28 | GTIOC1A | SSLB0-B | ET0_ERXD2 | | LCD_DATA12-B | | AN102 |
| 108 | | PE3 | D11[A11/ D11]/D3[A3/ D3] | MTIOC4B/ PO26/TOC3/ POE8# | GTIOC2A | CTS12#/ RTS12#/ SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| 109 | | PE2 | D10[A10/ D10]/D2[A2/ D2] | MTIOC4A/ PO23/TIC3 | GTIOC0B | RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| 110 | | PE1 | D9[A9/D9]/ D1[A1/D1] | MTIOC4C/ MTIOC3B/ PO18 | GTIOC1B | TXD12/ SMOSI12/ SSDA12/ TXDX12/ SIOX12/ SSLB2-B | | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| 111 | | PE0 | D8[A8/D8]/ D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/ SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| 112 | | P64 | WE#/D3[A3/ D3]/CS4# | | | | | | | | |
| 113 | | P63 | CAS#/ D2[A2/D2]/ CS3# | | | | | | | | |
| 114 | | P62 | RAS#/ D1[A1/D1]/ CS2# | | | | | | | | |
| 115 | | P61 | SDCS#/ D0[A0/D0]/ CS1# | | | | | | | | |
| 116 | VSS | | | | | | | | | | |



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**Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (7/7)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 144-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF, PDC) | | | |
| 117 | | P60 | CS0# | | | | | | | | |
| 118 | VCC | | | | | | | | | | |
| 119 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | SSLC3-A | | QMI-B/ QIO1-B/ SDHI_D1-B/ MMC_D1-B | LCD_DAT A17-B | IRQ7 | AN107 |
| 120 | | PD6 | D6[A6/D6] | MTIC5V/ MTIOC8A/ POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B | LCD_DAT A18-B | IRQ6 | AN106 |
| 121 | | PD5 | D5[A5/D5] | MTIC5W/ MTIOC8C/ MTCLKA/ POE10# | | SSLC1-A | | QSPCLK-B/ SDHI_CLK-B/ MMC_CLK-B | LCD_DAT A19-B | IRQ5 | AN113 |
| 122 | | PD4 | D4[A4/D4] | MTIOC8B/ POE11# | | SSLC0-A | | QSSL-B/ SDHI_CMD-B/ MMC_CMD-B | LCD_DAT A20-B | IRQ4 | AN112 |
| 123 | | PD3 | D3[A3/D3] | MTIOC8D/ TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/ SDHI_D3-B/ MMC_D3-B | LCD_DAT A21-B | IRQ3 | AN111 |
| 124 | | PD2 | D2[A2/D2] | MTIOC4D/ TIC2 | GTIOC0B | MISOC-A/ CRX0 | | QIO2-B/ SDHI_D2-B/ MMC_D2-B | LCD_DAT A22-B | IRQ2 | AN110 |
| 125 | | PD1 | D1[A1/D1] | MTIOC4B/ POE0# | GTIOC1A | MOSIC-A/ CTX0 | | | LCD_DAT A23-B | IRQ1 | AN109 |
| 126 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXT CLK-B | IRQ0 | AN108 |
| 127 | | P93 | A19 | POE0# | | CTS7#/ RTS7#/SS7# | | | | | AN117 |
| 128 | | P92 | A18 | POE4# | | RXD7/ SMISO7/ SSCL7 | | | | | AN116 |
| 129 | | P91 | A17 | | | SCK7 | | | | | AN115 |
| 130 | VSS | | | | | | | | | | |
| 131 | | P90 | A16 | | | TXD7/ SMOSI7/ SSDA7 | | | | | AN114 |
| 132 | VCC | | | | | | | | | | |
| 133 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| 134 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| 135 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| 136 | | P44 | | | | | | | | IRQ12-DS | AN004 |
| 137 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| 138 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| 139 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| 140 | VREFL0 | | | | | | | | | | |
| 141 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| 142 | VREFH0 | | | | | | | | | | |
| 143 | AVCC0 | | | | | | | | | | |
| 144 | | P07 | | | | | | | | IRQ15 | ADTRG0# |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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## 1.6.6 100-Pin LFQFP

**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 1 | AVCC1 | | | | | | | | | | |
| 2 | EMLE | | | | | | | | | | |
| 3 | AVSS1 | | | | | | | | | | |
| 4 | | PJ3 | EDACK1 | MTIOC3C | | CTS6#/ RTS6#/ SS6#/ CTS0#/ RTS0#/ SS0#/ SSITXD0 | ET0_EXOUT | | | | |
| 5 | VCL | | | | | | | | | | |
| 6 | VBATT | | | | | | | | | | |
| 7 | MD/FINED | | | | | | | | | | |
| 8 | XCIN | | | | | | | | | | |
| 9 | XCOUT | | | | | | | | | | |
| 10 | RES# | | | | | | | | | | |
| 11 | XTAL | P37 | | | | | | | | | |
| 12 | VSS | | | | | | | | | | |
| 13 | EXTAL | P36 | | | | | | | | | |
| 14 | VCC | | | | | | | | | | |
| 15 | UPSEL | P35 | | | | | | | | NMI | |
| 16 | TRST# | P34 | | MTIOC0A/ TMCI3/PO12/ POE10# | | SCK6/SCK0 | ET0_LINKSTA | | | IRQ4 | |
| 17 | | P33 | EDREQ1 | MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11# | | RXD6/ SMISO6/ SSCL6/ RXD0/ SMISO0/ SSCL0/ CRX0 | | | | IRQ3-DS | |
| 18 | | P32 | | MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCIC2/ RTCOUT/ POE0#/ POE10# | | TXD6/ SMOSI6/ SSDA6/ TXD0/ SMOSI0/ SSDA0/ CTX0/ USB0_VBUSEN | | | | IRQ2-DS | |
| 19 | TMS | P31 | | MTIOC4D/ TMCI2/PO9/ RTCIC1 | | CTS1#/ RTS1#/ SS1#/ SSLB0-A | | | | IRQ1-DS | |
| 20 | TDI | P30 | | MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8# | | RXD1/ SMISO1/ SSCL1/ MISOB-A | | | | IRQ0-DS | |
| 21 | TCK | P27 | CS7# | MTIOC2B/ TMCI3/PO7 | | SCK1/ RSPCKB-A | | | | | |
| 22 | TDO | P26 | CS6# | MTIOC2A/ TMO1/PO6 | | TXD1/ SMOSI1/ SSDA1/ CTS3#/ RTS3#/ SS3#/ MOSIB-A | | | | | |



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**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 23 | CLKOUT | P25 | CS5#/ EDACK1 | MTIOC4C/ MTCLKB/ TIOCA4/PO5 | | RXD3/ SMISO3/ SSCL3/ SSIDATA1 | | | | | ADTRG0# |
| 24 | | P24 | CS4#/ EDREQ1 | MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4 | | SCK3/ USB0_VBUS EN/SSIBCK1 | | | | | |
| 25 | | P23 | EDACK0 | MTIOC3D/ MTCLKD/ TIOCD3/PO3 | GTIOC0A | TXD3/ SMOSI3/ SSDA3/ CTS0#/ RTS0#/ SS0#/CTX1/ SSIBCK0 | | | | | |
| 26 | | P22 | EDREQ0 | MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2 | GTIOC1A | SCK0/ USB0_OVRC URB/ AUDIO_CLK | | | | | |
| 27 | | P21 | | MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1 | GTIOC2A | RXD0/ SMISO0/ SSCL0/ USB0_EXIC EN/ SSILRCK0/ SCL1 | | | | IRQ9 | |
| 28 | | P20 | | MTIOC1A/ TIOCB3/ TMRI0/PO0 | | TXD0/ SMOSI0/ SSDA0/ USB0_ID/ SSIRXD0/ SDA1 | | | | IRQ8 | |
| 29 | | P17 | | MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8# | GTIOC0B | SCK1/TXD3/ SMOSI3/ SSDA3/ SDA2-DS/ SSITXD0 | | | | IRQ7 | ADTRG1# |
| 30 | | P16 | | MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/ RTCOUT | | TXD1/ SMOSI1/ SSDA1/ RXD3/ SMISO3/ SSCL3/ SCL2-DS/ USB0_VBUS EN/ USB0_VBUS / USB0_OVRC URB | | | | IRQ6 | ADTRG0# |
| 31 | | P15 | | MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13 | GTETRGA | RXD1/ SMISO1/ SSCL1/ SCK3/ CRX1-DS/ SSILRCK1 | | | | IRQ5 | |
| 32 | | P14 | | MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/TMRI2/ PO15 | GTETRG D | CTS1#/ RTS1#/ SS1#/CTX1/ USB0_OVRC URA | | | | IRQ4 | |
| 33 | | P13 | | MTIOC0B/ TIOCA5/ TMO3/PO13 | GTADSM1 | TXD2/ SMOSI2/ SSDA2/ SDA0[FM+] | | | | IRQ3 | ADTRG1# |
| 34 | | P12 | | TMCI1 | GTADSM0 | RXD2/ SMISO2/ SSCL2/ SCL0[FM+] | | | | IRQ2 | |



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**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 35 | VCC_USB | | | | | | | | | | |
| 36 | | | | | | USB0_DM | | | | | |
| 37 | | | | | | USB0_DP | | | | | |
| 38 | VSS_USB | | | | | | | | | | |
| 39 | | P55 | D0[A0/D0]/ WAIT#/ EDREQ0 | MTIOC4D/ TMO3 | | CRX1 | ET0_EXOUT | | | IRQ10 | |
| 40 | | P54 | ALE/ D1[A1/D1]/ EDACK0 | MTIOC4B/ TMCI1 | | CTS2#/ RTS2#/ SS2#/CTX1 | ET0_LINKSTA | | | | |
| 41 | | P53*1 | BCLK | | | | | | | | |
| 42 | | P52 | RD# | | | RXD2/ SMISO2/ SSCL2/ SSLB3-A | | | | | |
| 43 | | P51 | WR1#/ BC1#/ WAIT# | | | SCK2/ SSLB2-A | | | | | |
| 44 | | P50 | WR0#/WR# | | | TXD2/ SMOSI2/ SSDA2/ SSLB1-A | | | | | |
| 45 | UB | PC7 | A23/CS0# | MTIOC3A/ MTCLKB/ TMO2/PO31/ TOC0/ CACREF | GTIOC3A | TXD8/ SMOSI8/ SSDA8/ SMOSI10/ SSDA10/ TXD10/ MISOA-A | ET0_COL | | | IRQ14 | |
| 46 | | PC6 | D2[A2/D2]/ A22/CS1# | MTIOC3C/ MTCLKA/ TMCI2/PO30/ TIC0 | GTIOC3B | RXD8/ SMISO8/ SSCL8/ SMISO10/ SSCL10/ RXD10/ MOSIA-A | ET0_ETXD3 | | | IRQ13 | |
| 47 | | PC5 | D3[A3/D3]/ A21/CS2#/ WAIT# | MTIOC3B/ MTCLKD/ TMRI2/PO29 | GTIOC1A | SCK8/ RTS8#/ SCK10/ RSPCKA-A | ET0_ETXD2 | | | | |
| 48 | | PC4 | A20/CS3# | MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0# | GTETRGC | SCK5/ CTS8#/ SS8#/SS10#/ CTS10#/ RTS10#/ SSLA0-A | ET0_TX_CLK | | | | |
| 49 | | PC3 | A19 | MTIOC4D/ TCLKB/PO24 | GTIOC1B | TXD5/ SMOSI5/ SSDA5 | ET0_TX_ER | | | | |
| 50 | | PC2 | A18 | MTIOC4B/ TCLKA/PO21 | GTIOC2B | RXD5/ SMISO5/ SSCL5/ SSLA3-A | ET0_RX_DV | | | | |
| 51 | | PC1 | A17 | MTIOC3A/ TCLKD/PO18 | | SCK5/ SSLA2-A | ET0_ERXD2 | | | IRQ12 | |
| 52 | | PC0 | A16 | MTIOC3C/ TCLKC/PO17 | | CTS5#/ RTS5#/ SS5#/ SSLA1-A | ET0_ERXD3 | | | IRQ14 | |
| 53 | | PB7 | A15 | MTIOC3B/ TIOCB5/PO31 | | TXD9/ SMOSI9/ SSDA9/ SMOSI11/ SSDA11/ TXD11 | ET0_CRS/ RMII0_CRS_DV | | | | |



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**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 54 | | PB6 | A14 | MTIOC3D/ TIOCA5/PO30 | | RXD9/ SMISO9/ SSCL9/ SMISO11/ SSCL11/ RXD11 | ET0_ETXD 1/ RMII0_TXD 1 | | | | |
| 55 | | PB5 | A13 | MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4# | | SCK9/ RTS9#/ SCK11 | ET0_ETXD 0/ RMII0_TXD 0 | | LCD_CLK-B | | |
| 56 | | PB4 | A12 | TIOCA4/PO28 | | CTS9#/ SS9#/SS11#/ CTS11#/ RTS11# | ET0_TX_E N/ RMII0_TXD _EN | | LCD_TCO N0-B | | |
| 57 | | PB3 | A11 | MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE11# | | SCK6 | ET0_RX_E R/ RMII0_RX_ ER | | LCD_TCO N1-B | | |
| 58 | | PB2 | A10 | TIOCC3/ TCLKC/PO26 | | CTS6#/ RTS6#/SS6# | ET0_RX_C LK/ REF50CK0 | | LCD_TCO N2-B | | |
| 59 | | PB1 | A9 | MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25 | | TXD6/ SMOSI6/ SSDA6 | ET0_ERXD 0/ RMII0_RX D0 | | LCD_TCO N3-B | IRQ4-DS | |
| 60 | VCC | | | | | | | | | | |
| 61 | | PB0 | A8 | MTIC5W/ TIOCA3/PO24 | | RXD6/ SMISO6/ SSCL6 | ET0_ERXD 1/ RMII0_RX D1 | | LCD_DAT A0-B | IRQ12 | |
| 62 | VSS | | | | | | | | | | |
| 63 | | PA7 | A7 | TIOCB2/PO23 | | MISOA-B | ET0_WOL | | LCD_DAT A1-B | | |
| 64 | | PA6 | A6 | MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10# | GTETRGB | CTS5#/ RTS5#/ SS5#/ MOSIA-B | ET0_EXOU T | | LCD_DAT A2-B | | |
| 65 | | PA5 | A5 | MTIOC6B/ TIOCB1/PO21 | GTIOC0A | RSPCKA-B | ET0_LINK STA | | LCD_DAT A3-B | | |
| 66 | | PA4 | A4 | MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20 | | TXD5/ SMOSI5/ SSDA5/ SSLA0-B | ET0_MDC/ PMGI0_MD C | | LCD_DAT A4-B | IRQ5-DS | |
| 67 | | PA3 | A3 | MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19 | | RXD5/ SMISO5/ SSCL5 | ET0_MDIO / PMGI0_MD IO | | LCD_DAT A5-B | IRQ6-DS | |
| 68 | | PA2 | A2 | MTIOC7A/ PO18 | GTIOC1A | RXD5/ SMISO5/ SSCL5/ SSLA3-B | | | LCD_DAT A6-B | | |
| 69 | | PA1 | A1 | MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17 | GTIOC2A | SCK5/ SSLA2-B | ET0_WOL | | LCD_DAT A7-B | IRQ11 | |
| 70 | | PA0 | BC0#/A0 | MTIOC4A/ MTIOC6D/ TIOCA0/PO16/ CACREF | GTIOC0B | SSLA1-B | ET0_TX_E N/ RMII0_TXD _EN | | LCD_DAT A8-B | | |
| 71 | | PE7 | D15[A15/ D15]/D7[A7/ D7] | MTIOC6A/ TOC1 | GTIOC3A | MISOB-B | | SDHI_WP/ MMC_RES#-B | LCD_DAT A9-B | IRQ7 | AN105 |



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**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (5/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 72 | | PE6 | D14[A14/D14]/D6[A6/D6] | MTIOC6C/TIC1 | GTIOC3B | MOSIB-B | | SDHI_CD/MMC_CD-B | LCD_DATA10-B | IRQ6 | AN104 |
| 73 | | PE5 | D13[A13/D13]/D5[A5/D5] | MTIOC4C/MTIOC2B | GTIOC0A | RSPCKB-B | ET0_RX_CLK/REF50CK0 | | LCD_DATA11-B | IRQ5 | AN103 |
| 74 | | PE4 | D12[A12/D12]/D4[A4/D4] | MTIOC4D/MTIOC1A/PO28 | GTIOC1A | SSLB0-B | ET0_ERXD2 | | LCD_DATA12-B | | AN102 |
| 75 | | PE3 | D11[A11/D11]/D3[A3/D3] | MTIOC4B/PO26/TOC3/POE8# | GTIOC2A | CTS12#/RTS12#/SS12# | ET0_ERXD3 | MMC_D7-B | LCD_DATA13-B | | AN101 |
| 76 | | PE2 | D10[A10/D10]/D2[A2/D2] | MTIOC4A/PO23/TIC3 | GTIOC0B | RXD12/SMISO12/SSCL12/RXDX12/SSLB3-B | | MMC_D6-B | LCD_DATA14-B | IRQ7-DS | AN100 |
| 77 | | PE1 | D9[A9/D9]/D1[A1/D1] | MTIOC4C/MTIOC3B/PO18 | GTIOC1B | TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLB2-B | | MMC_D5-B | LCD_DATA15-B | | ANEX1 |
| 78 | | PE0 | D8[A8/D8]/D0[A0/D0] | MTIOC3D | GTIOC2B | SCK12/SSLB1-B | | MMC_D4-B | LCD_DATA16-B | | ANEX0 |
| 79 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | SSLC3-A | | QMI-B/QIO1-B/SDHI_D1-B/MMC_D1-B | LCD_DATA17-B | IRQ7 | AN107 |
| 80 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/POE4# | | SSLC2-A | | QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B | LCD_DATA18-B | IRQ6 | AN106 |
| 81 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/MTCLKA/POE10# | | SSLC1-A | | QSPCLK-B/SDHI_CLK-B/MMC_CLK-B | LCD_DATA19-B | IRQ5 | AN113 |
| 82 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | SSLC0-A | | QSSL-B/SDHI_CMD-B/MMC_CMD-B | LCD_DATA20-B | IRQ4 | AN112 |
| 83 | | PD3 | D3[A3/D3] | MTIOC8D/TOC2/POE8# | GTIOC0A | RSPCKC-A | | QIO3-B/SDHI_D3-B/MMC_D3-B | LCD_DATA21-B | IRQ3 | AN111 |
| 84 | | PD2 | D2[A2/D2] | MTIOC4D/TIC2 | GTIOC0B | MISOC-A/CRX0 | | QIO2-B/SDHI_D2-B/MMC_D2-B | LCD_DATA22-B | IRQ2 | AN110 |
| 85 | | PD1 | D1[A1/D1] | MTIOC4B/POE0# | GTIOC1A | MOSIC-A/CTX0 | | | LCD_DATA23-B | IRQ1 | AN109 |
| 86 | | PD0 | D0[A0/D0] | POE4# | GTIOC1B | | | | LCD_EXTCLK-B | IRQ0 | AN108 |
| 87 | | P47 | | | | | | | | IRQ15-DS | AN007 |
| 88 | | P46 | | | | | | | | IRQ14-DS | AN006 |
| 89 | | P45 | | | | | | | | IRQ13-DS | AN005 |
| 90 | | P44 | | | | | | | | IRQ12-DS | AN004 |
| 91 | | P43 | | | | | | | | IRQ11-DS | AN003 |
| 92 | | P42 | | | | | | | | IRQ10-DS | AN002 |
| 93 | | P41 | | | | | | | | IRQ9-DS | AN001 |
| 94 | VREFL0 | | | | | | | | | | |
| 95 | | P40 | | | | | | | | IRQ8-DS | AN000 |
| 96 | VREFH0 | | | | | | | | | | |
| 97 | AVCC0 | | | | | | | | | | |
| 98 | | P07 | | | | | | | | IRQ15 | ADTRG0# |



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**Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (6/6)**

| Pin Number | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timer | | Communication | | Memory I/F Camera I/F | GLCDC | Interrupt | A/D D/A |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 100-Pin LFQFP | | | | (MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | (GPTW, POEG) | (SCI, RSPI, RIIC, CAN, USB, SSIE) | (ETHERC, PMGI) | (QSPI, SDHI, MMCIF) | | | |
| 99 | AVSS0 | | | | | | | | | | |
| 100 | | P05 | | | | SSILRCK1 | | | | IRQ13 | DA1 |

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.



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# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute Maximum Rating**

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

| Item | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power supply voltage | | VCC, VCC_USB | –0.3 to +4.0 | V |
| $V_{BATT}$ power supply voltage | | $V_{BATT}$ | –0.3 to +4.0 | V |
| Input voltage (except for ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 0.3 (up to 4.0) | V |
| Input voltage (ports for 5 V tolerant*1) | | $V_{in}$ | –0.3 to VCC + 4.0 (up to 5.8) | V |
| Reference power supply voltage | | VREFH0 | –0.3 to AVCC0 + 0.3 (up to 4.0) | V |
| Analog power supply voltage | | AVCC0, AVCC1*2 | –0.3 to +4.0 | V |
| Analog input voltage | | $V_{AN}$ | –0.3 to AVCC + 0.3 (up to 4.0) | V |
| Junction temperature | D version | $T_j$ | –40 to +105 | °C |
| | G version | $T_j$ | –40 to +125 | °C |
| Storage temperature | | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.

Note 2. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.



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## 2.2 Recommended Operating Conditions

**Table 2.2 Recommended Operating Conditions (1)**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage*1 | VCC | 2.7 | — | 3.6 | V |
| | VSS | — | 0 | — | |
| $V_{BATT}$ power supply voltage | $V_{BATT}$ | 1.62*2 | — | 3.6 | V |
| USB power supply voltage | VCC_USB | — | VCC | — | V |
| | VSS_USB | — | 0 | — | |
| Analog power supply voltage*1, *3 | AVCC0 | — | VCC | — | V |
| | AVSS0 | — | 0 | — | |
| | AVCC1 | — | VCC | — | |
| | AVSS1 | — | 0 | — | |
| | VREFH0 | 2.7 | — | AVCC0 | |
| | VREFL0 | — | 0 | — | |
| Input voltage (except for 5 V tolerant ports, except for P03, P05 and P40 to P47)*4 | $V_{in}$ | –0.3 | — | VCC + 0.3 | V |
| Input voltage (P03, P05 and P40 to P47) | $V_{in}$ | –0.3 | — | AVCC0 + 0.3 | V |
| Input voltage (5V tolerant ports: P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3)*5 | $V_{in}$ | –0.3 | — | VCC + 3.6 (up to 5.5) | V |
| Input voltage (5V tolerant port: P07) | $V_{in}$ | –0.3 | — | AVCC0 + 3.6 (up to 5.5) | V |
| Operating temperature (D version) | $T_{opr}$ | –40 | — | 85 | °C |
| Operating temperature (G version) | $T_{opr}$ | –40 | — | 105 | °C |

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB
Note 2. The low CL crystal unit cannot be used when the $V_{BATT}$ voltage is less than 2.0 V.
Note 3. For details, refer to section 54.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.
Note 4. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.
Note 5. For P30 to P32, input as follows when the $V_{BATT}$ power supply is selected.
$V_{in}$ Min. = –0.3, Max. = $V_{BATT}$ + 0.3 ($V_{BATT}$ = 1.62 to 3.6 V)

**Table 2.3 Recommended Operating Conditions (2)**

| Item | Symbol | Value |
|---|---|---|
| Decoupling capacitance for stabilizing the internal voltage | $C_{VCL}$ | 0.22 µF ± 30%*1 |

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 0.22 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.



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## 2.3 DC Characteristics

**Table 2.4 DC Characteristics (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | IRQ input pin*1, MTU input pin*1, POE input pin*1, TPU input pin*1, TMR input pin*1, CMTW input pin*1, SCI input pin*1, CAN input pin*1, CAC input pin*1, ADTRG# input pin*1, QSPI input pin*1, SSIE input pin*1, GPTW input pin*1, POEG input pin*1, RES#, NMI, TCK | $V_{IH}$ | 0.8 × VCC | — | — | V | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| | | $\Delta V_T$ | 0.06 × VCC | — | — | | |
| | RIIC input pin (except for SMBus) | $V_{IH}$ | 0.7 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.3 × VCC | | |
| | | $\Delta V_T$ | 0.05 × VCC | — | — | | |
| | Ports for 5 V tolerant*2 | $V_{IH}$ | 0.8 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| | Other input pins excluding ports for 5 V tolerant*3 | $V_{IH}$ | 0.8 × VCC | — | — | | |
| | | $V_{IL}$ | — | — | 0.2 × VCC | | |
| High level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | 0.9 × VCC | — | — | V | |
| | EXTAL, RSPI input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, PMGI input pin | | 0.8 × VCC | — | — | | |
| | ETHERC input pin | | 2.3 | — | — | | |
| | D0 to D31 | | 0.7 × VCC | — | — | | |
| | RIIC (SMBus) | | 2.1 | — | — | | |
| Low level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | — | — | 0.1 × VCC | V | |
| | EXTAL, RSPI input pin, ETHERC input pin, EXDMAC input pin, WAIT#, SDHI input pin, MMC input pin, PDC input pin, PMGI input pin | | — | — | 0.2 × VCC | | |
| | D0 to D31 | | — | — | 0.3 × VCC | | |
| | RIIC (SMBus) | | — | — | 0.8 | | |

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. P07, P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3 are 5 V tolerant.
Note 3. For P30 to P32, input as follows when the $V_{BATT}$ power supply is selected.
$V_{IH}$ Min. = $V_{BATT}$ × 0.8, $V_{IL}$ Max. = $V_{BATT}$ × 0.2 ($V_{BATT}$ = 1.62 to 3.6 V)



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**Table 2.5 DC Characteristics (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output high voltage | All output pins | $V_{OH}$ | VCC – 0.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins (except for RIIC pins and ETHERC output pin) | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | RIIC output pin | | — | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | RIIC output pin (only P12 and P13 in channel 0) | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | | — | 0.4 | — | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| | ETHERC output pin | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES#, MD pin, EMLE*1, BSCANP*1, NMI | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | Other than ports for 5 V tolerant | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | Ports for 5 V tolerant | | — | — | 5.0 | | $V_{in}$ = 0 V<br>$V_{in}$ = 5.5 V |
| Input pull-up resistor current | Other than P35 | $I_p$ | –300 | — | –10 | µA | VCC = 2.7 to 3.6 V<br>$V_{in}$ = 0 V |
| Input pull-down resistor current | EMLE, BSCANP | $I_p$ | 10 | — | 300 | µA | $V_{in}$ = VCC |
| Input capacitance | All input pins (except for P03, P05, P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, and USB0_DM) | $C_{in}$ | — | — | 8 | pF | Vbias = 0 V<br>Vamp = 20 mV<br>f = 1 MHz<br>$T_a$ = 25°C |
| | P03, P05, P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, and USB0_DM | | — | — | 16 | | |
| Output voltage of the VCL pin | | $V_{CL}$ | — | 1.18 | — | V | |

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when $V_{in}$ = 0 V.



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**Table 2.6 DC Characteristics (3)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | | Symbol | D version | | G version | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ. | Max. | Typ. | Max. | | |
| Supply current *1 | High-speed operating mode | Full operation*2 | | $I_{CC}$*3 | — | 211 | — | 270 | mA | ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz |
| | | Normal operation | Peripheral module clocks are supplied *4 | | 49 | — | 49 | — | | |
| | | | Peripheral module clocks are stopped *4, *5 | | 18 | — | 18 | — | | |
| | | Core Mark | Peripheral module clocks are stopped *4, *5 | | 23 | — | 23 | — | | |
| | | Sleep mode: Peripheral module clocks are supplied*4 | | | 42 | 144 | 42 | 196 | | |
| | | All module clock stop mode (reference value) | | | 14 | 115 | 14 | 167 | | |
| | | Increased by BGO operation*8 | Reading from the code flash memory while the data flash memory is being programmed | | 6 | — | 6 | — | | |
| | | | Reading from the code flash memory while the code flash memory is being programmed | | 7 | — | 7 | — | | |
| | | Increased by Trusted Secure IP operation | | | — | 15 | — | 15 | | |
| | Low-speed operating mode 1: Peripheral module clocks are stopped*4 | | | | 4.2 | — | 4.2 | — | | All clocks 1 MHz |
| | Low-speed operating mode 2: Peripheral module clocks are stopped*4 | | | | 4.2 | — | 4.2 | — | | All clocks 32.768 kHz |
| | Software standby mode | | | | 3.95 | 107 | 3.95 | 155 | | |
| | Deep software standby mode | Power is supplied to the standby RAM and USB resume detecting unit (USB0 only) | | | 15.5 | 70 | 15.5 | 98 | μA | |
| | | Power is not supplied to the standby RAM and USB resume detecting unit (USB0 only) | Low power consumption function of the power-on reset circuit is disabled*6 | | 11.5 | 42 | 11.5 | 58 | | |
| | | | Low power consumption function of the power-on reset circuit is enabled*7 | | 4.9 | 32 | 4.9 | 47 | | |
| | | Increase current by operating RTC | When a low $C_L$ crystal is in use | | 1 | — | 1 | — | | |
| | | | When a standard $C_L$ crystal is in use | | 2 | — | 2 | — | | |
| | When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function) | | When a low $C_L$ crystal is in use | | 0.9 | — | 0.9 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 1.6 | — | 1.6 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | | | When a standard $C_L$ crystal is in use | | 1.6 | — | 1.6 | — | | $V_{BATT}$ = 1.62 V, VCC = 0 V |
| | | | | | 1.7 | — | 1.7 | — | | $V_{BATT}$ = 2.0 V, VCC = 0 V |
| | | | | | 3.3 | — | 3.3 | — | | $V_{BATT}$ = 3.3 V, VCC = 0 V |
| | Inrush current on returning from deep software standby mode | | Inrush current*9 | $I_{RUSH}$ | — | 211 | — | 211 | mA | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.
Note 2. Peripheral module clocks are supplied.
Note 3. $I_{CC}$ depends on the f (ICLK) as follows.
(when ICLK : PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 2 : 1 : 2 : 1 and EXTAL = 12 MHz)
- D version
  $I_{CC}$ max. = 0.82 × f + 113 (full operation in high-speed operating mode)
  $I_{CC}$ typ. = 0.35 × f + 7 (normal operation in high-speed operating mode)



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$I_{CC}$ typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
$I_{CC}$ max. = 0.26 × f + 113 (sleep mode)

- G version
  $I_{CC}$ max. = 0.88 × f + 164 (full operation in high-speed operating mode)
  $I_{CC}$ typ. = 0.35 × f + 7 (normal operation in high-speed operating mode)
  $I_{CC}$ typ. = 0.50 × f + 3.7 (ICLK 1 MHz max) (low-speed operating mode 1)
  $I_{CC}$ max. = 0.27 × f + 164 (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 9. Reference value

**Table 2.7 DC Characteristics (4)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | D version | | | G version | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Analog power supply current*1, *3 | During 12-bit A/D conversion (unit 0) | | $AI_{CC}$ | — | 0.8 | 1 | — | 0.8 | 1 | mA | IAVCC0_AD |
| | During 12-bit A/D conversion (unit 0) with channel-dedicated sample-and-hold circuits (3 channels) | | | — | 1.7 | 2.5 | — | 1.7 | 2.5 | | IAVCC0_AD + SH |
| | During 12-bit A/D conversion (unit 1) | | | — | 0.6 | 1 | — | 0.6 | 1 | | IAVCC1_AD |
| | During 12-bit A/D conversion (unit 1) + temperature sensor | | | — | 0.7 | 1.1 | — | 0.7 | 1.1 | | IAVCC1_AD + TEMP |
| | During D/A conversion (2 channels) | Unbuffered output | | — | 0.25 | 0.4 | — | 0.25 | 0.4 | | IAVCC1_DA |
| | | Buffered output | | — | 0.75 | 1.1 | — | 0.75 | 1.1 | | |
| | Waiting for A/D, D/A, and temperature sensor conversion (all units) | | | — | 0.9 | 1.4 | — | 0.9 | 1.4 | | IAVCC0 + IAVCC1 |
| | A/D, D/A, and temperature sensor are in standby mode (all units) | | | — | 1.4 | 6.7 | — | 1.4 | 9.0 | µA | IAVCC0 + IAVCC1 |
| Reference power supply current | During 12-bit A/D conversion (unit 0) | | $AI_{REFH}$ | — | 38 | 60 | — | 38 | 60 | µA | IVREFH0 |
| | Waiting for 12-bit A/D conversion (unit 0) | | | — | 0.07 | 0.5 | — | 0.07 | 0.6 | | IVREFH0 |
| | 12-bit A/D converter in module stop mode (unit 0) | | | — | 0.07 | 0.4 | — | 0.07 | 0.5 | | IVREFH0 |
| USB operating current | Low speed | USB0 | $I_{CCUSBLS}$ | — | 3.7 | 6.5 | — | 3.7 | 6.5 | mA | VCC_USB |
| | Full speed | USB0 | $I_{CCUSBFS}$ | — | 4.2 | 10 | — | 4.2 | 10 | mA | VCC_USB |
| RAM retension voltage | | | $V_{RAM}$ | 2.7 | — | — | 2.7 | — | — | V | |
| VCC rising gradient | | | SrVCC | 8.4 | — | 20000 | 8.4 | — | 20000 | µs/V | |
| VCC falling gradient*2 | | | SfVCC | 8.4 | — | — | 8.4 | — | — | µs/V | |

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1) and D/A converter.
Note 2. This applies when $V_{BATT}$ is used.
Note 3. Supply current values are measured when all output pins are unloaded.



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**Table 2.8 Permissible Output Currents**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 2.0 | mA |
| | All output pins*2 | High drive | | — | — | 3.8 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | 7.5 | |
| Permissible output low current (max. value per pin) | All output pins*1 | Normal drive | $I_{OL}$ | — | — | 4.0 | mA |
| | All output pins*2 | High drive | | — | — | 7.6 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | 15 | |
| Permissible output low current (total) | Total of all output pins | | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –2.0 | mA |
| | All output pins*2 | High drive | | — | — | –3.8 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | –7.5 | |
| Permissible output high current (max. value per pin) | All output pins*1 | Normal drive | $I_{OH}$ | — | — | –4.0 | mA |
| | All output pins*2 | High drive | | — | — | –7.6 | |
| | All output pins*3 | High-speed interface high-drive | | — | — | –15 | |
| Permissible output high current (total) | Total of all output pins | | $\Sigma I_{OH}$ | — | — | –80 | mA |

Caution: To protect the MCU's reliability, the output current values should not exceed the values in Table 2.8.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

**Table 2.9 Thermal Resistance Value (Reference)**

| Item | Package | Symbol | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Thermal resistance | 176-pin LFQFP (PLQP0176KB-C) | $\theta_{ja}$ | 31.5 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 144-pin LFQFP (PLQP0144KA-B) | | 32.6 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | 34.0 | | |
| | 224-pin LFBGA (PLBG0224GA-A) | | 23.1 | | JESD51-2 and JESD51-9 compliant |
| | 176-pin LFBGA (PLBG0176GA-A) | | 30.5 | | |
| | 145-pin TFLGA (PTLG0145KA-A) | | 22.9 | | |
| | 176-pin LFQFP (PLQP0176KB-C) | $\Psi_{jt}$ | 0.4 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 144-pin LFQFP (PLQP0144KA-B) | | 0.5 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | 0.6 | | |
| | 224-pin LFBGA (PLBG0224GA-A) | | 0.2 | | JESD51-2 and JESD51-9 compliant |
| | 176-pin LFBGA (PLBG0176GA-A) | | 0.3 | | |
| | 145-pin TFLGA (PTLG0145KA-A) | | 0.2 | | |

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.



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## 2.4 AC Characteristics

**Table 2.10 Operating Frequency (High-Speed Operating Mode)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | — | — | 120 | MHz |
| | Peripheral module clock (PCLKA) | | | — | — | 120 | |
| | Peripheral module clock (PCLKB) | | | — | — | 60 | |
| | Peripheral module clock (PCLKC) | | | — | — | 60 | |
| | Peripheral module clock (PCLKD) | | | — | — | 60 | |
| | Flash-IF clock (FCLK) | | | —*1 | — | 60 | |
| | External bus clock (BCLK) | Package of 144 pins or more | | — | — | 120 | |
| | | 100-pin package | | — | — | 60 | |
| | BCLK pin output | Package of 144 pins or more | | — | — | 80 | |
| | | 100-pin package | | — | — | 30 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 80 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 80 | |

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

**Table 2.11 Operating Frequency (Low-Speed Operating Mode 1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | — | — | 1 | MHz |
| | Peripheral module clock (PCLKA) | | | — | — | 1 | |
| | Peripheral module clock (PCLKB) | | | — | — | 1 | |
| | Peripheral module clock (PCLKC)*1 | | | — | — | 1 | |
| | Peripheral module clock (PCLKD)*1 | | | — | — | 1 | |
| | Flash-IF clock (FCLK) | | | — | — | 1 | |
| | External bus clock (BCLK) | | | — | — | 1 | |
| | BCLK pin output | | | — | — | 1 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 1 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 1 | |

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.



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**Table 2.12 Operating Frequency (Low-Speed Operating Mode 2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | | f | 32 | — | 264 | kHz |
| | Peripheral module clock (PCLKA) | | | — | — | 264 | |
| | Peripheral module clock (PCLKB) | | | — | — | 264 | |
| | Peripheral module clock (PCLKC)*1 | | | — | — | 264 | |
| | Peripheral module clock (PCLKD)*1 | | | — | — | 264 | |
| | Flash-IF clock (FCLK) | | | 32 | — | 264 | |
| | External bus clock (BCLK) | | | — | — | 264 | |
| | BCLK pin output | | | — | — | 264 | |
| | SDRAM clock (SDCLK) | Package of 144 pins or more | | — | — | 264 | |
| | SDCLK pin output | Package of 144 pins or more | | — | — | 264 | |

Note 1. The 12-bit A/D converter cannot be used.



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## 2.4.1 Reset Timing

**Table 2.13 Reset Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RES# pulse width | Power-on | $t_{RESWP}$ | 1 | — | — | ms | Figure 2.1 |
| | Deep software standby mode | $t_{RESWD}$ | 0.6 | — | — | ms | Figure 2.2 |
| | Software standby mode, low-speed operating mode 2 | $t_{RESWS}$ | 0.3 | — | — | ms | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | $t_{RESWF}$ | 200 | — | — | µs | |
| | Other than above | $t_{RESW}$ | 200 | — | — | µs | |
| Waiting time after release from the RES# pin reset | | $t_{RESWT}$ | 54 | — | 55 | $t_{Lcyc}$ | Figure 2.1 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | $t_{RESW2}$ | 100 | — | 108 | $t_{Lcyc}$ | |

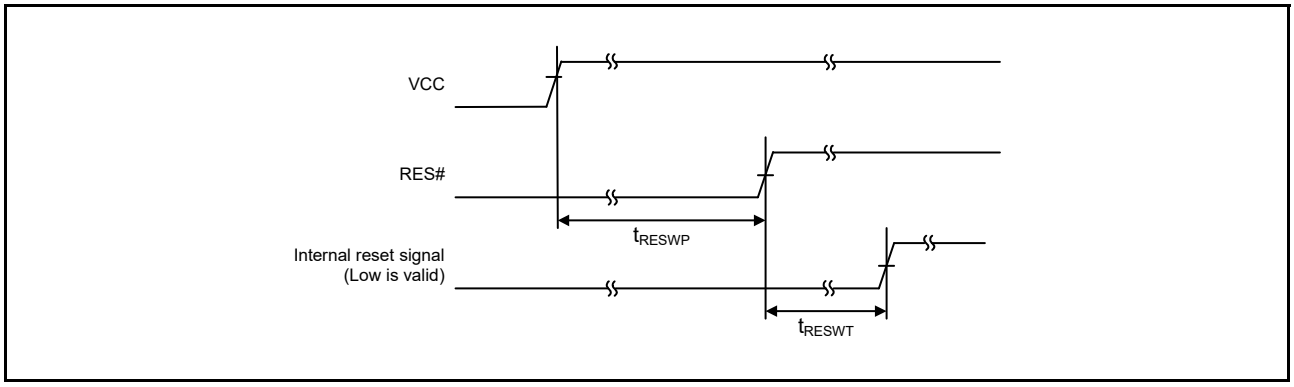



**Figure 2.1 Reset Input Timing at Power-On**

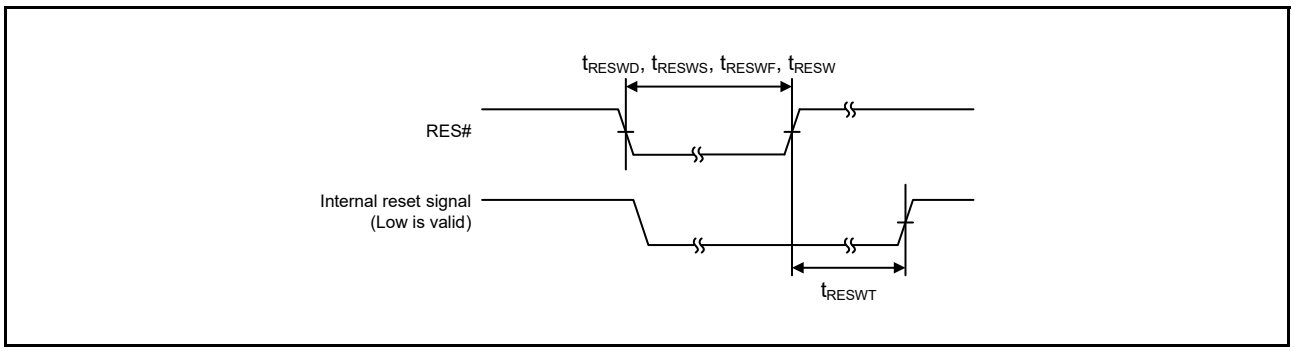



**Figure 2.2 Reset Input Timing**



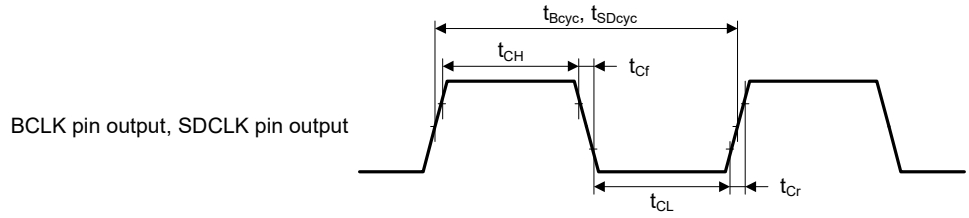
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## 2.4.2 Clock Timing

**Table 2.14 BCLK Pin Output, SDCLK Pin Output Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| BCLK pin output cycle time | Package of 144 pins or more | $t_{Bcyc}$ | 12.5 | — | — | ns | Figure 2.3 |
| | 100-pin package | | 33.2 | — | — | | |
| BCLK pin output high pulse width | | $t_{CH}$ | 3.25 | — | — | ns | |
| BCLK pin output low pulse width | | $t_{CL}$ | 3.25 | — | — | ns | |
| BCLK pin output rising time | | $t_{Cr}$ | — | — | 3 | ns | |
| BCLK pin output falling time | | $t_{Cf}$ | — | — | 3 | ns | |
| SDCLK pin output cycle time | Package of 144 pins or more | $t_{Bcyc}$ | 12.5 | — | — | ns | |
| SDCLK pin output high pulse width | | $t_{CH}$ | 3.25 | — | — | ns | |
| SDCLK pin output low pulse width | | $t_{CL}$ | 3.25 | — | — | ns | |
| SDCLK pin output rising time | | $t_{Cr}$ | — | — | 3 | ns | |
| SDCLK pin output falling time | | $t_{Cf}$ | — | — | 3 | ns | |




Test conditions: $V_{OH}$ = 0.7 × VCC, $V_{OL}$ = 0.3 × VCC, C = 30 pF

**Figure 2.3 BCLK Pin and SDCLK Pin Output Timing**



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**Table 2.15 EXTAL Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | $f_{EXMAIN}$ ≤ 24 MHz | | | $f_{EXMAIN}$ > 24 MHz | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| EXTAL external clock input cycle time | $t_{EXcyc}$ | 41.66 | — | — | 33.33 | — | — | ns | Figure 2.4 |
| EXTAL external clock input frequency | $f_{EXMAIN}$ | — | — | 24 | — | — | 30 | MHz | |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 15.83 | — | — | 13.33 | — | — | ns | |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 15.83 | — | — | 13.33 | — | — | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | — | — | 5 | — | — | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | — | — | 5 | — | — | 5 | ns | |

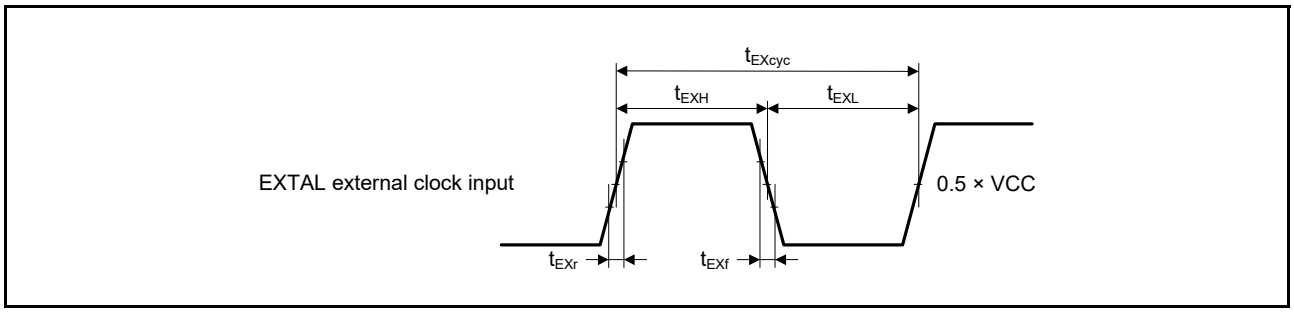



**Figure 2.4 EXTAL External Clock Input Timing**

**Table 2.16 Main Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Main clock oscillation frequency | $f_{MAIN}$ | 8 | — | 24 | MHz | |
| Main clock oscillator stabilization time (crystal) | $t_{MAINOSC}$ | — | — | —*1 | ms | Figure 2.5 |
| Main clock oscillation stabilization wait time (crystal) | $t_{MAINOSCWT}$ | — | — | —*2 | ms | |

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / $f_{LOCO}$

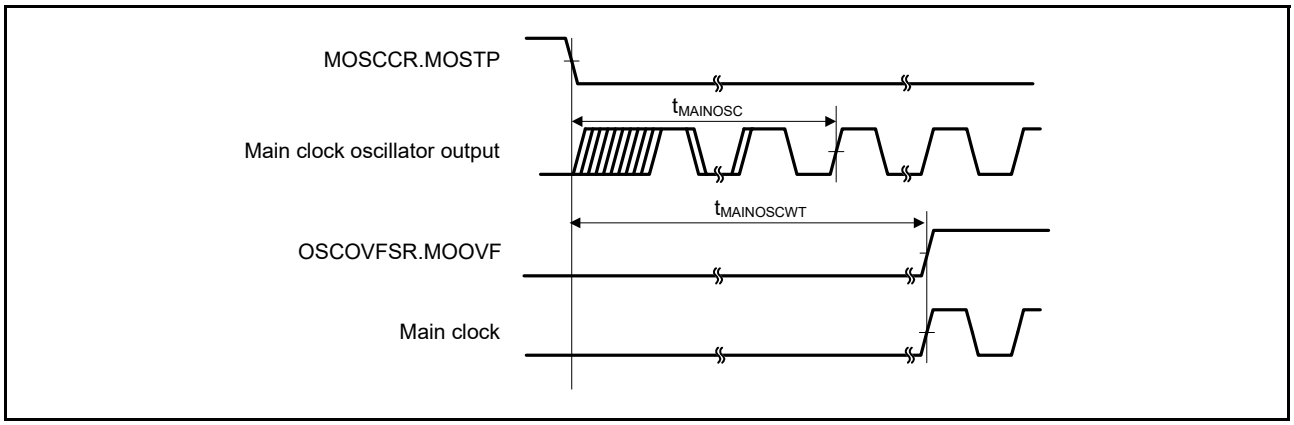



**Figure 2.5 Main Clock Oscillation Start Timing**



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**Table 2.17 LOCO and IWDT-Dedicated Low-Speed Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LOCO clock cycle time | $t_{Lcyc}$ | 4.63 | 4.16 | 3.78 | µs | |
| LOCO clock oscillation frequency | $f_{LOCO}$ | 216 | 240 | 264 | kHz | |
| LOCO clock oscillation stabilization wait time | $t_{LOCOWT}$ | — | — | 44 | µs | Figure 2.6 |
| IWDT-dedicated low-speed clock cycle time | $t_{ILcyc}$ | 9.26 | 8.33 | 7.57 | µs | |
| IWDT-dedicated low-speed clock oscillation frequency | $f_{ILOCO}$ | 108 | 120 | 132 | kHz | |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{ILOCOWT}$ | — | 142 | 190 | µs | Figure 2.7 |

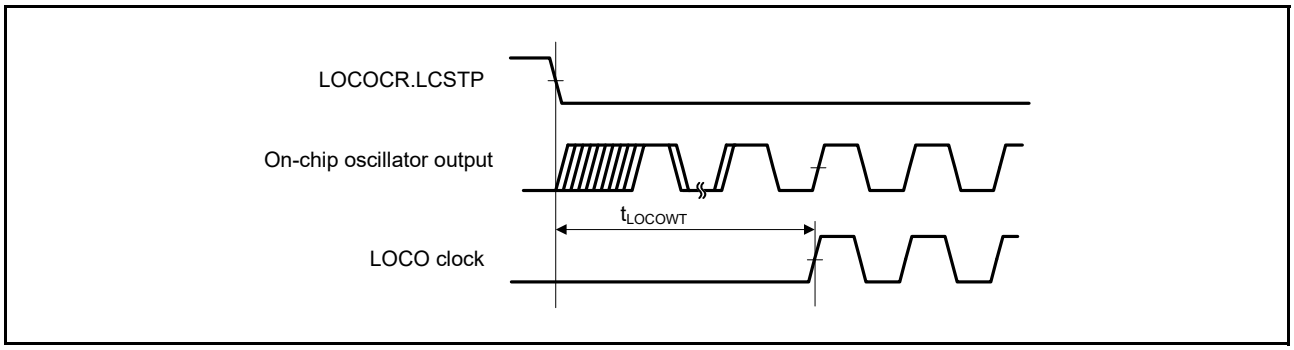



**Figure 2.6 LOCO Clock Oscillation Start Timing**

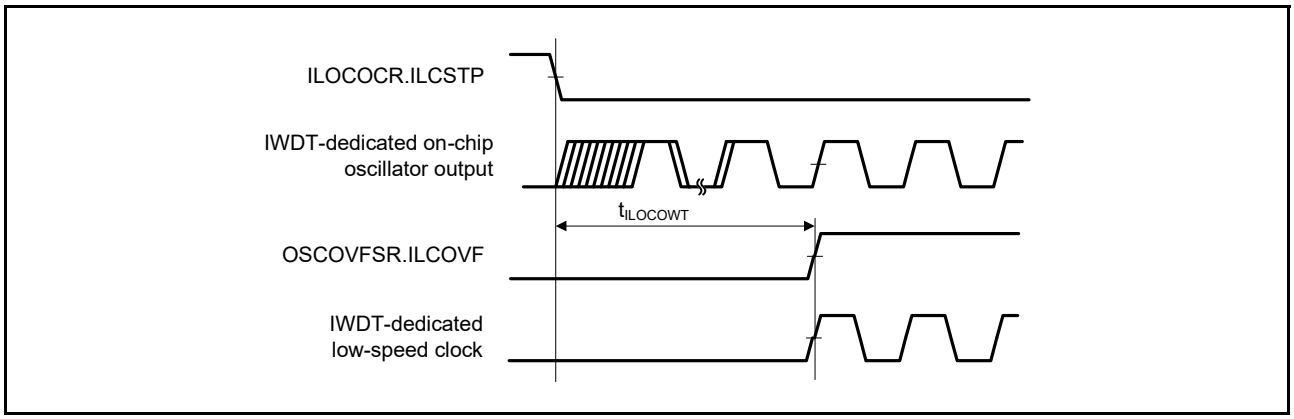



**Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing**



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**Table 2.18 HOCO Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| HOCO clock oscillation frequency | $f_{HOCO}$ | 15.61 | 16 | 16.39 | MHz | $T_a \geq -20°C$ |
| | | 17.56 | 18 | 18.44 | | |
| | | 19.52 | 20 | 20.48 | | |
| | | 15.52 | 16 | 16.48 | | $-40°C \leq T_a < -20°C$ |
| | | 17.46 | 18 | 18.54 | | |
| | | 19.4 | 20 | 20.6 | | |
| HOCO clock oscillation stabilization wait time | $t_{HOCOWT}$ | — | 105 | 149 | μs | Figure 2.8 |
| HOCO clock power supply stabilization time | $t_{HOCOP}$ | — | — | 150 | μs | Figure 2.9 |

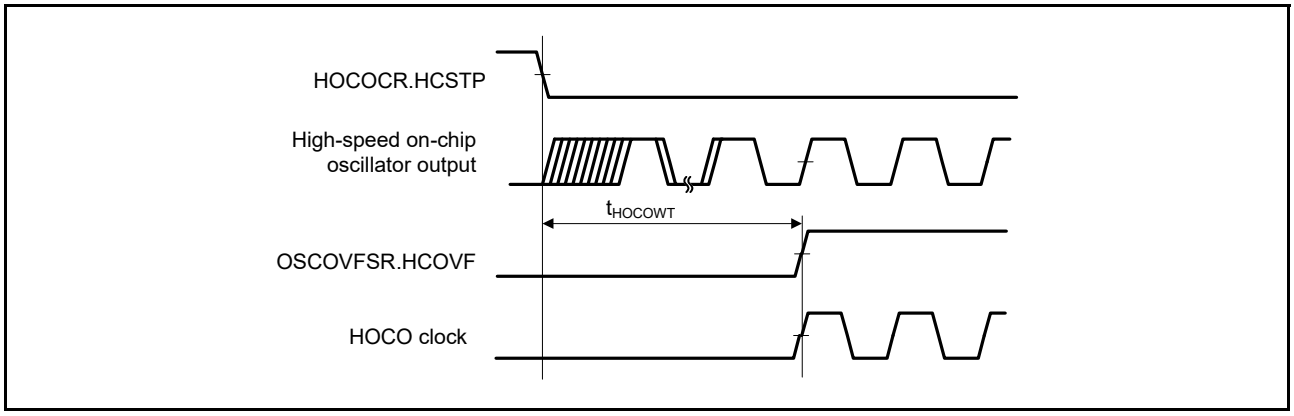



**Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)**

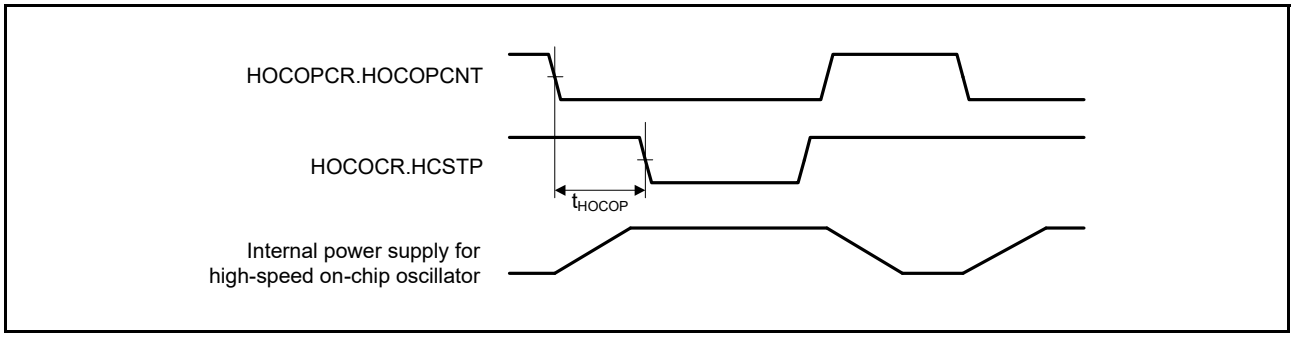



**Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing**



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**Table 2.19 PLL/PPLL Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PLL/PPLL clock oscillation frequency | $f_{PLL}$ | 120 | — | 240 | MHz | |
| PLL/PPLL clock oscillation stabilization wait time | $t_{PLLWT}$ | — | 259 | 320 | µs | Figure 2.10 |

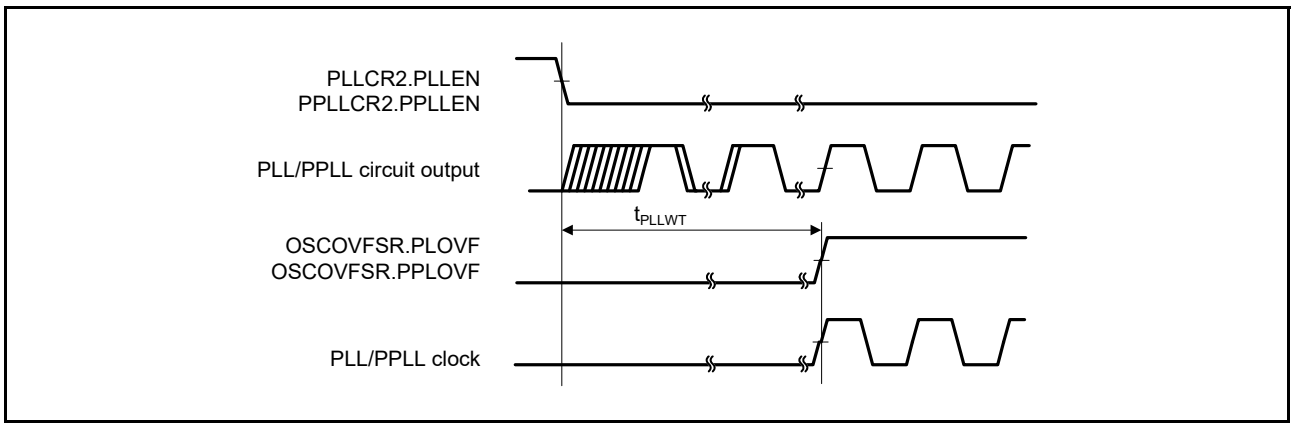



**Figure 2.10 PLL/PPLL Clock Oscillation Start Timing**

**Table 2.20 Sub-Clock Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$V_{BATT}$ = 1.62 to 3.6 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sub-clock oscillation frequency | $f_{SUB}$ | — | 32.768 | — | kHz | |
| Sub-clock oscillation stabilization time | $t_{SUBOSC}$ | — | — | *1 | s | Figure 2.11 |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | *2 | s | |

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / $f_{LOCO}$

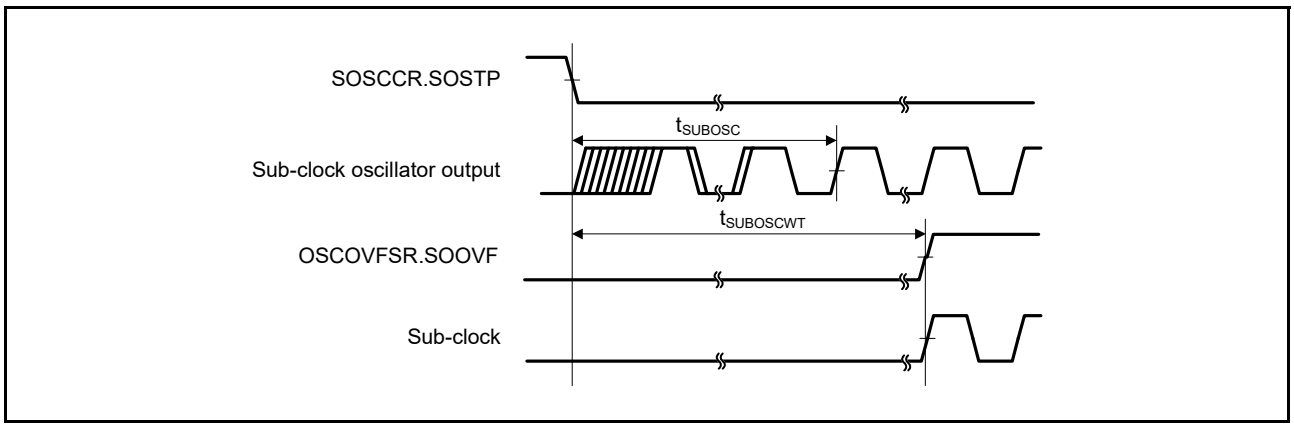



**Figure 2.11 Sub-Clock Oscillation Start Timing**



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**Table 2.21 CLKOUT Pin Output Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| CLKOUT pin output cycle time | $t_{Ccyc}$ | 25 | — | — | ns | Figure 2.12 $t_{Ccyc}$ = 25 ns |
| CLKOUT pin output high pulse width*1 | $t_{CH}$ | 5 | — | — | ns | |
| CLKOUT pin output low pulse width*1 | $t_{CL}$ | 5 | — | — | ns | |
| CLKOUT pin output rising time | $t_{Cr}$ | — | — | 5 | ns | |
| CLKOUT pin output falling time | $t_{Cf}$ | — | — | 5 | ns | |

Note 1. If the main clock oscillator is selected by the CLKOUT output source select bit (CKOCR.CKOSEL[2:0]) and the external clock input is selected by the main clock oscillator switching bit (MOFCR.MOSEL), the pulse width depends on the input clock wave form.

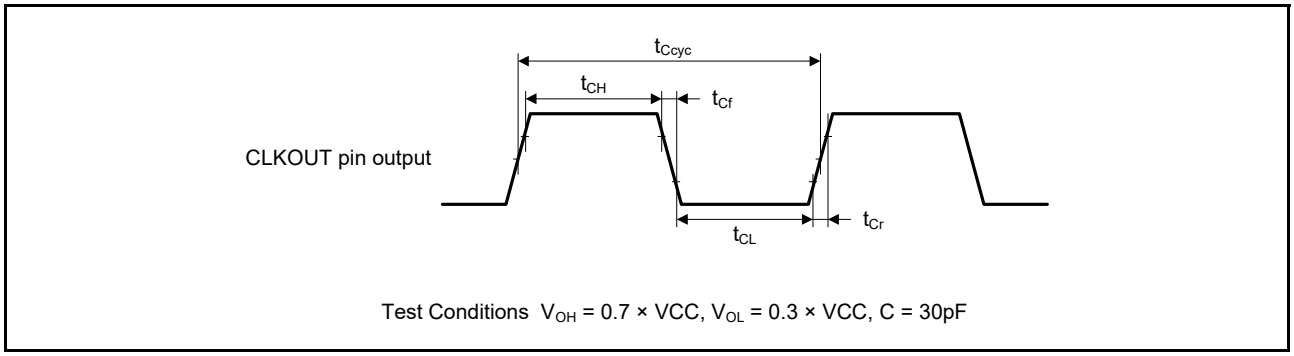



**Figure 2.12 CLKOUT Pin Output Timing**

**Table 2.22 CLKOUT25M Pin Output Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
High-speed interface high-drive is selected by the drive capacity control register

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| CLKOUT25M pin output cycle time | $t_{Ccyc}$ | — | 40 | — | ns | Figure 2.13 |
| CLKOUT25M pin output high pulse width | $t_{CH}$ | 13 | — | — | ns | |
| CLKOUT25M pin output low pulse width | $t_{CL}$ | 13 | — | — | ns | |
| CLKOUT25M pin output rising time | $t_{Cr}$ | — | — | 3 | ns | |
| CLKOUT25M pin output falling time | $t_{Cf}$ | — | — | 3 | ns | |

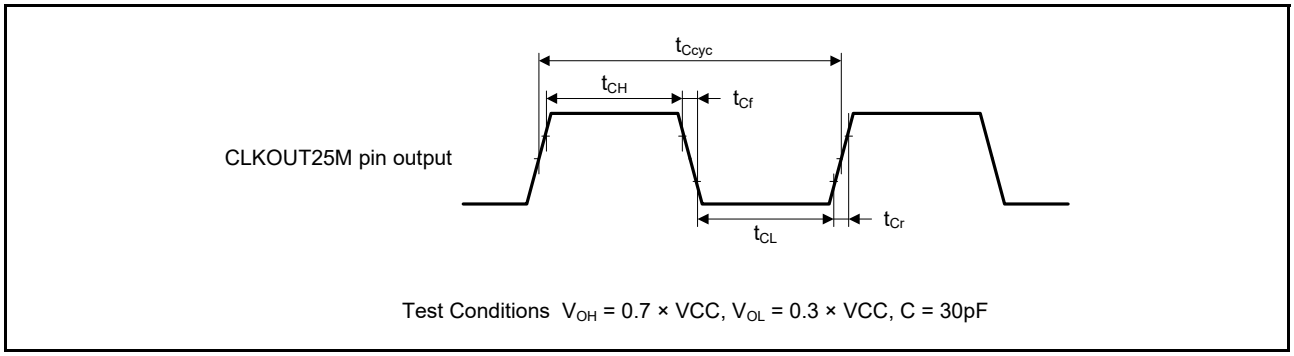



**Figure 2.13 CLKOUT25M Pin Output Timing**



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## 2.4.3 Timing of Recovery from Low Power Consumption Modes

**Table 2.23 Timing of Recovery from Low Power Consumption Modes (1)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $t_{SBYOSCWT}$*2 | $t_{SBYSEQ}$*3 | | |
| Recovery time from software standby mode *1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | — | — | {(MSTS[7:0] bit × 32) + 76} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{MAIN}$ | µs | Figure 2.14 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | | | {(MSTS[7:0] bit × 32) + 138} / 0.216 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | | | 352 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | | | 639 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | | | {(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / $f_{FCLK}$ | 100 + 4 / $f_{ICLK}$ + 2n / $f_{SUE}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | $t_{SBYHO}$ | | | 454 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | $t_{SBYPH}$ | | | 741 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating*4 | | $t_{SBYLO}$ | | | 338 | 100 + 7 / $f_{ICLK}$ + 2n / $f_{LOCO}$ | | |

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer ($t_{SBYSEQ}$).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when $f_{ICLK}$:$f_{FCLK}$ = 1:1, 2:1, or 4:1.



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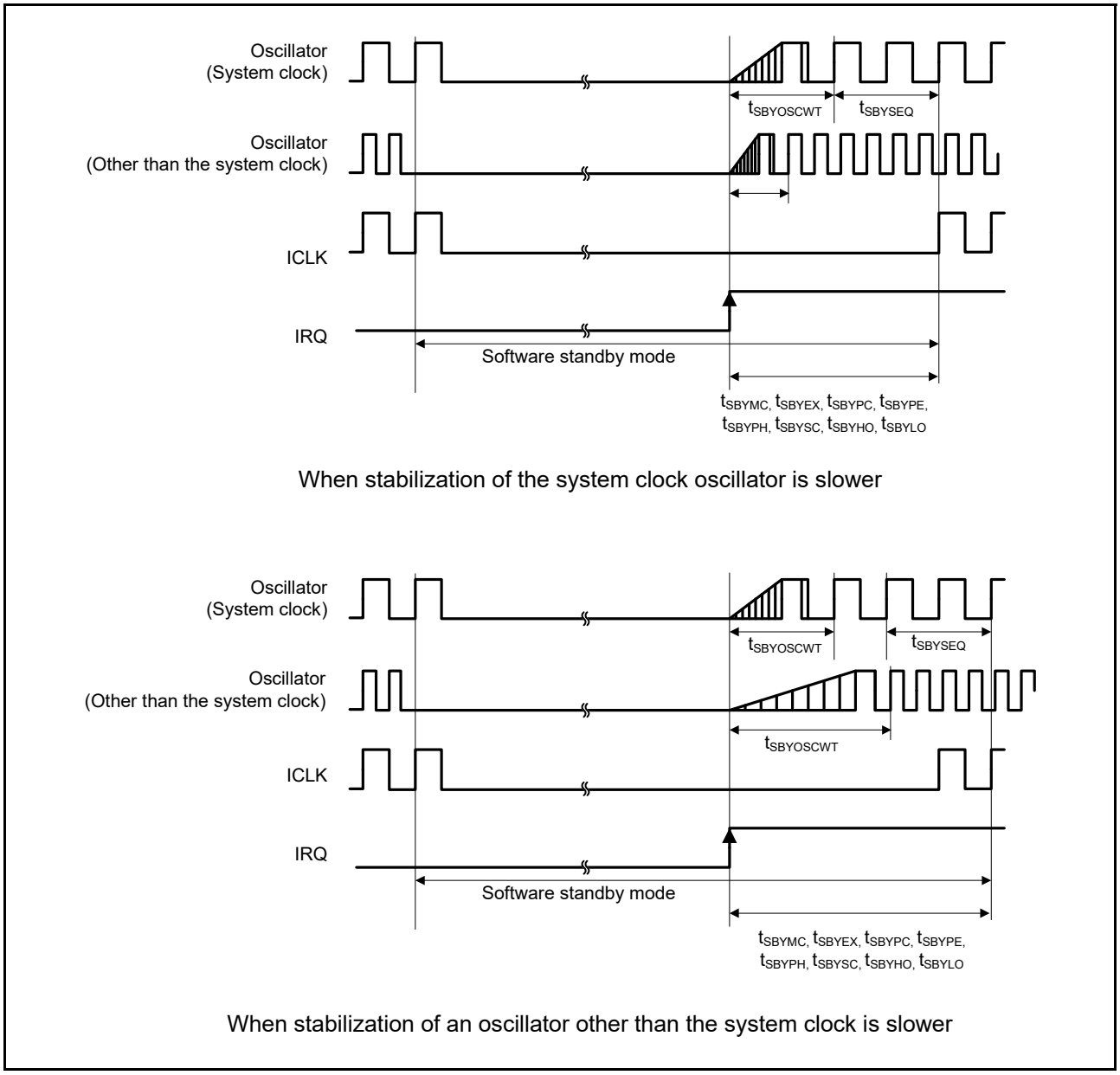



**Figure 2.14 Software Standby Mode Recovery Timing**



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**Table 2.24 Timing of Recovery from Low Power Consumption Modes (2)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Recovery time from deep software standby mode | $t_{DSBY}$ | — | — | 0.9 | ms | Figure 2.15 |
| Wait time after recovery from deep software standby mode | $t_{DSBYWT}$ | 23 | — | 24 | $t_{Lcyc}$ | |

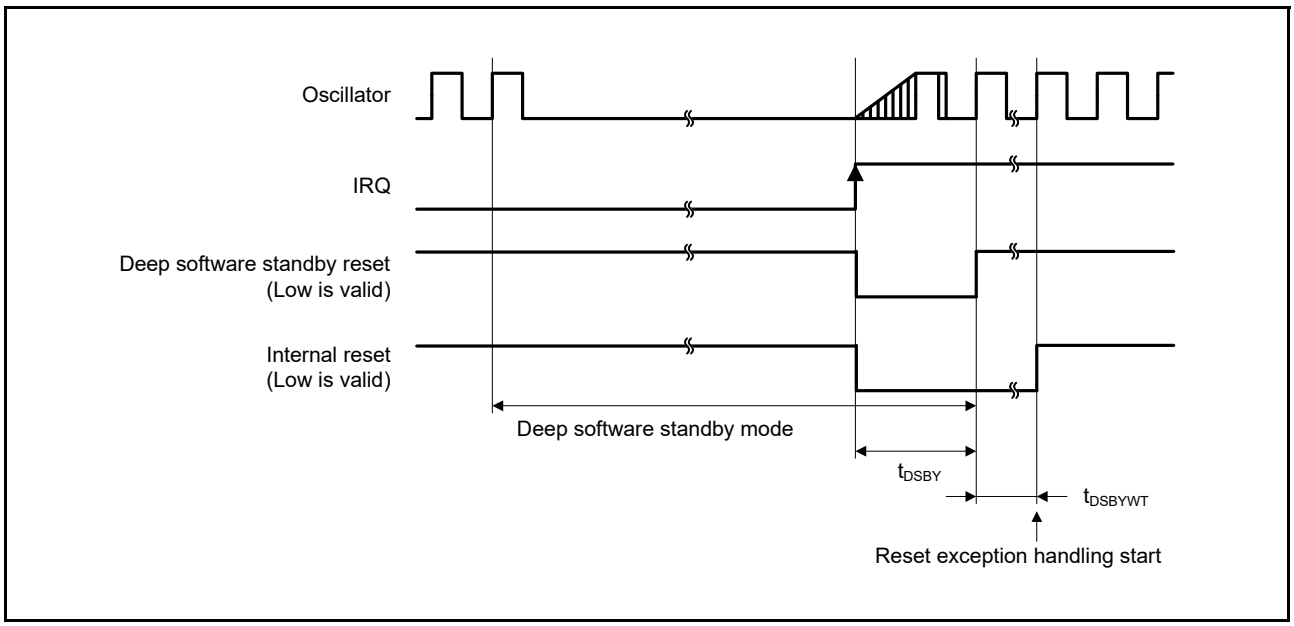



**Figure 2.15 Deep Software Standby Mode Recovery Timing**



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## 2.4.4 Control Signal Timing

**Table 2.25 Control Signal Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 2.16 |
| | | $t_{PBcyc}$ × 2 | — | — | | $t_{PBcyc}$ × 2 > 200 ns, Figure 2.16 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{PBcyc}$ × 2 ≤ 200 ns, Figure 2.17 |
| | | $t_{PBcyc}$ × 2 | — | — | | $t_{PBcyc}$ × 2 > 200 ns, Figure 2.17 |

Note 1. $t_{PBcyc}$: PCLKB cycle

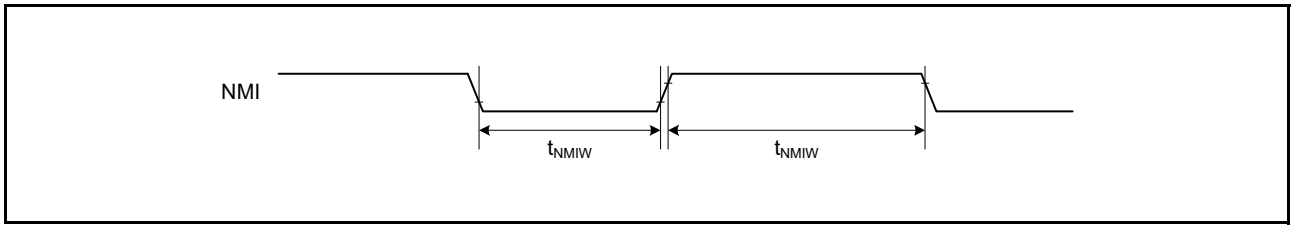



**Figure 2.16 NMI Interrupt Input Timing**

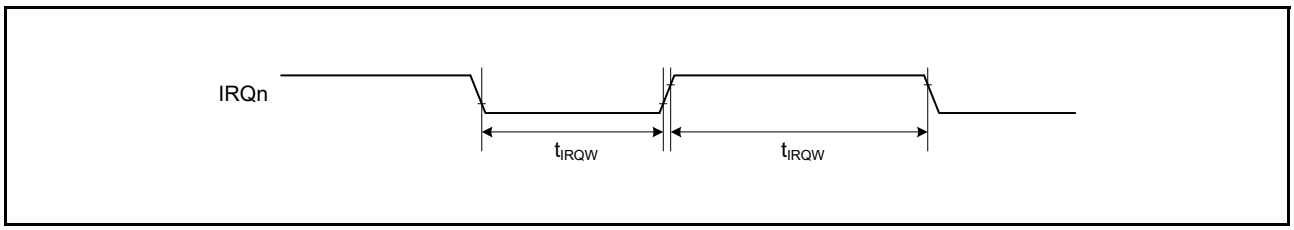



**Figure 2.17 IRQ Interrupt Input Timing**



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## 2.4.5 Bus Timing

**Table 2.26 Bus Timing**

Conditions 1: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Conditions 2: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = 60 to 120 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, 60 MHz < BCLK = SDCLK ≤ 80 MHz,
$T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC,
C = 15 pF for the SDCLK pin, C = 30 pF for other pins.

To control the drive capacity when using the SDRAM: set the PFBCR3.SDCLKDRV bit in external bus control register 1 to 1 to select the drive capacity of the SDCLK pin, and set the SDRAM pins other than the SDCLK pin as high-speed-interface driving outputs.

| Item | Symbol | Conditions 1 | | Conditions 2 | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| Address delay time | $t_{AD}$ | — | 12.5 | — | 12.5 | ns | Figure 2.18 to Figure 2.23 |
| Byte control delay time | $t_{BCD}$ | — | 12.5 | — | 12.5 | ns | |
| CS# delay time | $t_{CSD}$ | — | 12.5 | — | 12.5 | ns | |
| ALE delay time | $t_{ALED}$ | — | 12.5 | — | 12.5 | ns | |
| RD# delay time | $t_{RSD}$ | — | 12.5 | — | 12.5 | ns | |
| Read data setup time | $t_{RDS}$ | 12.5 | — | 12.5 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | 0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 12.5 | — | 12.5 | ns | |
| Write data delay time | $t_{WDD}$ | — | 12.5 | — | 12.5 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 12.5 | — | 12.5 | — | ns | Figure 2.24 |
| WAIT# hold time | $t_{WTH}$ | 0 | — | 0 | — | ns | |
| Address delay time 2 (SDRAM) | $t_{AD2}$ | 1 | 12.5 | 1 | 10.0 | ns | Figure 2.25 to Figure 2.31 |
| CS# delay time 2 (SDRAM) | $t_{CSD2}$ | 1 | 12.5 | 1 | 10.0 | ns | |
| DQM delay time (SDRAM) | $t_{DQMD}$ | 1 | 12.5 | 1 | 10.0 | ns | |
| CKE delay time (SDRAM) | $t_{CKED}$ | 1 | 12.5 | 1 | 10.0 | ns | |
| Read data setup time 2 (SDRAM) | $t_{RDS2}$ | 10 | — | 6.0 | — | ns | |
| Read data hold time 2 (SDRAM) | $t_{RDH2}$ | 0 | — | 0 | — | ns | |
| Write data delay time 2 (SDRAM) | $t_{WDD2}$ | — | 12.5 | — | 10.0 | ns | |
| Write data hold time 2 (SDRAM) | $t_{WDH2}$ | 1 | — | 1 | — | ns | |
| WE# delay time (SDRAM) | $t_{WED}$ | 1 | 12.5 | 1 | 10.0 | ns | |
| RAS# delay time (SDRAM) | $t_{RASD}$ | 1 | 12.5 | 1 | 10.0 | ns | |
| CAS# delay time (SDRAM) | $t_{CASD}$ | 1 | 12.5 | 1 | 10.0 | ns | |



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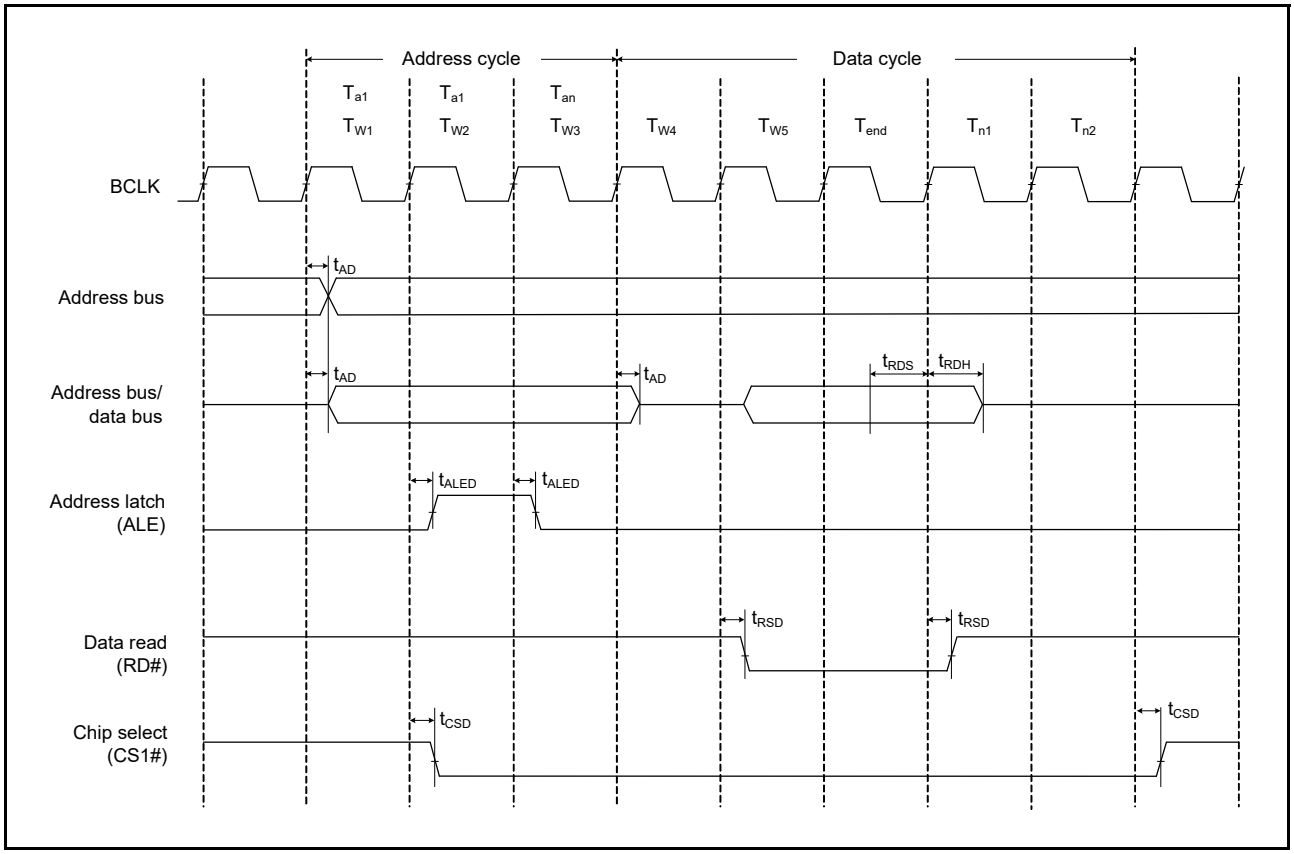



**Figure 2.18 Address/Data Multiplexed Bus Read Access Timing**

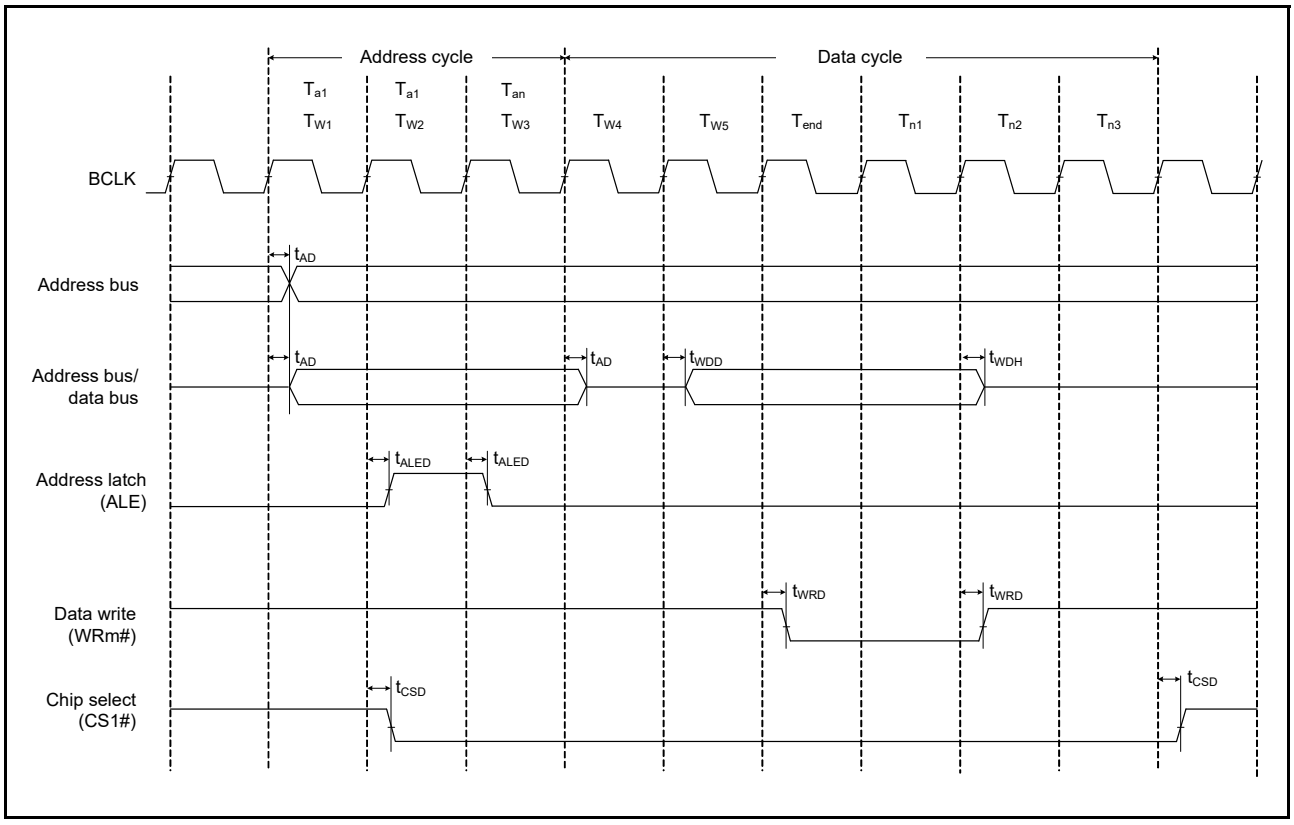



**Figure 2.19 Address/Data Multiplexed Bus Write Access Timing**



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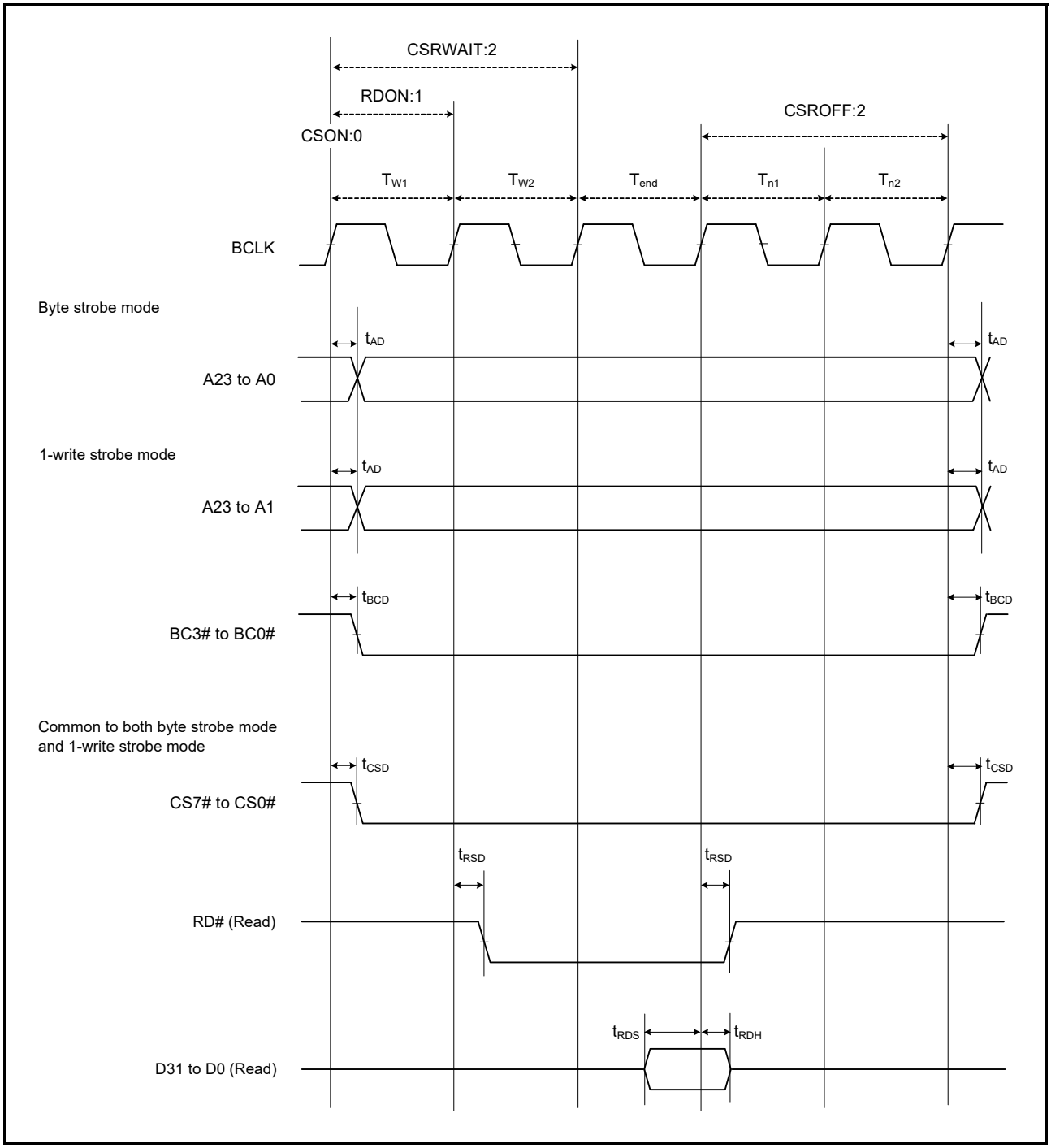
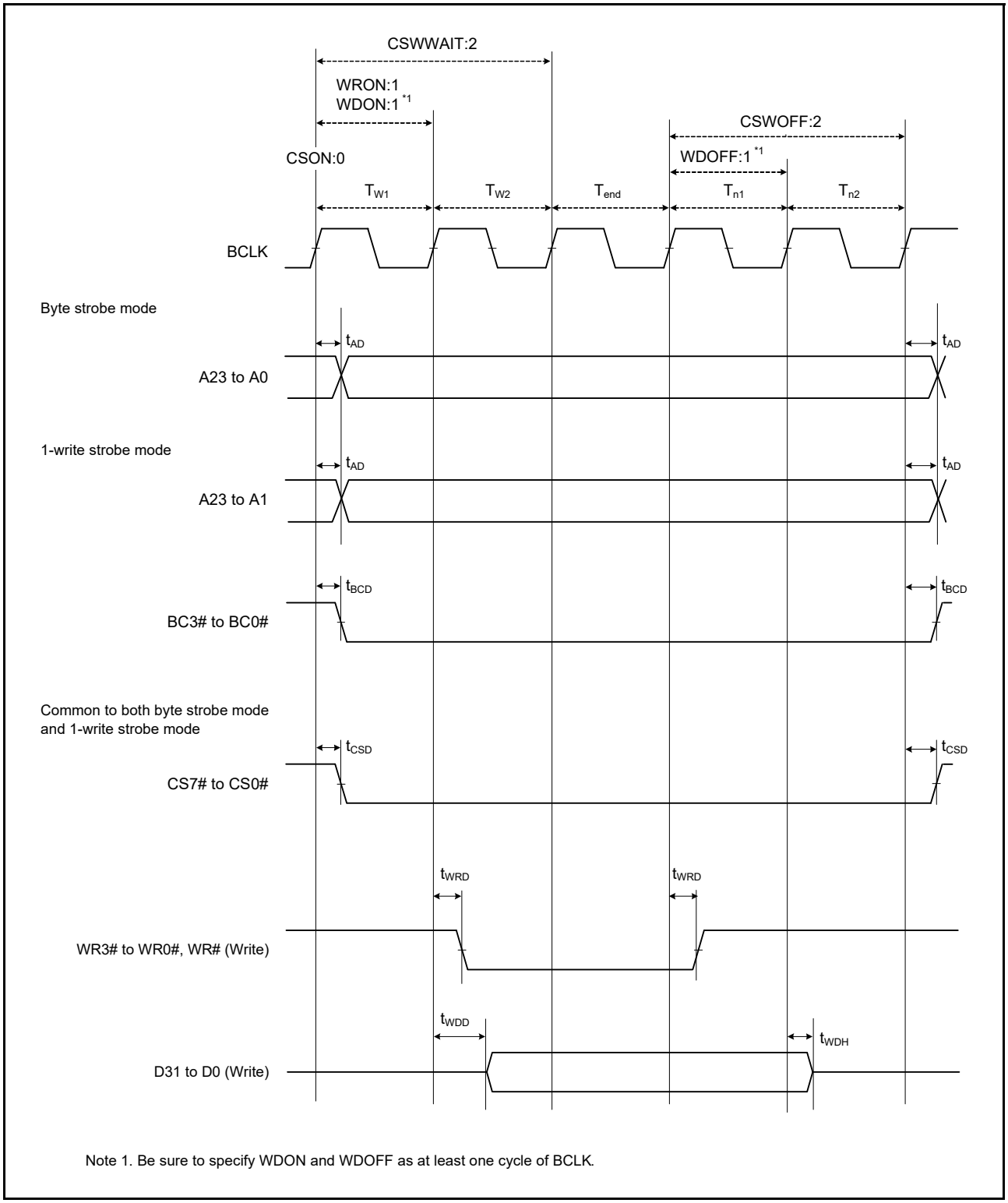



**Figure 2.20 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**



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Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

**Figure 2.21 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)**



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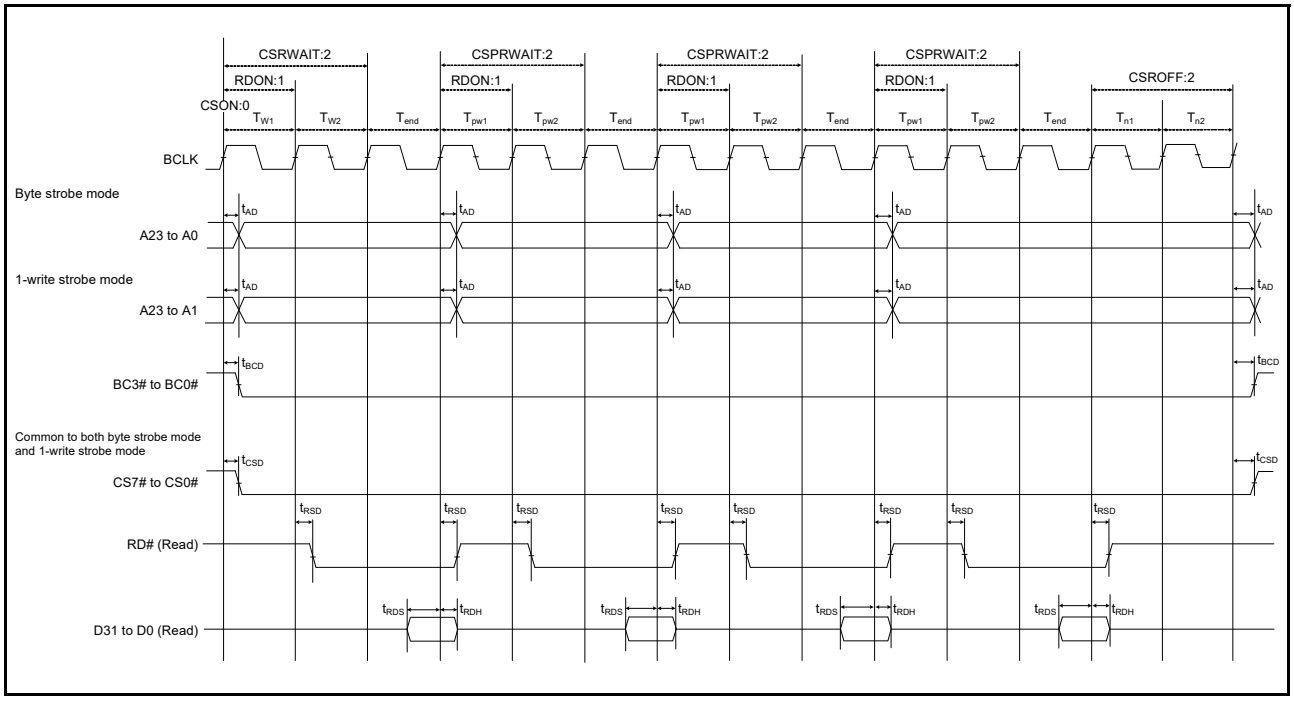
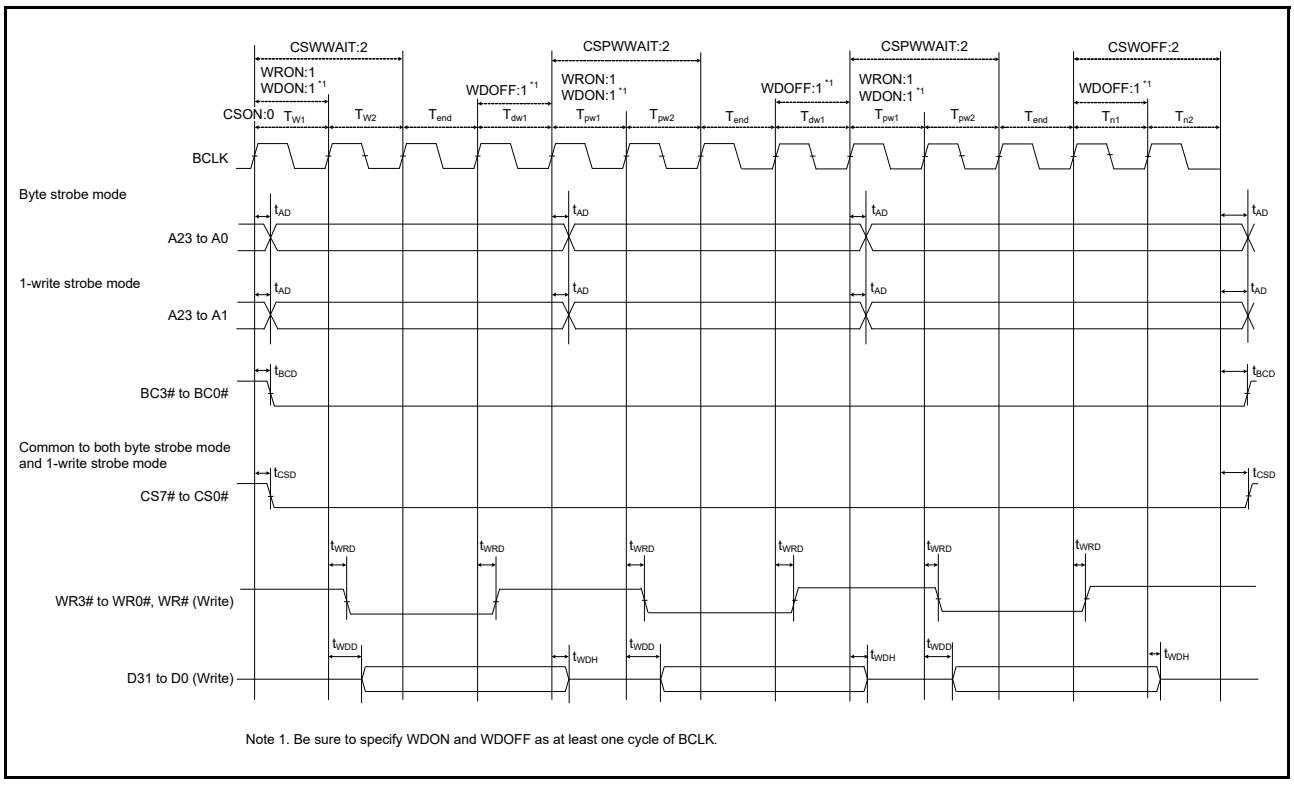



**Figure 2.22 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)**




Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

**Figure 2.23 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)**



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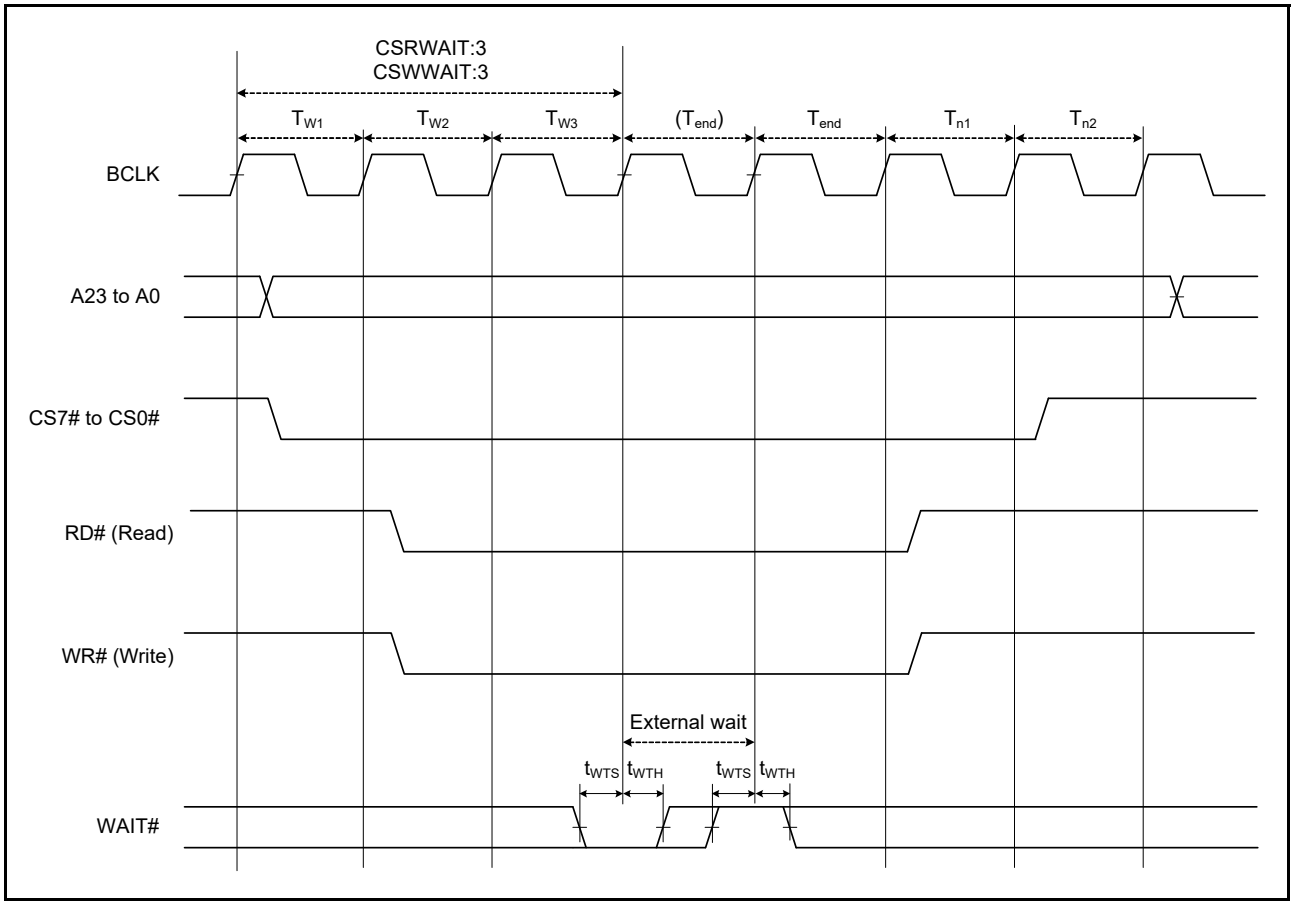
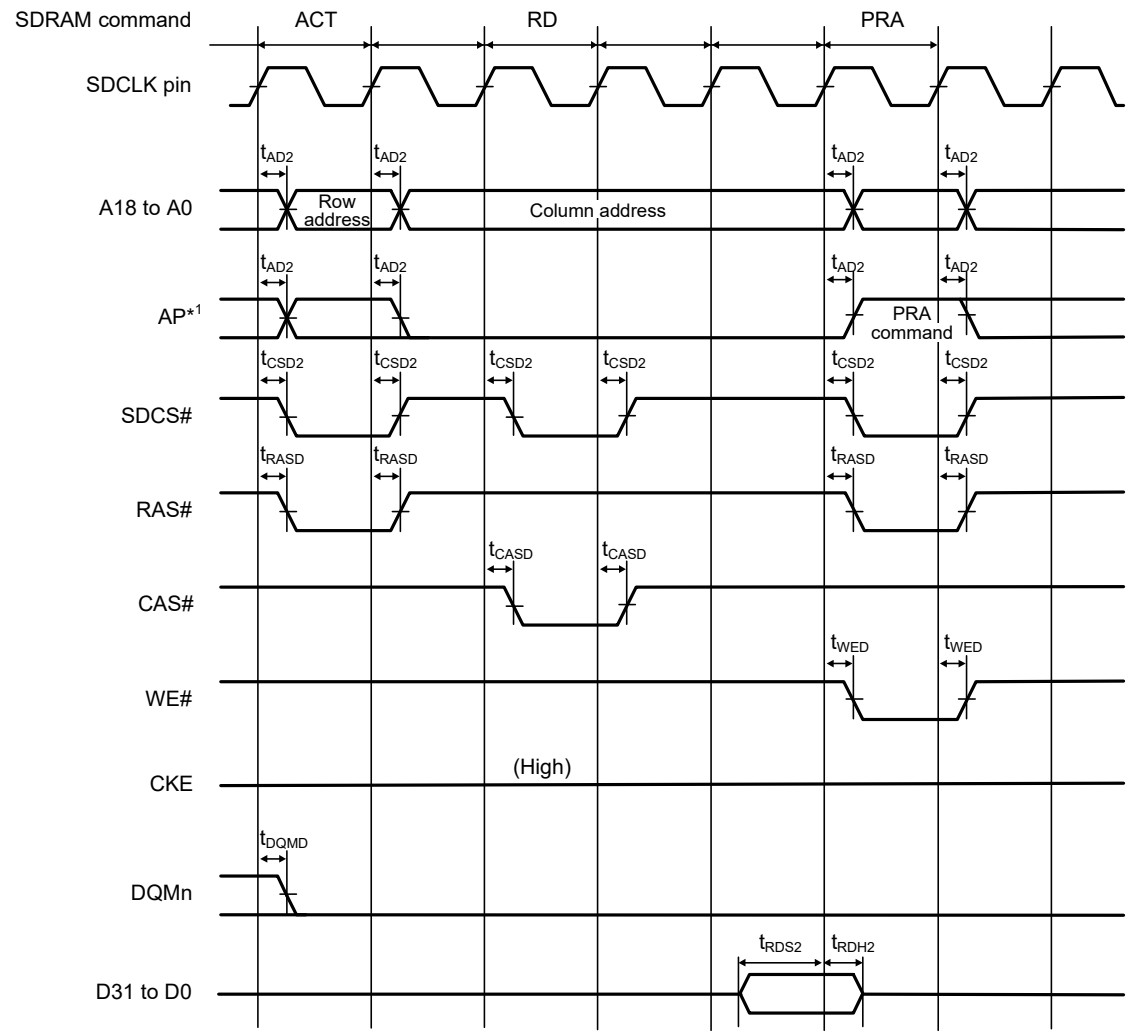



**Figure 2.24 External Bus Timing/External Wait Control**



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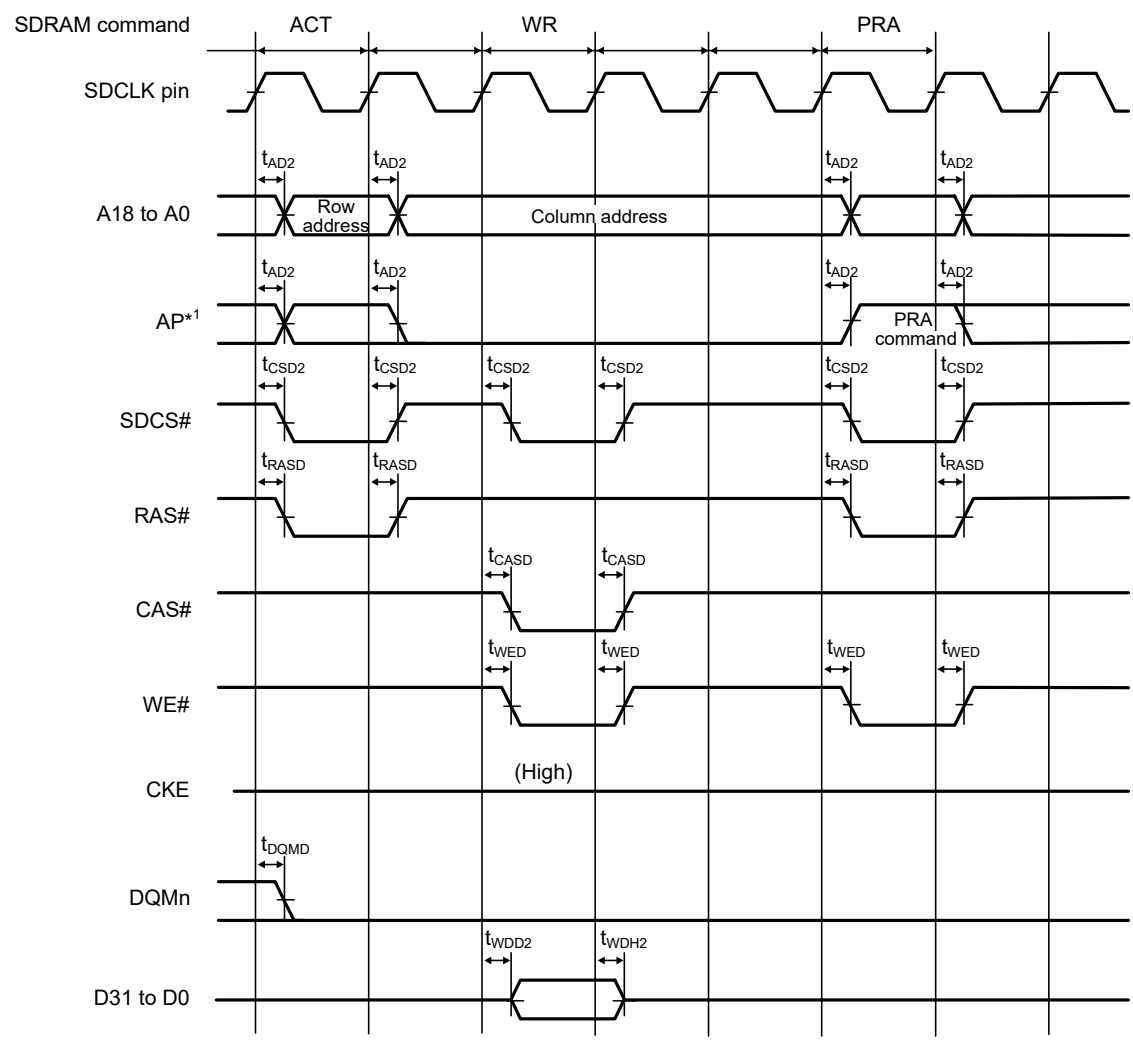



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.25 SDRAM Space Single Read Bus Timing**



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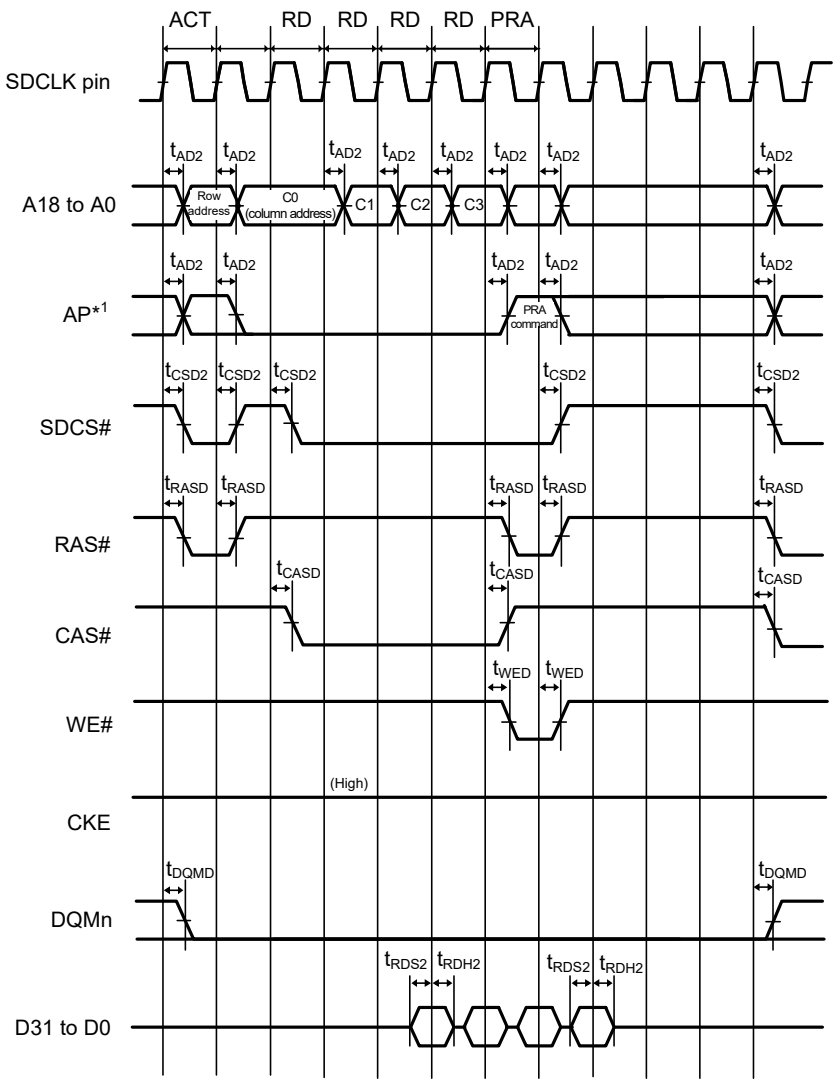



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.26 SDRAM Space Single Write Bus Timing**



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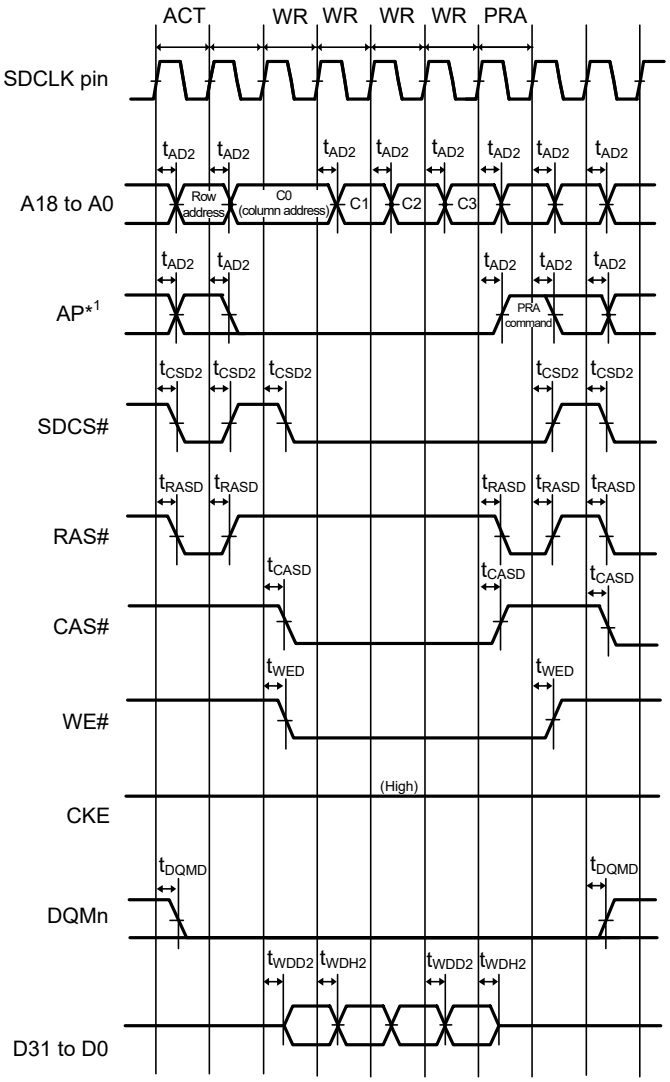



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.27 SDRAM Space Multiple Read Bus Timing**



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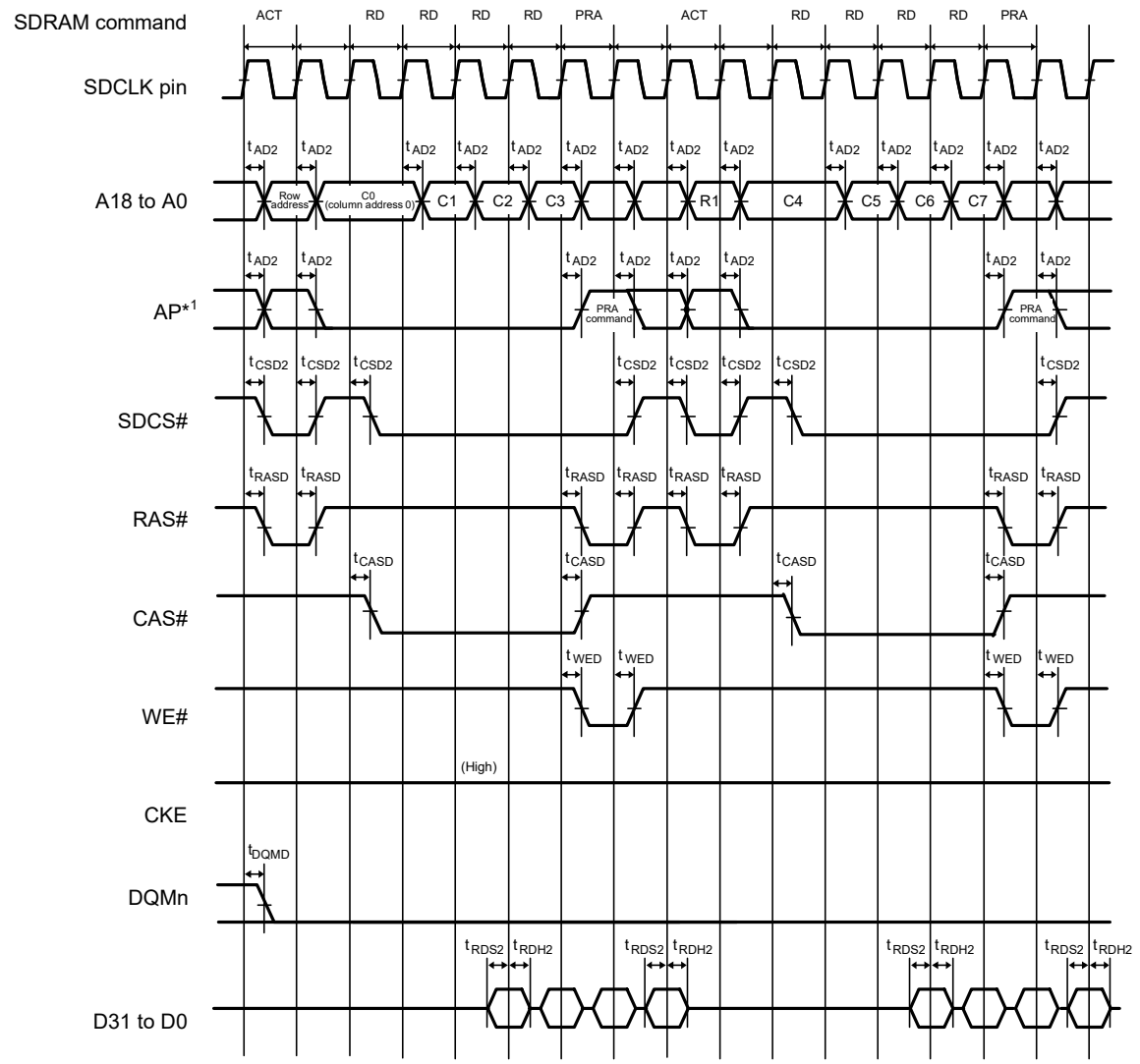



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.28 SDRAM Space Multiple Write Bus Timing**



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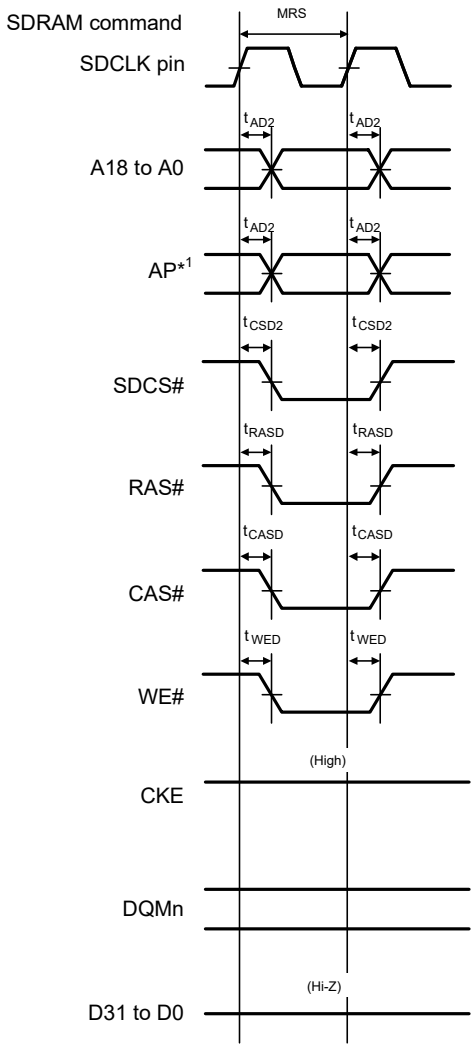



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.29 SDRAM Space Multiple Read Line Stride Bus Timing**



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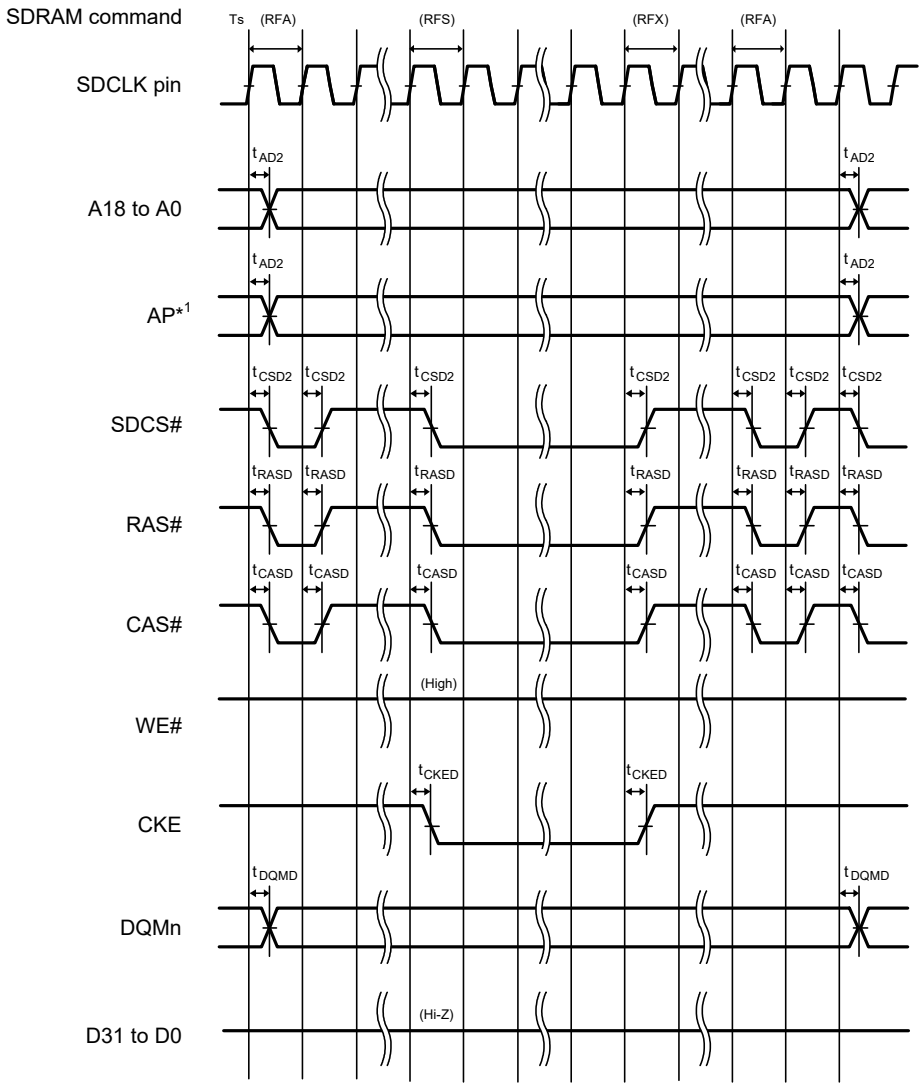



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.30 SDRAM Space Mode Register Set Bus Timing**



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Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 2.31 SDRAM Space Self-Refresh Bus Timing**



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## 2.4.6 EXDMAC Timing

**Table 2.27 EXDMAC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, BCLK = SDCLK = 8 to 80 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 13 | — | ns | Figure 2.32 |
| | EDREQ hold time | $t_{EDRQH}$ | 2 | — | ns | |
| | EDACK delay time | $t_{EDACD}$ | — | 13 | ns | Figure 2.33, Figure 2.34 |

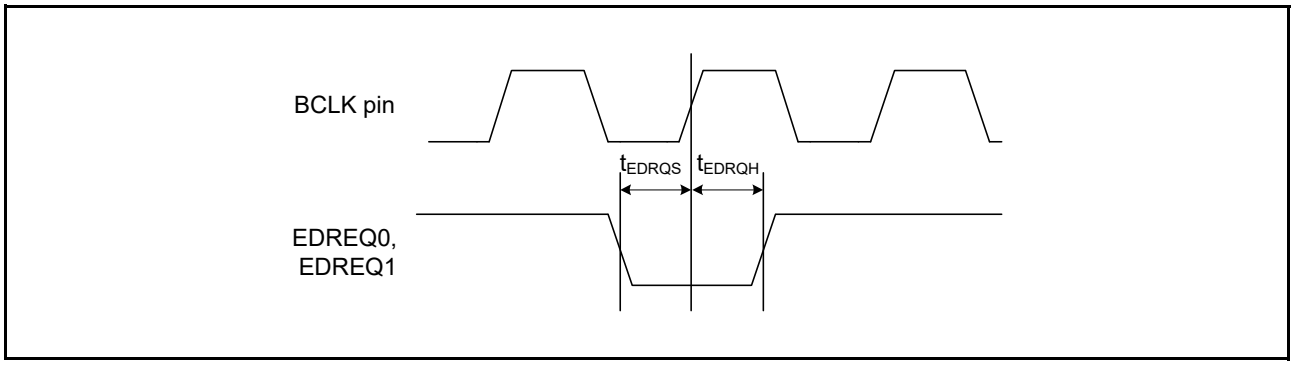



**Figure 2.32 EDREQ0 and EDREQ1 Input Timing**

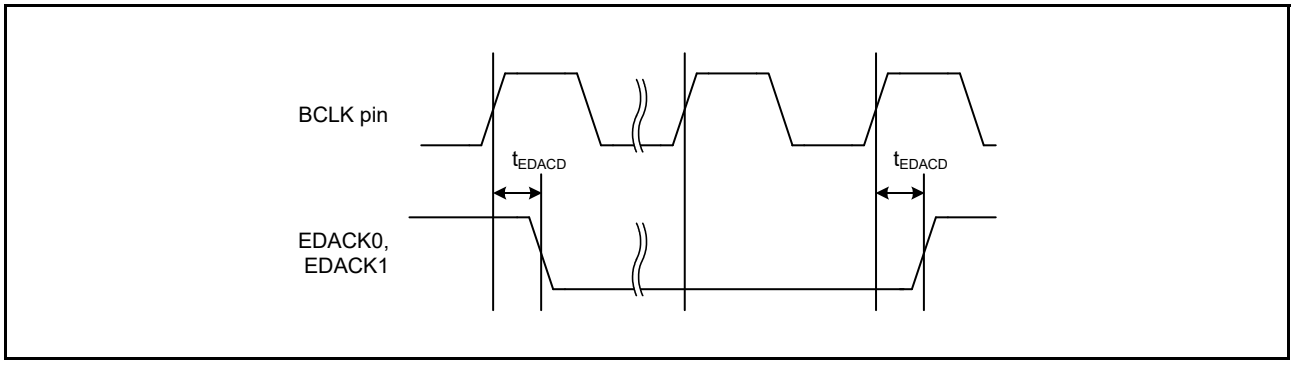



**Figure 2.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**

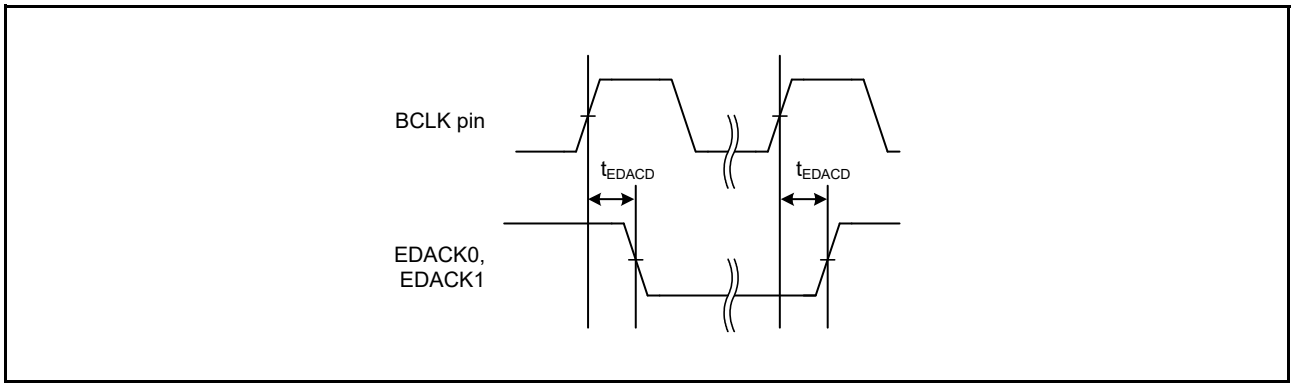



**Figure 2.34 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**



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## 2.4.7 Timing of On-Chip Peripheral Modules

### 2.4.7.1 I/O Port

**Table 2.28 I/O Port Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | $t_{PRW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.35 |

Note 1. $t_{PBcyc}$: PCLKB cycle

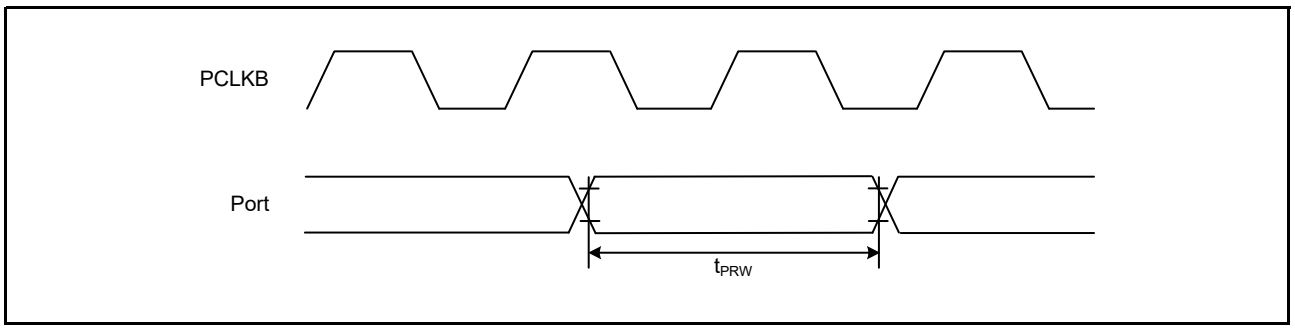



**Figure 2.35 I/O Port Input Timing**



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### 2.4.7.2 TPU

**Table 2.29 TPU Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TPU | Input capture input pulse width | Single-edge setting | $t_{TICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.36 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{TCKWH}$, $t_{TCKWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.37 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

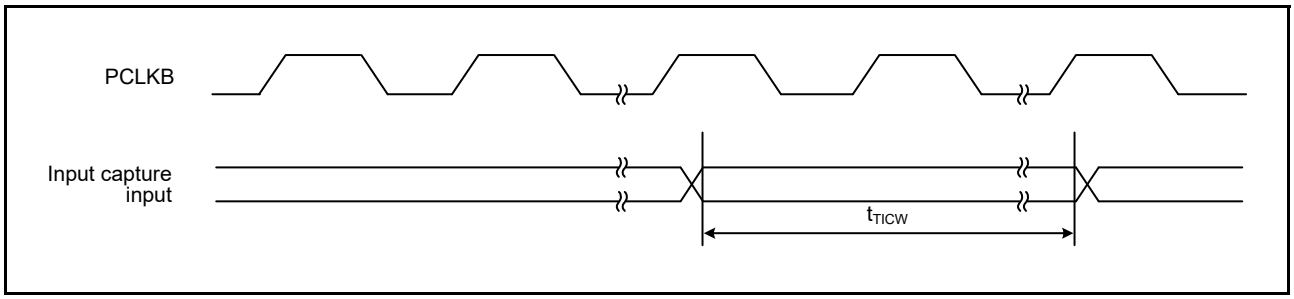



**Figure 2.36 TPU Input Capture Input Timing**

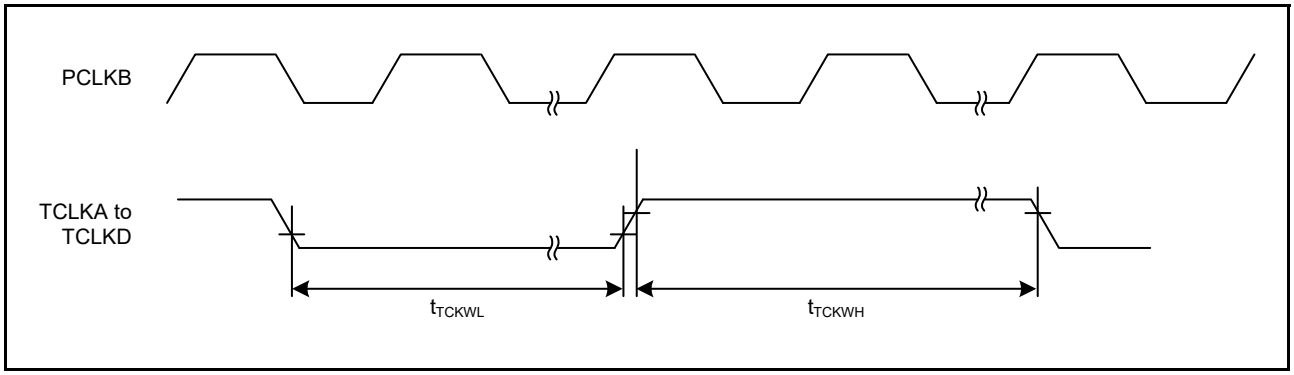



**Figure 2.37 TPU Clock Input Timing**



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### 2.4.7.3 TMR

**Table 2.30 TMR Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TMR | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$, $t_{TMCWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.38 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

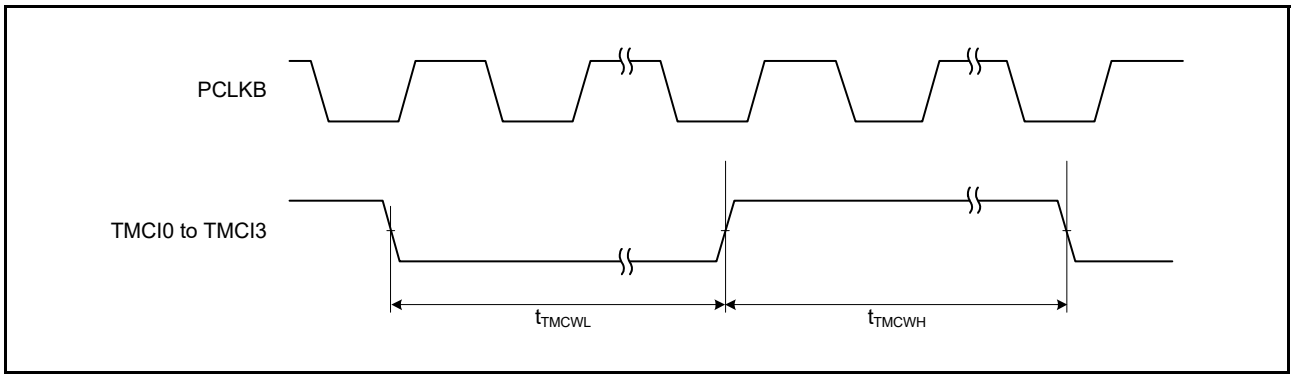



**Figure 2.38 TMR Clock Input Timing**

### 2.4.7.4 CMTW

**Table 2.31 CMTW Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| CMTW | Input capture input pulse width | Single-edge setting | $t_{CMTWTICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.39 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

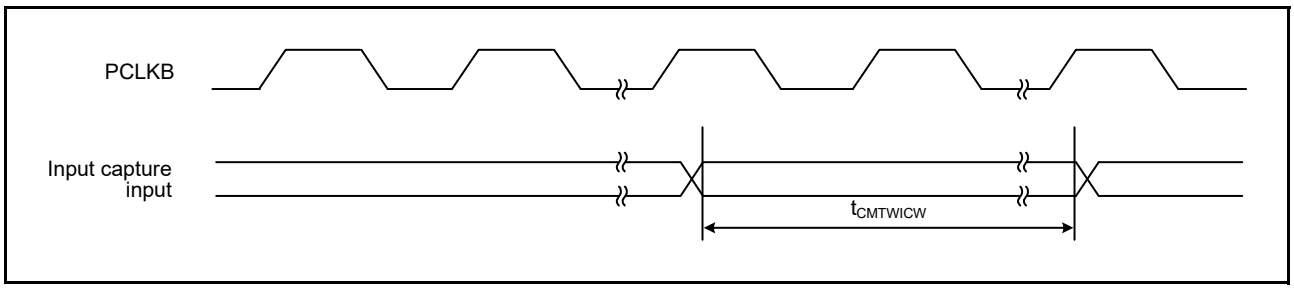



**Figure 2.39 CMTW Input Capture Input Timing**



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### 2.4.7.5 MTU

**Table 2.32 MTU Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| MTU | Input capture input pulse width | Single-edge setting | $t_{MTICW}$ | 1.5 | — | $t_{PAcyc}$ | Figure 2.40 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{MTCKWH}$, $t_{MTCKWL}$ | 1.5 | — | $t_{PAcyc}$ | Figure 2.41 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. $t_{PAcyc}$: PCLKA cycle

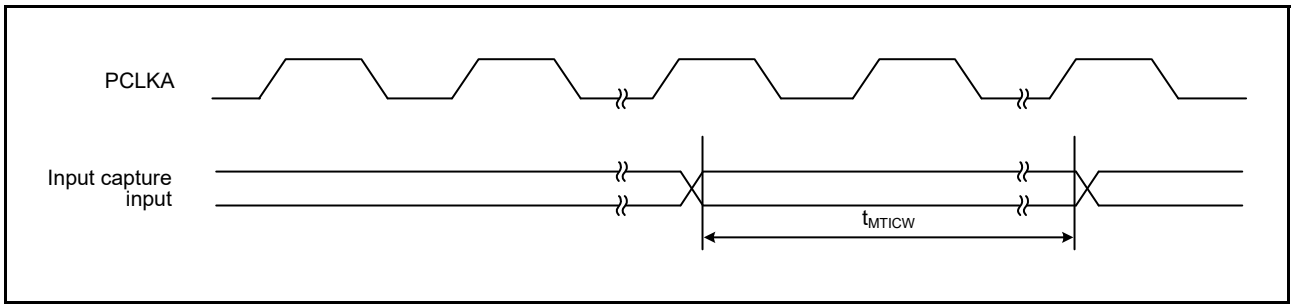



**Figure 2.40 MTU Input Capture Input Timing**

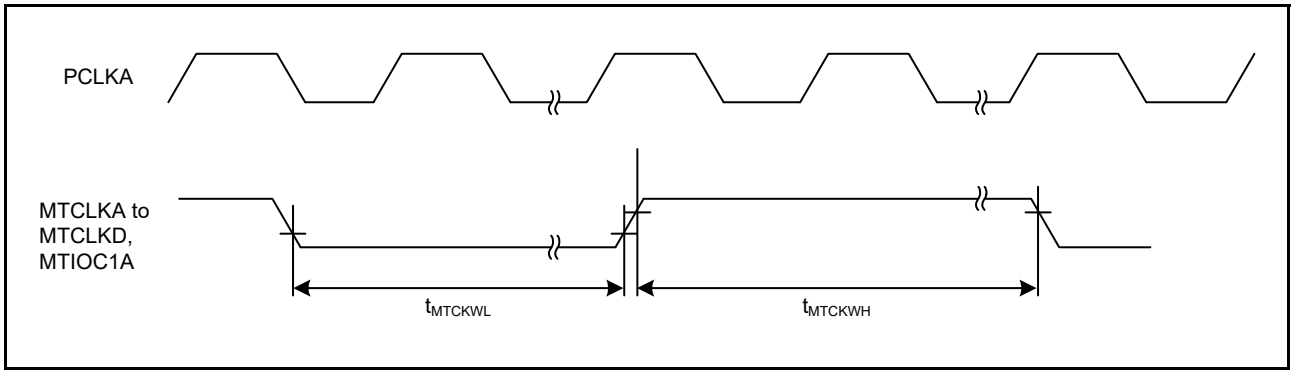



**Figure 2.41 MTU Clock Input Timing**



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### 2.4.7.6 POE

**Table 2.33 POE Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Typ. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| POE | POEn# input pulse width (n = 0, 4, 8, 10, 11) | | $t_{POEW}$ | 1.5 | — | — | $t_{PBcyc}$ | Figure 2.42 |
| | Output disable time | Transition of the POEn# signal level | $t_{POEDI}$ | — | — | 5 PCLKB + 0.24 | µs | Figure 2.43<br>When detecting falling edges (ICSRm.POEnM[3:0] = 0000 (m = 1 to 5; n = 0, 4, 8, 10, 11)) |
| | | Simultaneous conduction of output pins | $t_{POEDO}$ | — | — | 3 PCLKB + 0.2 | µs | Figure 2.44 |
| | | Register setting | $t_{POEDS}$ | — | — | 1 PCLKB + 0.2 | µs | Figure 2.45<br>Time for access to the register is not included. |
| | | Oscillation stop detection | $t_{POEDOS}$ | — | — | 21 | µs | Figure 2.46 |

Note 1. $t_{PBcyc}$: PCLKB cycle

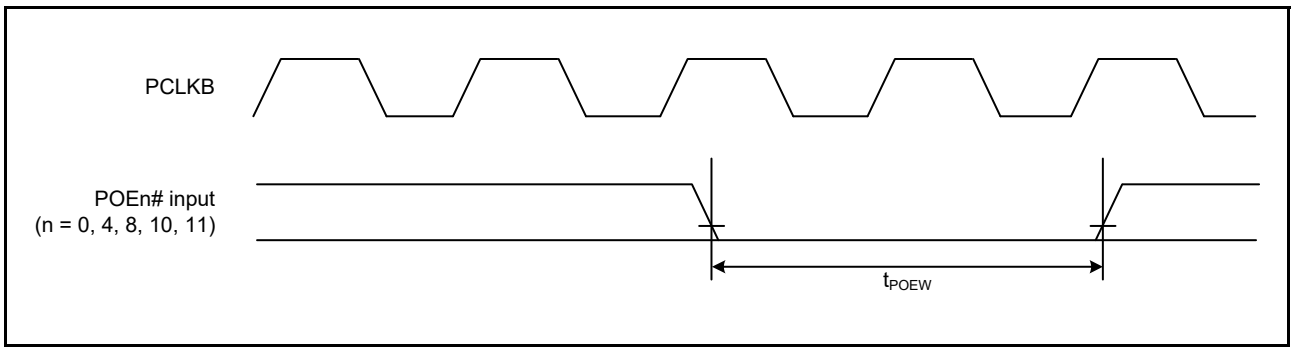



**Figure 2.42 POE# Input Timing**

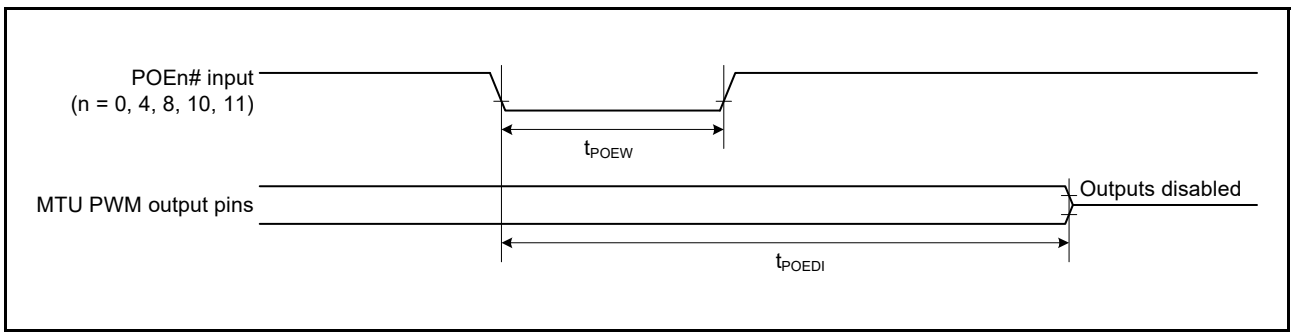
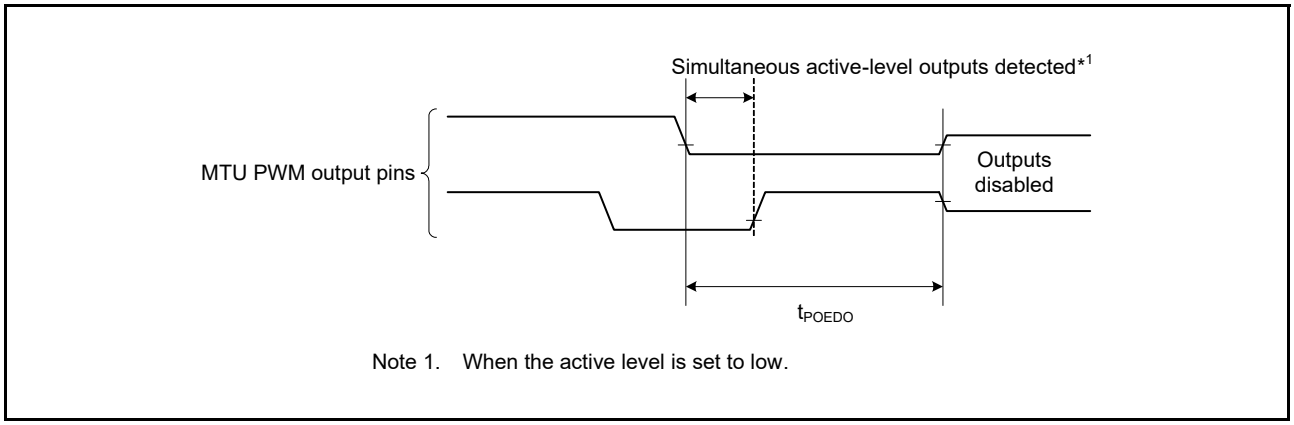



**Figure 2.43 Output Disable Time for POE in Response to Transition of the POEn# Signal Level**



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Note 1. When the active level is set to low.

**Figure 2.44 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins**

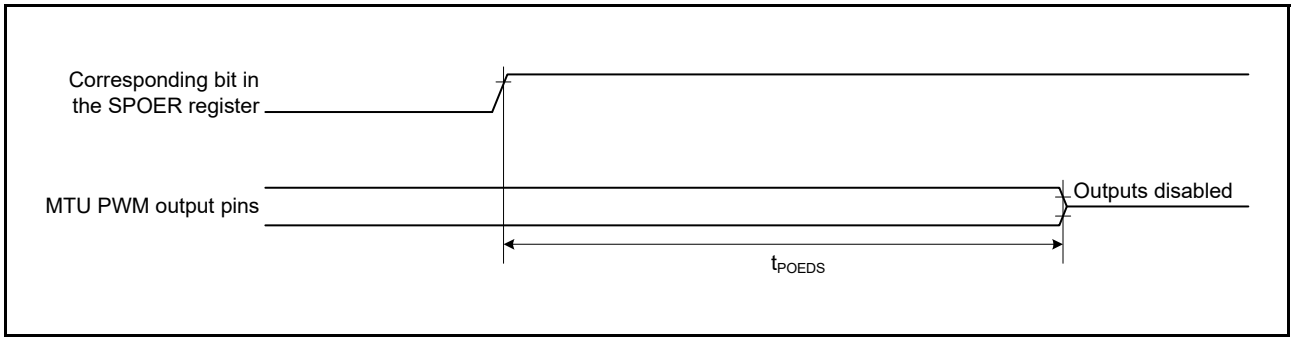



**Figure 2.45 Output Disable Time for POE in Response to the Register Setting**

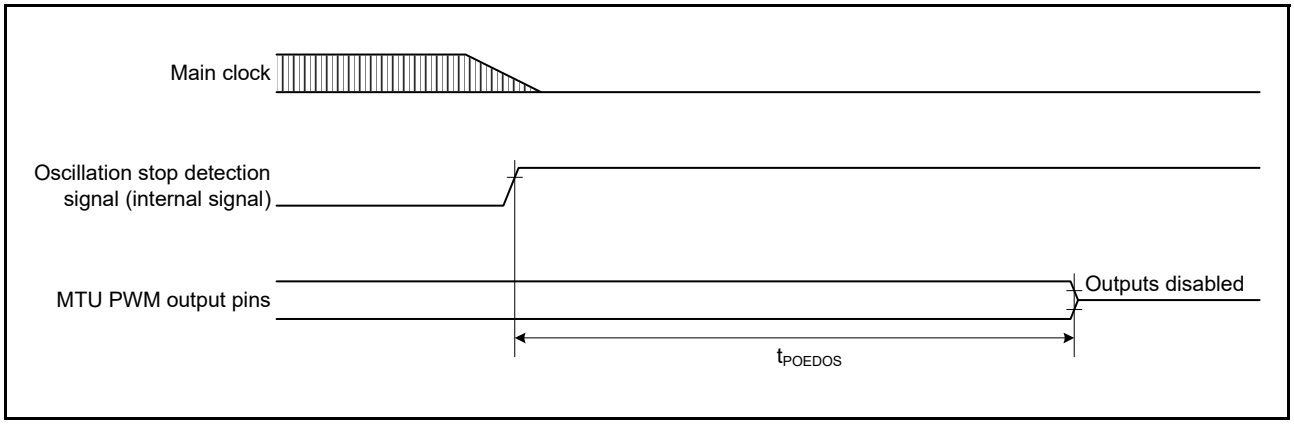



**Figure 2.46 Output Disable Time for POE in Response to the Oscillation Stop Detection**



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### 2.4.7.7 POEG

**Table 2.34 POEG Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Typ. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| POEG | GTETRGn input pulse width (n = A to D) | | $t_{POEGW}$ | 1.5 | — | — | $t_{PBcyc}$ | Figure 2.47 |
| | Output disable time | Input level detection of the GTETRGn pin (via flag) | $t_{POEGDI}$ | — | — | 3 PCLKB + 0.34 | µs | Figure 2.48<br>When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D)) |
| | | Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output) | $t_{POEGDE}$ | — | — | 0.5 | µs | Figure 2.49 |
| | | Register setting | $t_{POEGDS}$ | — | — | 1 PCLKB + 0.3 | µs | Figure 2.50<br>Time for access to the register is not included. |
| | | Oscillation stop detection | $t_{POEGDOS}$ | — | — | 21 | µs | Figure 2.51 |

Note 1. $t_{PBcyc}$: PCLKB cycle

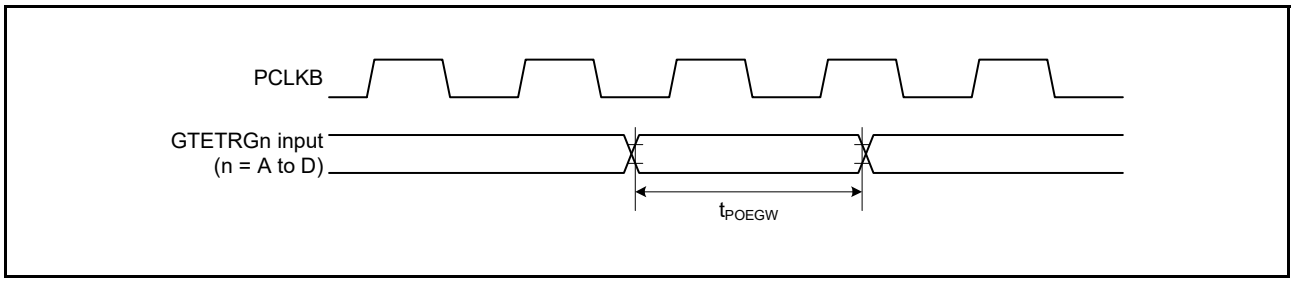



**Figure 2.47 POEG Input Timing**

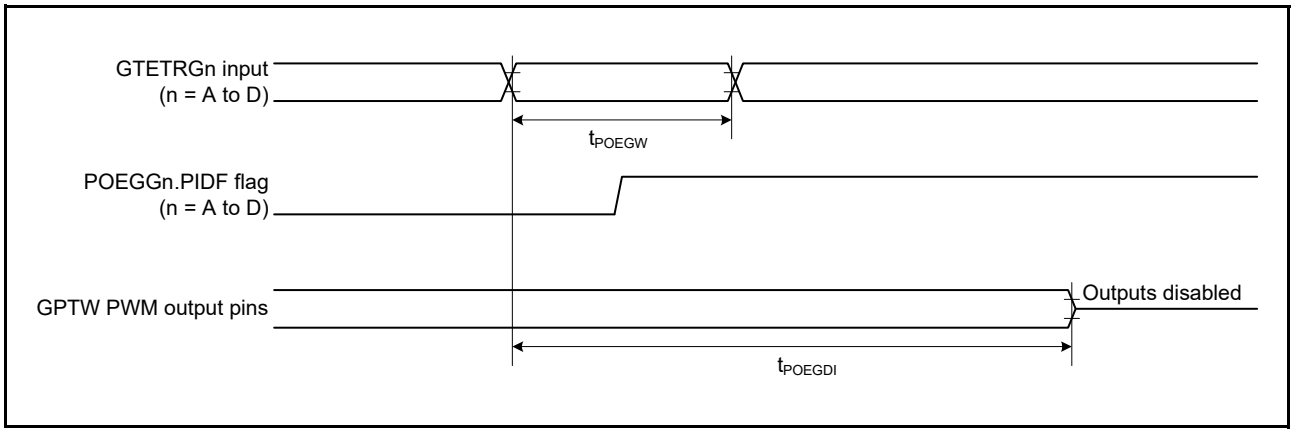
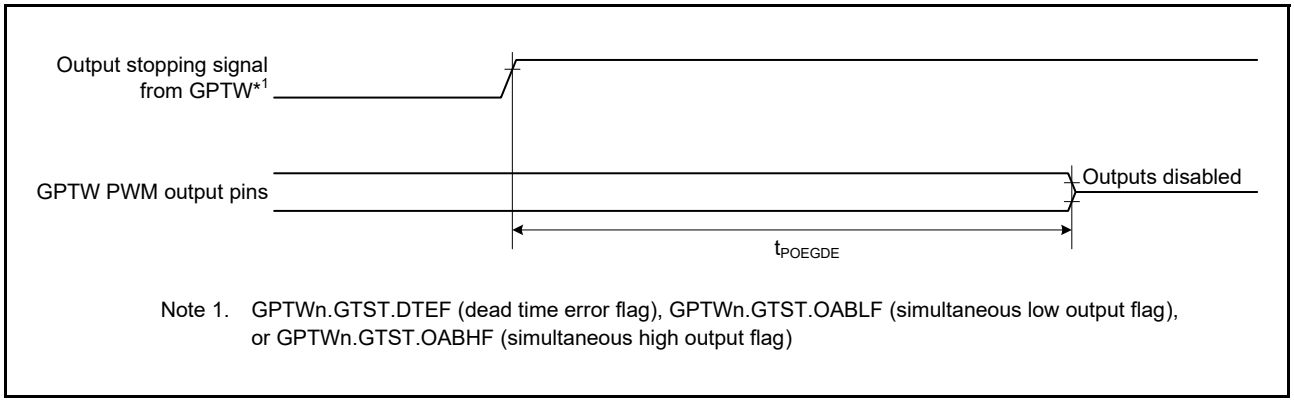



**Figure 2.48 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin**



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Note 1. GPTWn.GTST.DTEF (dead time error flag), GPTWn.GTST.OABLF (simultaneous low output flag), or GPTWn.GTST.OABHF (simultaneous high output flag)

**Figure 2.49 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW**

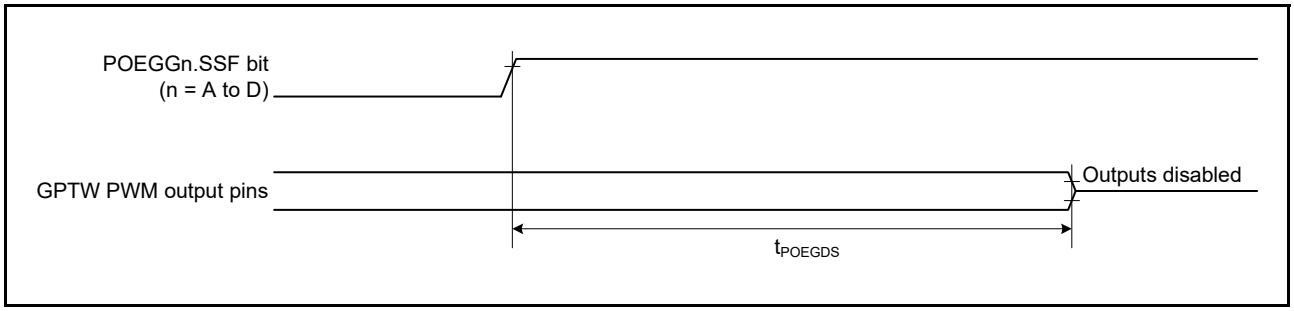



**Figure 2.50 Output Disable Time for POEG in Response to the Register Setting**

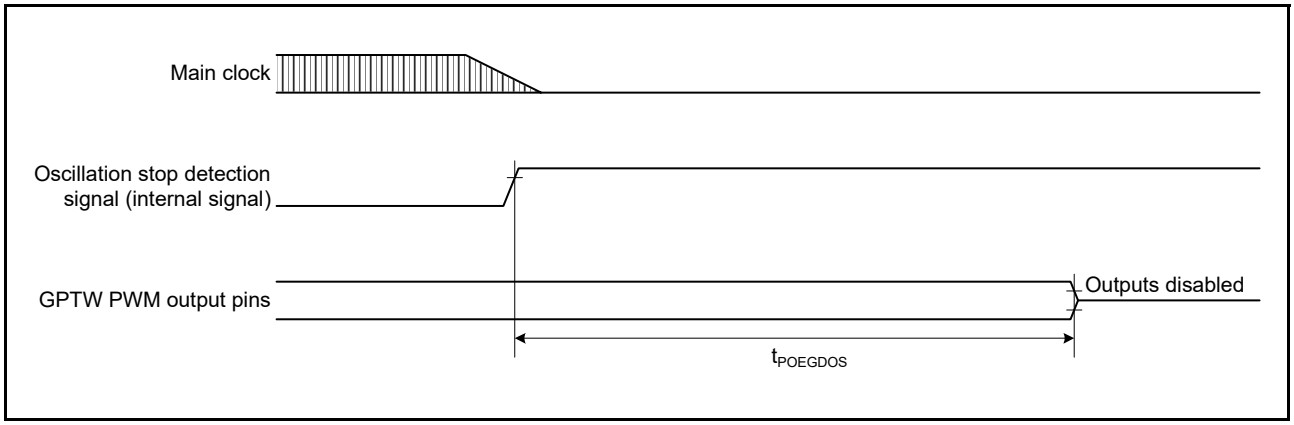



**Figure 2.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection**



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### 2.4.7.8 GPTW

**Table 2.35 GPTW Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1, *2 | Test Conditions |
|---|---|---|---|---|---|---|---|
| GPTW | Input capture input pulse width | Single-edge setting | $t_{GTICW}$ | 1.5 | — | $t_{PAcyc}$ | Figure 2.52 |
| | | Both-edge setting | | 2.5 | — | | |
| | External trigger input pulse width | Single-edge setting | $t_{GTEW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.53 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PAcyc}$: PCLKA cycle
Note 2. $t_{PBcyc}$: PCLKB cycle

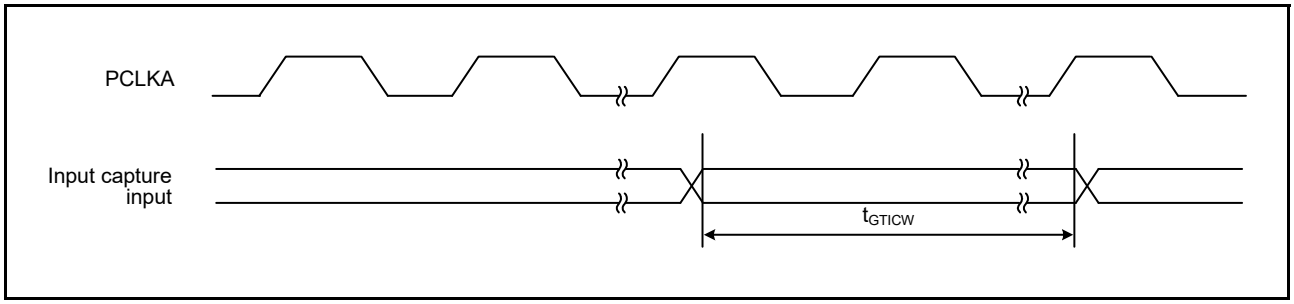



**Figure 2.52 GPTW Input Capture Input Timing**

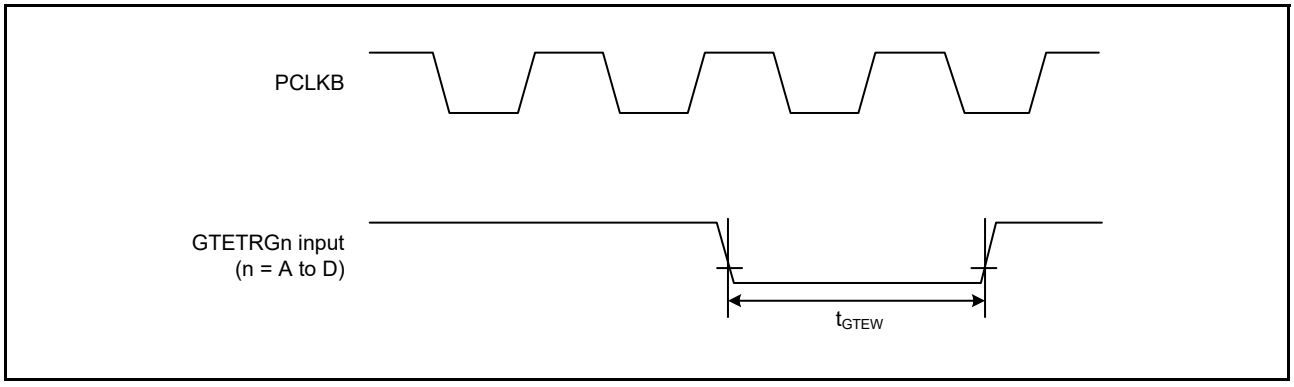



**Figure 2.53 GPTW External Trigger Input Timing**



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## 2.4.7.9 SCI

**Table 2.36 SCI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCIh, SCIj | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PBcyc}$ | Figure 2.54 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{PBcyc}$ | |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 28 | ns | Figure 2.55 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 15 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | ns | |
| SCIi | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{PAcyc}$ | Figure 2.54 |
| | | Clock synchronous | | 12 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Output clock cycle | Asynchronous*2 | $t_{Scyc}$ | 8 | — | $t_{PAcyc}$ | |
| | | Clock synchronous | | 8 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 5 | ns | |
| | Transmit data delay time | Master | $t_{TXD}$ | — | 15 | ns | Figure 2.55 |
| | | Slave | | — | 28 | | |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 20 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle; $t_{PAcyc}$: PCLKA cycle
Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1



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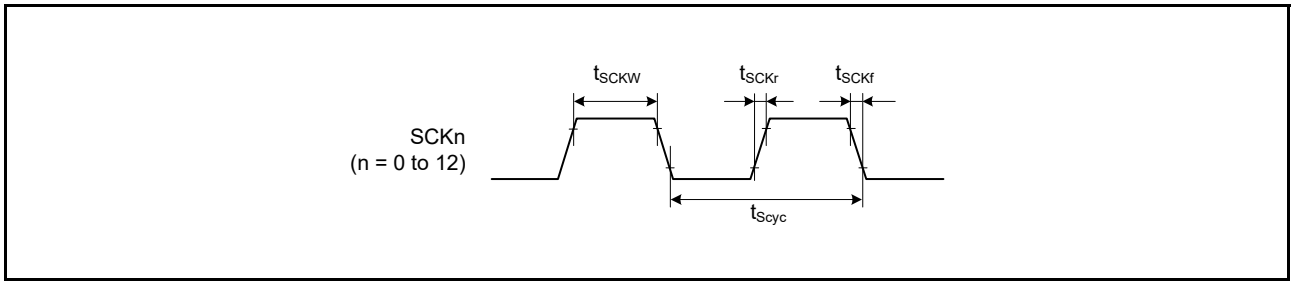



**Figure 2.54 SCK Clock Input Timing**

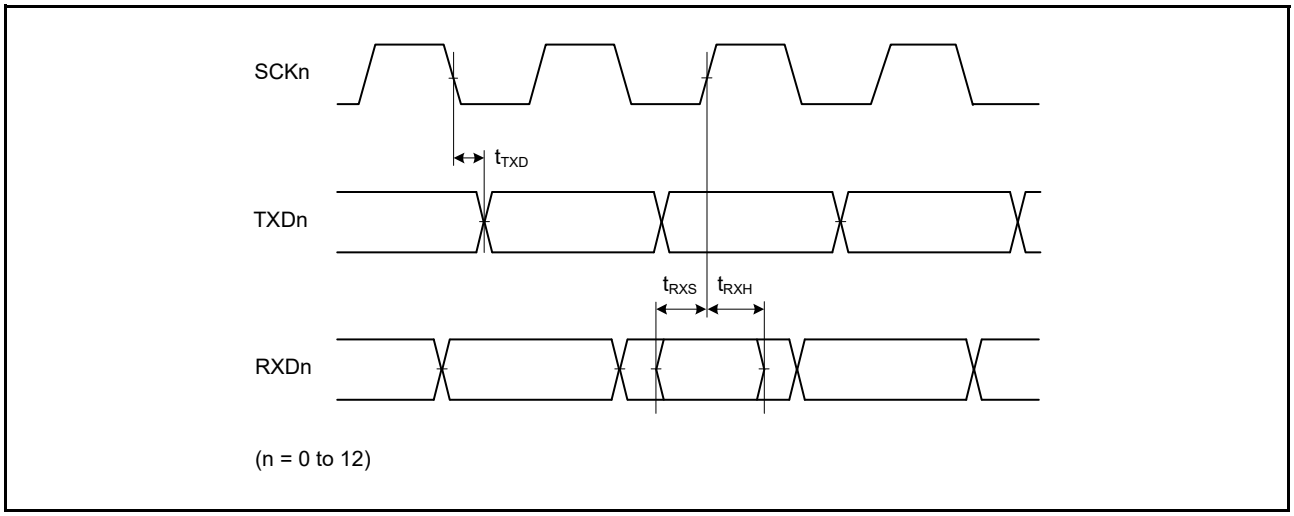



**Figure 2.55 SCI Input/Output Timing: Clock Synchronous Mode**



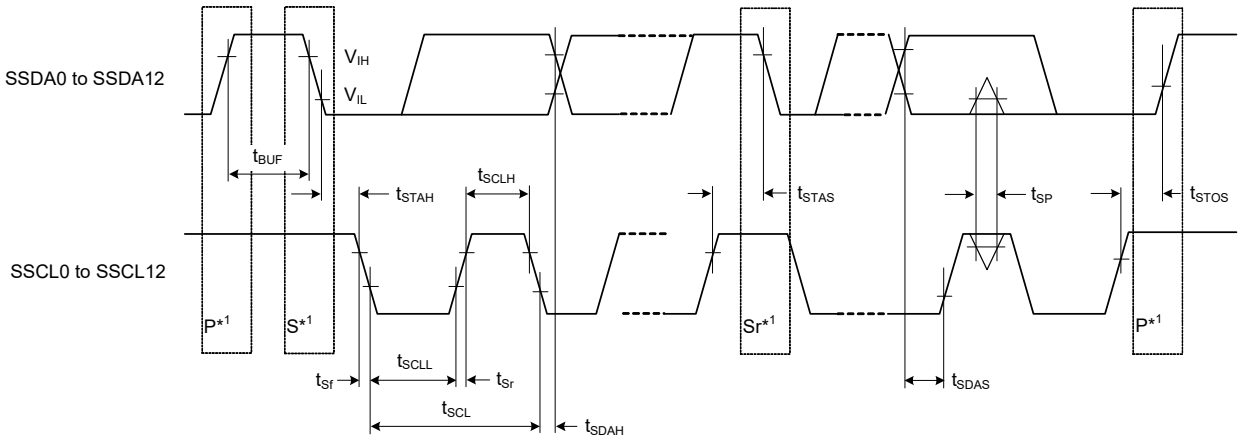
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**Table 2.37 Simple IIC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard-mode) | SSDA input rise time | $t_{Sr}$ | — | 1000 | ns | Figure 2.56 |
| | SSDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SSDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SSCL, SSDA capacitive load | $C_b$*1 | — | 400 | pF | |
| Simple IIC (Fast-mode) | SSCL, SSDA input rise time | $t_{Sr}$ | — | 300 | ns | |
| | SSCL, SSDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SSCL, SSDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SSCL, SSDA capacitive load | $C_b$*1 | — | 400 | pF | |

Note: $t_{PBcyc}$: PCLKB cycle
Note 1. Cb is the total capacitance of the bus lines.




Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH}$ = 0.7 × VCC, $V_{IL}$ = 0.3 × VCC
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA

**Figure 2.56 Simple IIC Bus Interface Input/Output Timing**



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**Table 2.38 Simple SPI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PAcyc}$ | Figure 2.57 |
| | SCK clock cycle input (slave) | | 8 | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 2.58 to Figure 2.61 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 5 | $t_{PBcyc}$ | Figure 2.60, Figure 2.61 |
| | Slave output release time | $t_{REL}$ | — | 5 | $t_{PBcyc}$ | |

Note 1. $t_{PAcyc}$: PCLKA cycle, $t_{PBcyc}$: PCLKB cycle

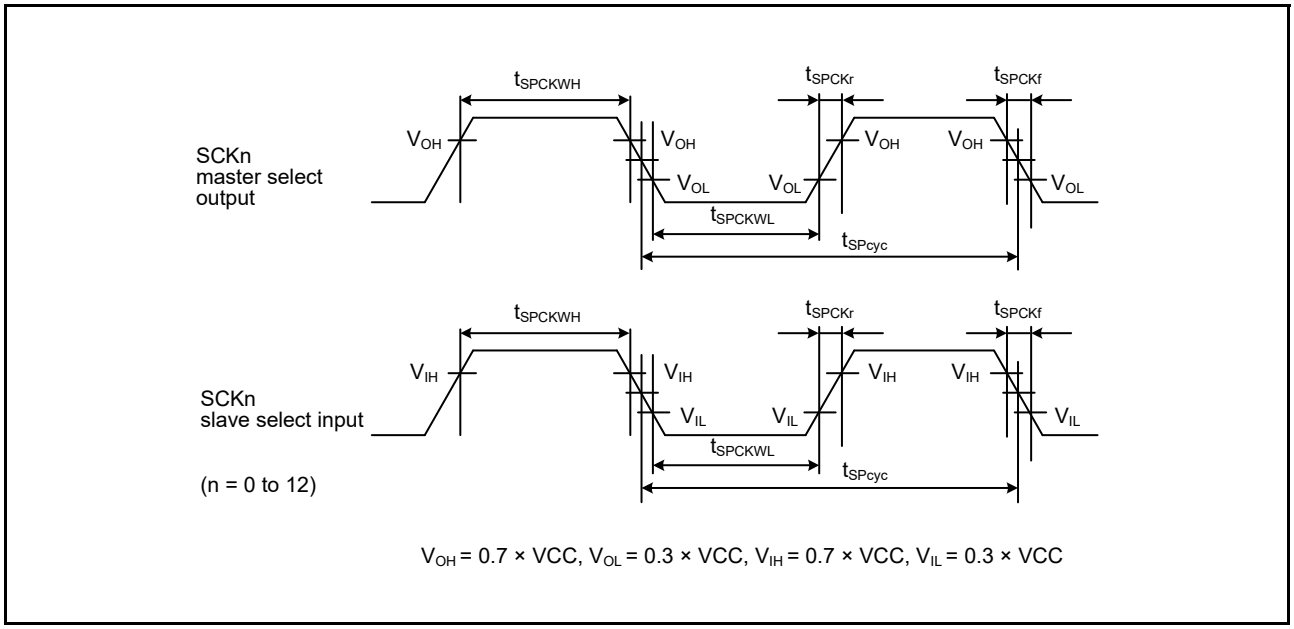



**Figure 2.57 Simple SPI Clock Timing**



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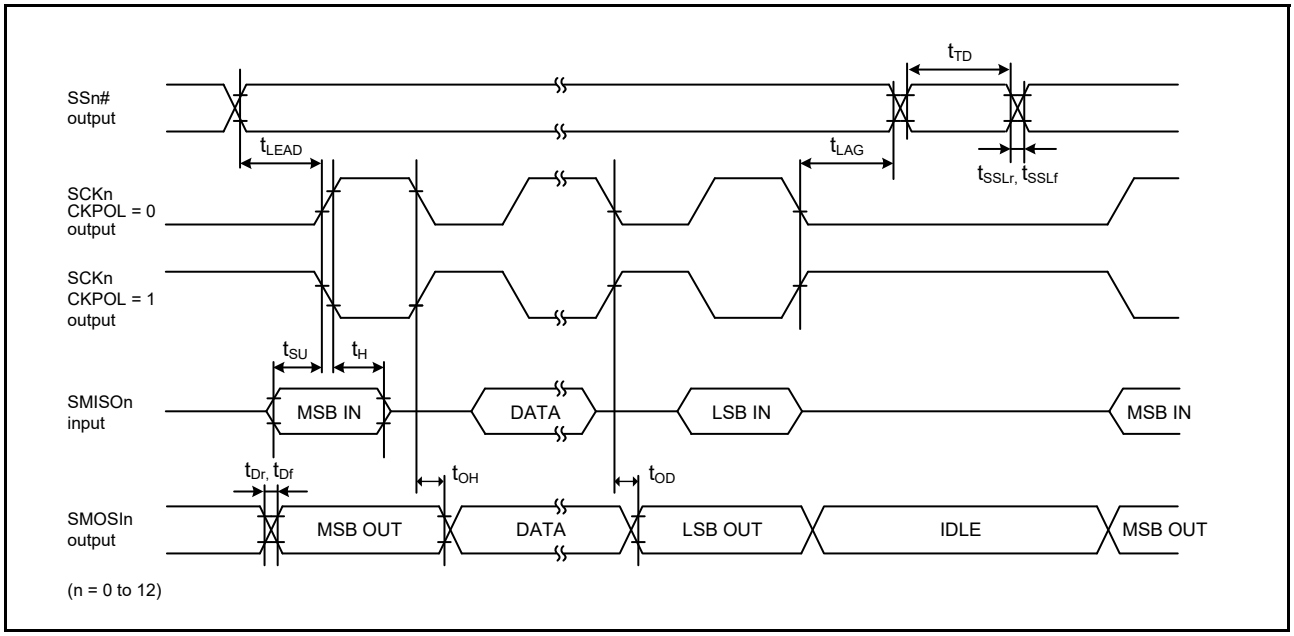



**Figure 2.58 Simple SPI Timing (Master, CKPH = 1)**

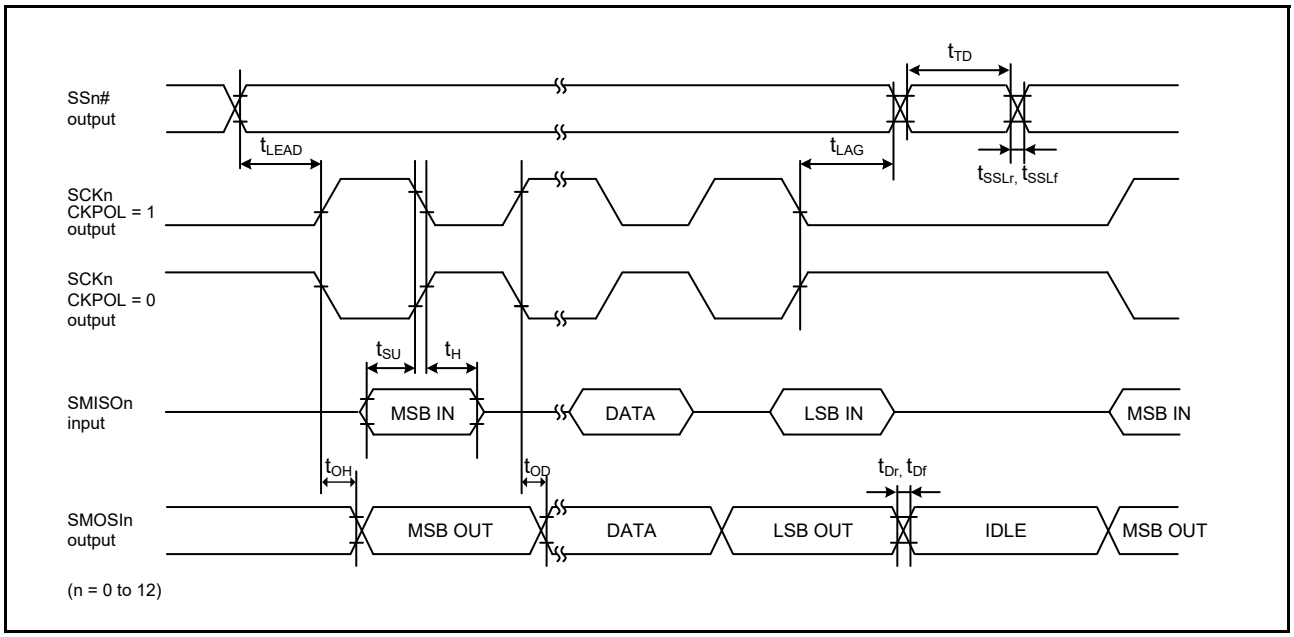



**Figure 2.59 Simple SPI Timing (Master, CKPH = 0)**



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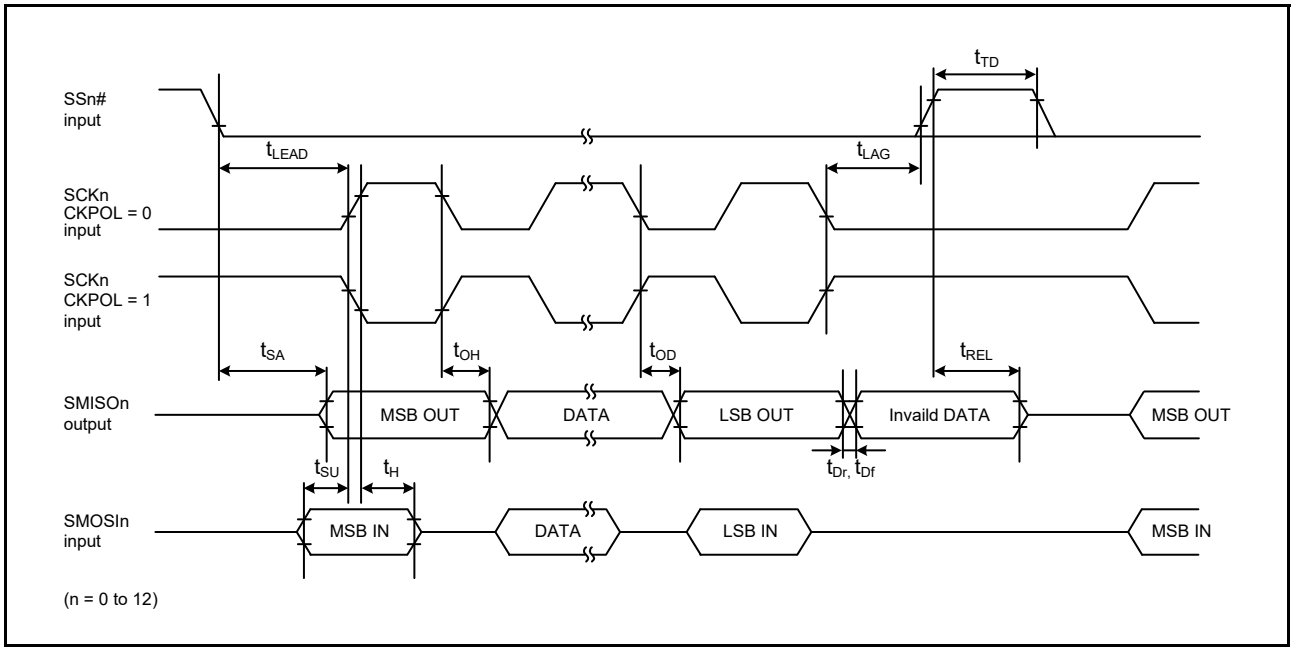



**Figure 2.60 Simple SPI Timing (Slave, CKPH = 1)**

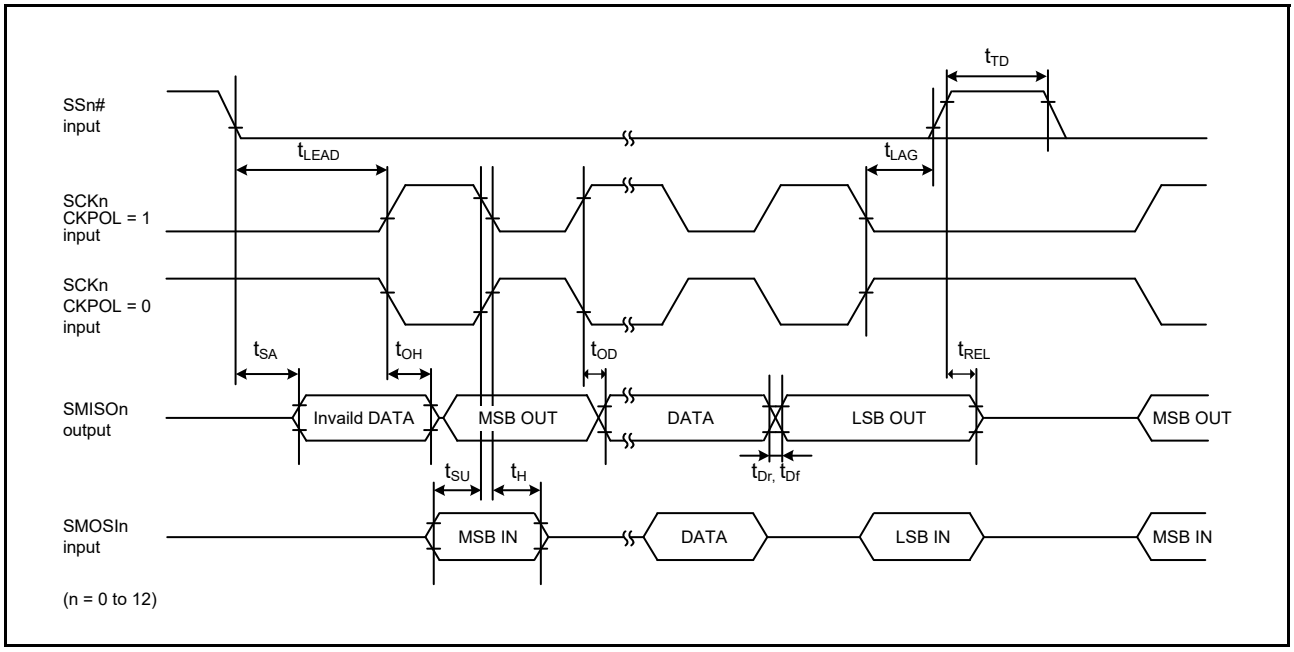



**Figure 2.61 Simple SPI Timing (Slave, CKPH = 0)**



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## 2.4.7.10 RIIC

**Table 2.39 RIIC Timing**

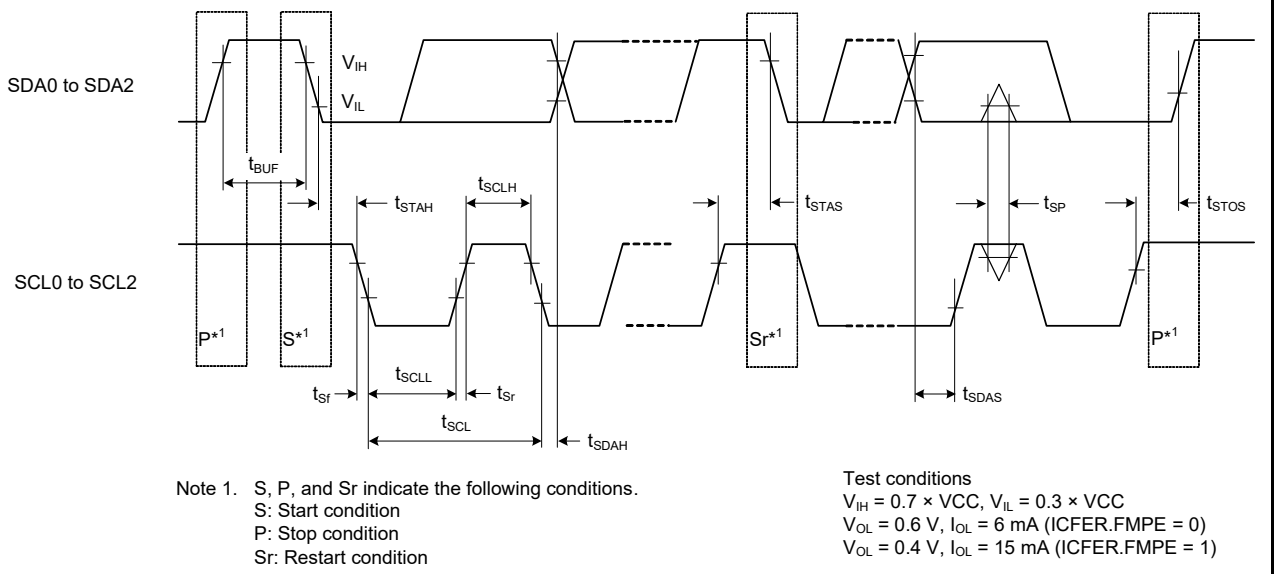
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 2.62 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$*2 | — | 400 | pF | |
| RIIC (Fast-mode) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 × (External pull-up voltage/5.5V) | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 × (External pull-up voltage/5.5V) | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$*2 | — | 400 | pF | |
| RIIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 240 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 120 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 120 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 20 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$*2 | — | 550 | pF | |



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Note: $t_{IICcyc}$: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.




Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH}$ = 0.7 × VCC, $V_{IL}$ = 0.3 × VCC
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA (ICFER.FMPE = 0)
$V_{OL}$ = 0.4 V, $I_{OL}$ = 15 mA (ICFER.FMPE = 1)

**Figure 2.62 RIIC Bus Interface Input/Output Timing**



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## 2.4.7.11 RSPI

**Table 2.40 RSPI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | | Symbol | Min.*1 | Max.*1 | Unit*1 | Test Conditions*2 |
|---|---|---|---|---|---|---|---|---|
| RSPI | RSPCK clock cycle | Master | | $t_{SPcyc}$ | 2 | — | $t_{PAcyc}$ | Figure 2.63 |
| | | Slave | | | 4 | — | | |
| | RSPCK clock high pulse width | Master | | $t_{SPCKWH}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | | |
| | RSPCK clock low pulse width | Master | | $t_{SPCKWL}$ | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | |
| | | Slave | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | | |
| | RSPCK clock rise/fall time | Output | | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | Data input setup time | Master | | $t_{SU}$ | 6 | — | ns | Figure 2.64 to Figure 2.69 |
| | | Slave | | | 8.3 | — | | |
| | Data input hold time | Master | PCLKA division ratio set to 1/2 | $t_{HF}$ | 0 | — | ns | |
| | | | PCLKA division ratio set to a value other than 1/2 | $t_H$ | $t_{PAcyc}$ | — | | |
| | | Slave | | | 8.3 | — | | |
| | SSL setup time | Master | | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 6 | — | $t_{PAcyc}$ | |
| | SSL hold time | Master | | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | | 6 | — | $t_{PAcyc}$ | |
| | Data output delay time | Master | | $t_{OD}$ | — | 6.3 | ns | |
| | | Slave | | | — | 28 | | |
| | Data output hold time | Master | | $t_{OH}$ | 0 | — | ns | |
| | | Slave | | | 0 | — | | |
| | Successive transmission delay time | Master | | $t_{TD}$ | $t_{SPcyc} + 2 \times t_{PAcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{PAcyc}$ | ns | |
| | | Slave | | | $6 \times t_{PAcyc}$ | — | | |
| | MOSI and MISO rise/fall time | Output | | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | SSL rise/fall time | Output | | $t_{SSLr}$, tSSLf | — | 5 | ns | |
| | | Input | | | — | 1 | µs | |
| | Slave access time | | | $t_{SA}$ | — | $2 \times t_{PAcyc} + 28$ | ns | Figure 2.68, Figure 2.69 |
| | Slave output release time | | | $t_{REL}$ | — | $2 \times t_{PAcyc} + 28$ | ns | |

Note 1. $t_{PAcyc}$: PCLKA cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.



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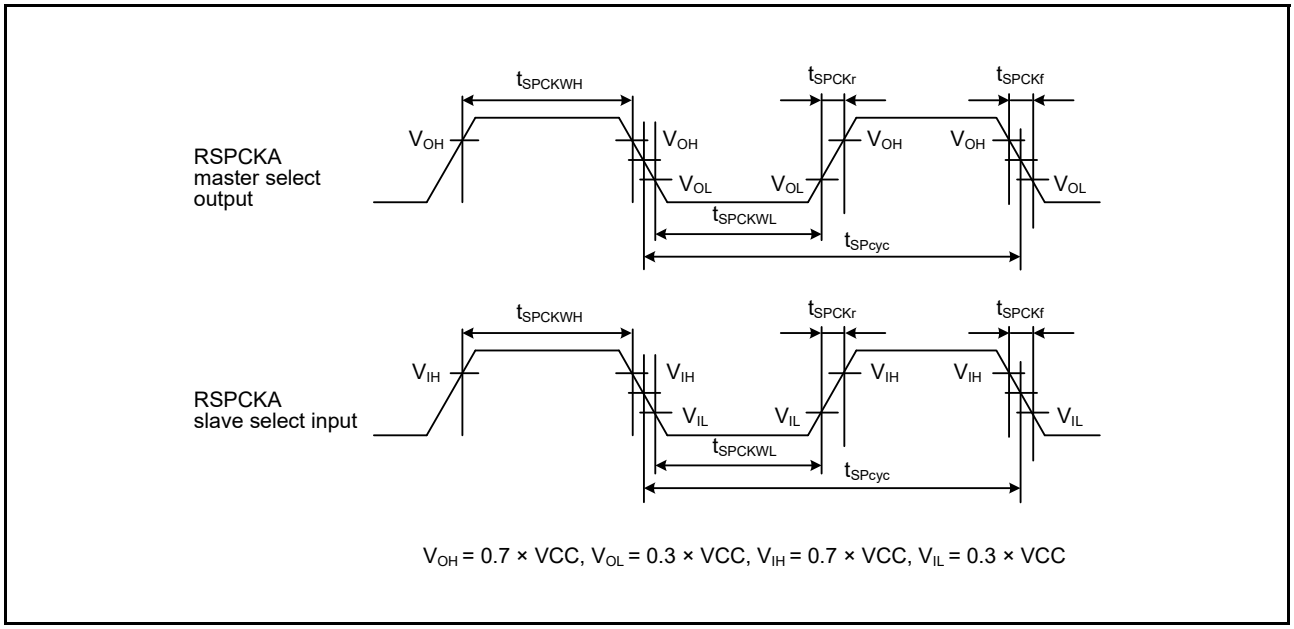



**Figure 2.63 RSPI Clock Timing**

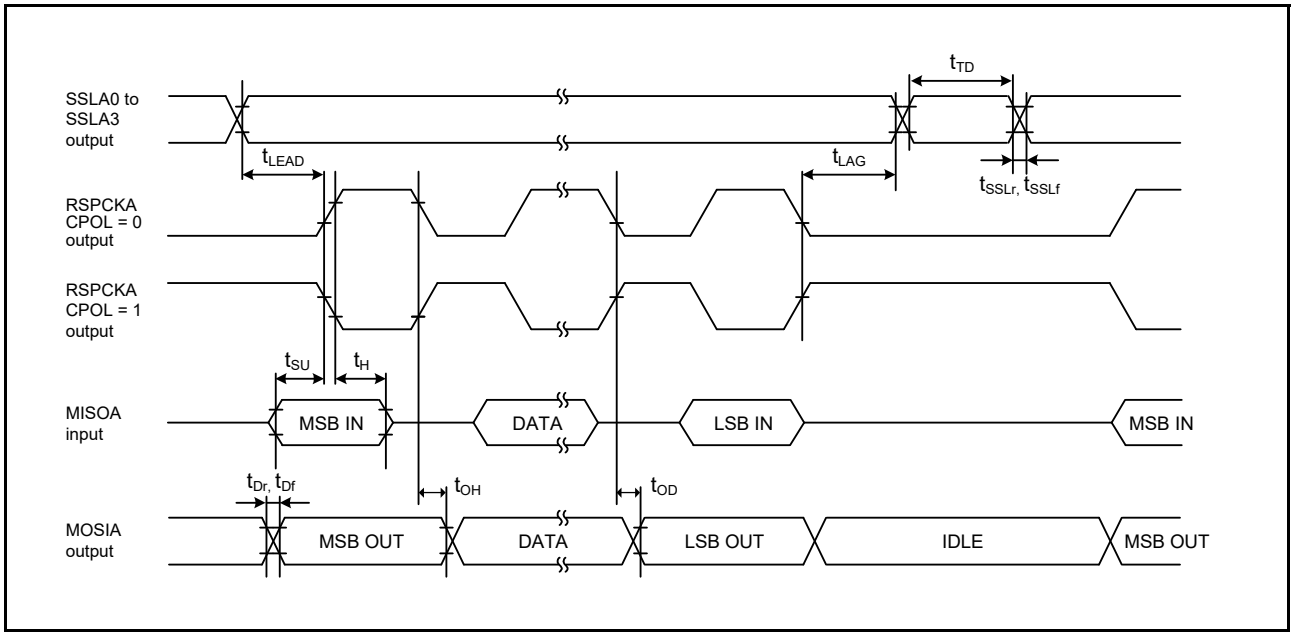



**Figure 2.64 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)**



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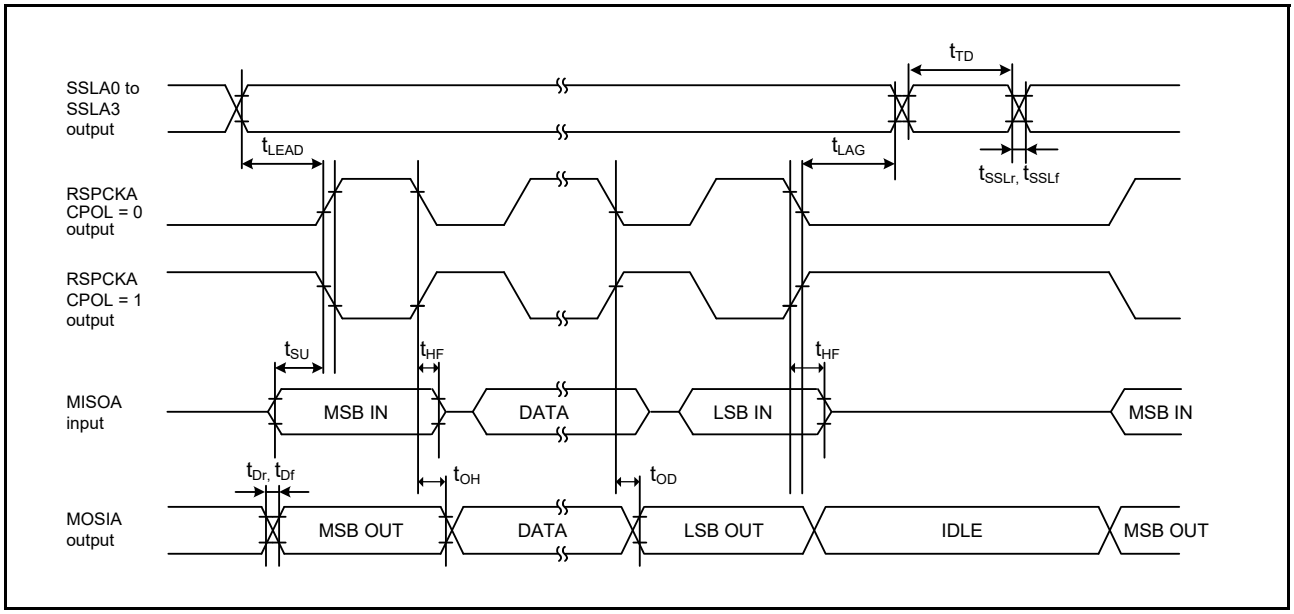



**Figure 2.65 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)**

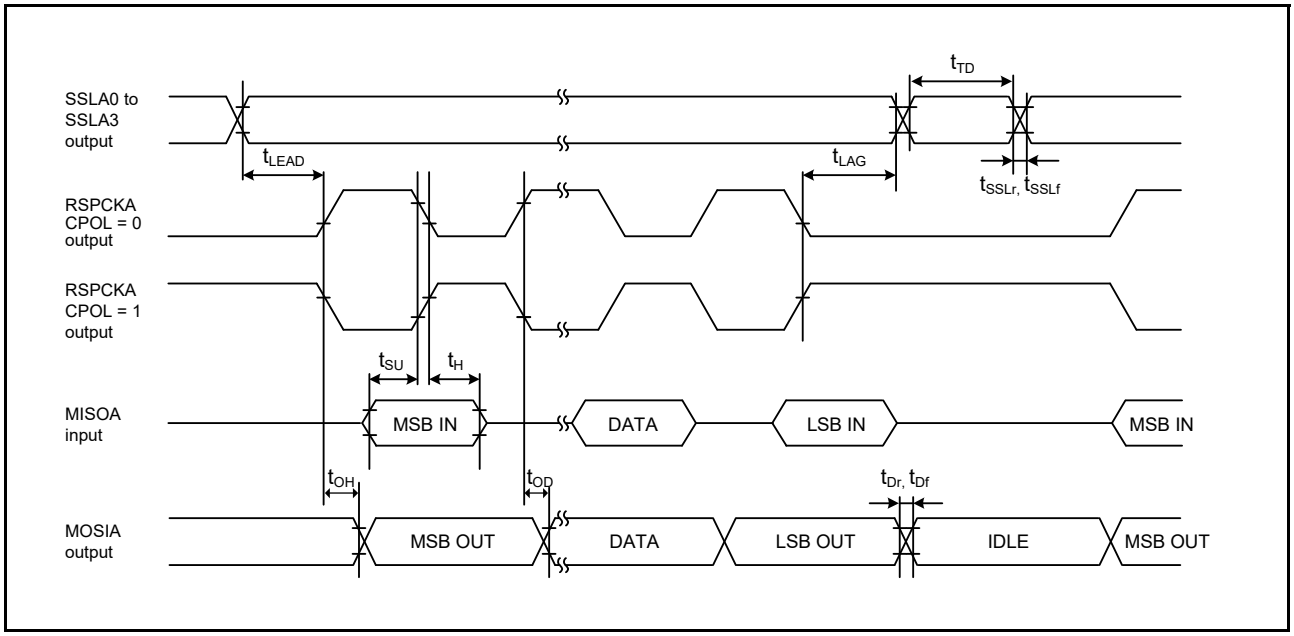



**Figure 2.66 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)**



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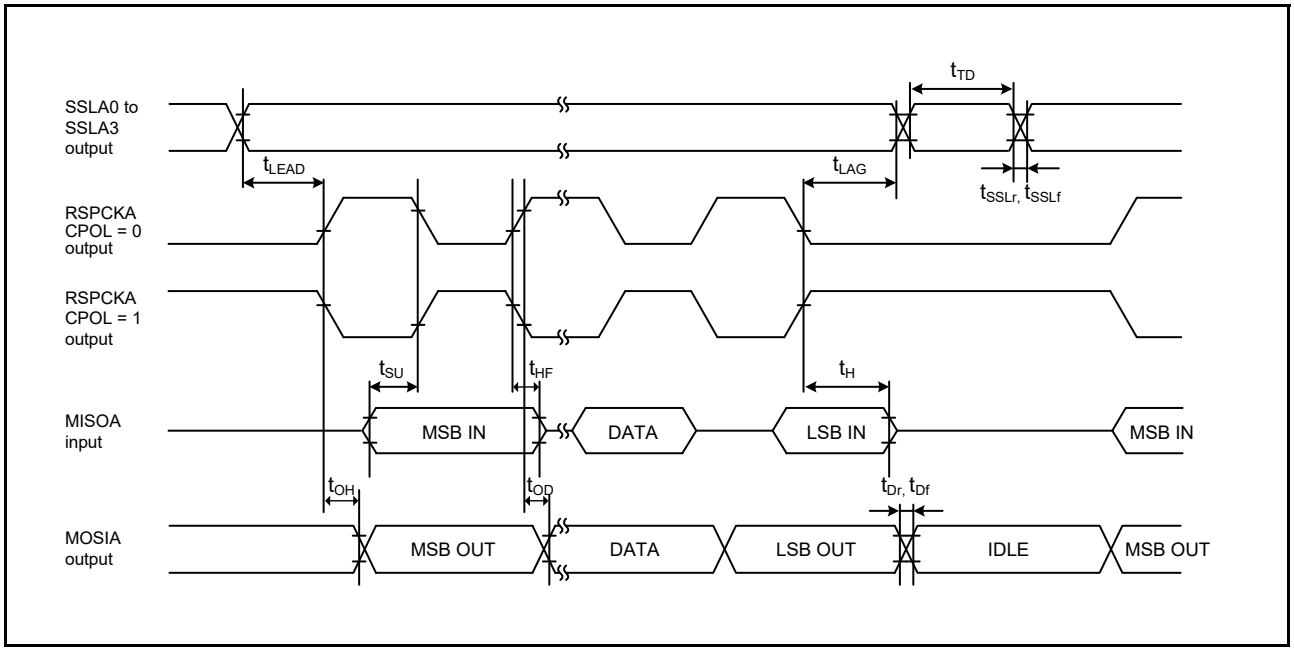



**Figure 2.67 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)**

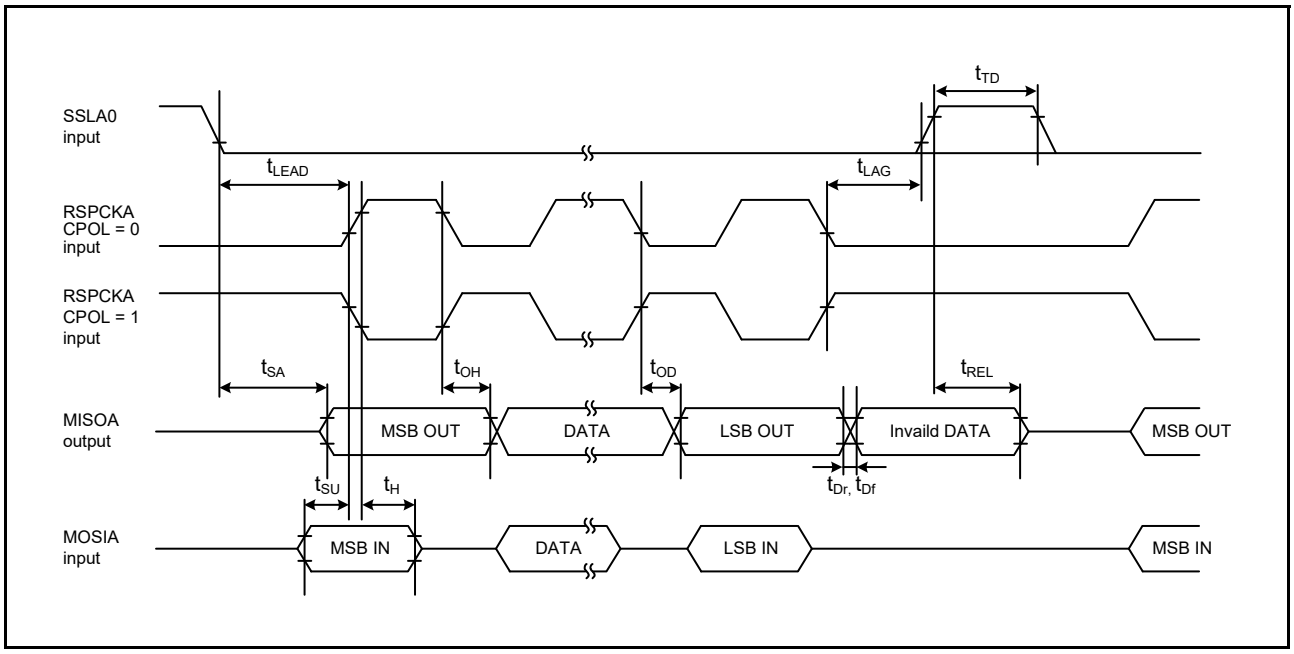



**Figure 2.68 RSPI Timing (Slave, CPHA = 0)**



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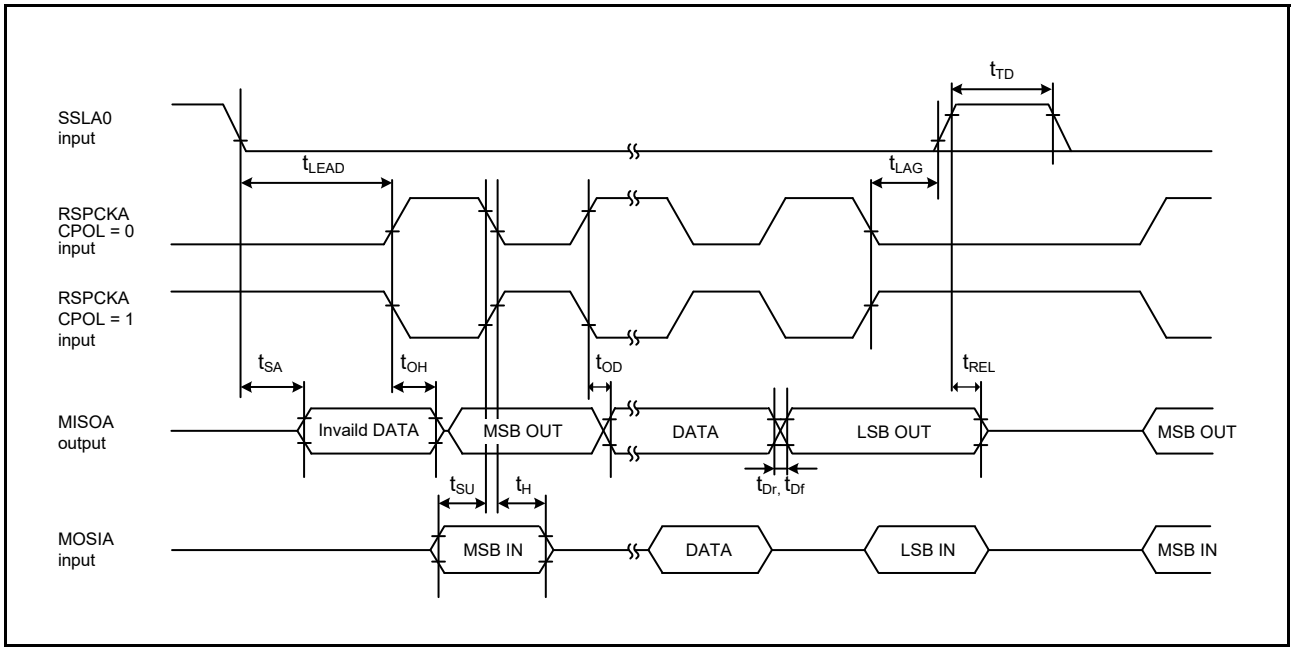



**Figure 2.69 RSPI Timing (Slave, CPHA = 1)**



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## 2.4.7.12 QSPI

**Table 2.41 QSPI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions*2 |
|---|---|---|---|---|---|---|
| QSPI | QSPCLK clock cycle | $t_{QScyc}$ | 2 | 4080 | $t_{PBcyc}$ | Figure 2.70 |
| | Data input setup time | $t_{Su}$ | 6.5 | — | ns | Figure 2.71, Figure 2.72 |
| | Data input hold time | $t_{IH}$ | 5 | — | ns | |
| | SS setup time | $t_{LEAD}$ | 1.5 | 8.5 | $t_{QScyc}$ | |
| | SS hold time | $t_{LAG}$ | 1 | 8 | $t_{QScyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 10.0 | ns | |
| | Data output hold time | $t_{OH}$ | –5 | — | ns | |
| | Successive transmission delay time | $t_{TD}$ | 1 | 8 | $t_{QScyc}$ | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.

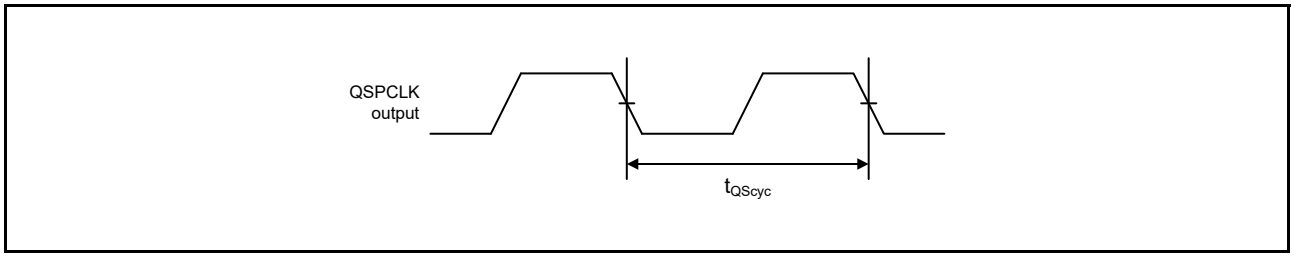



**Figure 2.70 QSPI Clock Timing**

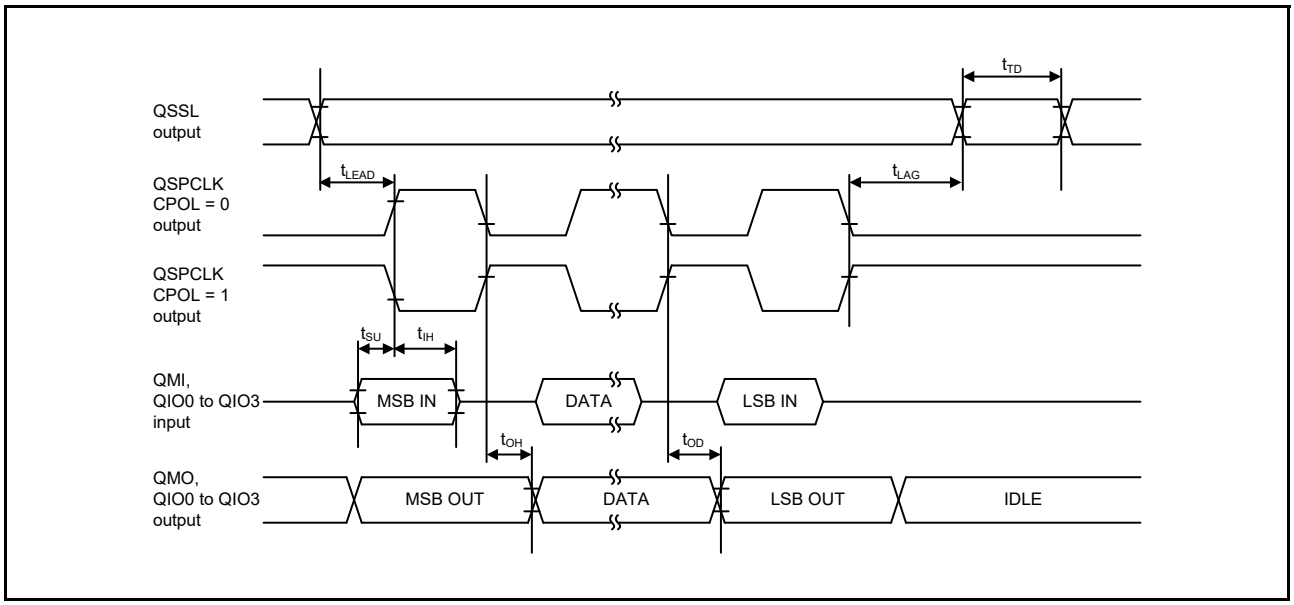



**Figure 2.71 Transmit/Receive Timing (CPHA = 0)**



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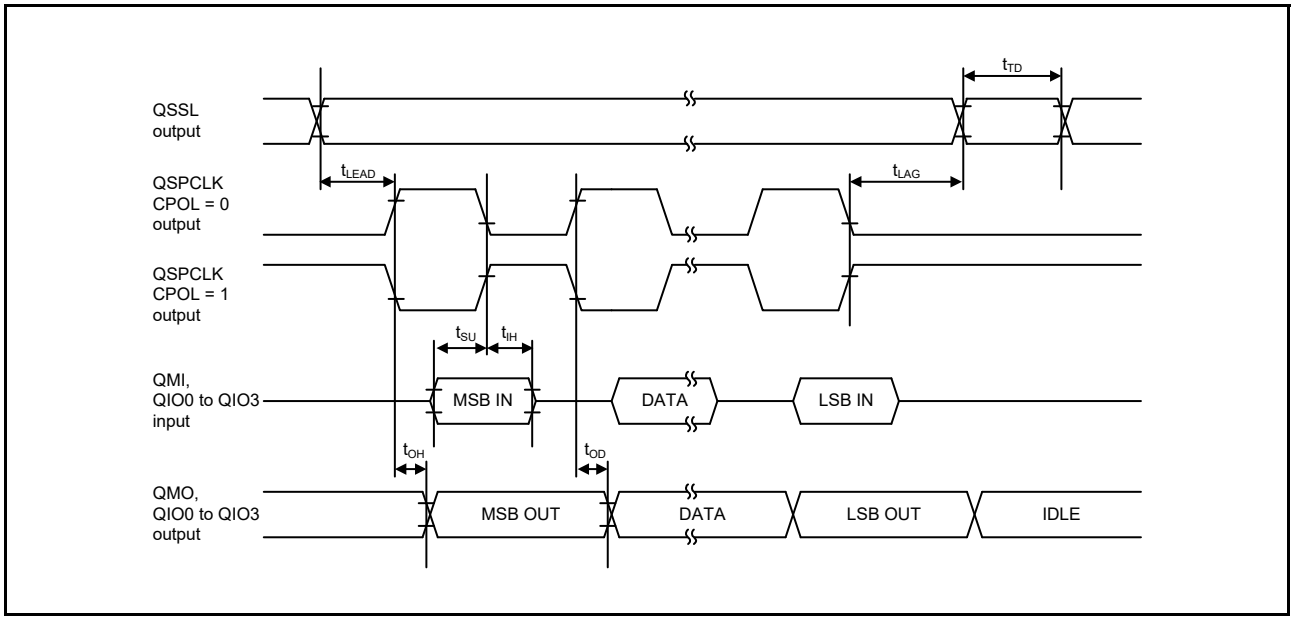



**Figure 2.72 Transmit/Receive Timing (CPHA = 1)**



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## 2.4.7.13 SSIE

**Table 2.42 Expansion Serial Sound Interface Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| AUDIO_CLK | Cycle | | $t_{EXcyc}$ | 20 | — | ns | Figure 2.73 |
| | High/low level | | $t_{EXL}/t_{EXH}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |
| SSIBCKn | Cycle | Master | $t_O$ | 80 | — | ns | Figure 2.74 |
| | | Slave | $t_I$ | 80 | — | ns | |
| | Output clock high level | Master | $t_{HC}$ | 0.35 | — | $t_O$ | |
| | Output clock low level | | $t_{LC}$ | 0.35 | — | $t_O$ | |
| | Input clock high level | Slave | $t_{HC}$ | 0.35 | — | $t_I$ | |
| | Input clock low level | | $t_{LC}$ | 0.35 | — | $t_I$ | |
| | Output clock rise time | Master | $t_{RC}$ | — | 0.15 | $t_O$ | |
| | Output clock fall time | | $t_{FC}$ | — | 0.15 | $t_O$ | |
| | Input clock rise time | Slave | $t_{RC}$ | — | 0.15 | $t_I$ | |
| | Input clock fall time | | $t_{FC}$ | — | 0.15 | $t_I$ | |
| SSILRCKn,SSITXD0, SSIRXD0, SSIDATA1 | Input setup time | Master | $t_{SR}$ | 12 | — | ns | Figure 2.75, Figure 2.76 |
| | | Slave | | 12 | — | ns | |
| | Input hold time | Master | $t_{HR}$ | 8 | — | ns | |
| | | Slave | | 15 | — | ns | |
| | Output delay time | Master | $t_{DTR}$ | –10 | 5 | ns | |
| | | Slave | | 0 | 20 | ns | |
| | Output delay time from when an SSILRCK0 signal is changed*1 | Slave | $t_{DTRW}$ | — | 20 | ns | Figure 2.77 |

n = 0, 1

Note 1. The SSIE has a single path for transmission in slave mode. To generate the data for transmission, the signals input through the SSILRCKn pin through the abovementioned path are used. After that, the data for transmission proceed to be used as the logical outputs to the SSITXD0 or SSIDATA1 pin.

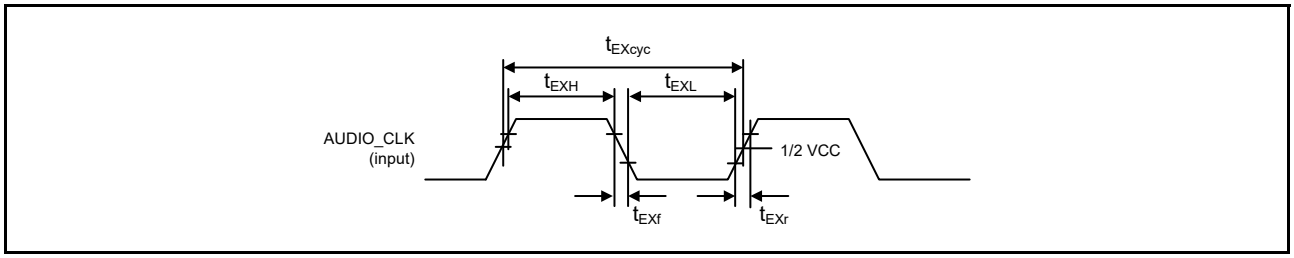



**Figure 2.73 Clock Input Timing**

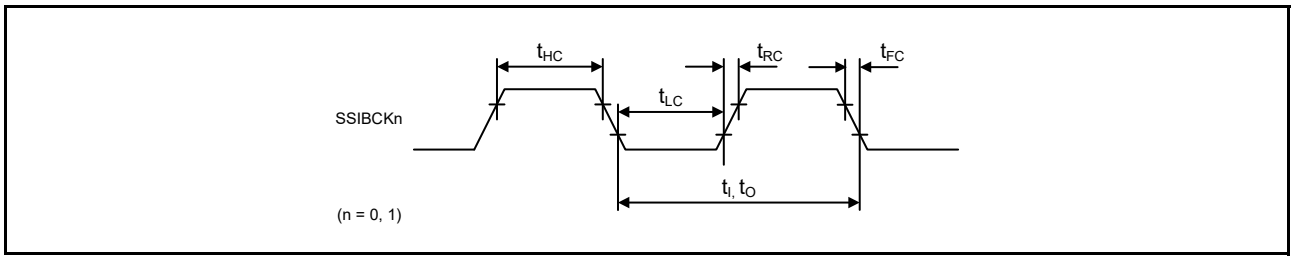



**Figure 2.74 SSIE Clock Input/Output Timing**



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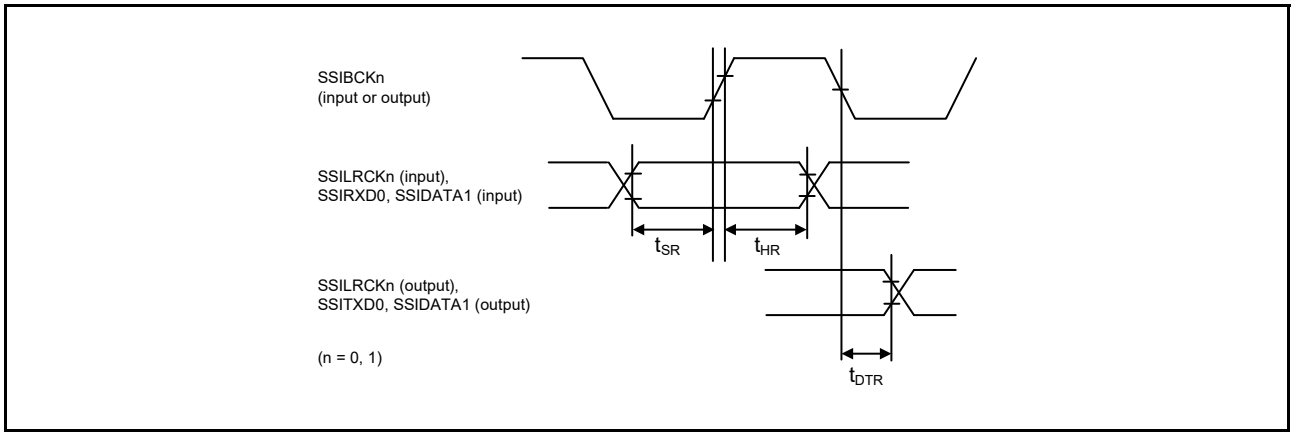



**Figure 2.75 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 0**

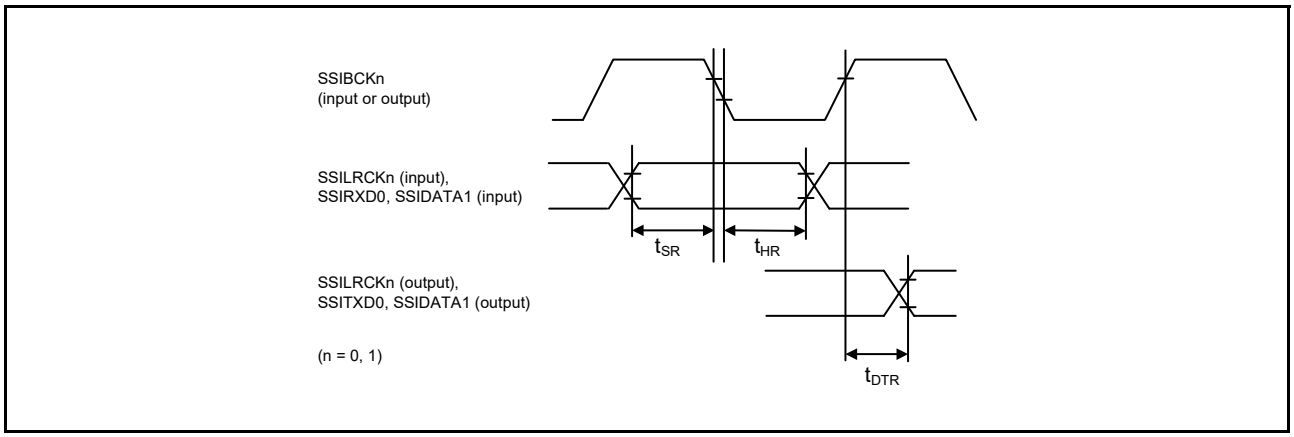



**Figure 2.76 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 1**

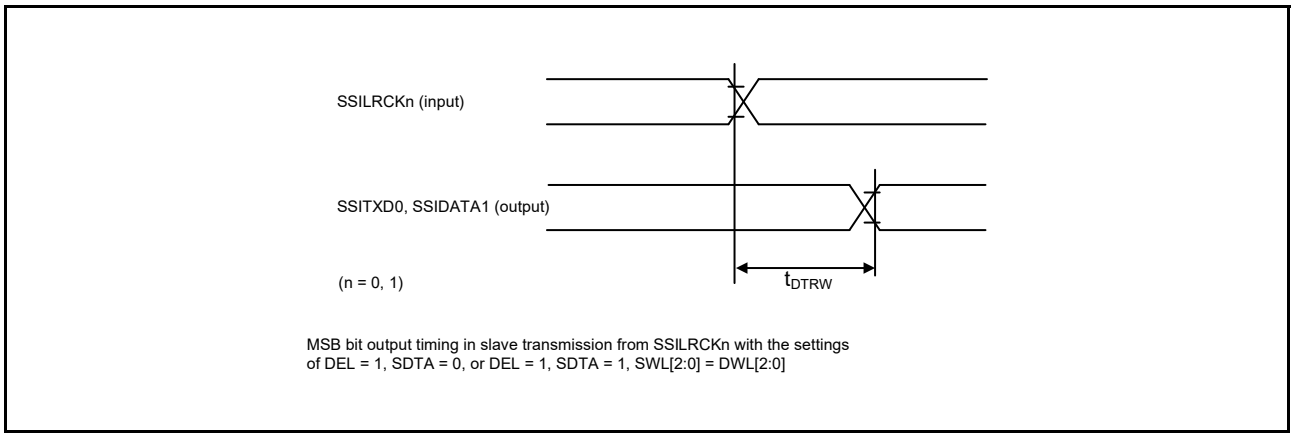



**Figure 2.77 Output Delay of the SSIE Data from When an SSILRCKn Signal is Changed**



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### 2.4.7.14 PMGI

**Table 2.43 PMGI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PMGI | PMGI0_MDC output cycle | $t_{MDC}$ | 80 | — | ns | Figure 2.78 |
| | PMGI0_MDIO setup time (relative to PMGI0_MDC↑) | $t_{SMDIO}$ | 20 | — | ns | |
| | PMGI0_MDIO hold time (relative to PMGI0_MDC↑) | $t_{HMDIO}$ | 0 | — | ns | |
| | PMGI0_MDIO output delay time (relative to PMGI0_MDC↑) | $t_{DMDIO}$ | 0 | 20 | ns | |

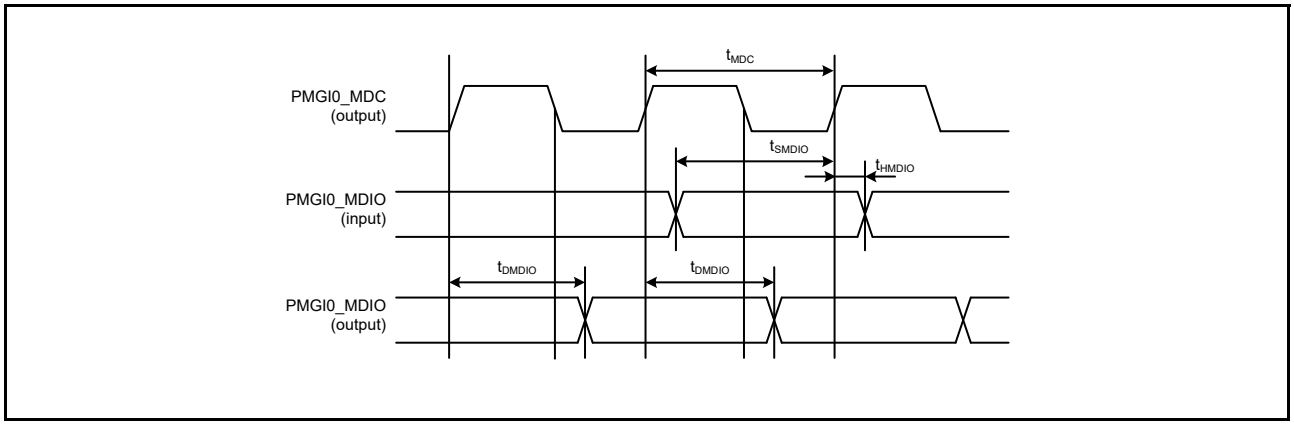



**Figure 2.78 Timing of Serial Management Access**



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## 2.4.7.15 MMC

**Table 2.44 MMC Host Interface Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions*2 |
|---|---|---|---|---|---|---|
| MMCIF | MMC_CLK clock cycle | $t_{MMCPP}$ | 2 × $t_{PBcyc}$ | — | ns | Figure 2.79 |
| | MMC_CLK clock high level width | $t_{MMCWH}$ | 6.5 | — | ns | |
| | MMC_CLK clock low level width | $t_{MMCWL}$ | 6.5 | — | ns | |
| | MMC_CLK clock rising time | $t_{MMCLH}$ | — | 3 | ns | |
| | MMC_CLK clock falling time | $t_{MMCHL}$ | — | 3 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode) | $t_{MMCODLY}$ | –6.6 | 6.6 | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data setup | $t_{MMCISU}$ | 8 | — | ns | |
| | MMC_CMD, MMC_D7 to MMC_D0 input data hold | $t_{MMCIH}$ | 2.5 | — | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc.) to indicate group membership appended to their names as groups. For the MMC interface, the AC portion of the electrical characteristics is measured for each group.

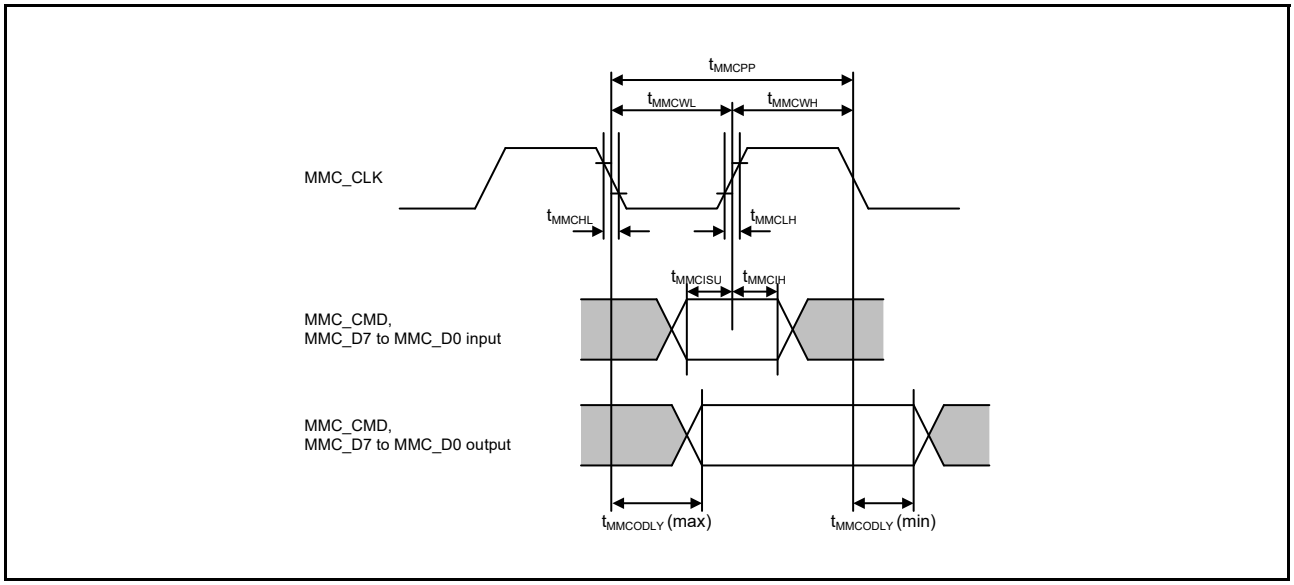



**Figure 2.79 MMC Interface**



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## 2.4.7.16 SDHI

**Table 2.45 SDHI Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6V, 2.7V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, Ta = $T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30pF
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| SDHI | SDHI_CLK output cycle time | $t_{PP(SD)}$ | 20 | — | ns | Figure 2.80 |
| | SDHI_CLK output width at high level | $t_{WH(SD)}$ | 0.4 × $t_{PP(SD)}$ | — | ns | |
| | SDHI_CLK output width at low level | $t_{WL(SD)}$ | 0.4 × $t_{PP(SD)}$ | — | ns | |
| | SDHI_CLK output rising time | $t_{TLH(SD)}$ | — | 3 | ns | |
| | SDHI_CLK output falling time | $t_{THL(SD)}$ | — | 3 | ns | |
| | SDHI_CMD, SDHI_D3 to SDHI_D0 output data delay (data transfer mode) | $t_{ODLY(SD)}$ | –6.5 | 4 | ns | |
| | SDHI_CMD, SDHI_D3 to SDHI_D0 input data setup time | $t_{ISU(SD)}$ | 6 | — | ns | |
| | SDHI_CMD, SDHI_D3 to SDHI_D0 input data hold time | $t_{IH(SD)}$ | 2 | — | ns | |

Note 1. We recommend using pin names that have a letter (“-A”, “-B”, etc.) to indicate group membership per group in the test. For the SDHI, the AC portion of the electrical characteristics is measured per group.

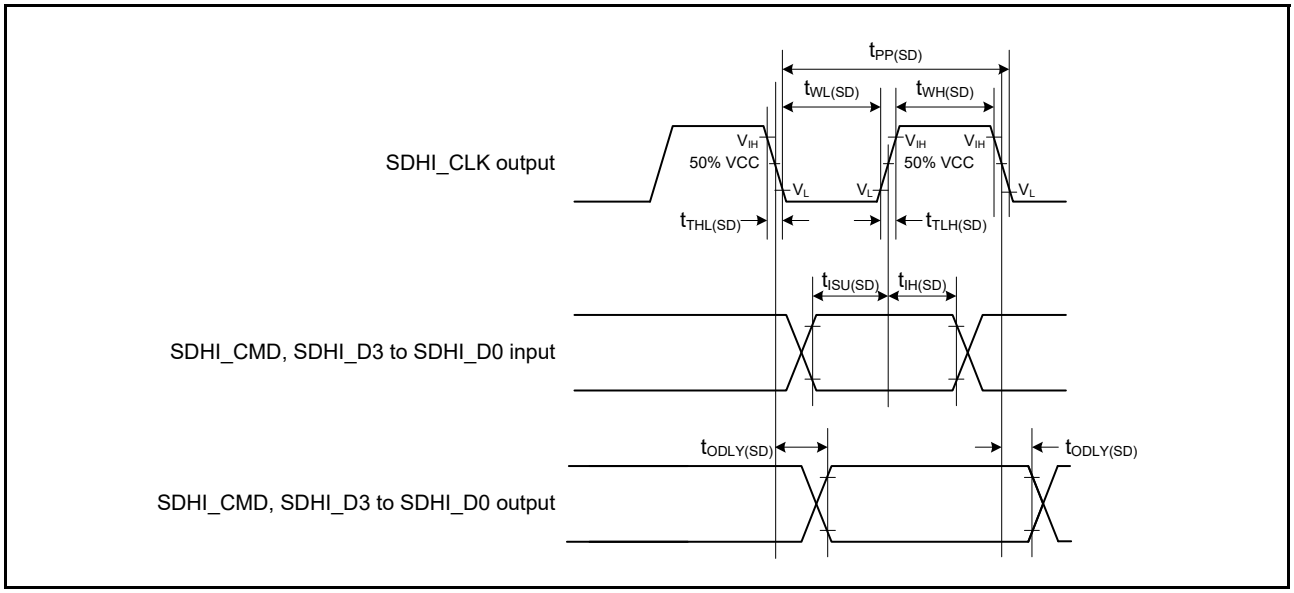



**Figure 2.80 SD Host Interface Input/Output Signal Timing**



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## 2.4.7.17 ETHERC

**Table 2.46 ETHERC Timing**

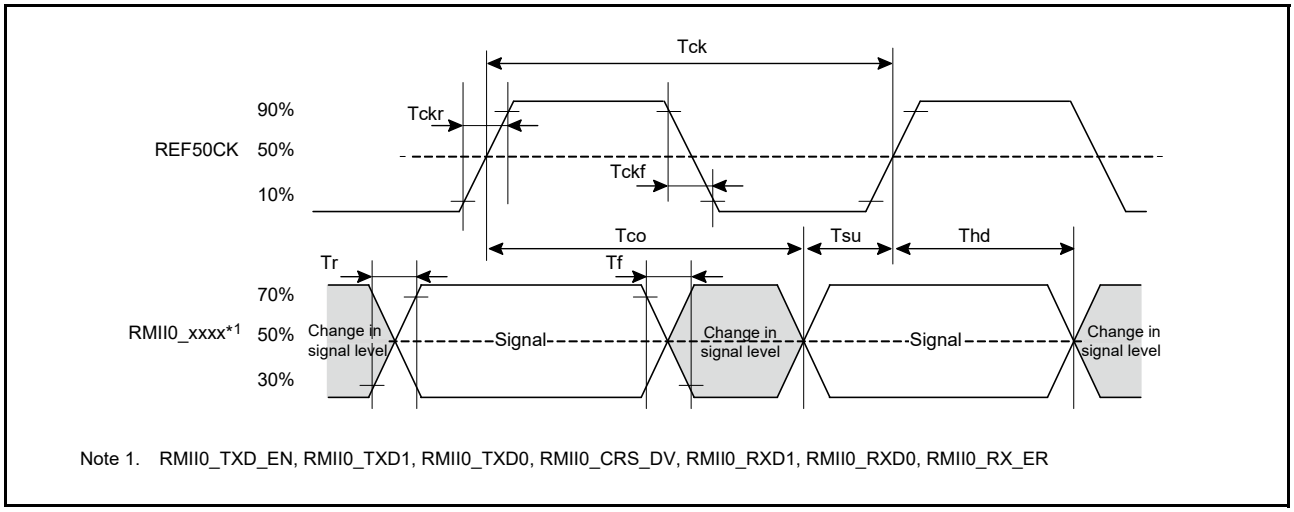
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
RMII: High-drive output for the high-speed interface is selected in the drive capacity control register.
MII: High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC (RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 2.81 to Figure 2.84 |
| | REF50CK frequency Typ. 50 MHz | — | — | 50 + 100 ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII0_xxxx*1 output delay time | $T_{co}$ | 2.5 | 15.0 | ns | |
| | RMII0_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII0_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII0_xxxx*1, *2 rise/fall time | $T_r/T_f$ | — | 5 | ns | |
| | ET0_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 2.85 |
| ETHERC (MII) | ET0_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET0_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 2.86 |
| | ET0_ETXD0 to ET0_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET0_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET0_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET0_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 2.87 |
| | ET0_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET0_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET0_RX_DV setup time | $t_{RDVs}$ | 10 | — | ns | Figure 2.88 |
| | ET0_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET0_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET0_ERXD0 to ET0_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET0_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 2.89 |
| | ET0_RX_ER hold time | $t_{RERh}$ | 10 | — | ns | |
| | ET0_WOL output delay time | $t_{WOLd}$ | 1 | 23.5 | ns | Figure 2.90 |

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER



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Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

**Figure 2.81 Timing with the REF50CK and RMII Signals**

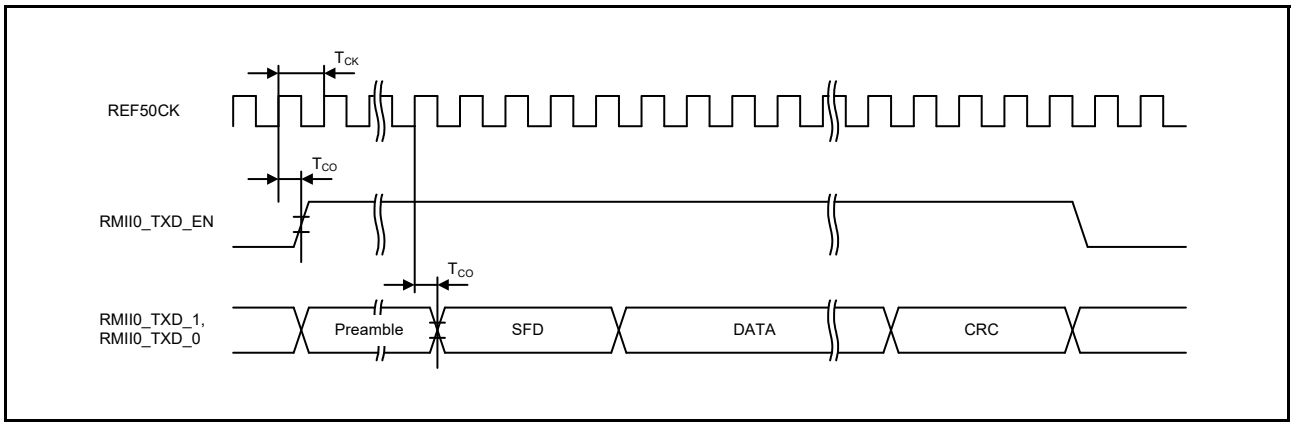



**Figure 2.82 RMII Transmission Timing**

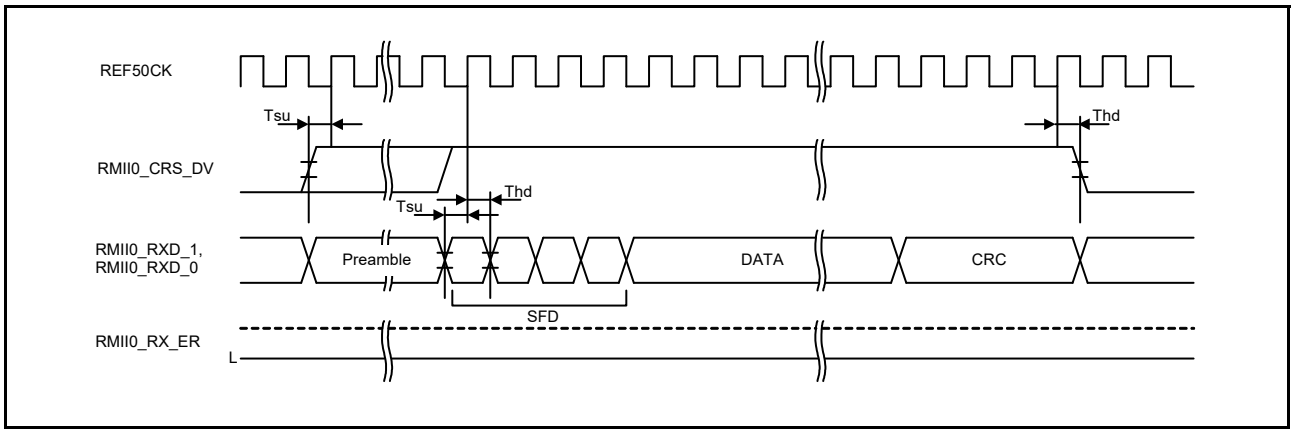



**Figure 2.83 RMII Reception Timing (Normal Operation)**



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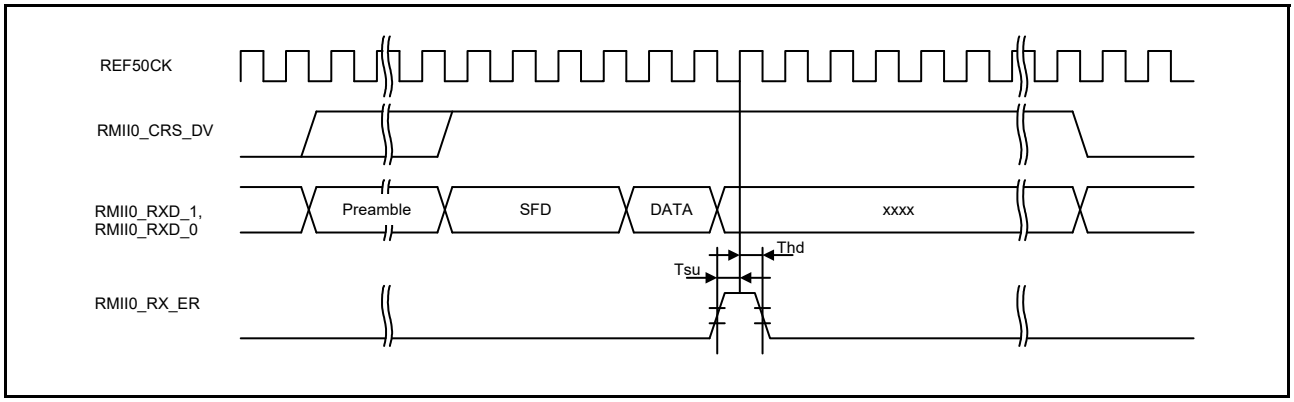



**Figure 2.84 RMII Reception Timing (Error Occurrence)**

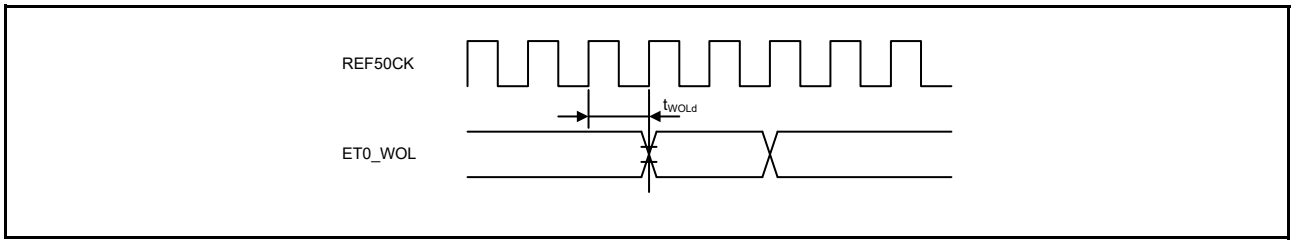



**Figure 2.85 WOL Output Timing (RMII)**

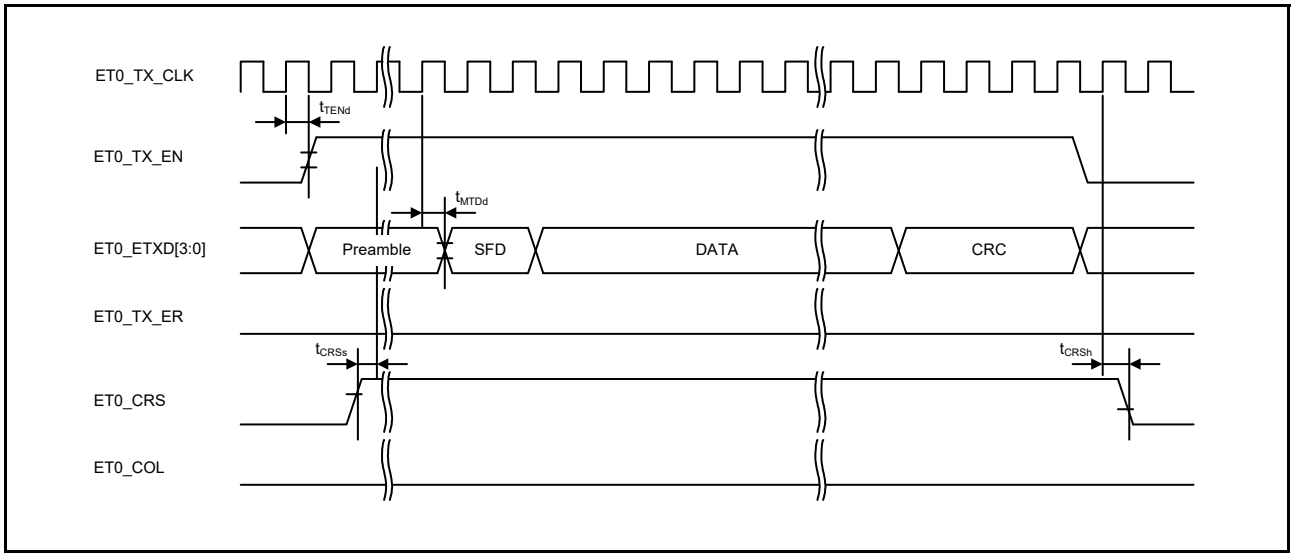



**Figure 2.86 MII Transmission Timing (Normal Operation)**



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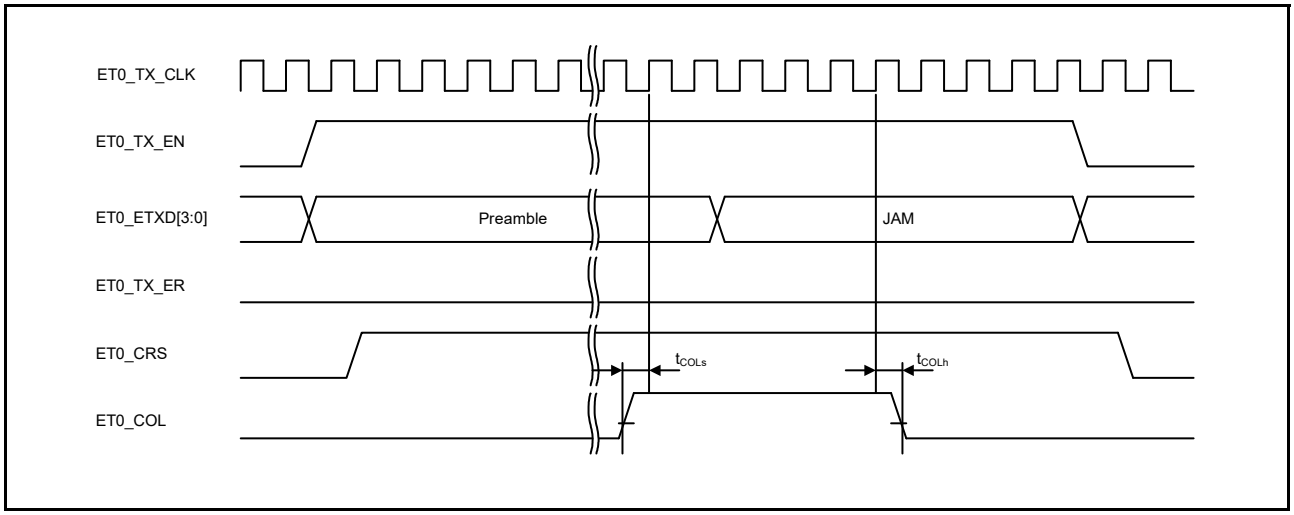



**Figure 2.87 MII Transmission Timing (Conflict Occurrence)**

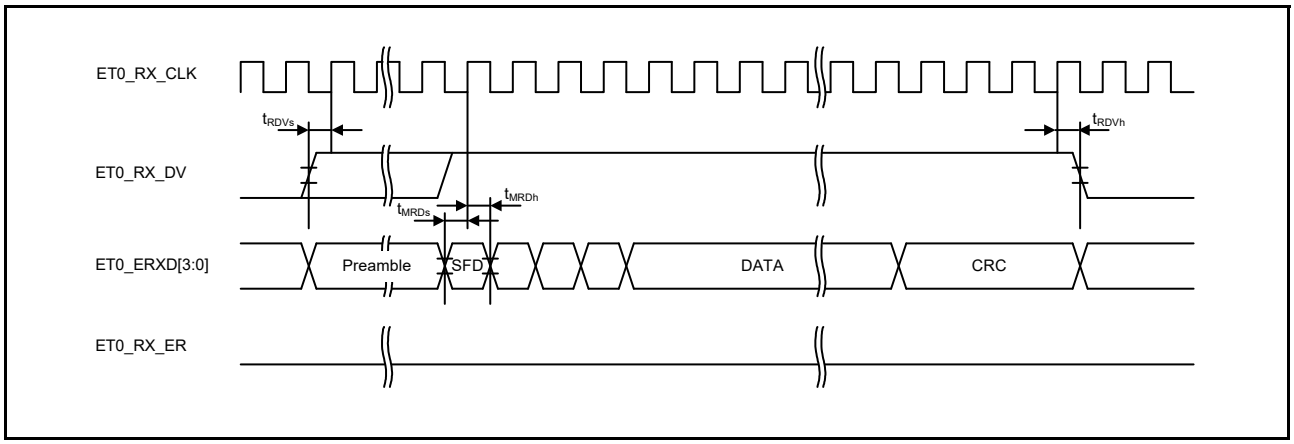



**Figure 2.88 MII Reception Timing (Normal Operation)**

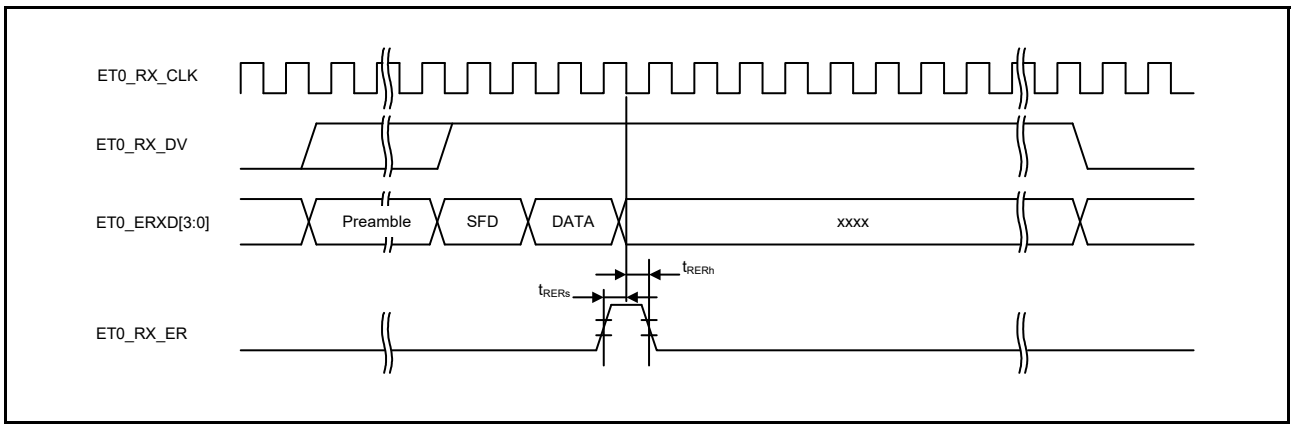



**Figure 2.89 MII Reception Timing (Error Occurrence)**



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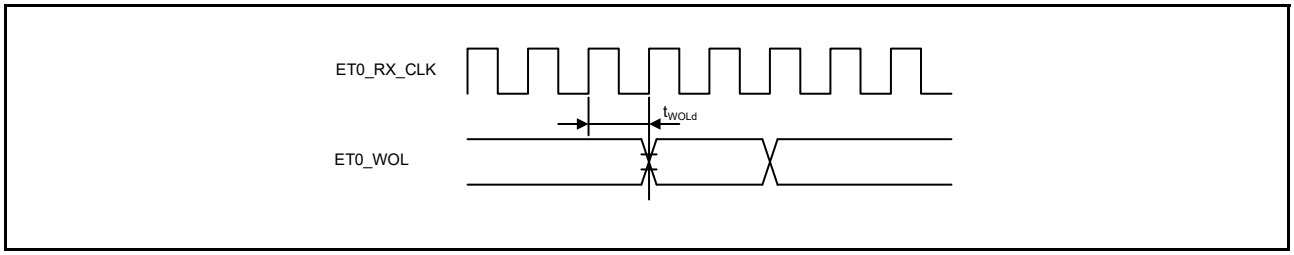



**Figure 2.90 WOL Output Timing (MII)**



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## 2.4.7.18 PDC

**Table 2.47 PDC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| PDC | PIXCLK input cycle time | $t_{PIXcyc}$ | 37 | — | ns | Figure 2.91 |
| | PIXCLK input high pulse width | $t_{PIXH}$ | 10 | — | ns | |
| | PIXCLK input low pulse width | $t_{PIXL}$ | 10 | — | ns | |
| | PIXCLK rising time | $t_{PIXr}$ | — | 5 | ns | |
| | PIXCLK falling time | $t_{PIXf}$ | — | 5 | ns | |
| | PCKO output cycle time | $t_{PCKcyc}$ | 2 × $t_{PBcyc}$ | — | ns | Figure 2.92 |
| | PCKO output high pulse width | $t_{PCKH}$ | ($t_{PCKcyc}$ – $t_{PCKr}$ – $t_{PCKf}$)/2 – 3 | — | ns | |
| | PCKO output low pulse width | $t_{PCKL}$ | ($t_{PCKcyc}$ – $t_{PCKr}$ – $t_{PCKf}$)/2 – 3 | — | ns | |
| | PCKO rising time | $t_{PCKr}$ | — | 5 | ns | |
| | PCKO falling time | $t_{PCKf}$ | — | 5 | ns | |
| | VSYNC/HSYNC input setup time | $t_{SYNCS}$ | 10 | — | ns | Figure 2.93 |
| | VSYNC/HSYNC input hold time | $t_{SYNCH}$ | 5 | — | ns | |
| | PIXD input setup time | $t_{PIXDS}$ | 10 | — | ns | |
| | PIXD input hold time | $t_{PIXDH}$ | 5 | — | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle

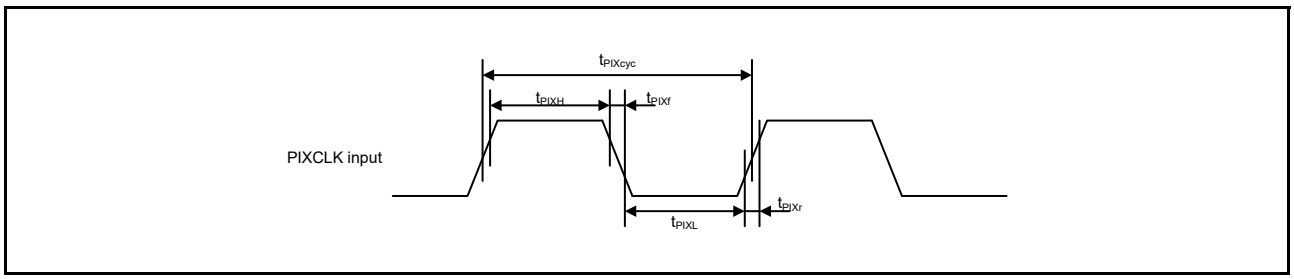



**Figure 2.91 PDC Input Clock Timing**

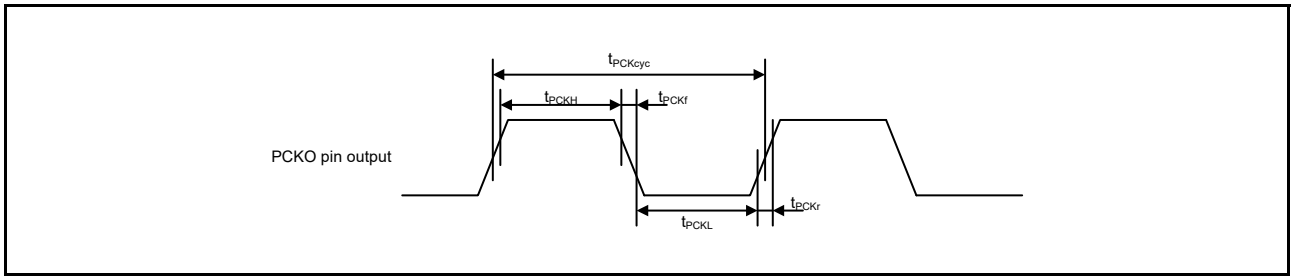



**Figure 2.92 PDC Output Clock Timing**



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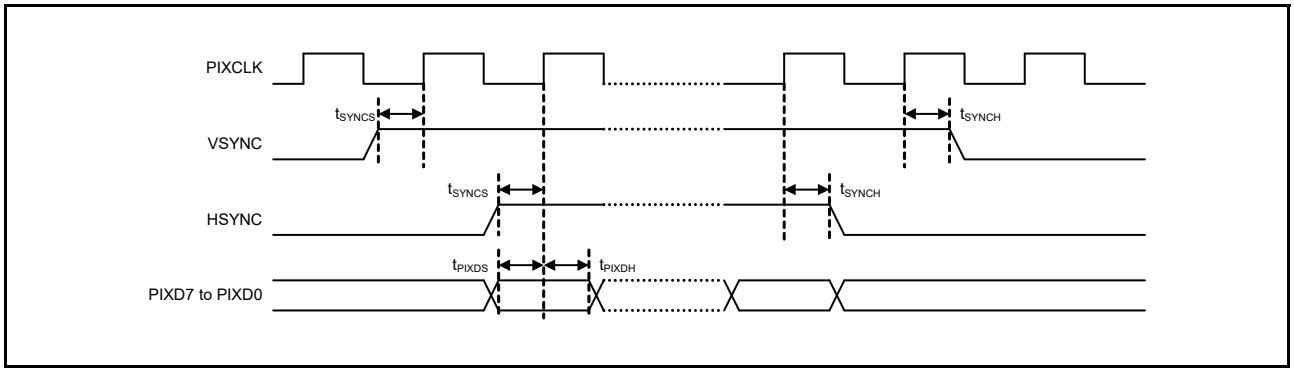



**Figure 2.93 PDC AC Timing**



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## 2.4.7.19 GLCDC

**Table 2.48 GLCDC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| LCD_EXTCLK Input clock frequency | $t_{Ecyc}$ | — | — | 30*1 | MHz | Figure 2.94 |
| LCD_EXTCLK Input clock Low pulse width | $t_{WL}$ | 0.45 | — | 0.55 | $t_{Ecyc}$ | |
| LCD_EXTCLK Input clock High pulse width | $t_{WH}$ | 0.45 | — | 0.55 | $t_{Ecyc}$ | |
| LCD_CLK Output clock frequency | $t_{Lcyc}$ | — | — | 30*1 | MHz | Figure 2.95 |
| LCD_CLK Output clock Low pulse width | $t_{LOL}$ | 0.4 | — | 0.6 | $t_{Lcyc}$ | |
| LCD_CLK Output clock High pulse width | $t_{LOH}$ | 0.4 | — | 0.6 | $t_{Lcyc}$ | |
| LCD_CLK Output clock rise time | $t_{LOR}$ | — | — | 5 | ns | |
| LCD_CLK Output clock fall time | $t_{LOF}$ | — | — | 5 | ns | |
| LCD data output Delay timing | $t_{DD}$ | –3.5*2 | — | 4*2 | ns | Figure 2.96 |

Note 1. Parallel RGB888,666,565: Max. 27 MHz
Serial RGB888: Max. 30 MHz (4x speed)
Note 2. We recommend using pins that have a letter (“-A”, “-B”, etc) to indicate group membership appended to their names as groups.
For the GLCDC interface, the AC portion of the electrical characteristics is measured for each group.
If we use group “-A” and “-B” combination, “LCD data output Delay timing ($t_{DD}$)” is Min = –5.0 ns, Max = 5.5 ns.

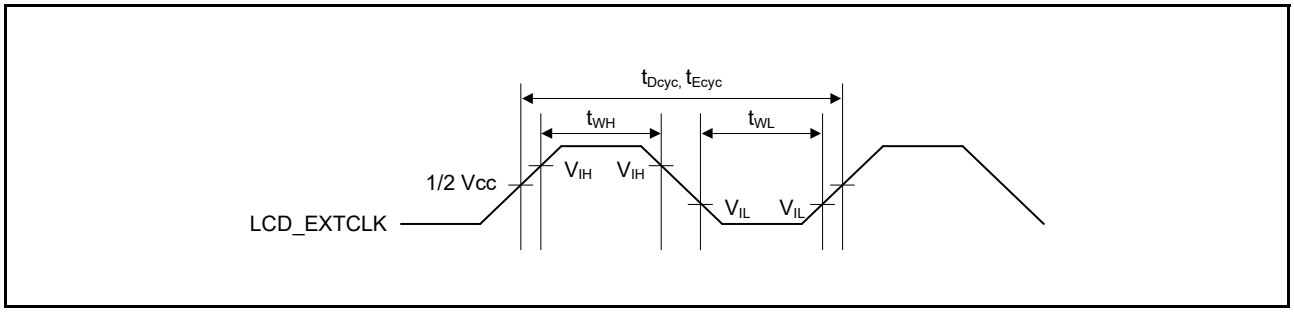



**Figure 2.94 LCD_EXTCLK Clock Input Timing**

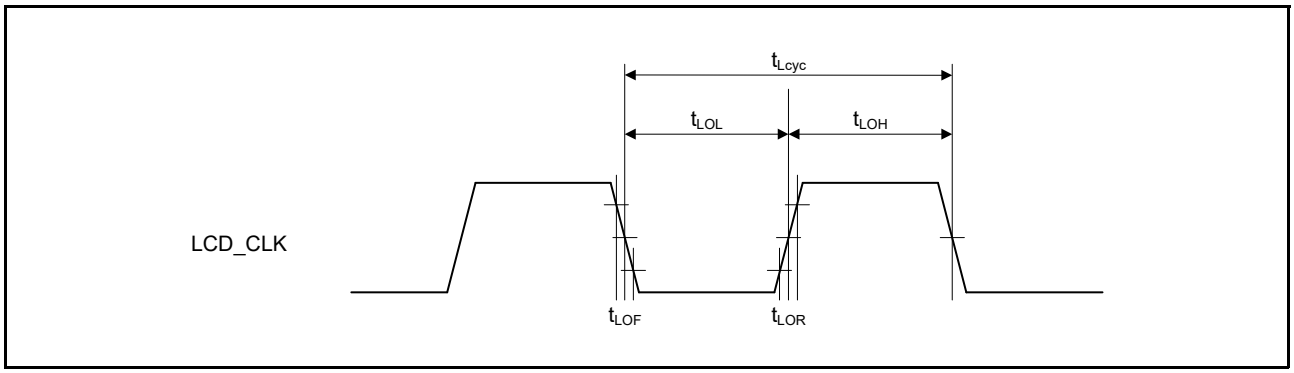



**Figure 2.95 LCD_CLK Clock Output Timing**



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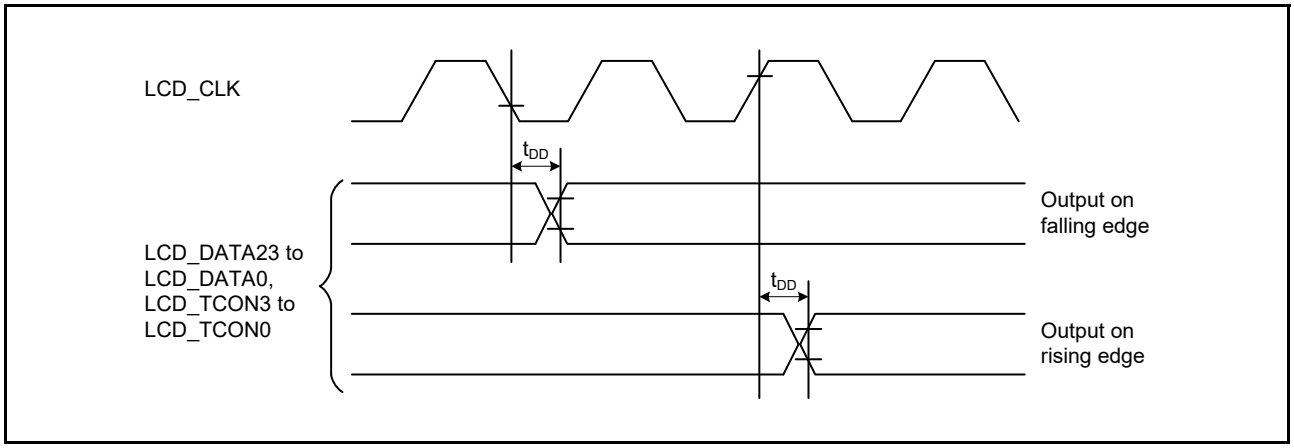



**Figure 2.96 LCD Output Data Timing**



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### 2.4.7.20 A/D Converter Trigger

**Table 2.49 A/D Converter Trigger Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| A/D converter | A/D converter trigger input pulse width | $t_{TRGW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 2.97 |

Note 1. $t_{PBcyc}$: PCLKB cycle

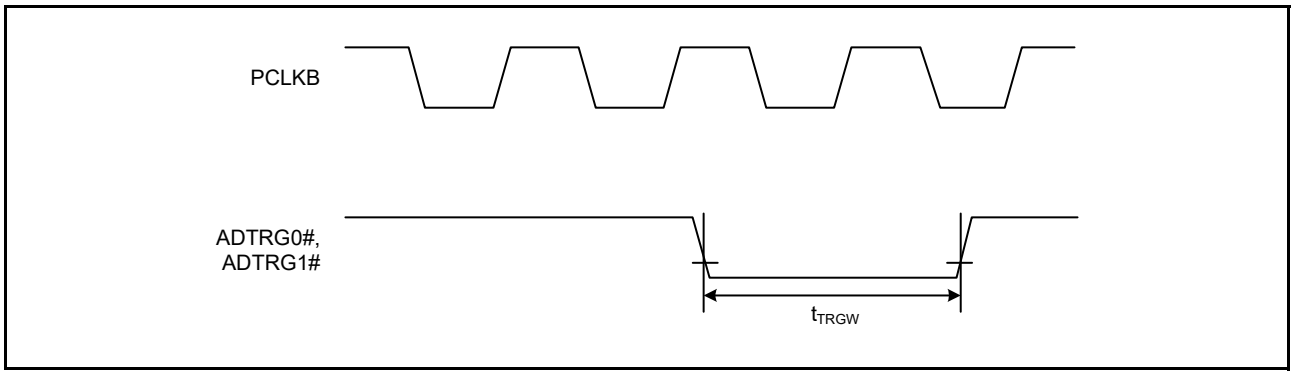



**Figure 2.97 A/D Converter Trigger Input Timing**



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### 2.4.7.21 CAC

**Table 2.50 CAC Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item*1, *2 | | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}$ | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{PBcyc}$ | — | ns | |
| | | $t_{PBcyc} > t_{cac}$ | | 5 $t_{cac}$ + 6.5 $t_{PBcyc}$ | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle
Note 2. $t_{cac}$: CAC count clock source cycle



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## 2.5 USB Characteristics

**Table 2.51 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| DP – DM \| |
| | Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 μA |
| | Output low level voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 2.98 |
| | Rise time | $t_{LR}$ | 75 | — | 300 | ns | |
| | Fall time | $t_{LF}$ | 75 | — | 300 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 80 | — | 125 | % | $t_{LR}$/ $t_{LF}$ |
| Pull-down characteristics | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

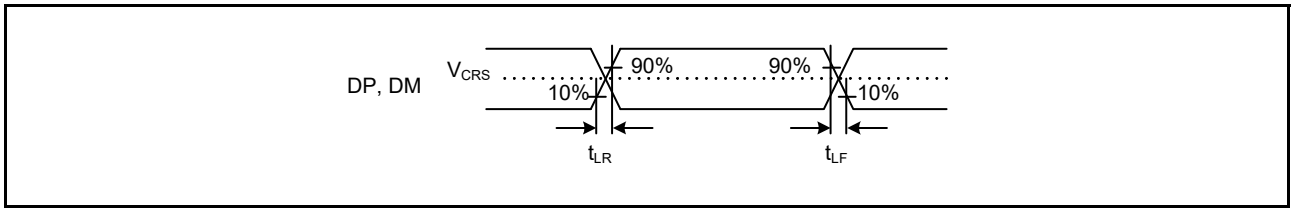



**Figure 2.98 DP and DM Output Timing (Low Speed)**

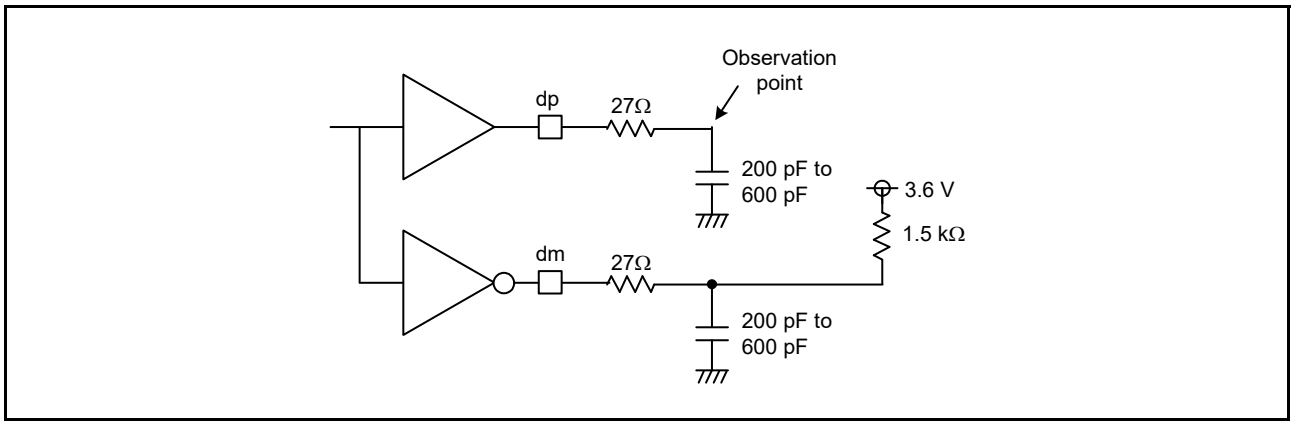



**Figure 2.99 Test Circuit (Low Speed)**



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**Table 2.52 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz, PCLKA = 8 to 120 MHz,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | — | V | |
| | Input low level voltage | $V_{IL}$ | — | — | 0.8 | V | |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | — | — | V | \| DP – DM \| |
| | Differential common mode range | $V_{CM}$ | 0.8 | — | 2.5 | V | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | — | 3.6 | V | $I_{OH}$ = –200 µA |
| | Output low level voltage | $V_{OL}$ | 0.0 | — | 0.3 | V | $I_{OL}$ = 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | — | 2.0 | V | Figure 2.100 |
| | Rise time | $t_{FR}$ | 4 | — | 20 | ns | |
| | Fall time | $t_{FF}$ | 4 | — | 20 | ns | |
| | Rise/fall time ratio | $t_{FR}$ / $t_{FF}$ | 90 | — | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | — | 44 | Ω | Rs = 27 Ω included |
| Pull-up and pull-down characteristics | DP pull-up resistance (when the function controller function is selected) | $R_{pu}$ | 0.900 | — | 1.575 | kΩ | Idle state |
| | | | 1.425 | — | 3.090 | | At transmission and reception |
| | DP/DM pull-down resistance (when the host controller function is selected) | $R_{pd}$ | 14.25 | — | 24.80 | kΩ | |

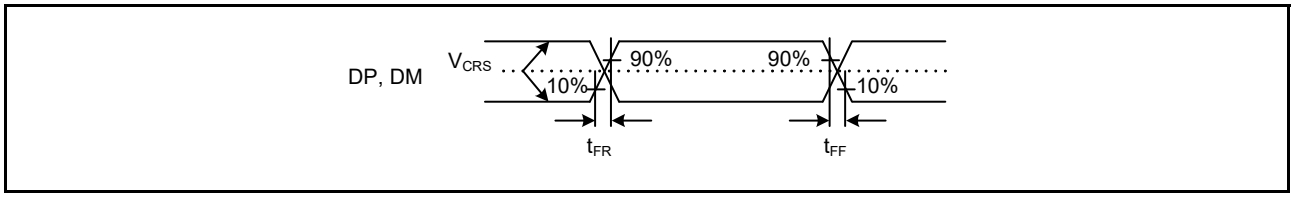



**Figure 2.100 DP and DM Output Timing (Full-Speed)**

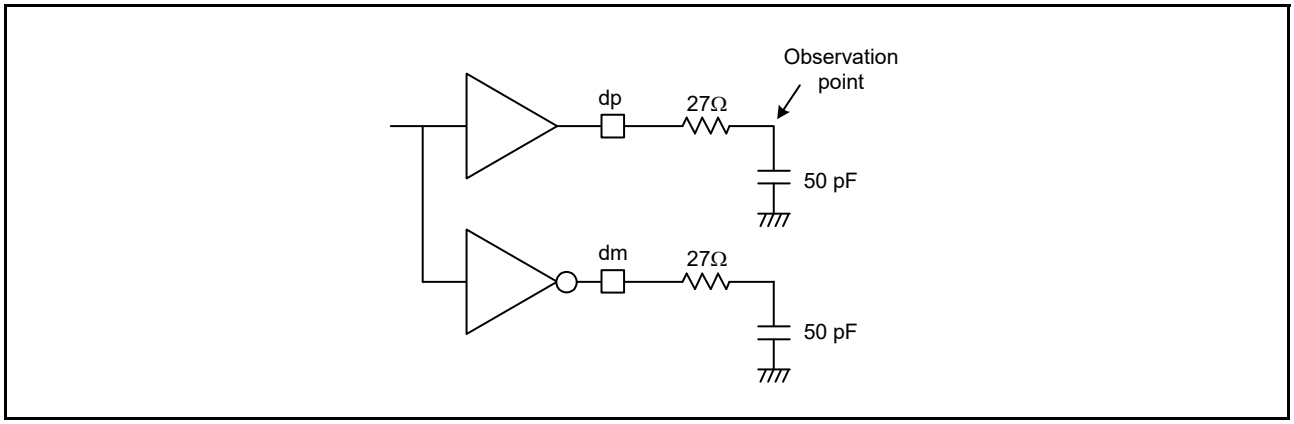



**Figure 2.101 Test Circuit (Full-Speed)**



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## 2.6 A/D Conversion Characteristics

**Table 2.53 12-Bit A/D (Unit 0) Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$, Source impedance = 1.0 kΩ

| Item | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 8 | — | 12 | Bit | |
| Analog input capacitance | | — | — | 30 | pF | |
| Channel-dedicated sample-and-hold circuits in use (AN000 to AN002) | Conversion time*1 (Operation at PCLKC = 60 MHz) | 1.06 (0.4 + 0.25) *2 | — | — | µs | • Sampling of channel-dedicated sample-and-hold circuits in 24 states<br>• Sampling in 15 states |
| | Offset error | — | ±1.5 | ±3.5 | LSB | AN000 to AN002 = 0.25 V |
| | Full-scale error | — | ±1.5 | ±3.5 | LSB | AN000 to AN002 = VREFH0 – 0.25 V |
| | Quantization error | — | ±0.5 | — | LSB | |
| | Absolute accuracy | — | ±3.0 | ±5.5 | LSB | |
| | DNL differential nonlinearity error | — | ±1.0 | ±2.0 | LSB | |
| | INL integral nonlinearity error | — | ±1.5 | ±3.0 | LSB | |
| | Holding characteristics of sample-and-hold circuits | — | — | 20 | µs | |
| | Dynamic range | 0.25 | — | VREFH0 – 0.25 | V | |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007) | Conversion time*1 (Operation at PCLKC = 60 MHz) | 0.48 (0.267)*2 | — | — | µs | Sampling in 16 states |
| | Offset error | — | ±1.0 | ±2.5 | LSB | |
| | Full-scale error | — | ±1.0 | ±2.5 | LSB | |
| | Quantization error | — | ±0.5 | — | LSB | |
| | Absolute accuracy | — | ±2.5 | ±4.5 | LSB | |
| | DNL differential nonlinearity error | — | ±0.5 | ±1.5 | LSB | |
| | INL integral nonlinearity error | — | ±1.0 | ±2.5 | LSB | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.



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**Table 2.54 12-Bit A/D (Unit 1) Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$, Source impedance = 1.0 kΩ

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 8 | — | 12 | Bit | |
| Conversion time*1 (Operation at PCLKD = 60 MHz) | 0.88 (0.633)*2 | — | — | µs | Sampling in 38 states (ADSAM.SAM = 1) |
| Conversion time*1 (Operation at PCLKD = 30 MHz) | 1 (0.500)*2 | — | — | µs | Sampling in 15 states (ADSAM.SAM = 1) |
| Analog input capacitance | — | — | 30 | pF | |
| Offset error | — | ±2.0 | ±3.5 | LSB | |
| Full-scale error | — | ±2.0 | ±3.5 | LSB | |
| Quantization error | — | ±0.5 | — | LSB | |
| Absolute accuracy | — | ±4.0 | ±6.0 | LSB | |
| DNL differential nonlinearity error (Operation at PCLKD = 60 MHz) | — | ±1.5 | ±4.0 | LSB | |
| DNL differential nonlinearity error (Operation at PCLKD = 30 MHz) | — | ±1.5 | ±2.5 | LSB | |
| INL integral nonlinearity error (Operation at PCLKD = 60 MHz) | — | ±2.0 | ±4.0 | LSB | |
| INL integral nonlinearity error (Operation at PCLKD = 30 MHz) | — | ±2.0 | ±3.5 | LSB | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

**Table 2.55 A/D Internal Reference Voltage Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | |



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## 2.7 D/A Conversion Characteristics

**Table 2.56 D/A Conversion Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | — | 12 | 12 | 12 | Bit | |
| Unbuffered output | Absolute accuracy | — | — | — | ±6.0 | LSB | 2-MΩ resistive load<br>10-bit conversion |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | 2-MΩ resistive load |
| | Output resistance | $R_O$ | — | 8.6 | — | kΩ | |
| | Setting time | $t_S$ | — | — | 3 | μs | 20-pF capacitive load |
| Buffered output | Load resistance | $R_L$ | 5 | — | — | kΩ | |
| | Load capacitance | $C_L$ | — | — | 50 | pF | |
| | Output voltage | $V_O$ | 0.2 | — | AVCC1 – 0.2 | V | |
| | Differential nonlinearity error | DNL | — | ±1.0 | ±2.0 | LSB | |
| | Integral nonlinearity error | INL | — | ±2.0 | ±4.0 | LSB | |
| | Setting time | $t_S$ | — | — | 4 | μs | |

## 2.8 Temperature Sensor Characteristics

**Table 2.57 Temperature Sensor Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Relative accuracy | — | ±1 | — | °C | |
| Temperature slope | — | 4 | — | mV/°C | |
| Output voltage | — | 1.21 | — | V | $T_a$ = 25°C |
| Temperature sensor start time | — | — | 30 | μs | |
| Sampling time*1 | 4.15 | — | — | μs | |

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.



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## 2.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 2.58 Power-on Reset Circuit and Voltage Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | Low power consumption function disabled*1 | $V_{POR}$ | 2.5 | 2.6 | 2.7 | V | Figure 2.102 |
| | | Low power consumption function enabled*2 | | 1.8 | 2.25 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | $V_{det0_1}$ | 2.84 | 2.94 | 3.04 | | Figure 2.103 |
| | | | $V_{det0_2}$ | 2.77 | 2.87 | 2.97 | | |
| | | | $V_{det0_3}$ | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | | $V_{det1_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.104 |
| | | | $V_{det1_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det1_3}$ | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | | $V_{det2_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.105 |
| | | | $V_{det2_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det2_3}$ | 2.75 | 2.85 | 2.95 | | |
| Internal reset time | Power-on reset time | | $t_{POR}$ | — | 4.6 | — | ms | Figure 2.102 |
| | LVD0 reset time | | $t_{LVD0}$ | — | 0.70 | — | | Figure 2.103 |
| | LVD1 reset time | | $t_{LVD1}$ | — | 0.57 | — | | Figure 2.104 |
| | LVD2 reset time | | $t_{LVD2}$ | — | 0.57 | — | | Figure 2.105 |
| Minimum VCC down time | | | $t_{VOFF}$ | 200 | — | — | μs | Figure 2.102, Figure 2.103 |
| Response delay time | | | $t_{det}$ | — | — | 200 | μs | Figure 2.102 to Figure 2.105 |
| LVD operation stabilization time (after LVD is enabled) | | | $t_{d(E-A)}$ | — | — | 10 | μs | Figure 2.104, Figure 2.105 |
| Hysteresis width (LVD1 and LVD2) | | | $V_{LVH}$ | — | 70 | — | mV | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/ LVD.
Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

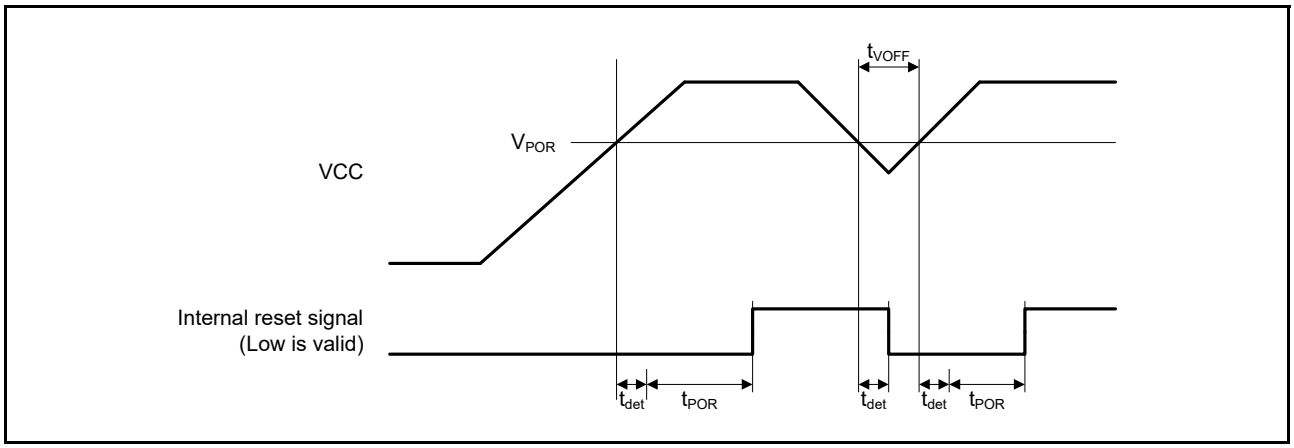



**Figure 2.102 Power-on Reset Timing**



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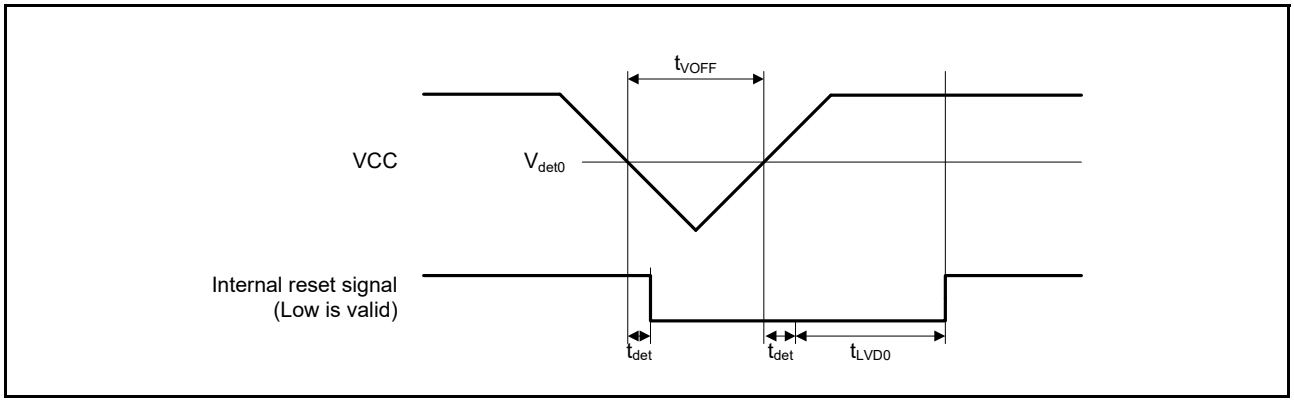



**Figure 2.103 Voltage Detection Circuit Timing ($V_{det0}$)**

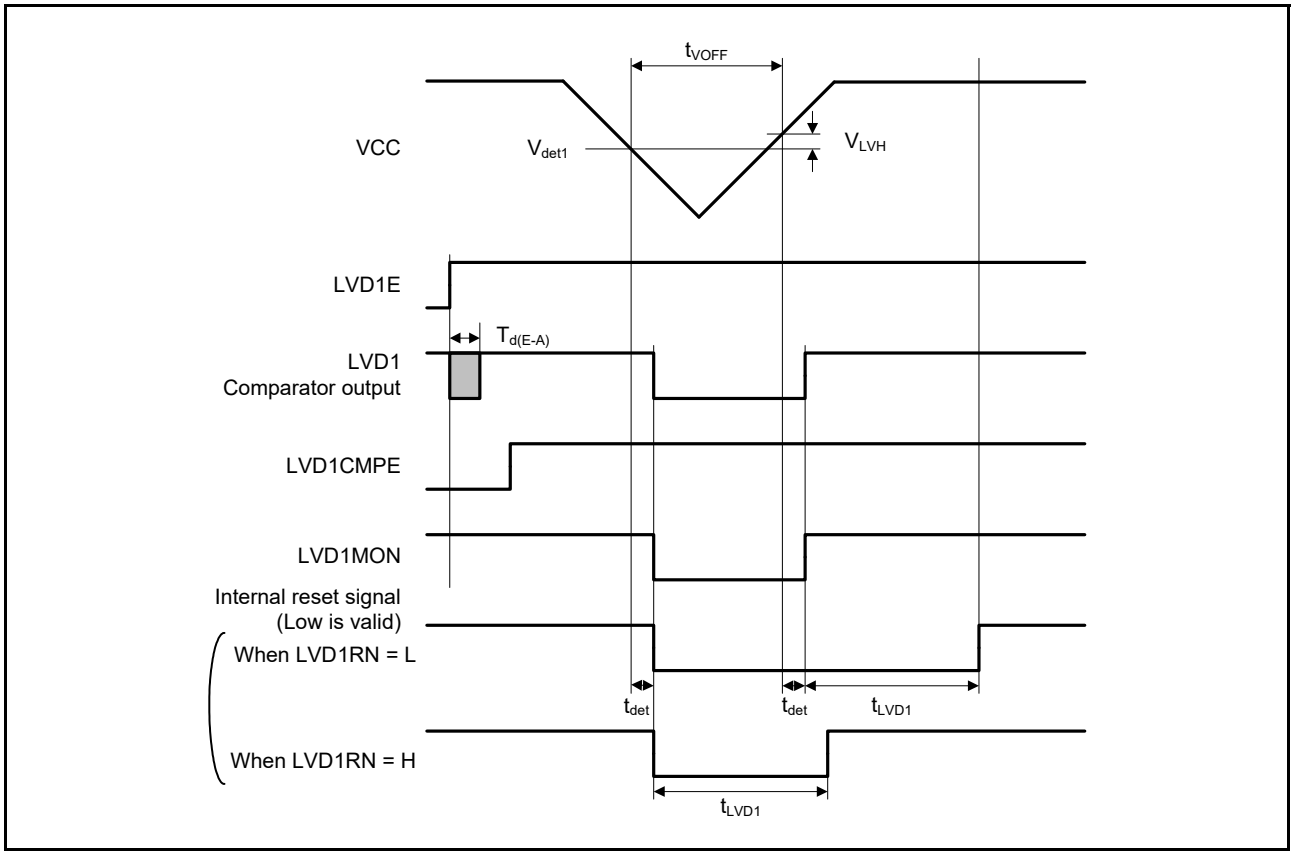



**Figure 2.104 Voltage Detection Circuit Timing ($V_{det1}$)**



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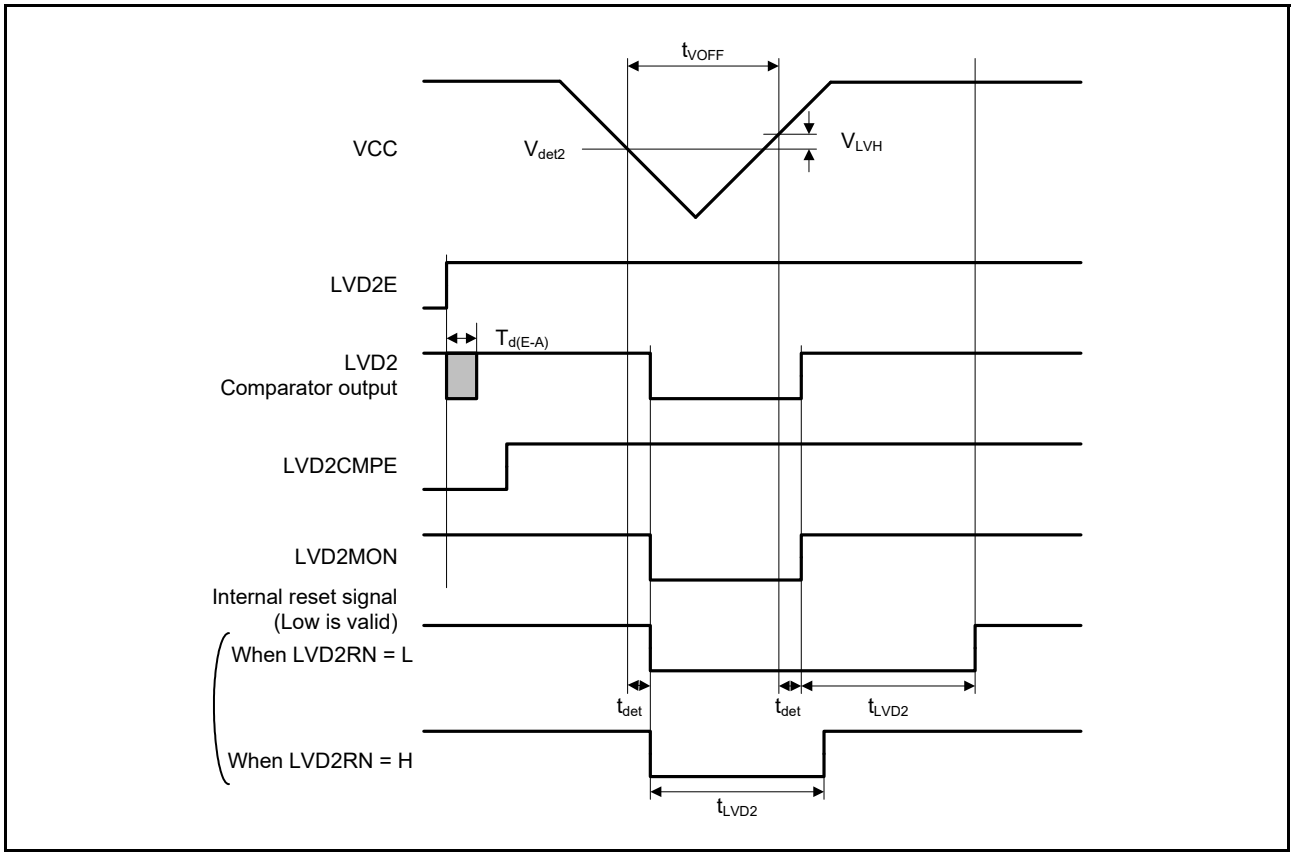



**Figure 2.105 Voltage Detection Circuit Timing ($V_{det2}$)**



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## 2.10 Oscillation Stop Detection Timing

**Table 2.59 Oscillation Stop Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | — | — | 1 | ms | Figure 2.106 |

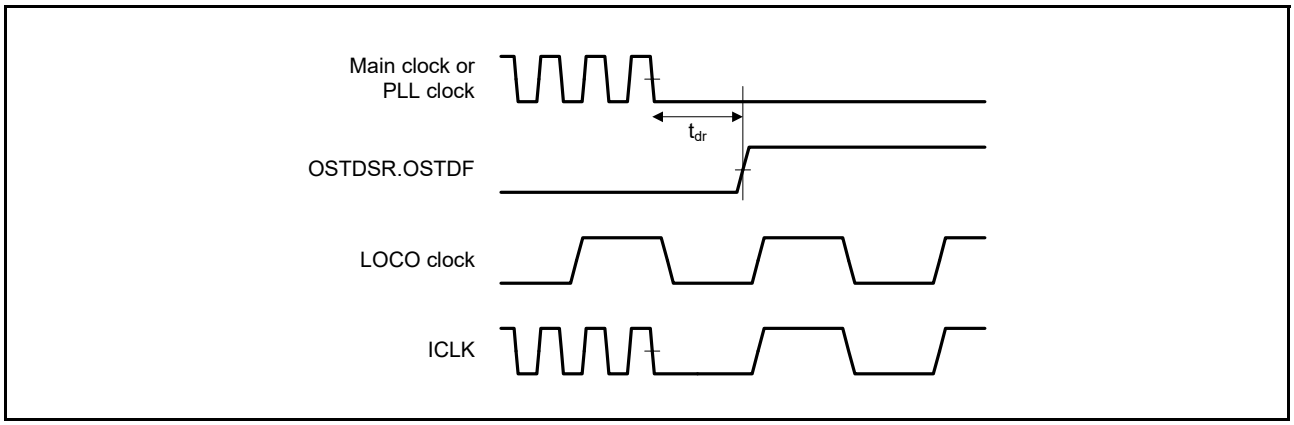



**Figure 2.106 Oscillation Stop Detection Timing**



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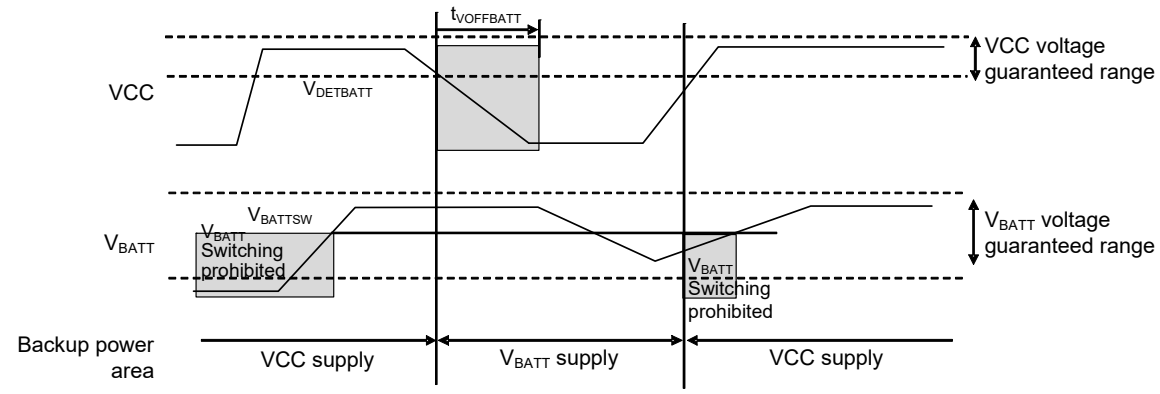
## 2.11 Battery Backup Function Characteristics

**Table 2.60 Battery Backup Function Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$V_{BATT}$ = 1.62 to 3.6 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.107 |
| Lower-limit $V_{BATT}$ voltage for power supply switching due to VCC voltage drop | $V_{BATTSW}$ | 2.70 | — | — | | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | — | — | µs | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).




Note. The $V_{BATT}$ voltage when the supplied power source switches from VCC to $V_{BATT}$ should not be lower than $V_{BATTSW}$, the lower-limit $V_{BATT}$ voltage for switching between power supplies due to a drop in the VCC voltage.

**Figure 2.107 Battery Backup Function Characteristics**



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## 2.12 Flash Memory Characteristics

**Table 2.61 Code Flash Memory Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time $N_{PEC}$ ≤ 100 times | 128 bytes | $t_{P128}$ | — | 0.75 | 13.2 | — | 0.38 | 6.6 | — | 0.34 | 6 | ms | |
| | 8 Kbytes | $t_{P8K}$ | — | 49 | 176 | — | 25 | 88 | — | 22 | 80 | ms | |
| | 32 Kbytes | $t_{P32K}$ | — | 194 | 704 | — | 97 | 352 | — | 88 | 320 | ms | |
| Programming time $N_{PEC}$ > 100 times | 128 bytes | $t_{P128}$ | — | 0.91 | 15.8 | — | 0.46 | 8 | — | 0.41 | 7.2 | ms | |
| | 8 Kbytes | $t_{P8K}$ | — | 60 | 212 | — | 30 | 106 | — | 27 | 96 | ms | |
| | 32 Kbytes | $t_{P32K}$ | — | 234 | 848 | — | 117 | 424 | — | 106 | 384 | ms | |
| Erasure time $N_{PEC}$ ≤ 100 times | 8 Kbytes | $t_{E8K}$ | — | 78 | 216 | — | 48 | 132 | — | 43 | 120 | ms | |
| | 32 Kbytes | $t_{E32K}$ | — | 283 | 864 | — | 173 | 528 | — | 157 | 480 | ms | |
| Erasure time $N_{PEC}$ > 100 times | 8 Kbytes | $t_{E8K}$ | — | 94 | 260 | — | 58 | 158 | — | 52 | 144 | ms | |
| | 32 Kbytes | $t_{E32K}$ | — | 341 | 1040 | — | 208 | 632 | — | 189 | 576 | ms | |
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 10000 *2 | — | — | 10000 *2 | — | — | 10000 *2 | — | — | Times | |
| Suspend delay time during programming | | $t_{SPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs | |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 216 | — | — | 132 | — | — | 120 | µs | |
| Second suspend delay time during erasure (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms | |
| Suspend delay time during erasure (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | — | — | 1.7 | ms | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs | |
| Data retention*3, *4 | | $t_{DRP}$ | 20 | — | — | 20 | — | — | 20 | — | — | Year | $T_a$ ≤ 85°C |
| | | | 10 | — | — | 10 | — | — | 10 | — | — | | $T_a$ ≤ 105°C |

Note 1. Definition of reprogram/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 128-byte program is performed 64 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristics when a self-programming library provided by Renesas Electronics or a flash programmer is used and the program/erase cycle does not exceed the specified value.

Note 4. This result is obtained from reliability testing.



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**Table 2.62 Data Flash Memory Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | FCLK = 15 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Programming time | 4 bytes | $t_{DP4}$ | — | 0.36 | 3.8 | — | 0.18 | 1.9 | — | 0.16 | 1.7 | ms | |
| Erasure time | 64 bytes | $t_{DP64}$ | — | 3.1 | 18 | — | 1.9 | 11 | — | 1.7 | 10 | ms | |
| | 128 bytes | $t_{DP128}$ | — | 4.7 | 27 | — | 2.9 | 16 | — | 2.6 | 15 | ms | |
| | 256 bytes | $t_{DP256}$ | — | 8.9 | 50 | — | 5.4 | 31 | — | 4.9 | 28 | ms | |
| Blank check time | 4 bytes | $t_{DBC4}$ | — | — | 84 | — | — | 33 | — | — | 30 | µs | |
| | 64 bytes | $t_{DBC64}$ | — | — | 280 | — | — | 110 | — | — | 100 | µs | |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 6160 | — | — | 2420 | — | — | 2200 | µs | |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 100000 *2 | — | — | 100000 *2 | — | — | 100000 *2 | — | — | Times | |
| Suspend delay time during programming | | $t_{DSPD}$ | — | — | 264 | — | — | 132 | — | — | 120 | µs | |
| First suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs | |
| | 128 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs | |
| | 256 bytes | — | — | — | 216 | — | — | 132 | — | — | 120 | µs | |
| Second suspend delay time during erasure (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs | |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs | |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs | |
| Suspend delay time during erasing (in suspend priority mode) | 64 bytes | — | — | — | 300 | — | — | 300 | — | — | 300 | µs | |
| | 128 bytes | — | — | — | 390 | — | — | 390 | — | — | 390 | µs | |
| | 256 bytes | — | — | — | 570 | — | — | 570 | — | — | 570 | µs | |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 22 | — | — | 20 | µs | |
| Data retention*3, *4 | | $t_{DDRP}$ | 20 | — | — | 20 | — | — | 20 | — | — | Year | $T_a \leq 85°C$ |
| | | | 10 | — | — | 10 | — | — | 10 | — | — | | $T_a \leq 105°C$ |

Note 1. Definition of reprogram/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristics when a self-programming library provided by Renesas Electronics or a flash programmer is used and the program/erase cycle does not exceed the specified value.

Note 4. This result is obtained from reliability testing.



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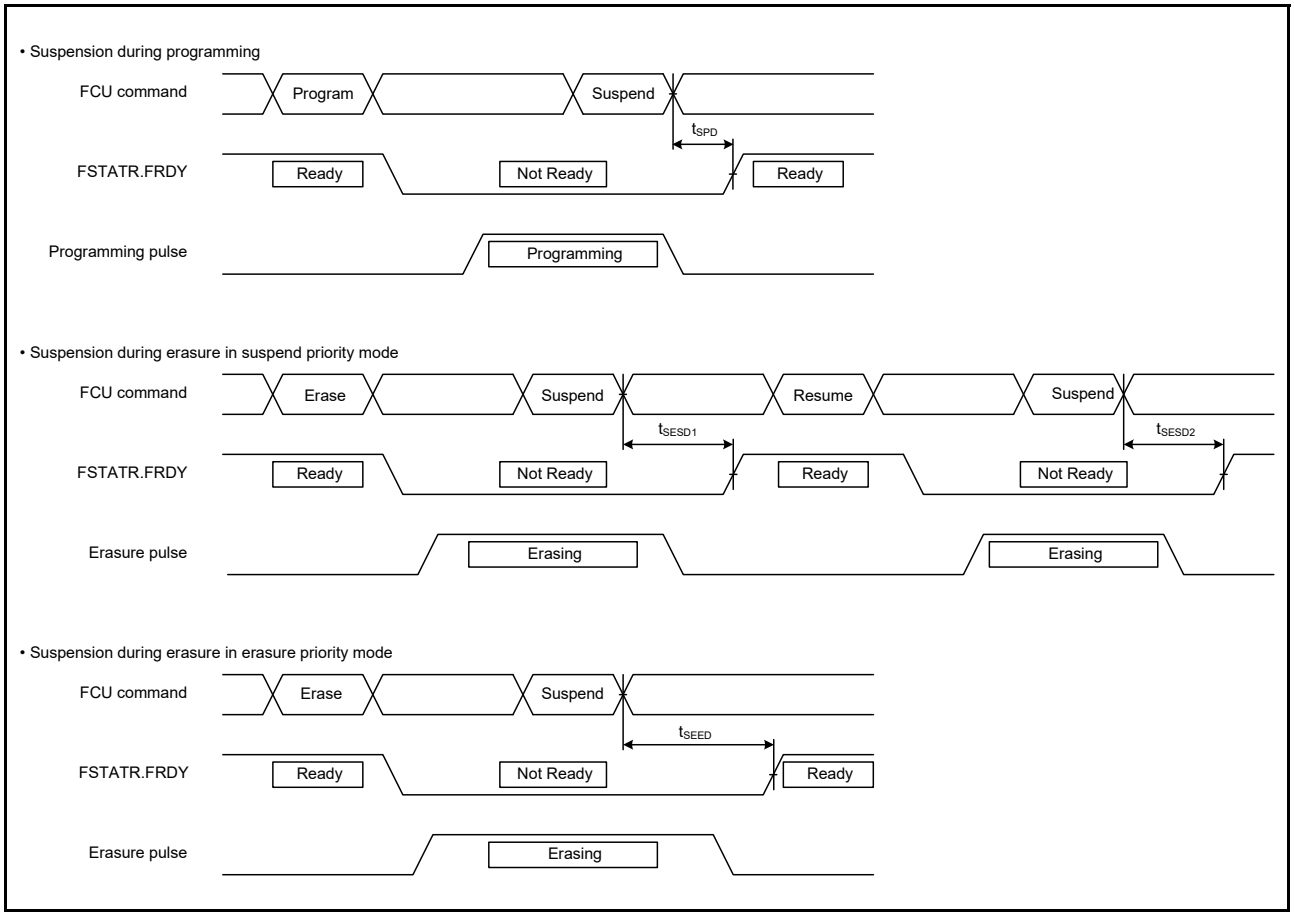



**Figure 2.108 Flash Memory Programming/Erasure Suspension Timing**



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## 2.13 Boundary Scan

**Table 2.63 Boundary Scan Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
Output load conditions: $V_{OH}$ = 0.5 × VCC, $V_{OL}$ = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 2.109 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rise time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | — | — | 5 | ns | |
| TRST# pulse width | $t_{TRSTW}$ | 20 | — | — | $t_{TCKcyc}$ | Figure 2.110 |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 2.111 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 40 | ns | |

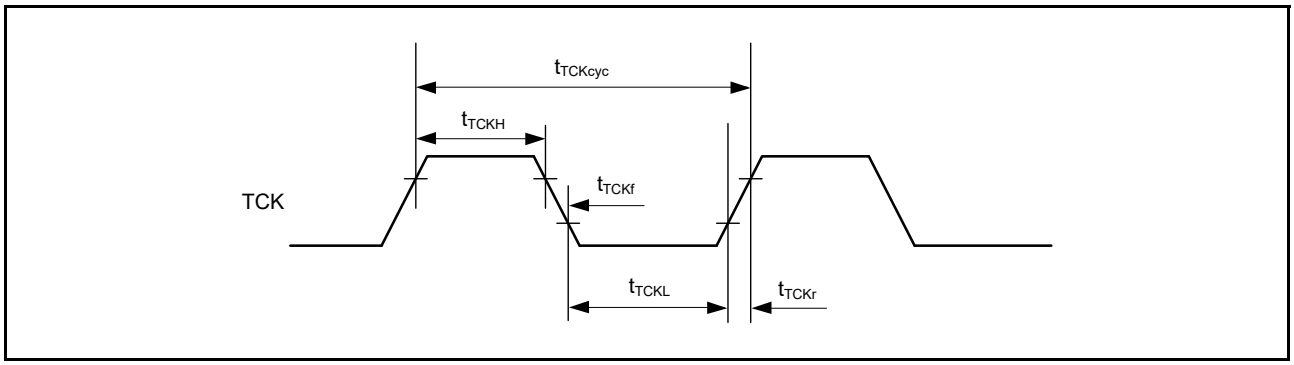



**Figure 2.109 Boundary Scan TCK Timing**

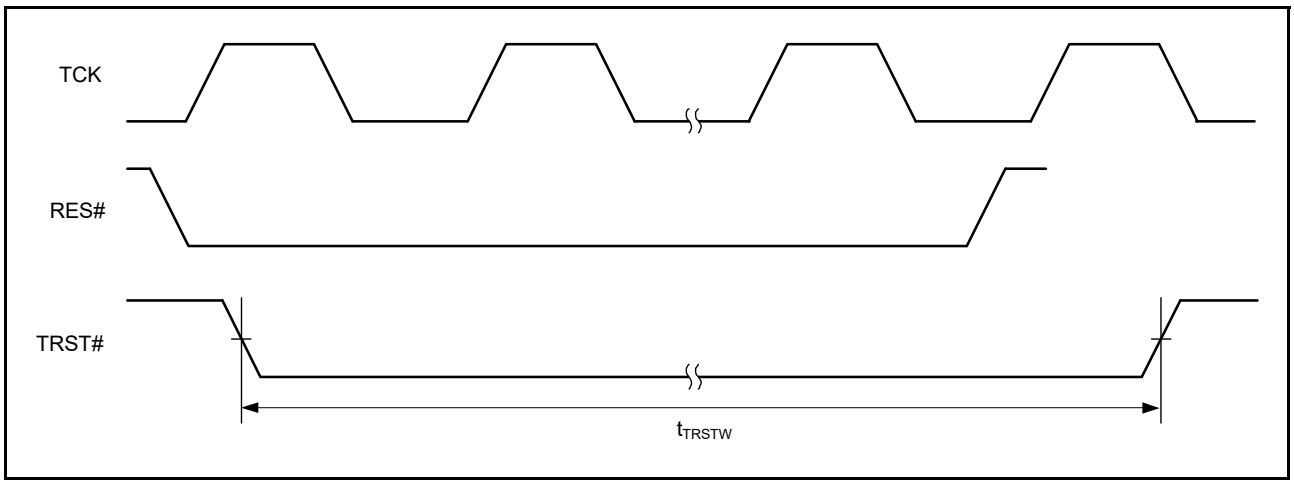



**Figure 2.110 Boundary Scan TRST# Timing**



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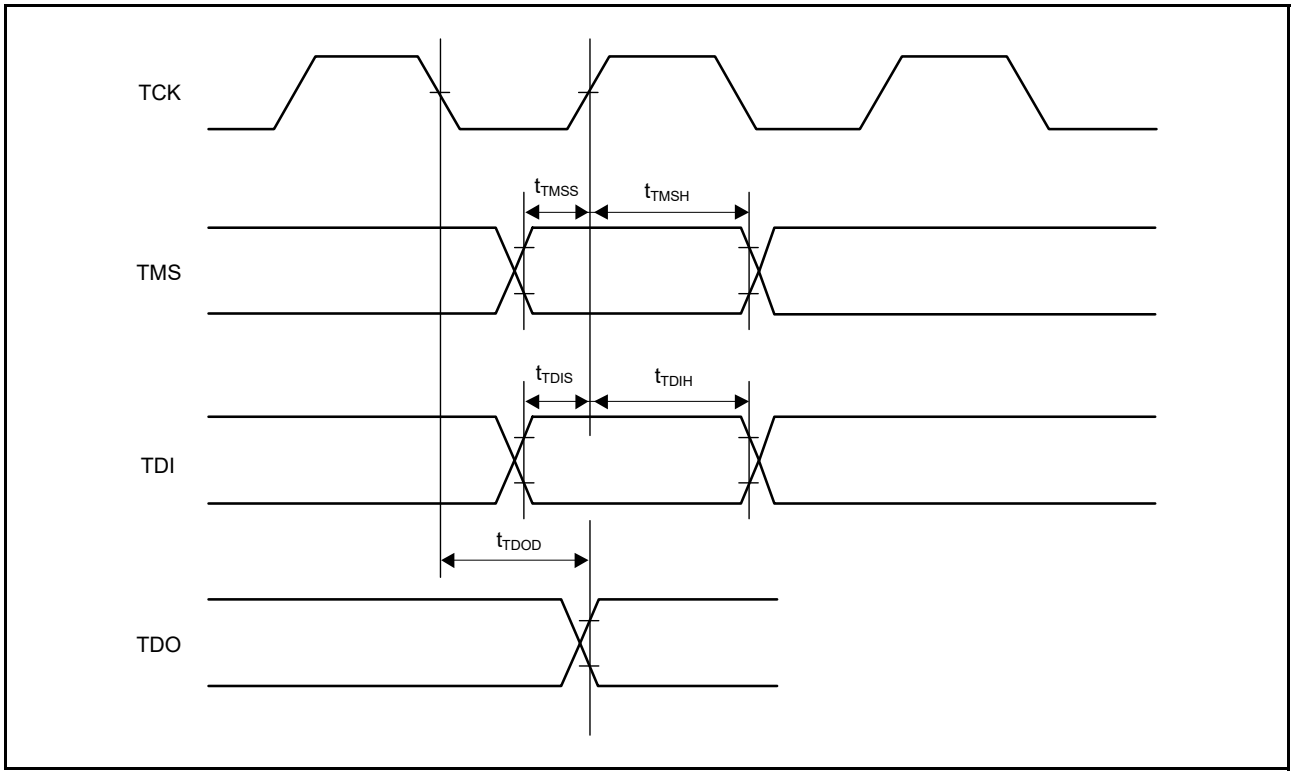



**Figure 2.111 Boundary Scan Input/Output Timing**



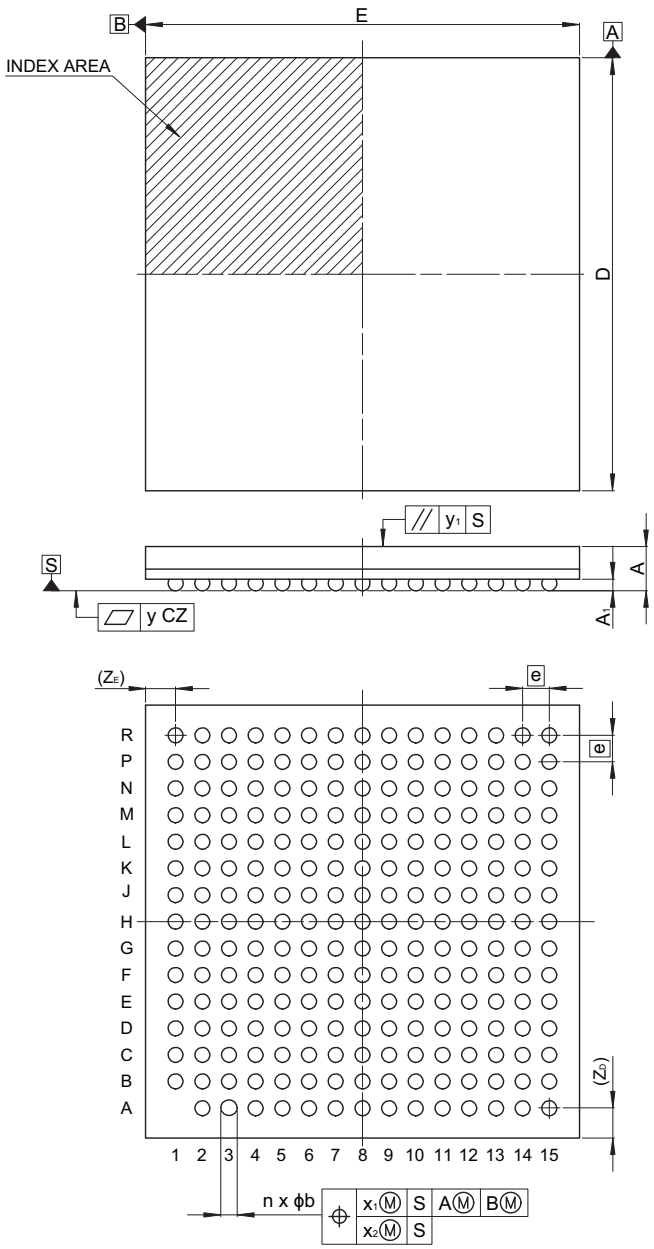
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# Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFBGA224-13x13-0.80 | PLBG0224GA-A | 224FHE | 0.4 |

Unit: mm



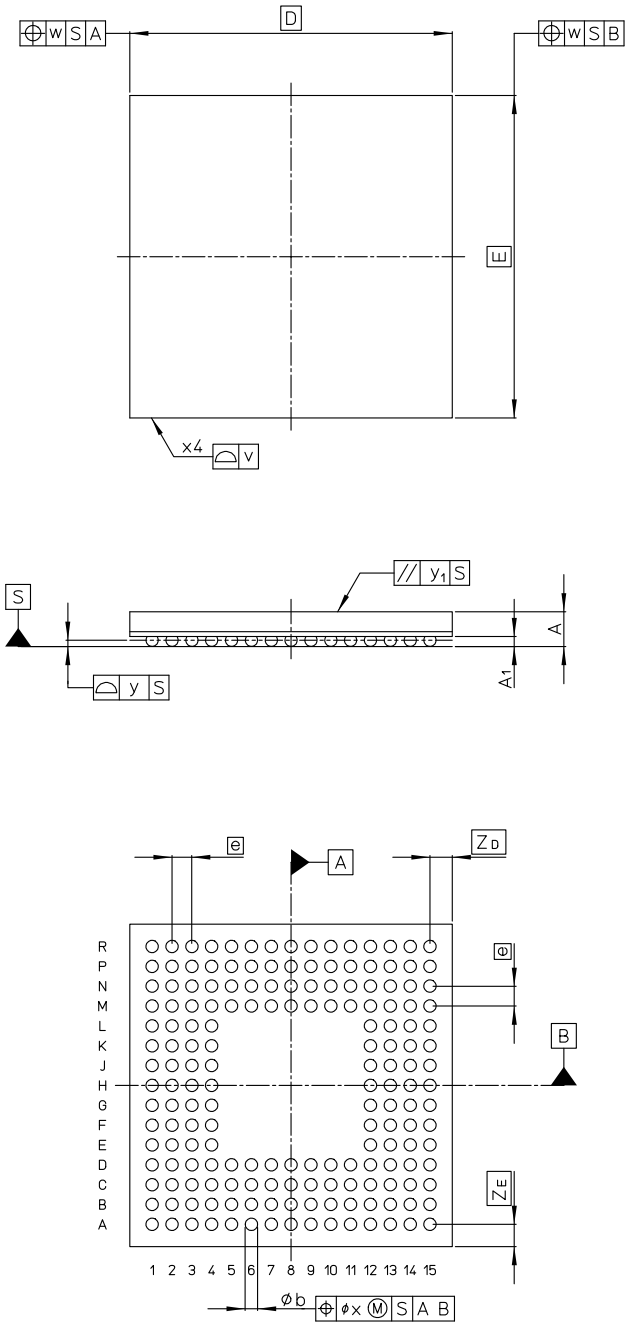

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 12.9 | 13.0 | 13.1 |
| E | 12.9 | 13.0 | 13.1 |
| A | — | — | 1.40 |
| $A_1$ | 0.30 | 0.35 | 0.40 |
| e | — | 0.80 | — |
| b | 0.40 | 0.45 | 0.50 |
| $x_1$ | — | — | 0.15 |
| $x_2$ | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.20 |
| n | — | 224 | — |
| $Z_D$ | — | 0.90 | — |
| $Z_E$ | — | 0.90 | — |

Figure A 224-Pin LFBGA (PLBG0224GA-A)



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| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-A | BP-176/BP-176V | 0.45g |



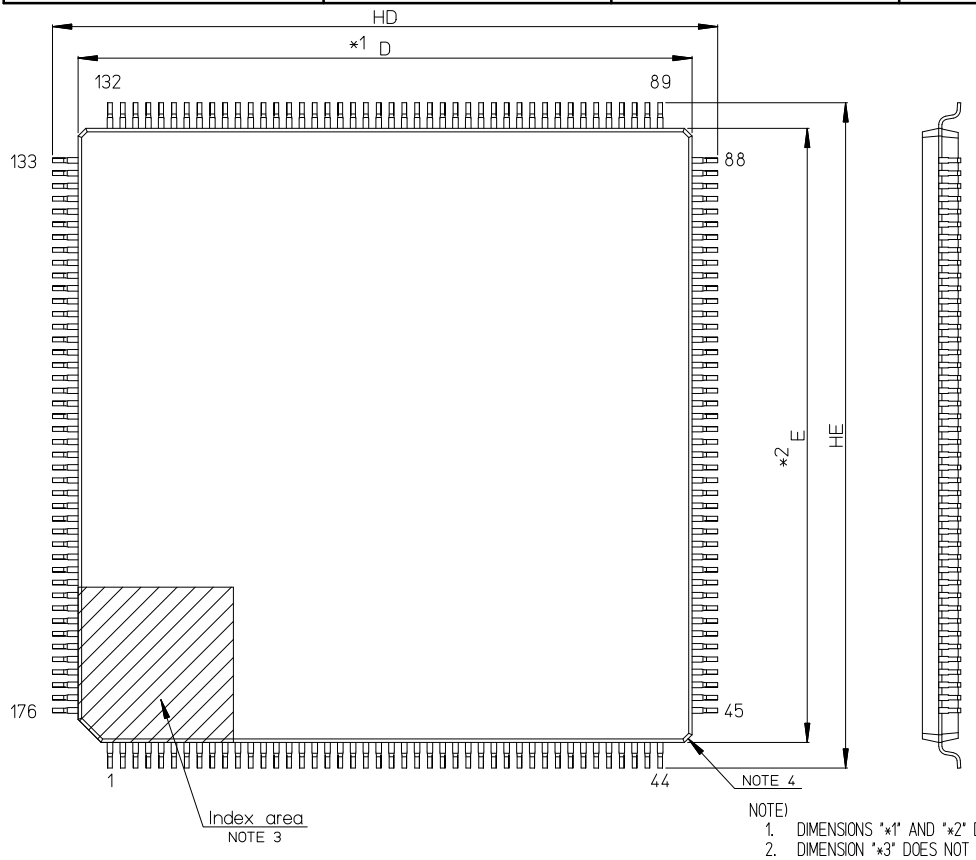

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 13.0 | — |
| E | — | 13.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.90 | — |
| $Z_E$ | — | 0.90 | — |

Figure B 176-Pin LFBGA (PLBG0176GA-A)

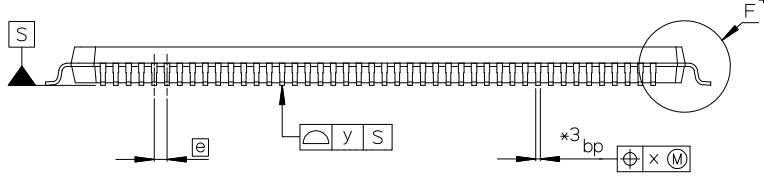


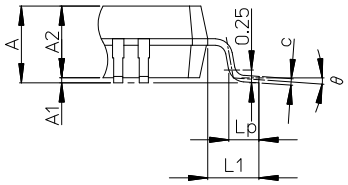
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| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP176-24x24-0.50 | PLQP0176KB-C | —— | 1.8g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.




Detail F

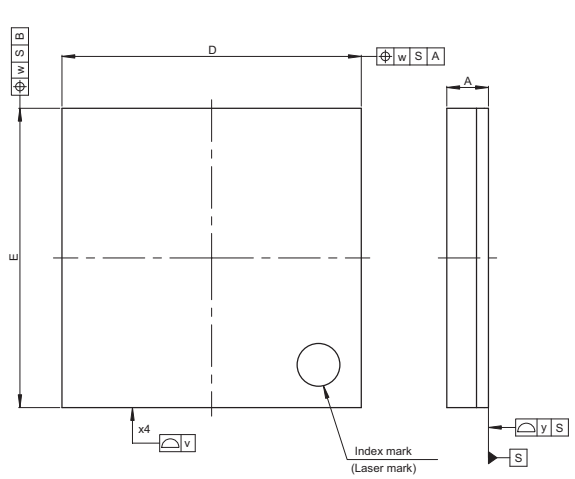
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 23.8 | 24.0 | 24.2 |
| E | 23.8 | 24.0 | 24.2 |
| A2 | —— | 1.4 | —— |
| HD | 25.8 | 26.0 | 26.2 |
| HE | 25.8 | 26.0 | 26.2 |
| A | —— | —— | 1.7 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.15 | 0.20 | 0.27 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.5 | —— |
| x | —— | —— | 0.08 |
| y | —— | —— | 0.08 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

Figure C 176-Pin LFQFP (PLQP0176KB-C)



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| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA145-7x7-0.50 | PTLG0145KA-A | 145F0G | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.5 | — |
| b | 0.21 | 0.25 | 0.29 |
| $b_1$ | 0.29 | 0.34 | 0.39 |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 0.5 | — |
| $Z_E$ | — | 0.5 | — |

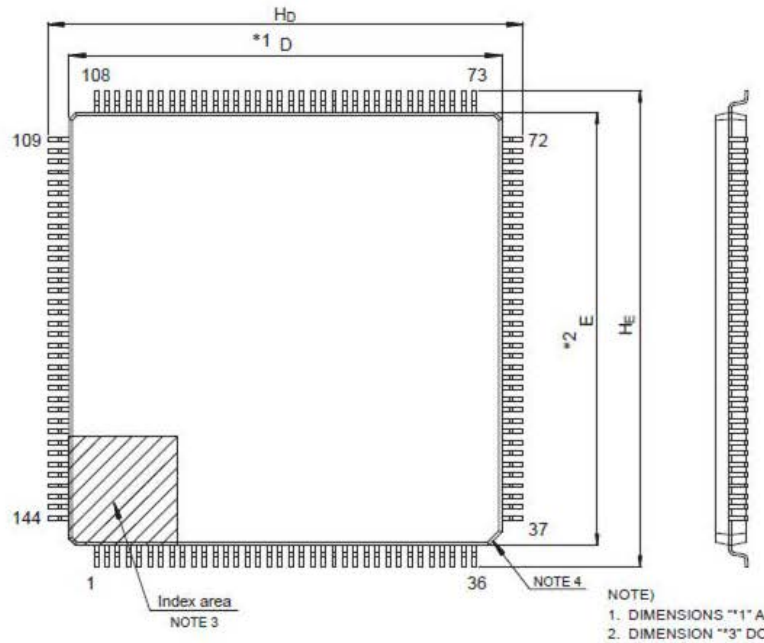
Figure D 145-Pin TFLGA (PTLG0145KA-A)

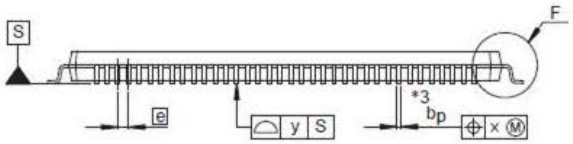


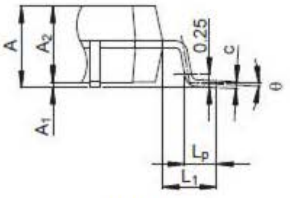
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| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP144-20x20-0.50 | PLQP0144KA-B | — | 1.2 |

Unit: mm




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

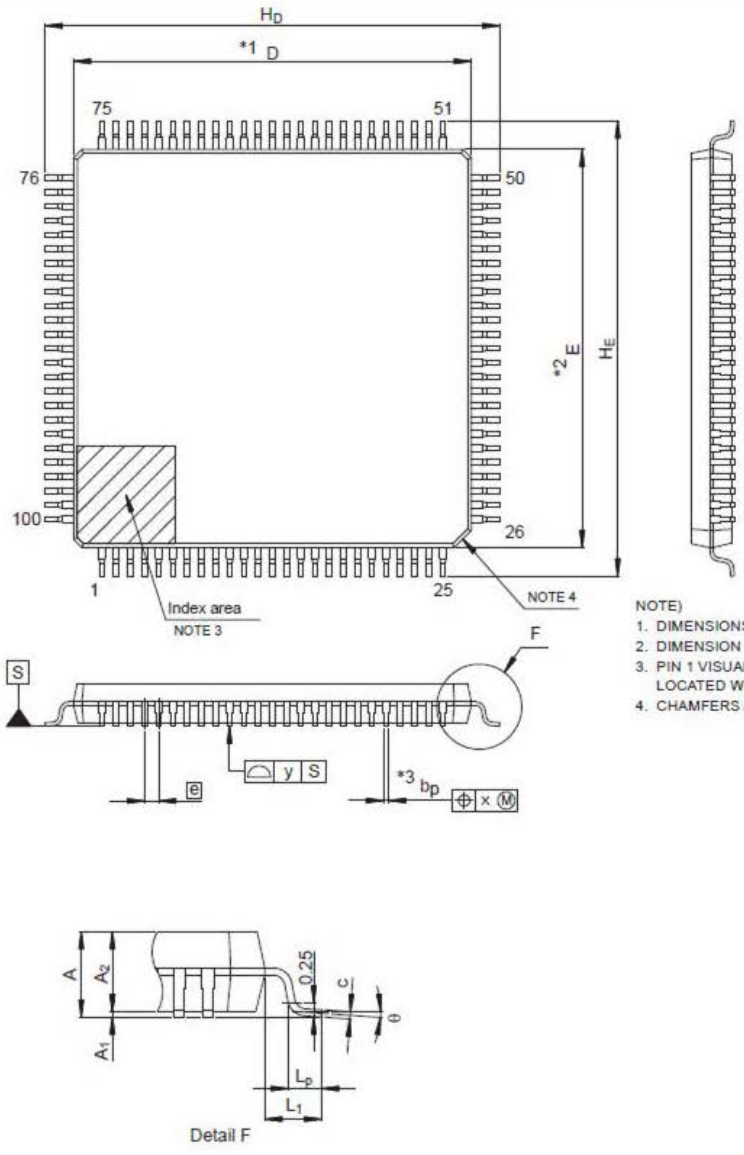
Figure E 144-Pin LFQFP (PLQP0144KA-B)



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| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

Figure F 100-Pin LFQFP (PLQP0100KB-B)



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| REVISION HISTORY | RX66N Group Datasheet |
|---|---|

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.00 | May 31, 2019 | — | First edition, issued | |
| 1.11 | Feb 26, 2021 | 1. Overview | | |
| | | 15, 16 | Table 1.3 List of Products, changed | |
| | | 2. Electrical Characteristics | | |
| | | 82, 83 | Table 2.6 DC Characteristics (3), Note 3, changed | TN-RX*-A0221A/E |
| | | 91 | Table 2.18 HOCO Clock Timing, changed | |
| | | 98 | Table 2.26 Bus Timing, Conditions 1, Conditions 2, changed | TN-RX*-A0244A/E |
| | | 101 | Figure 2.21 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized), changed | |
| | | 102 | Figure 2.23 External Bus Timing/Page Write Cycle (Bus Clock Synchronized), changed | |
| | | 111 | Table 2.27 EXDMAC Timing, Conditions, changed | |
| | | 112 to 151 | 2.4.7 Timing of On-Chip Peripheral Modules, order of tables changed | |
| | | 115 | Figure 2.41 MTU Clock Input Timing, changed | TN-RX*-A0244A/E |
| | | 119 | Figure 2.51 Output Disable Time of POEG in Response to the Oscillation Stop Detection, changed | |
| | | 123 | Figure 2.56 Simple IIC Bus Interface Input/Output Timing, added | |
| | | 148 | Table 2.48 GLCDC Timing, changed | |
| 1.20 | Nov 15, 2023 | 1. Overview | | |
| | | 12 | Table 1.1 Outline of Specifications (11/11), changed | TN-RX*-A0252A/E |
| | | 2. Electrical Characteristics | | |
| | | 79 | Table 2.2 Recommended Operating Conditions (1), changed | TN-RX*-A0252A/E |
| | | | Table 2.3 Recommended Operating Conditions (2), changed | TN-RX*-A0273A/E |
| | | 80 | Table 2.4 DC Characteristics (1), changed | TN-RX*-A0252A/E |
| | | 82, 83 | Table 2.6 DC Characteristics (3), changed | |
| | | 92 | Table 2.20 Sub-Clock Timing, changed | |
| | | 93 | Table 2.21 CLKOUT Pin Output Timing, changed | |
| | | | Table 2.22 CLKOUT25M Pin Output Timing, changed | |
| | | 161 | Table 2.60 Battery Backup Function Characteristics, changed | |
| | | 162 | Table 2.61 Code Flash Memory Characteristics, changed | TN-RX*-A0251A/E |
| | | 163 | Table 2.62 Data Flash Memory Characteristics, changed | |



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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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