REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R039-92. – sbr	91-11-13	M. A. Frye
B	Drawing updated to reflect current requirements. Editorial changes throughout. – drw	01-05-21	Raymond Monnin
C	Add case outline T. - drw	03-01-21	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																				
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SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
David H. Johnson

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-05-11

REVISION LEVEL
C

MICROCIRCUITS, LINEAR, 9 BIT A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88532**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E189-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88532	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TDC1049	9-Bit A/D converter

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	68	quad flatpack
U	CQCC2-J68	68	J-lead chip carrier
X	CDIP1-T64	64	dual-in-line
Y	See figure 1	64	dual-in-line
Z	CQCC1-N68	68	square leadless chip carried

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{EED} to D_{GND}	+0.5 V dc to -7.0 V dc
V_{EEA} to A_{GND}	+0.5 V dc to -7.0 V dc
V_{EEA} to V_{EED}	+0.5 V dc to -0.5 V dc
A_{GND} to D_{GND}	+1.0 V dc to -1.0 V dc
V_{IN}, V_{RT}, or V_{RB} to A_{GND}	+0.5 V dc to V_{EE}
CONV or $\overline{CONV}$ to D_{GND}	+0.5 V dc to V_{EE}
V_{RT} to V_{RB}	+2.5 V dc to -2.5 V dc
Output short circuit duration	Indefinite
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation, worst case (P_D)	6.07 W
Thermal resistance, junction-to-case (θ_{JC}):	
Cases U, X and Z	See MIL-STD-1835
Case Y	12°C/W
Case T	20°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Digital supply voltage to D_{GND} (V_{EED})	-4.9 V dc to -5.5 V dc
Analog supply voltage to A_{GND} (V_{EEA})	-4.9 V dc to -5.5 V dc
Analog ground voltage to A_{GND} (V_{AGND})	-0.1 V dc to +0.1 V dc
Supply voltage differential (V_{EEA} - V_{EED})	-0.1 V dc to +0.1 V dc
CONV pulse width, low (t_{PWL})	12 ns minimum
CONV pulse width, high (t_{PWH})	15 ns minimum
CONV input voltage, common mode (V_{ICM})	-0.5 V dc to -2.5 V dc
CONV input voltage, differential (V_{IDF})	+0.3 V dc to +1.2 V dc
Most positive reference input (V_{RT}) 1/	-0.1 V dc to +0.1 V dc
Most negative reference input (V_{RB}) 1/	-1.9 V dc to -2.1 V dc
Voltage reference differential (V_{RT} - V_{RB})	1.8 V dc to 2.1 V dc
Input voltage (V_{IN})	V_{RB} to V_{RT}
Operating case temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ V_{RT} must be more positive than V_{RB}, and $V_{RT} – V_{RB}$ must be within the specified range.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Block diagram. The logic diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

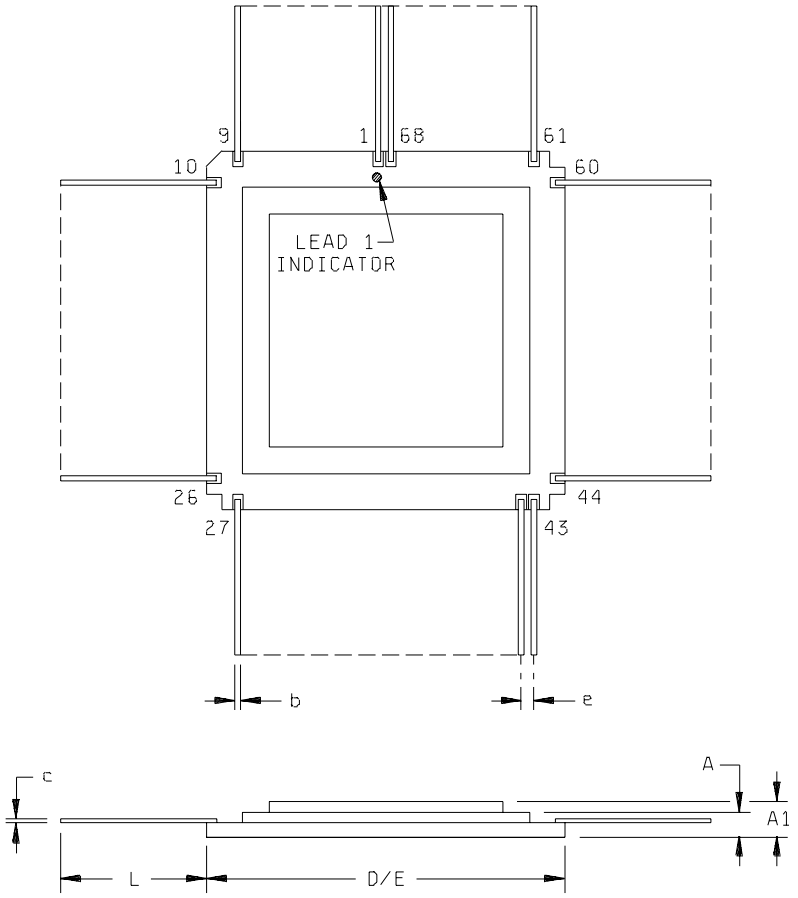
Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current	I_{EE}	$V_{EED} = V_{EEA} = -5.5$ V	1, 2, 3	All		-1090	mA
Reference current	I_{REF}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V, V_{EEA}, $V_{EED} = -5.5$ V	1, 2, 3	All		36	mA
Total reference resistance 2/	R_{REF}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	1, 2, 3	All	56	200	Ω
Input equivalent resistance 2/	R_{IN}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	1, 2, 3	All	16		kΩ
Input capacitance 2/	C_{IN}	$V_{RT} = 0.0$ V, $V_{RB} = -2.0$ V	4, 5, 6			160	pF
Input constant bias current	I_{CB}	$V_{IN} = 0.0$ V, $V_{EEA} = V_{EED} = 5.5$ V	1, 2, 3	All		750	µA
Digital input current (CONV, CONV)	I_I	$V_I = 0.7$ V, $V_{EEA} = V_{EED} = -5.5$ V	1, 2, 3	All		180	µA
Output low voltage	V_{OL}	V_{EEA}, $V_{EED} = -4.9$ V 3/	1, 2, 3	All		-1.5	V
Output high voltage	V_{OH}	V_{EEA}, $V_{EED} = -5.5$ V 3/	1, 2, 3	All	-1.1		V
Digital input capacitance 2/	C_I	$T_A = 25°C$, f = 1.0 MHz	4	All		20	pF
Maximum conversion rate 2/	F_S	V_{EEA}, $V_{EED} = -4.9$ V	4, 5, 6	All	30		MSPS 4/
Functional tests		V_{EEA}, $V_{EED} = -5.2$ V, F_S = 1.0 MSPS (check output coding), see 4.3.1b	7, 8	All			
Sampling time offset 2/	t_{STO}	See figure 5	9, 10, 11	All	-2.0	6.0	ns
Digital output delay	t_D	V_{EEA}, $V_{EED} = -4.9$ V 3/ See figure 5	9, 10, 11	All		31	ns
Digital output hold time	t_{HO}	See figure 5	9, 10, 11	All	3.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Linearity error integral	E_{LI}	V_{RT} = 0.0 V, V_{RB} = -2.0 V, F_S = 100 kHz		4, 5, 6	All		0.2	%
Linearity error, differential	E_{LD}	V_{RT} = 0.0 V, V_{RB} = -2.0 V, F_S = 100 kHz		4, 5, 6	All		0.1	%
Nominal code size	Q	V_{RT} = 0.0 V, V_{RB} = -2.0 V, F_S = 100 kHz		4, 5, 6	All	15	185	%
Offset error, top 2/	E_{OTS}	$V_{IN} = V_{RT}$, R_{TS} connected		1, 2, 3	All		±4.0	mV
	E_{OT}	$V_{IN} = V_{RT}$		1, 2, 3	All	0	+30	
Offset error, bottom 2/	E_{OBS}	$V_{IN} = V_{RB}$, R_{BS} connected		1, 2, 3	All		±4.0	mV
	E_{OB}	$V_{IN} = V_{RB}$		1, 2, 3	All	0	-30	
Temperature coefficient of offset error 2/	$\frac{\Delta E_O}{\Delta T}$	$V_{IN} = V_{RB}$		1, 2, 3	All		20	µV/°C
Bandwidth, full power input 2/	BW			4, 5, 6	All	15		MHz
Signal-to-noise ratio (30 MSPS conversion rate, 10 MHz bandwidth) 2/	SNR	Peak signal/ RMS noise	1.25 MHz input	4, 5, 6	All	57		dB
			5.0 MHz input	4, 5, 6	All	53		
		RMS signal/ RMS noise	1.25 MHz input	4, 5, 6	All	48		
			5.0 MHz input	4, 5, 6	All	44		
Differential phase error 2/	DP	F_S = 4 X NTSC subcarrier		4, 5, 6	All		0.5	degrees
Differential gain error 2/	DG	F_S = 4 X NTSC subcarrier		4, 5, 6	All		1.5	%

1/ Unless otherwise specified, characteristics apply over the recommended operating conditions specified in 1.4 herein.
2/ Guaranteed if not tested.
3/ Test load = 500 ohms to –2.0 V, and 20 pF to ground.
4/ Mega samples per second.

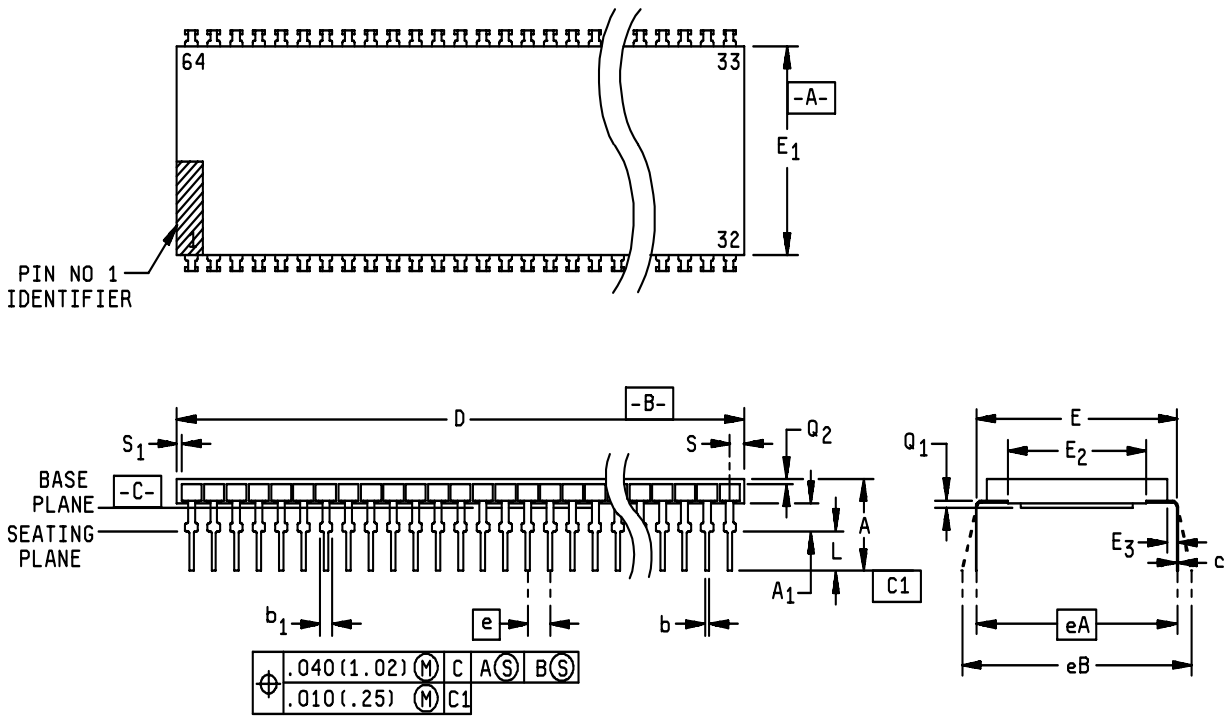


Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.070	0.100	1.778	2.540
A1	0.075	0.115	1.905	2.921
b	0.009	0.015	0.229	0.381
c	0.004	0.008	0.102	0.203
D/E	0.942	0.968	23.93	24.59
e	0.045	0.055	1.143	1.397
L	0.360	0.410	9.144	10.41

NOTES:

1. In case of conflict between the English and metric dimensions, the English dimensions control.

FIGURE 1. Case outline T.



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.110	.225	2.79	5.72	3
A1	.050	.105	1.27	2.67	3
b	.014	.023	0.35	0.58	
b1	.030	.070	0.78	1.78	
c	.007	.015	0.18	0.38	
D	3.170	3.240	80.52	82.30	4
E	.880	.940	22.35	23.88	5
E1	.790	.810	20.07	20.57	4
E2	.640	.680	16.26	17.27	

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
E3	.025	- -	.053	- -	
e	.100 BSC		2.54 BSC		
eA	.900 BSC		22.86 BSC		5
eB	- -	1.050	- -	26.67	6
L	.125	.200	3.17	5.08	3
Q1	.026	.035	0.66	0.89	
Q2	.005	- -	0.13	- -	9
S	.030	.100	0.76	2.54	
S1	.005	.060	0.13	1.52	9

NOTES:

1. In case of conflict between the English and metric dimensions, the English dimensions control.
2. Dimensioning and tolerance per ANSI-Y14.5M-1982.
3. Dimensions A, A1, and L are measured with the package seating in JEDEC Seating Plane Gauge GS-3.
4. D and E1 dimensions include allowance for package irregularities and lid misalignment.
5. E and eA measured with the leads constrained to be perpendicular to plane C.
6. eB measured at the lead tips with the leads unconstrained.
7. Pointed or rounded lead tips are preferred to ease insertion.
8. To facilitate automatic insertion, any raised irregularity on the top surface (step, mass, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
9. Metallization of closest approach (pad or lead) to package edge.

FIGURE 1. Case outline Y - continued.

Device type	01		
Case outline	X	Y	T, U, and Z
Terminal number	Terminal symbol		
1	$\overline{D_8}$	$\overline{D_8}$	$\overline{D_8}$
2	D_7	(LSB)$\overline{D_9}$	D_7
3	$\overline{D_7}$	(LSB)D_9	$\overline{D_7}$
4	D_6	D_{GND}	D_6
5	$\overline{D_6}$	CONV	$\overline{D_6}$
6	$\overline{D_5}$	$\overline{CONV}$	$\overline{D_5}$
7	D_5	D_{GND}	D_5
8	A_{GND}	R_{TS}	NC
9	NC	OFS	A_{GND}
10	NC	R_T	NC
11	V_{EED}	NC	NC
12	NC	V_{IN}	NC
13	NC	A_{GND}	V_{EED}
14	V_{EEA}	A_{GND}	V_{EEA}
15	NC	V_{IN}	NC
16	NC	V_{IN}	V_{EEA}
17	V_{EEA}	R_M	NC
18	NC	V_{IN}	V_{EEA}
19	V_{EEA}	A_{GND}	NC
20	NC	A_{GND}	V_{EEA}
21	NC	NC	V_{EEA}
22	V_{EED}	V_{IN}	V_{EED}
23	NC	NC	NC
24	NC	R_B	NC
25	A_{GND}	R_{BS}	NC
26	NC	D_{GND}	NC
27	NC	D_{GND}	A_{GND}
28	D_4	$\overline{OVF}$	NC
29	$\overline{D_4}$	$\overline{OVF}$	NC
30	$\overline{D_3}$	(MSB)D_1	NC
31	D_3	(MSB)$\overline{D_1}$	$\overline{D_4}$
32	$\overline{D_2}$	D_2	D_4
33	D_2	$\overline{D_2}$	$\overline{D_3}$
34	(MSB)$\overline{D_1}$	D_3	D_3

Device type	01		
Case outline	X	Y	T, U, and Z
Terminal number	Terminal symbol		
35	(MSB)D_1	$\overline{D_3}$	$\overline{D_2}$
36	OVF	D_4	D_2
37	OVF	D_4	(MSB)D_1
38	D_{GND}	NC	(MSB)D_1
39	D_{GND}	NC	$\overline{OVF}$
40	R_{BS}	A_{GND}	OVF
41	R_B	NC	D_{GND}
42	NC	NC	NC
43	V_{IN}	V_{EED}	R_{BS}
44	NC	NC	R_B
45	A_{GND}	NC	NC
46	A_{GND}	V_{EEA}	V_{IN}
47	V_{IN}	NC	NC
48	R_M	V_{EEA}	A_{GND}
49	V_{IN}	NC	A_{GND}
50	V_{IN}	NC	V_{IN}
51	A_{GND}	V_{EEA}	NC
52	A_{GND}	NC	R_M
53	V_{IN}	NC	V_{IN}
54	NC	V_{EED}	V_{IN}
55	R_T	NC	A_{GND}
56	OFS	NC	NC
57	R_{TS}	A_{GND}	A_{GND}
58	D_{GND}	D_5	V_{IN}
59	$\overline{CONV}$	$\overline{D_5}$	R_T
60	CONV	D_6	NC
61	D_{GND}	$\overline{D_6}$	OFS
62	(LSB)D_9	D_7	R_{TS}
63	(LSB)D_9	$\overline{D_7}$	$\overline{CONV}$
64	$\overline{D_8}$	D_8	CONV
65	- - -	- - -	D_{GND}
66	- - -	- - -	(LSB)$\overline{D_9}$
67	- - -	- - -	(LSB)D_9
68	- - -	- - -	$\overline{D_8}$

FIGURE 2. Terminal connections.

V_{IN}	OVF	D_1(MSB) – D_9(LSB)
+0.0039 V	1	000000000
0.0000 V	0	000000000
-0.0039 V	0	000000001
•	•	•
•	•	•
•	•	•
-0.9980 V	0	011111111
-1.0020 V	0	100000000
-1.0059 V	0	100000001
•	•	•
•	•	•
•	•	•
-1.9961 V	0	111111110
-2.0000 V	0	111111111

NOTE:

1. Voltages are code midpoints.

FIGURE 3. Truth table.

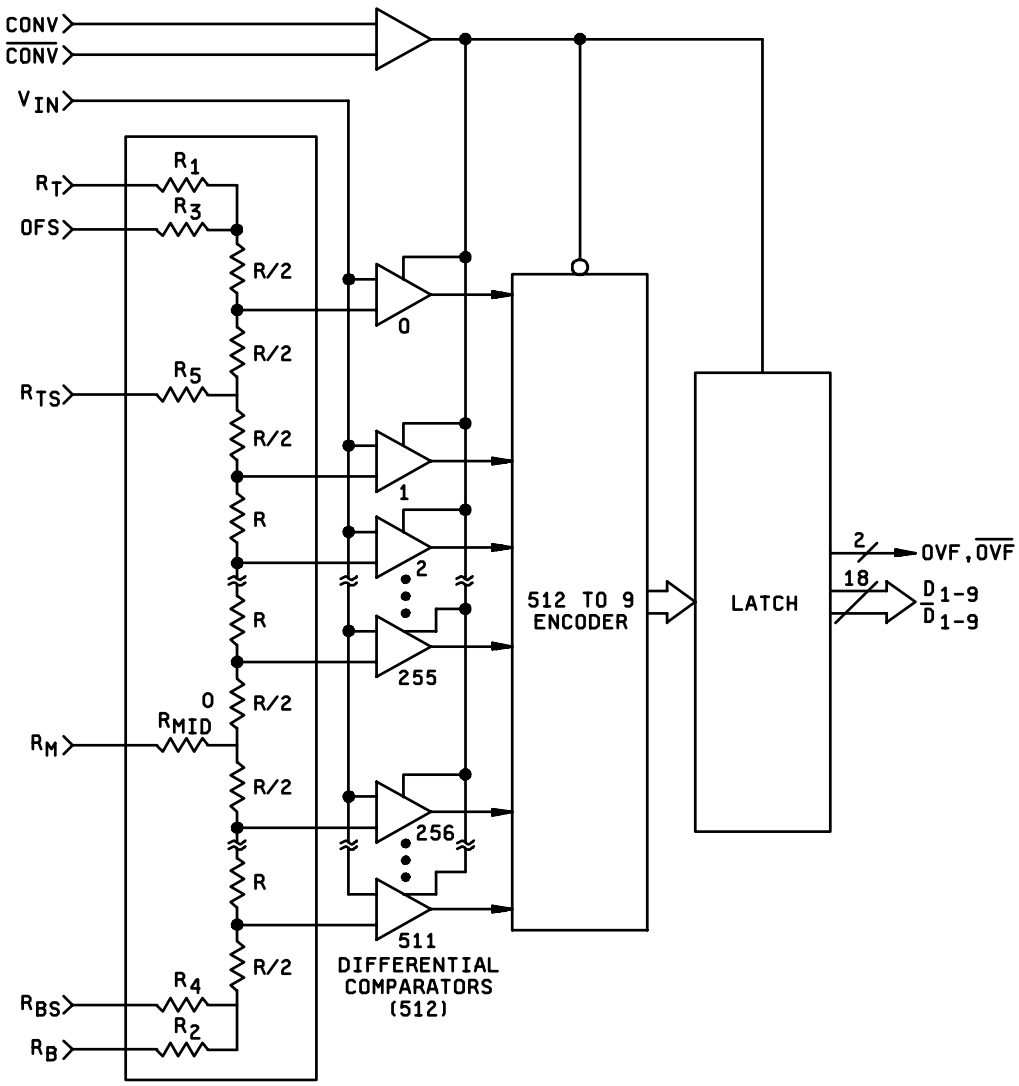


FIGURE 4. Block diagram.

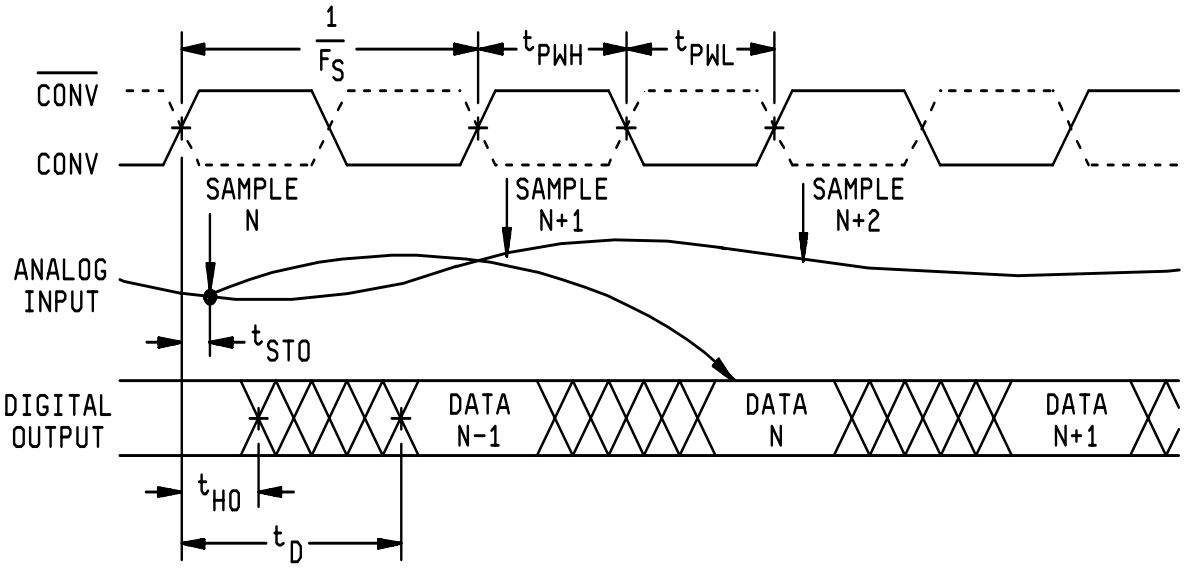


FIGURE 5. Timing diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 4, 7, 9
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 4, 7, 9

* PDA applies to subgroup 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-01-21

Approved sources of supply for SMD 5962-88532 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8853201TC	0C7V7	TDC1049/TC
5962-8853201UA	0C7V7	TDC1049L1V
5962-8853201XA	0C7V7	TDC1049J0V
5962-8853201YA	0C7V7	TDC1049J3V
5962-8853201ZA	0C7V7	TDC1049C1V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	Qualified Parts Laboratory, Inc. 3605 Kifer Road Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.