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NTE7131
Integrated Circuit
DC–Coupled Vertical Deflection Circuit

Description:
The NTE7131 is an integrated circuit in a 9–Lead SIP type package designed for use in 90° and 110° color deflection systems for field frequencies of 50 to 120Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

Features:
- Few External Components
- Highly Efficient Fully DC–Coupled Vertical Output Bridge Circuit
- Vertical Flyback Switch
- Guard Circuit
- Protection Against:
  - Short–Circuit of the Output Pins (7 and 4)
  - Short–Circuit of the Output Pins to V_P
- Temperature (Thermal) Protection
- High EMC Immunity because of Common Mode Inputs
- A Guard Signal in Zoom Mode

Absolute Maximum Ratings:

DC Supply

Supply Voltage, V_P
- Non–Operating 40V
- Operating 25V

Flyback Supply Voltage, V_{FB} 50V

Vertical Circuit

Output Current (Peak–to–Peak Value, Note 1), $I_{O(p–p)}$ 2A
Output Voltage (Pin7), $V_{O(A)}$ 52V

Flyback Switch

Peak Output Current, I_M . . . . ±1.5A

Thermal Data

Virtual Junction Temperature, T_{VJ} . . . . +150°C
Operating Ambient Temperatrure Range, T_A . . . . –25° to +75°C
Storage Temperature Range, T_{stg} . . . . –55° to +150°C
Thermal Resistance, Virtual Junction–to–Ambient (In Free Air), R_{thVJA} 40K/W
Thermal Resistance, Virtual Junction–to–Case, R_{thVJC} 4K/W
Short–Circuiting Time (Note 2), t_{sc} . . . . 1 Hour

Note 1. I_O maximum determined by current protection.
Note 2. Up to V_P = 18V.

Electrical Characteristics: (V_P = 14.5V, T_A = +25°C, V_{FB} = 45V, f_i = 50Hz, $I_{I(sb)}$ = 400μA unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Supply						
Operating Supply Voltage	V_P		9.0	4.5	25.0	V
Flyback Supply Voltage	V_{FB}		V_P	–	50	V
Supply Current	I_P	No Signal, No Load	–	30	55	mA
Vertical Circuit						
Output Voltage Swing (Scan)	V_O	I_{diff} = 0.6mA$_{(p–p)}$, V_{diff} = 1.8V$_{(p–p)}$, I_O = 2A$_{(p–p)}$	13.2	–	–	V
Linearity Error	LE	I_O = 2A$_{(p–p)}$, Note 3	–	1	4	%
		I_O = 50mA$_{(p–p)}$, Note 3	–	1	4	%
Output Voltage Swing (Flyback) $V_{O(A)} – V_{O(B)}$	V_O	I_{diff} = 0.3mA, I_O = 1A (M)	–	40	–	V
Forward Voltage of the Internal Efficiency Diode ($V_{O(A)} – V_{FB}$)	V_{DF}	I_O = –1A (M), I_{diff} = 0.3mA	–	–	1.5	V
Output Offset Current	$\|I_{OS}\|$	I_{diff} = 0, $I_{I(sb)}$ = 50 to 500μA	–	–	40	mA
Offset Voltage at the Input of the Feedback Amplifier ($V_{I(fb)} – V_{O(B)}$)	$\|V_{OS}\|$	I_{diff} = 0, $I_{I(sb)}$ = 50 to 500μA	–	–	24	mV
Output Offset Voltage as a Function of Temperature	$\Delta V_{OS}T$	I_{diff} = 0	–	–	72	μV/K
DC Output Voltage	$V_{O(A)}$	I_{diff} = 0, Note 4	–	6.5	–	V
Open–Loop Voltage Gain ($V_{7–4}/V_{1–2}$)	G_{vo}	Note 5, Note 6	–	80	–	dB
Open–Loop Voltage Gain ($V_{7–4}/V_{9–4}$, $V_{1–2}$ = 0)		Note 5	–	80	–	dB
Voltage Ratio $V_{1–2}/V_{9–4}$	V_R		–	0	–	dB
Frequency Response (–3dB)	f_{res}	Open Loop, Note 7	–	40	–	Hz
Current Gain (I_O/I_{diff})	G_I		–	5000	–	
Current Gain Drift as a Function of Temperature	ΔG_cT		–	–	10^{-4}	K
Signal Bias Current	$I_{I(sb)}$		50	400	500	μA
Flyback Supply Current	I_{FB}	During Scan	–	–	100	μA
Power Supply Ripple Rejection	PSRR	Note 8	–	80	–	dB
DC Input Voltage	$V_{I(DC)}$		–	2.7	–	V
Common Mode Input Voltage	$V_{I(CM)}$	$I_{I(sb)}$ = 0	0	–	1.6	V
Input Bias Current	I_{bias}	$I_{I(sb)}$ = 0	–	0.1	0.5	μA
Common Mode Output Current	$I_{O(CM)}$	$\Delta I_{I(sb)}$ = 300μA$_{(p–p)}$, f_i = 50Hz, I_{diff} = 0	–	0.2	–	mA
Guard Circuit						
Output Current	I_O	Not Active, $V_{O(guard)}$ = 0V	–	–	50	μA
		Active, $V_{O(guard)}$ = 4.5V	1.0	–	2.5	mA
Output Voltage on Pin8	$V_{O(guard)}$	I_O = 100μA	–	–	5.5	V
Allowable Voltage on Pin8		Maximum Leakage Current = 10μA	–	–	40	V

Notes:

Note 3. The linearity error is measured without S–correction and based on the same measurement principle as performed on the screen. The measuring method is as follows:
Divide the output signal $I_4 – I_7$ (V_{RM}) into 22 equal parts ranging from 1 to 22 inclusive. Measure the value of two succeeding parts called one block starting with part 2 and 3 (block 1) and ending with part 20 and 22 (block 10). Thus part 1 and 22 are unused. The equation for linearity error for adjacent blocks (LEAB) and not adjacent blocks (NAB) are given below

$$\text{LEAD} = \frac{a_k - a_{(k+1)}}{a_{avg}} \text{ ; NAB} = \frac{a_{max} - a_{min}}{a_{avg}}$$

Note 4. Related to V_P.

Niote 5. V values within formulae, relate to voltages at or between relative pin numbers, i.e. $V_{7–4}/V_{1–2}$ = voltage value across pins 7 and 4 divided by voltage value across pins 1 and 2.

Note 6. $V_{9–4}$ AC short–circuited.

Note 7. Frequency response $V_{7–4}/V_{9–4}$ is equal to frequency response $V_{7–4}/V_{1–2}$.

Note 8. At $V_{(ripple)}$ = 500mV eff; measured across R_M; f_i = 50Hz.

Functional Description:

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with devices that deliver symmetrical current signals. An external reisitor (R_{CON}) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: I_{diff} x R_{CON} = I_{coil} x R_M. The output current is adjustable from $0.5A_{(p–p)}$ to $2A_{(p–p)}$ by varying R_M. The maximum input differential voltage is 1.8V. In the application it is recommended that V_{diff} = 1.5V (Typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_P optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- Thermal Protection
- Short–Circuit Protection of the Output Pins (Pin4 and Pin7)
- Short–Circuit of the Output pins to V_P.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at tghe following conditions:

- During Flyback
- During Short–Circuit of the Coil and During Short–Circuit of the Output Pins (Pin4 and Pin7) to V_P or GND
- During Open Loop
- When the Thermal Protection is Activated

This signal can be used for blanking the picture tube screen.

Pin Connection Diagram
(Front View)