DC–65 GHz GaAs Broadband MMIC Amplifier with on–chip PLFX Bias–T

MMA035AA

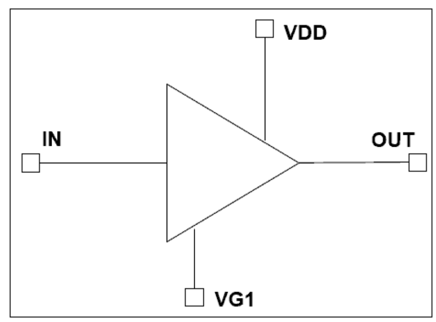
Product Overview

The MMA035AA is a DC–65 GHz, Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) pseudomorphic High-Electron Mobility Transistor (pHEMT) amplifier. Nominally biased at 6V and 120 mA, the amplifier offers a gain of 10 dB, P1dB of 16 dBm at 50 GHz, and is ideal for test instrumentation and EW applications requiring instantaneously wide bandwidth. The amplifier MMIC has an on-chip Bias-T network allowing for smooth operation from 10 GHz to 65 GHz. For operation below 10 GHz an external choke network should be used. The MMA035AA amplifier is DC coupled and features RF I/Os that are nominally matched to 50Ω.

Key Features

- Frequency range: DC to 65 GHz
- Gain: 10 dB
- High power: 13 dBm at 65 GHz
- Supply: 6V at 120 mA
- Integrated On-chip Bias-T
- 50Ω matched input/output
- Die size: 1.64 mm × 0.92 mm × 0.1 mm

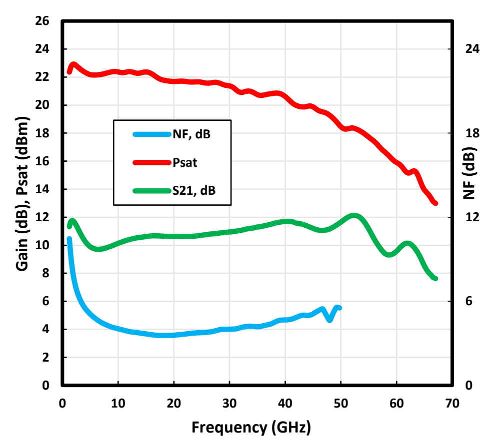
Functional Block Diagram



Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

Performance Curves



Performance Overview

Parameter	Typ.	Units
Operational frequency range	DC–65	GHz
Gain	10	dB
Noise figure	4.5	dB
P1dB at 50 GHz	16	dBm
P_{sat} at 50 GHz	17	dBm
IM3 at 50 GHz and 10 dBm	–25	dBc
Current at +6V supply	120	mA

Export Classification: 3A001.b.2.d

Table of Contents

1. Electrical Specifications

1.1. Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, V_{DD} = 6V, I_{DD} = 120 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		DC		65	GHz
Gain	DC–20 GHz	9	10		dB
	20 GHz–40 GHz	10	11		
	40 GHz–65 GHz	8	10		
Gain flatness	DC–20 GHz		±1		dB
	20 GHz–40 GHz		±1		
	40 GHz–65 GHz		±2		
Noise figure	3 GHz–20 GHz		4.5	8	dB
	20 GHz–40 GHz		4.5	6	
Input return loss	DC–20 GHz	16	17		dB
	20 GHz–40 GHz	16	17		
	40 GHz–65 GHz	9	12		
Output return loss	DC–20 GHz	10	15		dB
	20 GHz–40 GHz	15	16		
	40 GHz–65 GHz	7	10		
P1dB	DC–20 GHz	19	20		dB
	20 GHz–40 GHz	18	19		
	40 GHz–65 GHz	10	16		
P_{sat}	DC–20 GHz	20	21		dBm
	20 GHz–40 GHz	19	21		
	40 GHz–65 GHz	11	17		
OIP3	DC–20 GHz	30	31		dBm
	20 GHz–40 GHz	29	30		
	40 GHz–65 GHz	20	26		
V_{DD} (drain voltage supply)			6	8	V
I_{DD} (drain current)			120		mA

1.2. Absolute Maximum Ratings

Table 1-2 shows the absolute maximum ratings of the MMA035AA device at 25 °C, unless otherwise specified. Exceeding any of the maximum ratings could potentially cause damage and/or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	8V
Gate bias voltage (V_G)	–2V to 0.5V
RF input power (Pin)	20 dBm
Channel temperature	+165 °C
V_{DD} Current (I_{DD})	150 mA
DC power dissipation (T = 85 °C)	1.2W (8V × 150 mA)
Thermal resistance	20 °C/W
Storage temperature	–65 °C to +150 °C
Operating temperature	–55 °C to +85 °C


ESD Sensitive Device

1.3. Typical Performance Curves

1.3.1. Typical Performances vs. Temperature

The graphs shown in Figures 1-1 through 1-31 represent the typical performance versus temperature curves of the MMA035AA device under specific bias conditions. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-1. Gain vs. Temperature at 5V/100 mA

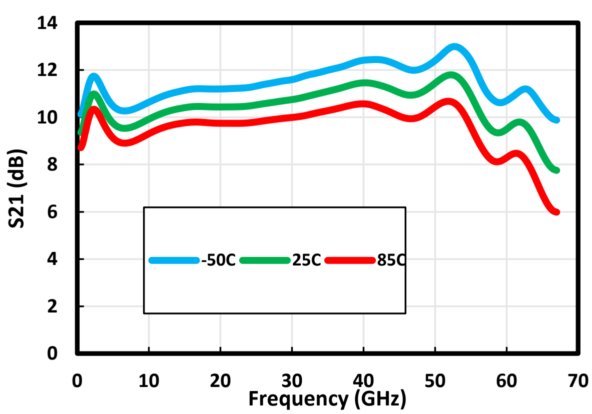


Figure 1-2. Gain vs. Temperature at 6V/120 mA

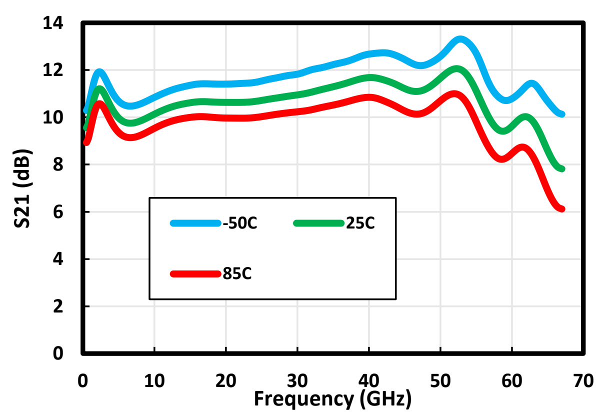


Figure 1-3. Gain vs. Temperature at 7V/150 mA

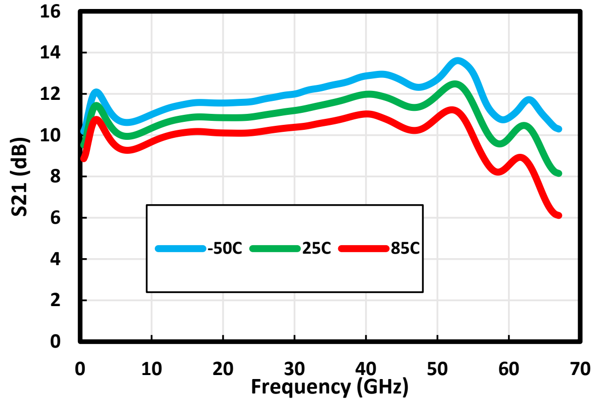


Figure 1-4. Gain vs. Temperature at 8V/150 mA

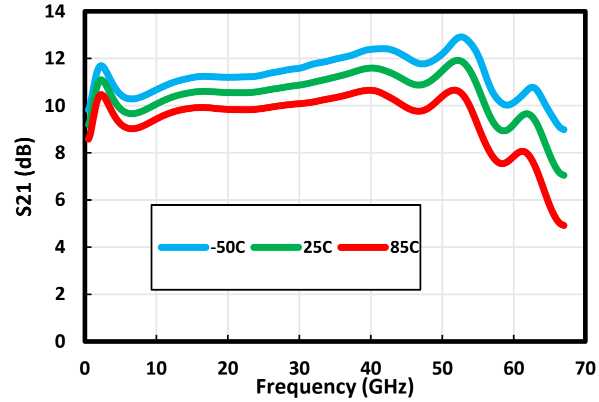


Figure 1-5. S11 vs. Temperature at 5V/100 mA

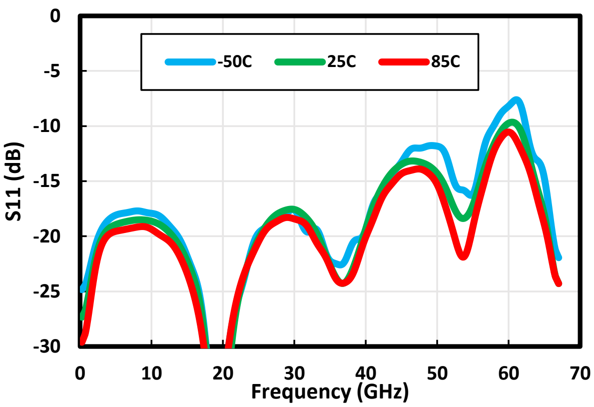


Figure 1-6. S11 vs. Temperature at 6V/120 mA

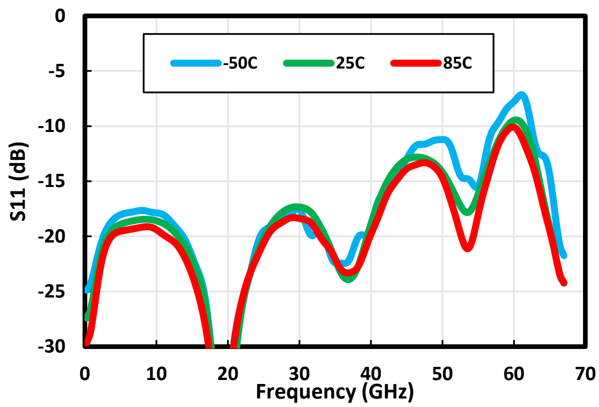


Figure 1-7. S11 vs. Temperature at 8V/150 mA

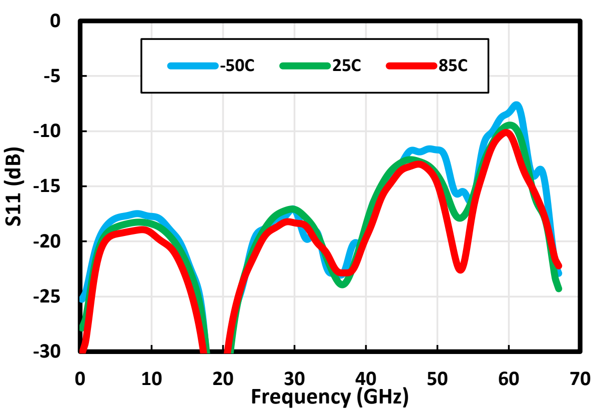


Figure 1-8. S22 vs. Temperature at 5V/100 mA

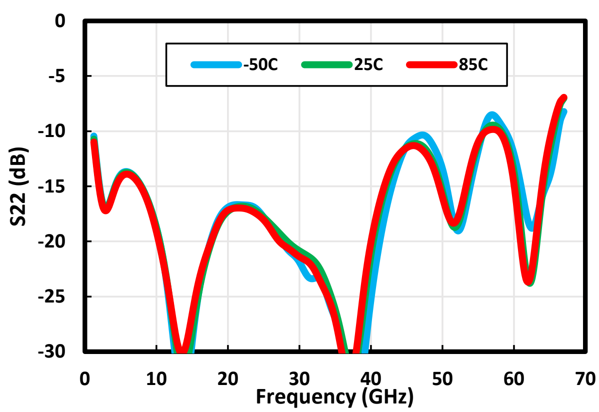


Figure 1-9. S22 vs. Temperature at 6V/120 mA

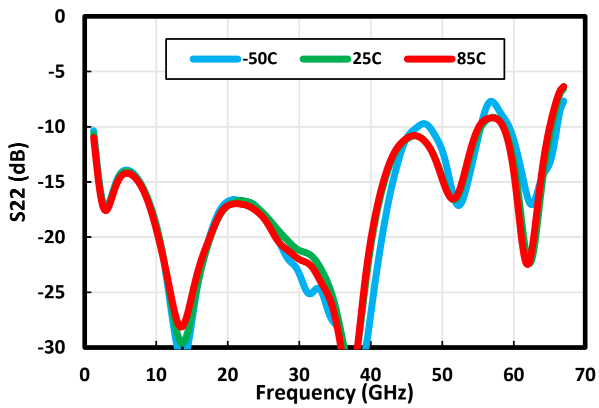


Figure 1-10. S22 vs. Temperature at 8V/150 mA

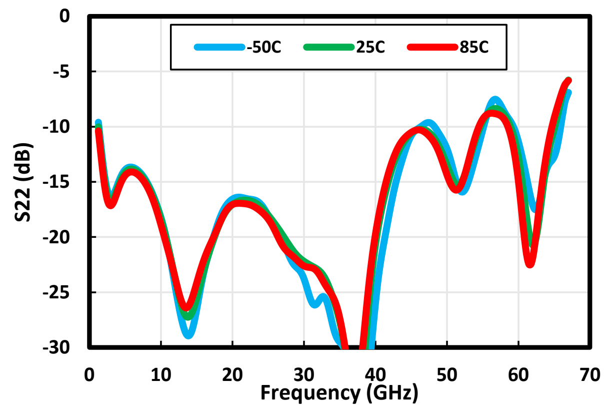


Figure 1-11. S12 vs. Temperature at 5V/100 mA

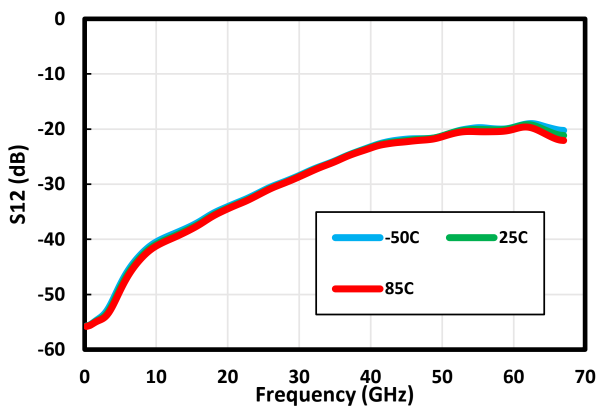


Figure 1-12. S12 vs. Temperature at 8V/150 mA

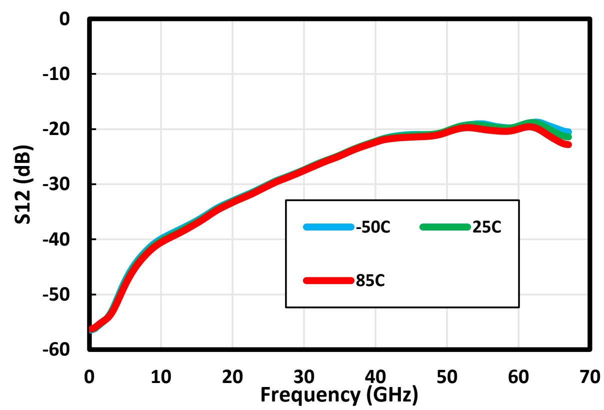


Figure 1-13. NF vs. Temperature at 5V/100 mA

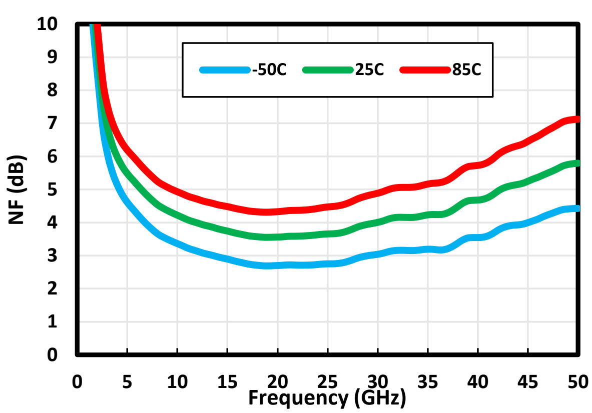


Figure 1-14. NF vs. Temperature at 7V/120 mA

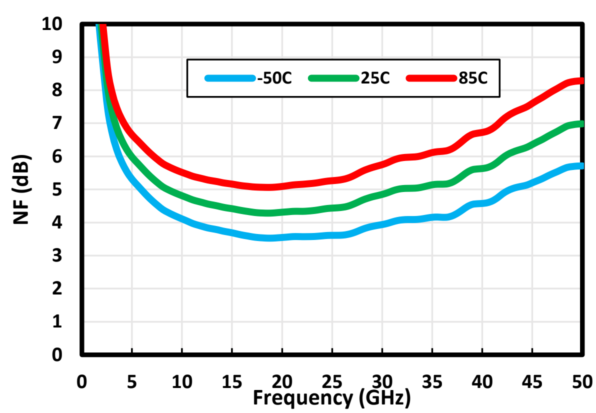


Figure 1-15. NF vs. Temperature at 8V/150 mA

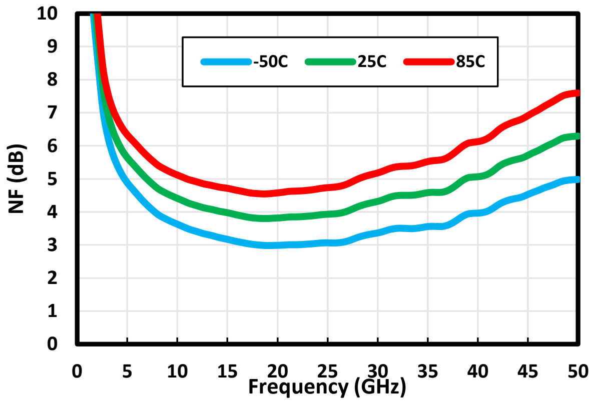


Figure 1-16. P1dB vs. Temperature at 5V/100 mA

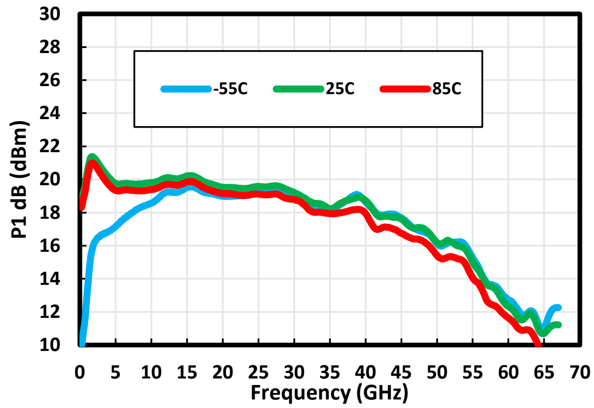


Figure 1-17. P1dB vs. Temperature at 6V/120 mA

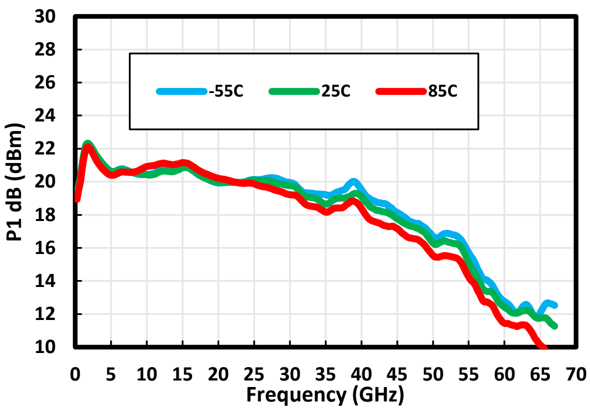


Figure 1-18. P1dB vs. Temperature at 7V/140 mA

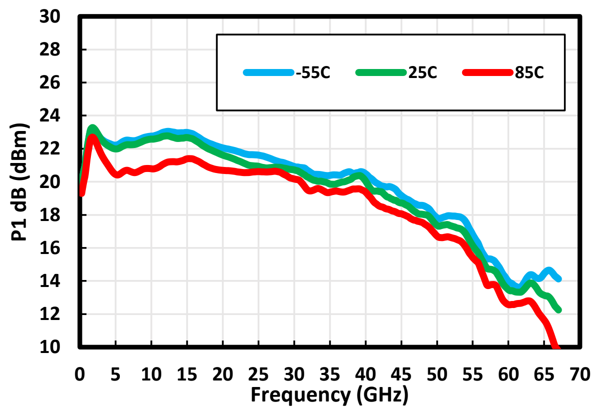


Figure 1-19. P1dB vs. Temperature at 8V/150 mA

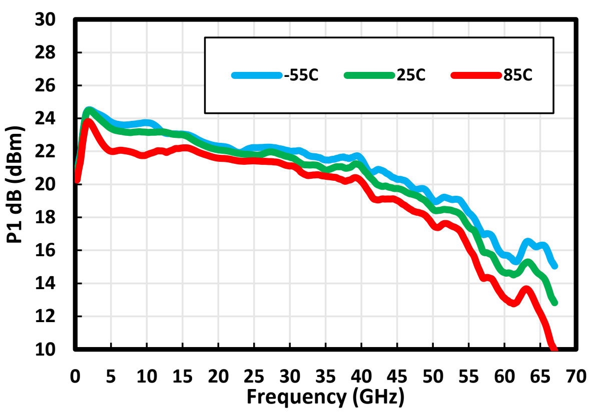


Figure 1-20. P_{sat} vs. Temperature at 5V/100 mA

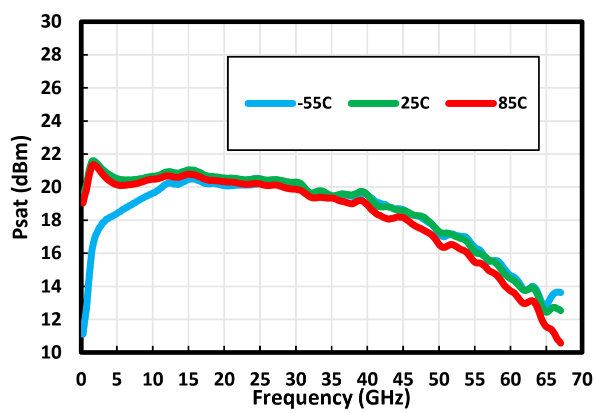


Figure 1-21. P_{sat} vs. Temperature at 6V/120 mA

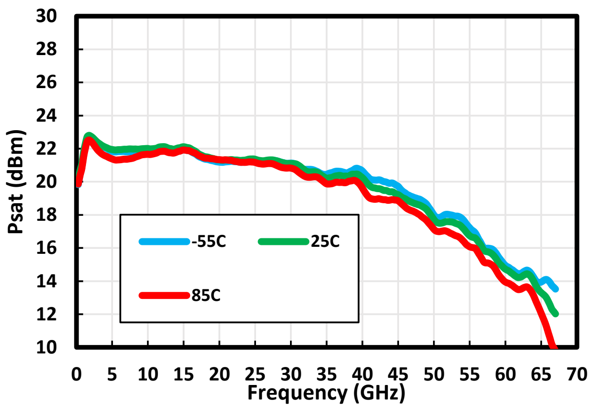


Figure 1-22. P_{sat} vs. Temperature at 7V/140 mA

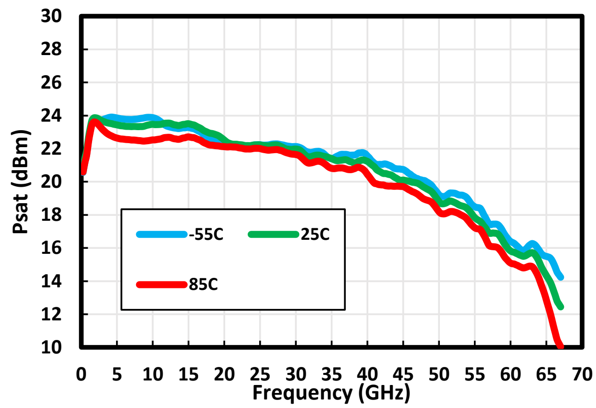


Figure 1-23. P_{sat} vs. Temperature at 8V/150 mA

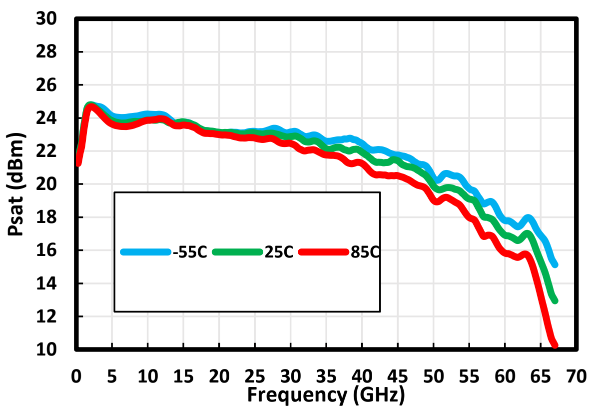


Figure 1-24. OIP2 vs. Temperature at 5V/100 mA

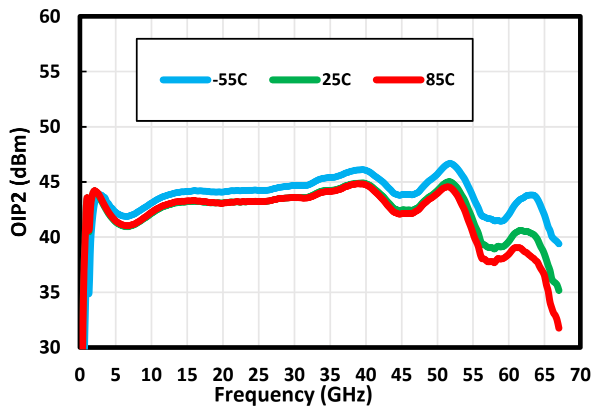


Figure 1-25. OIP2 vs. Temperature at 6V/120 mA

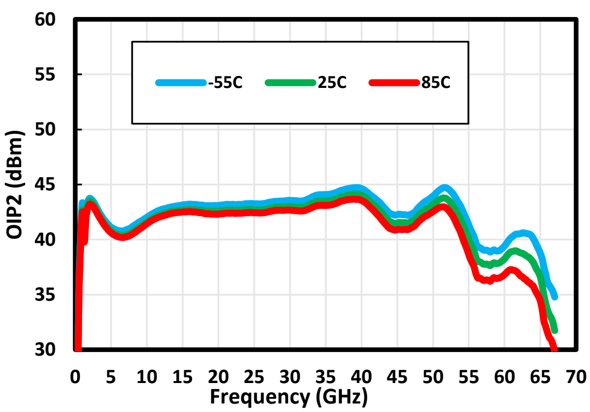


Figure 1-26. OIP2 vs. Temperature at 7V/140 mA

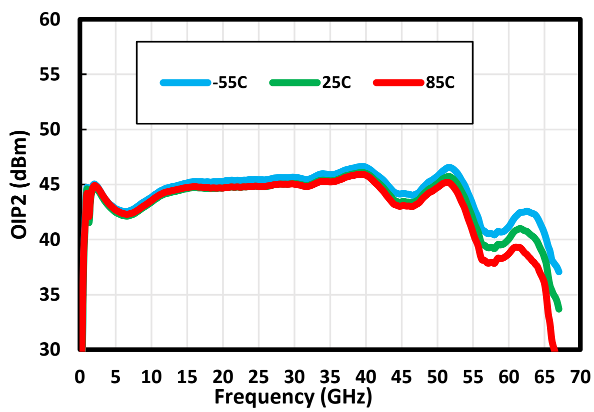


Figure 1-27. OIP2 vs. Temperature at 8V/150 mA

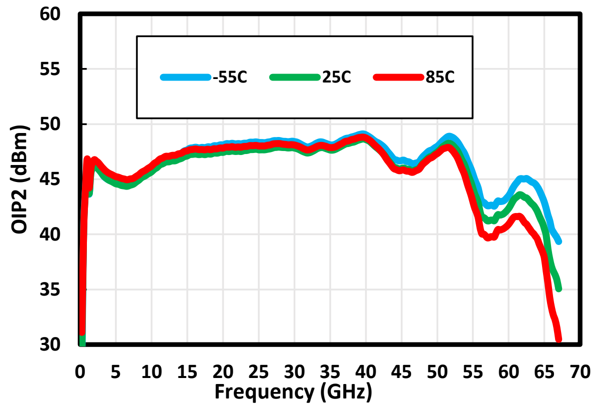


Figure 1-28. IM3 vs. Temperature at 5V/100 mA, 10 dBm (per tone)

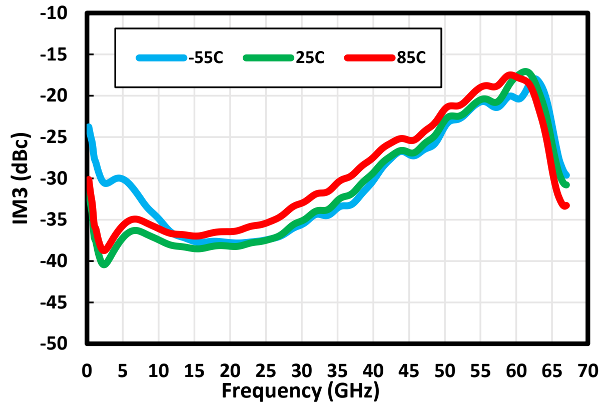


Figure 1-29. IM3 vs. Temperature at 6V/120 mA, 10 dBm (oer tone)

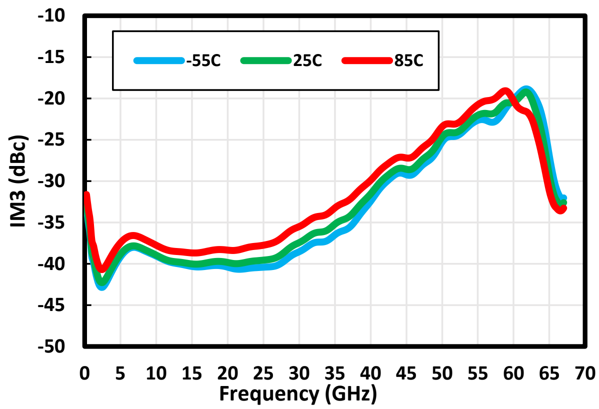


Figure 1-30. IM3 vs. Temperature at 7V/120 mA, 10 dBm (per tone)

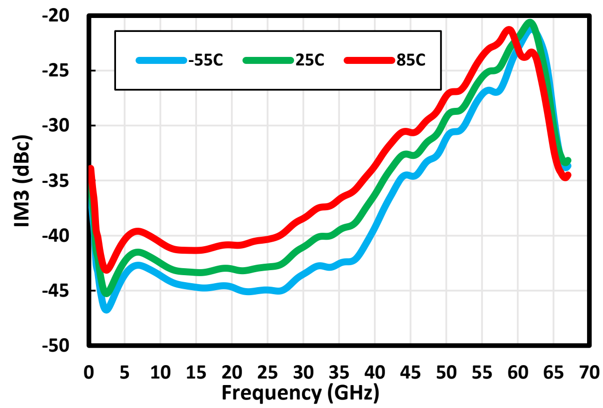
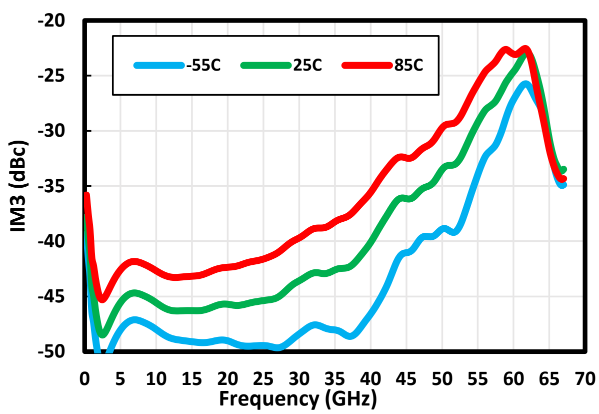


Figure 1-31. IM3 vs. Temperature at 8V/150 mA 10 dBm (per tone)



1.3.2. Typical Performances vs. Bias

The graphs shown in Figures 1-32 through 1-44 represent the typical performance versus bias curves of the MMA035AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-32. Gain vs. I_{DD} at 5V

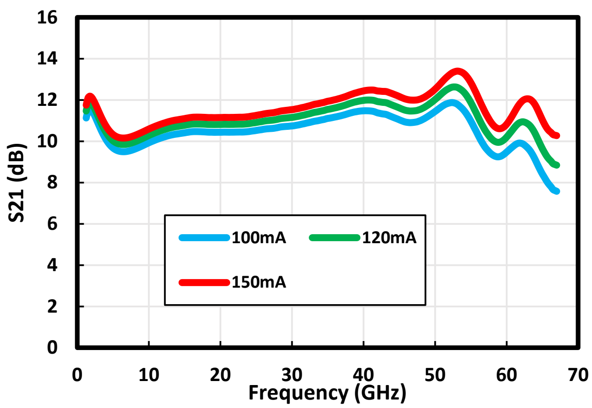


Figure 1-33. Low Band Gain vs. I_{DD} at 6V

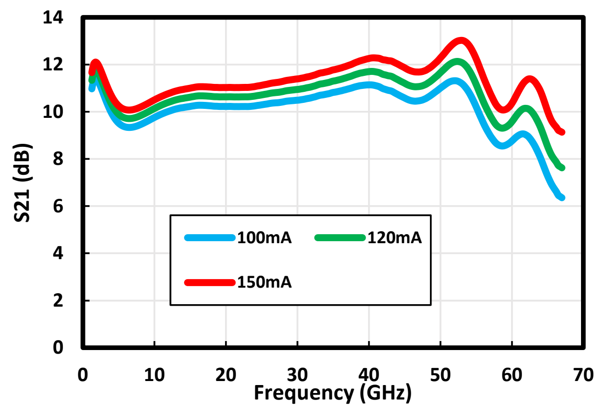


Figure 1-34. Gain vs. I_{DD} at 7V

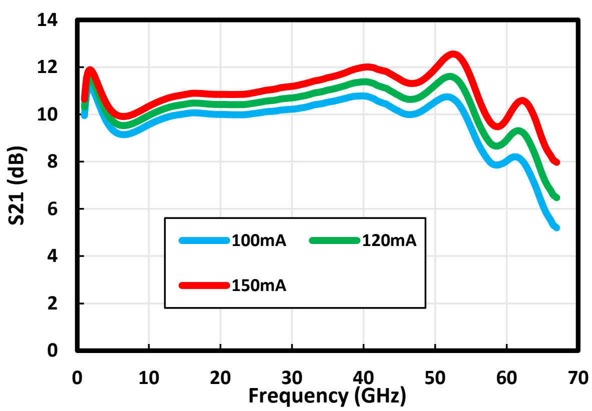


Figure 1-35. Gain vs. I_{DD} at 8V

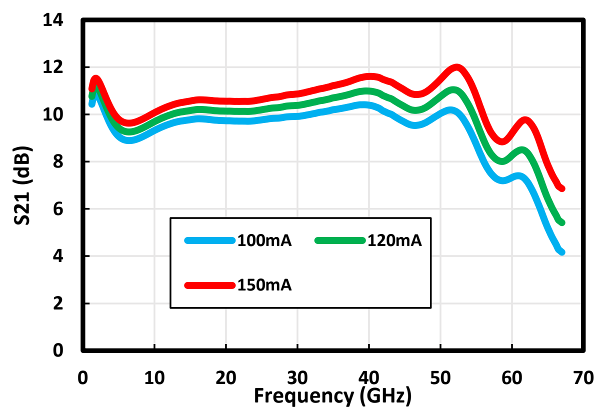


Figure 1-36. NF vs. I_{DD} at 5V

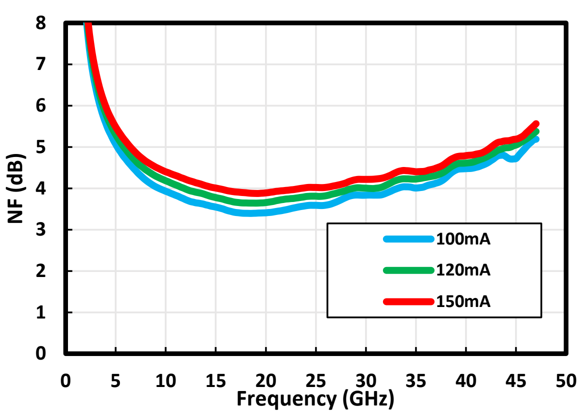


Figure 1-37. NF vs. I_{DD} at 6V

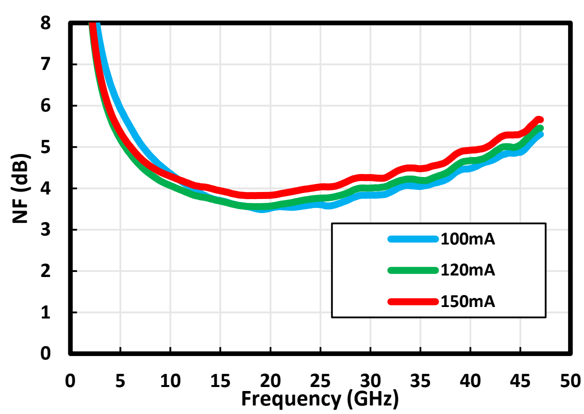


Figure 1-38. NF vs. I_{DD} at 7V

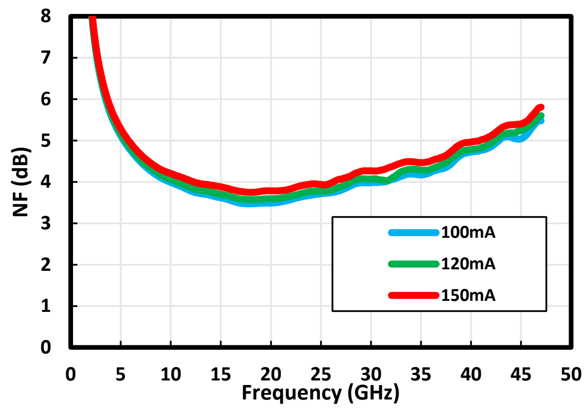


Figure 1-39. NF vs. I_{DD} at 8V

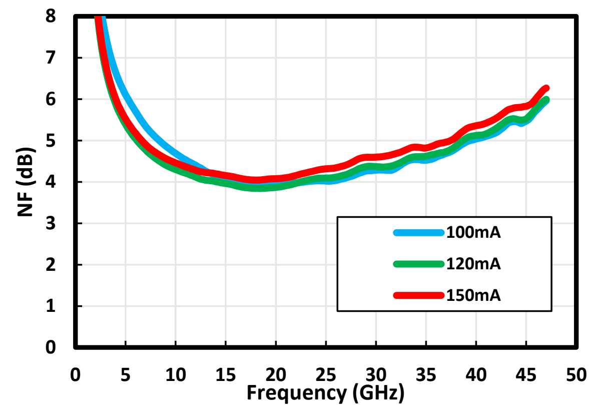


Figure 1-40. P1dB Bias

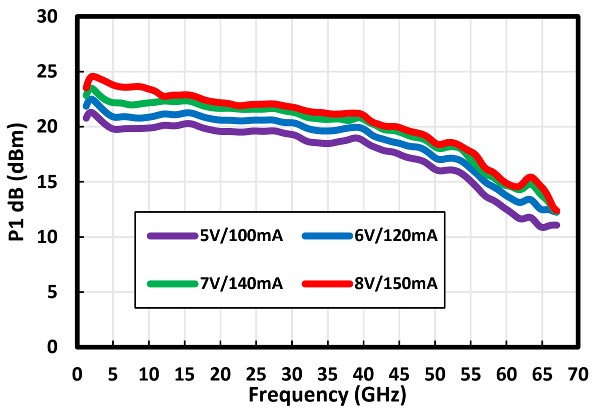


Figure 1-41. P_{sat} vs. Bias

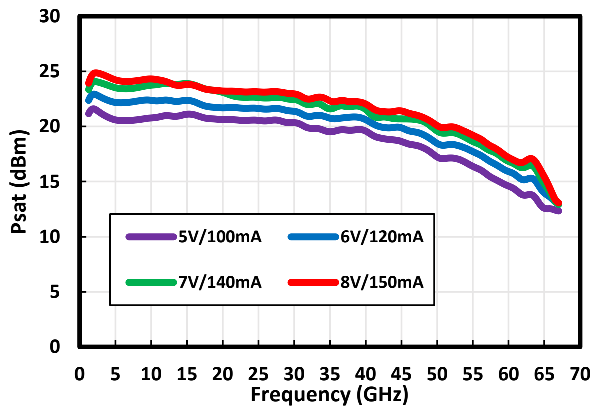


Figure 1-42. OIP3 vs. Bias

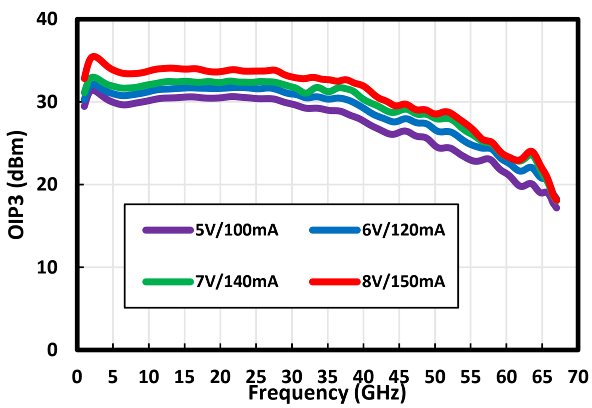


Figure 1-43. IM3 vs. Bias at 10 dBm per tone

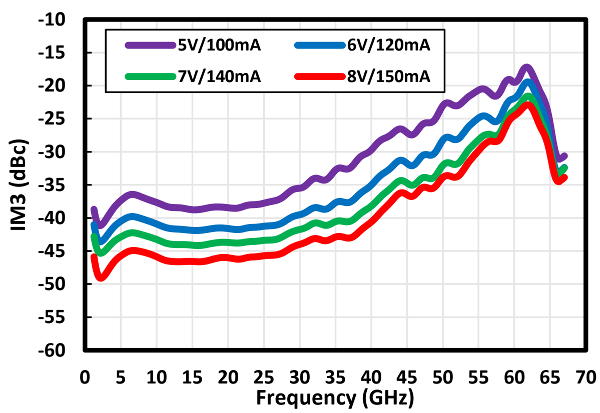
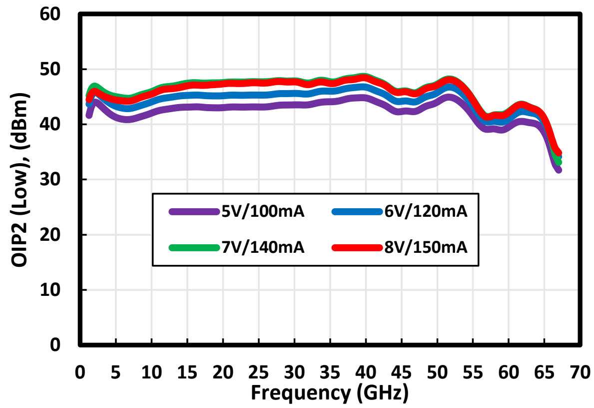


Figure 1-44. OIP2 Low at Δ = 10 MHz vs. Bias



1.3.3. Typical Performances vs. Output Power

The graphs shown in Figures 1-45 through 1-56 represent the typical performance versus output power curves of the MMA035AA under constant temperature of 25 °C. All measurements were taken using the test circuit shown in Figure 3-2.

Figure 1-45. IM2 vs. Power at 5V/100 mA

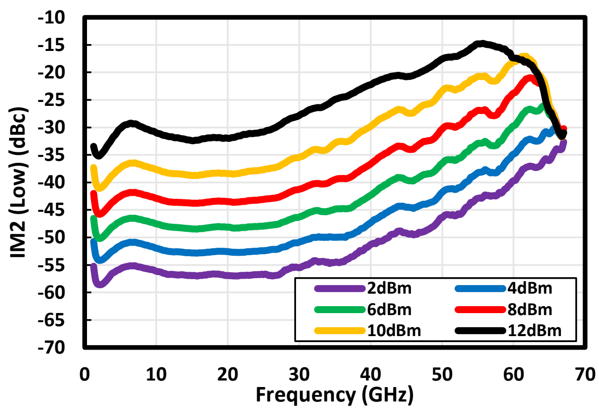


Figure 1-46. IM2 vs. Power at 6V/120 mA

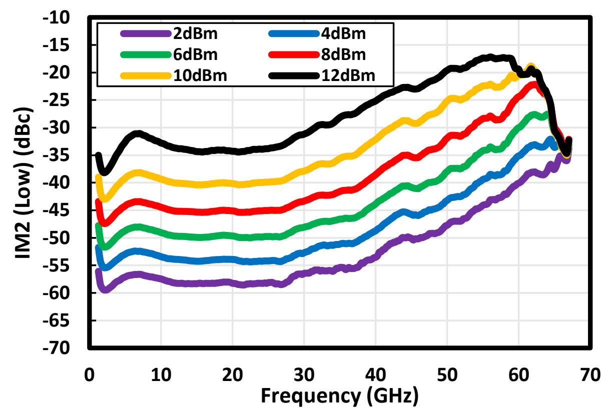


Figure 1-47. IM2 vs. Power at 7V/140 mA

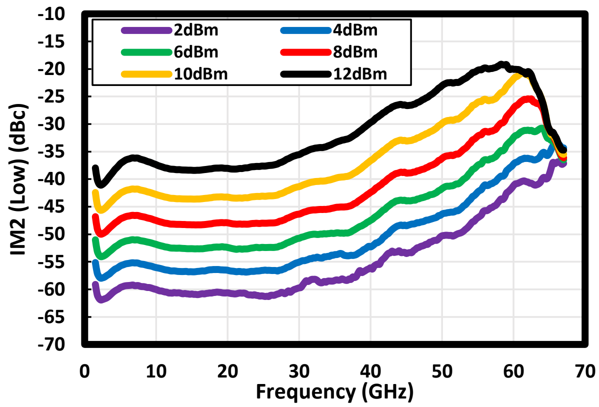


Figure 1-48. IM2 vs. Power at 8V/150 mA

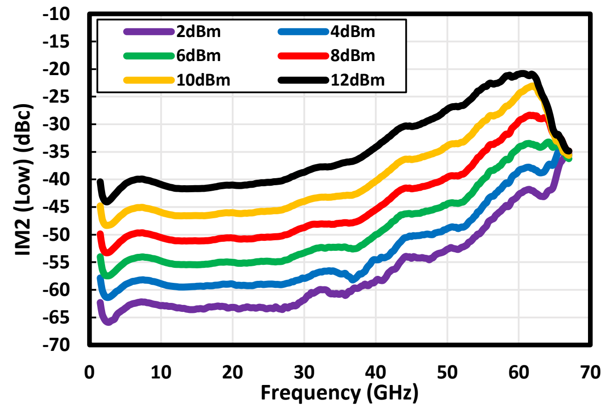


Figure 1-49. IM3 vs. Power at 5V/100 mA

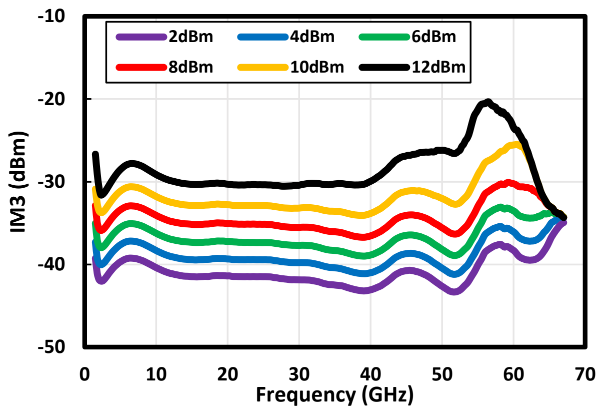


Figure 1-50. IM3 vs. Power at 6V/120 mA

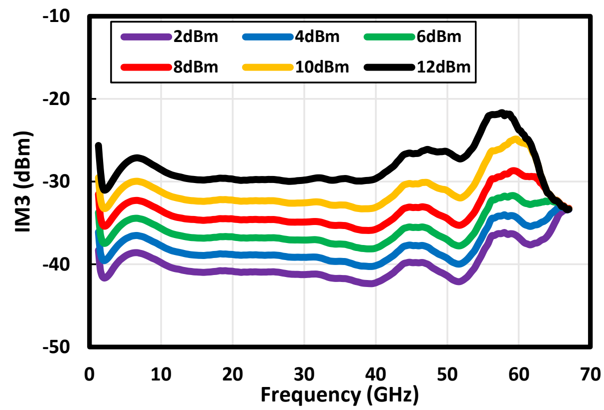


Figure 1-51. IM3 vs. Power at 7V/140 mA

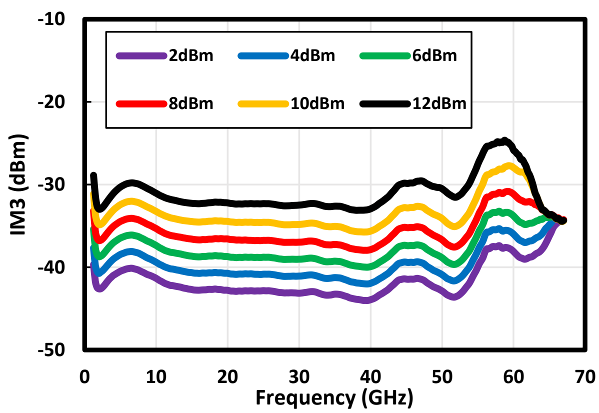


Figure 1-52. IM3 vs. Power at 8V/150 mA

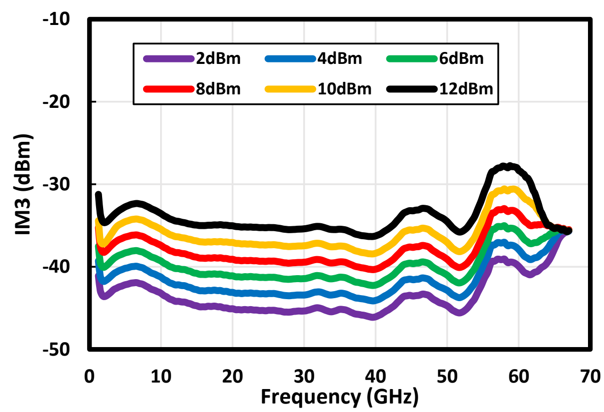


Figure 1-53. 2nd Harmonic vs. Power at 5V/100 mA

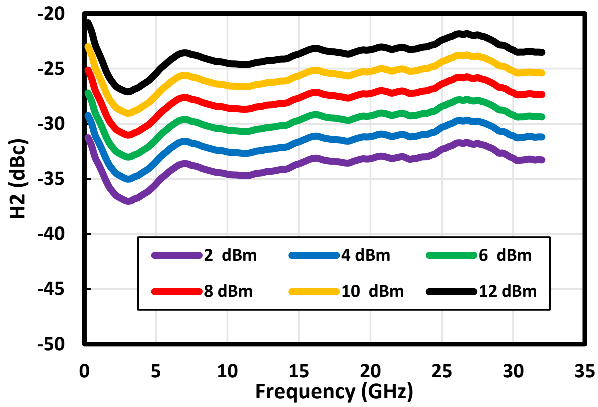


Figure 1-54. 2nd Harmonic vs. Power at 7V/120 mA

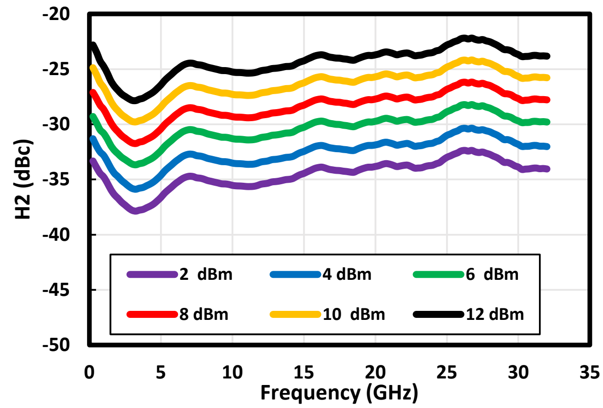
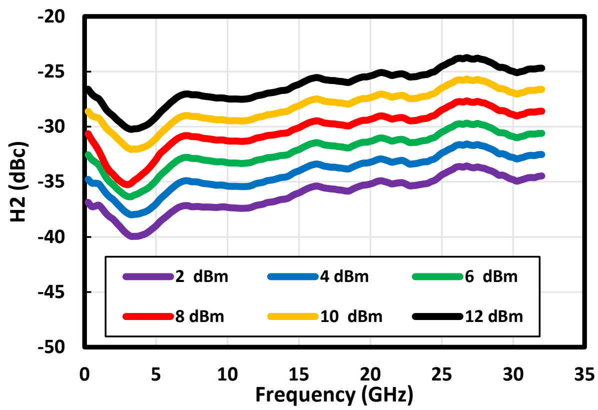
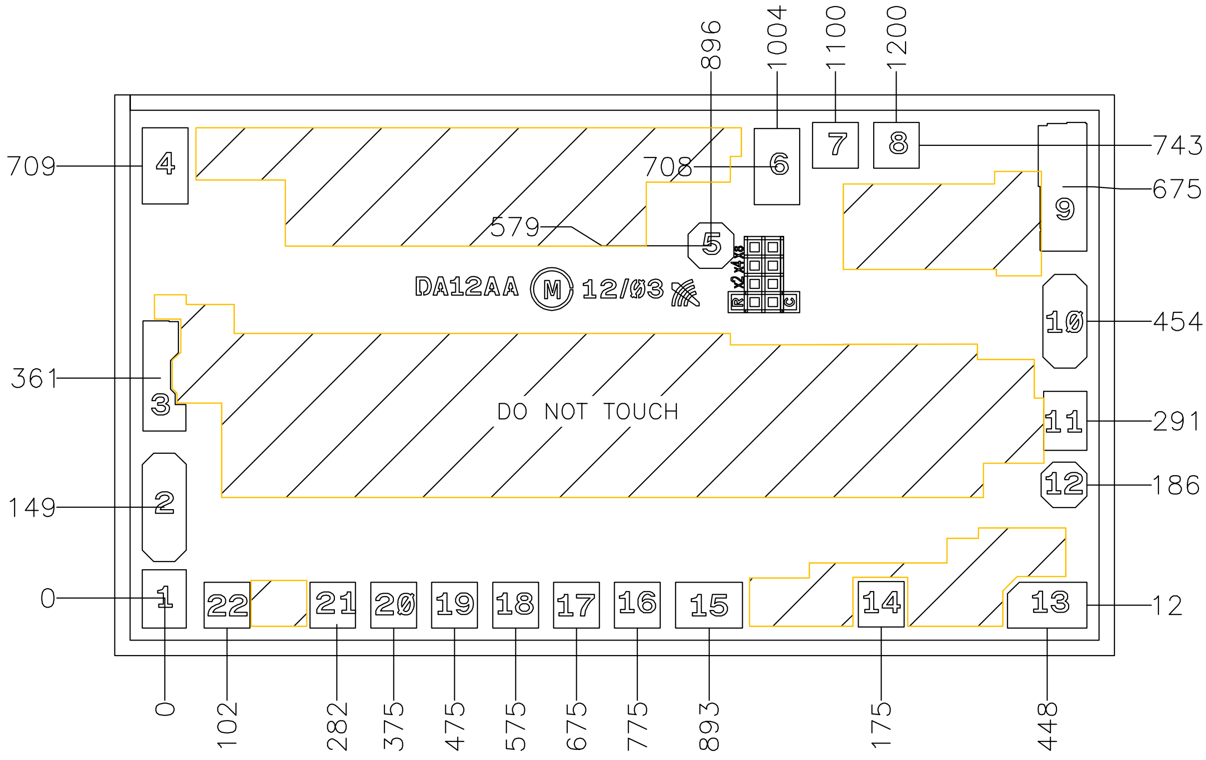


Figure 1-55. 2nd Harmonic vs. Power at 8V/150 mA



2. Die Specifications

Figure 2-1. Die Outline Drawing (µm)



PAD NO.	DESCRIPTION	µm SIZE	PAD NO.	DESCRIPTION	µm SIZE
1	GND	72x96	13	VG1A	130x75
2	RFIN	72x178	14	GND	75x75
3	GND	71x181	15	VG1	110x75
4	1st Drain Termination Bypass	75x125	16	1st Gate Termination Bypass	75x75
5	VDD	75x75	17	1st Gate Termination Bypass	75x75
6	2nd Drain Termination Bypass	75x125	18	1st Gate Termination Bypass	75x75
7	DC Det. Ref.	75x75	19	1st Gate Termination Bypass	75x75
8	RF Det	75x75	20	1st Gate Termination Bypass	75x75
9	GND	76x210	21	VTF	75x75
10	RFOUT	72x154	22	GND	75x75
11	GND	71x97			
12	VG2	75x75			

Table 2-1. I/O Description

Pad Number	Pad Name	Pad Description (Effective Pad Size in µm)
2	RF_{IN}	This pad is RF/DC coupled to the FET gates and nominally matched to 50Ω.
10	RF_{OUT}	This pad is RF/DC coupled to the FET drains and nominally matched to 50Ω.
4, 6	V_{D1}, V_{D2}	V_{D1} ,V_{D2} Low-frequency termination for drain ballast, DC Coupled to the FET drains.
5	V_{DD}	V_{DD} bias pad
7	V_{DREF}	Reference voltage for power detector (at V_{DD} level)
8	V_{DET}	Power detector output
12	V_{G2}	Access to Gate 2 bias.
15, 13	V_{G1}, V_{G1A}	First-gate low-frequency terminations DC coupled to the Gate 1 and used to set the Die Bias Current.
16, 17, 18, 19, 20	V_{G1B}, V_{G1C}, V_{G1D}, V_{G1E}, G1F	Complementary low-frequency terminations for the Gate 1, used to control low-frequency response slope.
21	V_{TF}	Reference diodes triple stack (anode)
1, 3, 9, 11, 14, 22	Ground	Ground connections used for die test purposes; DC/RF Ground is using die backside metal.

3. Applications Circuit

Figure 3-1. Application Circuit: Schematic

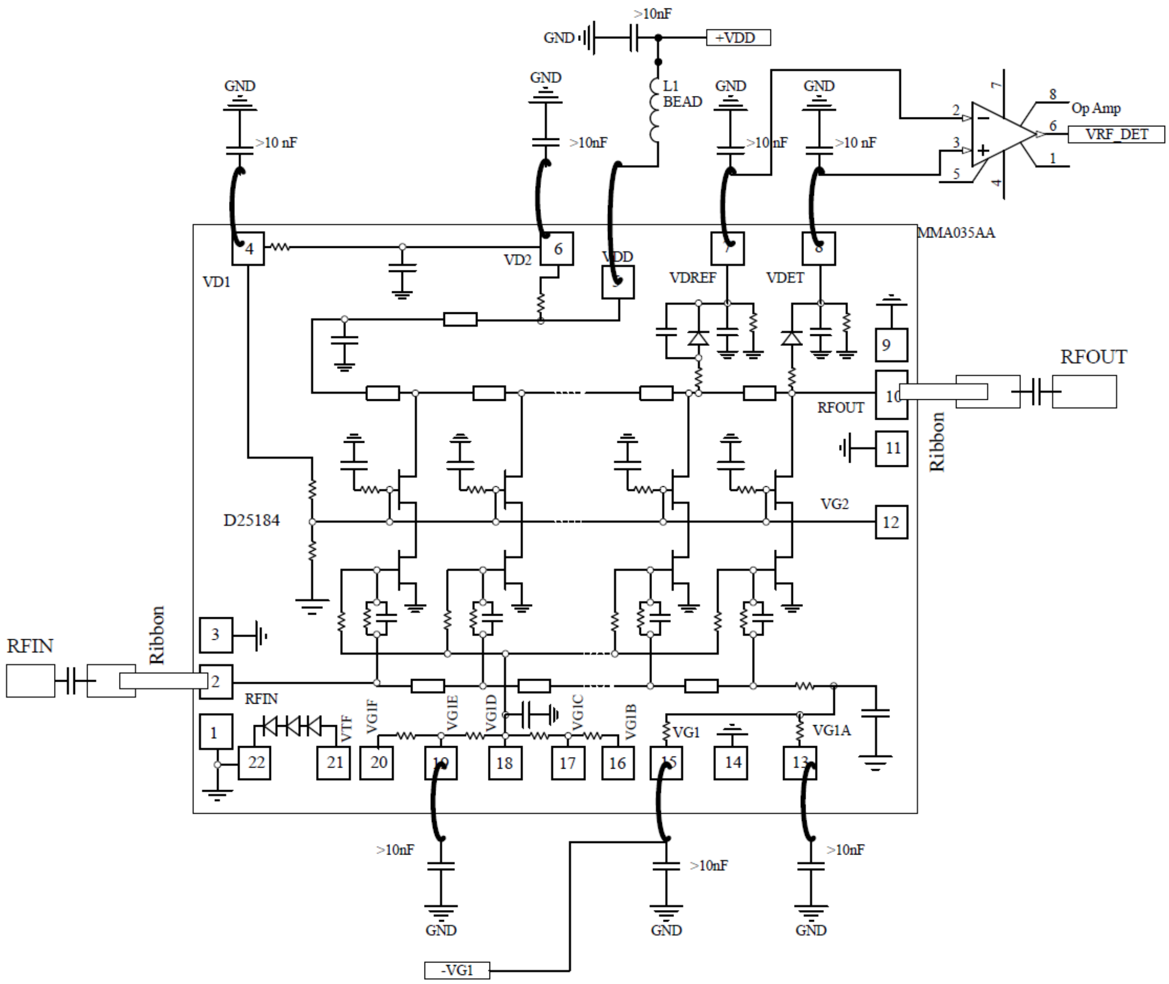


Figure 3-2. Die Test Circuit: Assembly Drawing

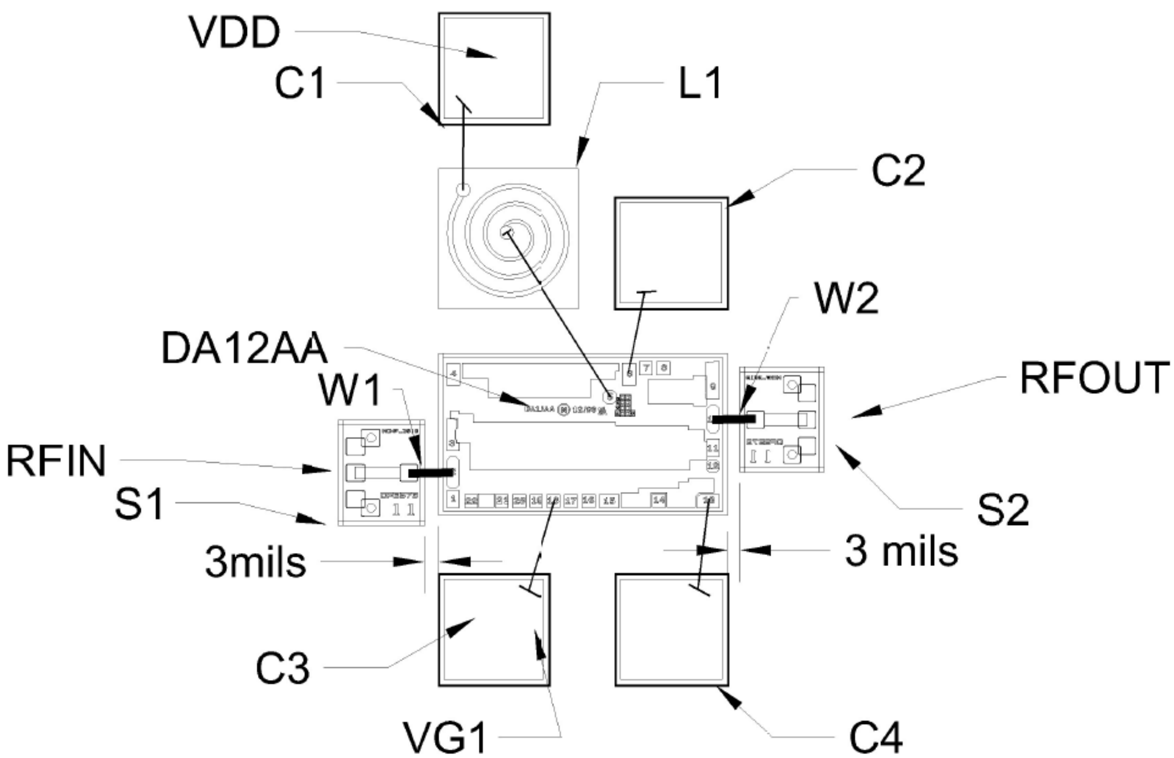


Table 3-1. List of Material for Test Circuit

Reference	Part Number	Description
DA12AA	MMA035AA	MMA035AA Amplifier Die
C1, C2, C3, C4	160U02A102MT4W	Johanson Dielectric, Cer.Cap 1 nF
S1, S2	E57311	Probe Launchers
L1	GC9001	Microchip Spiral Inductor, 6 nH
Epoxy	EpoTech H20E	Conductive Epoxy for die and cap mount

4. Ordering, Shipping, and Handling

4.1. Handling Recommendations

Gallium Arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedure and guidelines outlined in the Microchip application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2. Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA035AA	Die

4.3. Packing Information

Standard Format
Gel pack
50 pieces per pack

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	05/2025	Document created.

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1006-6

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.