

**AUTOMOTIVE, 125°C OPERATION,
3.8 μ A CURRENT CONSUMPTION
WATCHDOG TIMER WITH RESET FUNCTION**

The S-19405 Series is a watchdog timer developed using CMOS technology, which can operate with low current consumption of 3.8 μ A typ. The reset function and the low voltage detection function are available.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.

For more information regarding our FIT rate calculation, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- | | |
|--|---|
| • Detection voltage: | 2.0 V to 5.0 V, selectable in 0.1 V step |
| • Detection voltage accuracy: | $\pm 2.0\%$ |
| • Input voltage: | $V_{DD} = 0.9$ V to 6.0 V |
| • Hysteresis width: | 5% typ. |
| • Current consumption during watchdog timer operation: | 3.8 μ A typ. |
| • Reset time-out period: | 14.5 ms typ. ($C_{POR} = 2200$ pF) |
| • Watchdog time-out period: | 24.6 ms typ. ($C_{WDT} = 470$ pF) |
| • Watchdog operation is switchable: | Enable, Disable |
| • Watchdog operation voltage range: | $V_{DD} = 2.5$ V to 6.0 V |
| • Watchdog input edge is selectable: | Rising edge, falling edge |
| • Operation temperature range: | $T_a = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ |
| • Lead-free (Sn 100%), halogen-free | |
| • AEC-Q100 qualified*1 | |

*1. Contact our sales representatives for details.

■ Applications

- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Packages

- TMSOP-8
- HSNT-8(2030)

■ Block Diagrams

1. S-19405 Series A / B Type

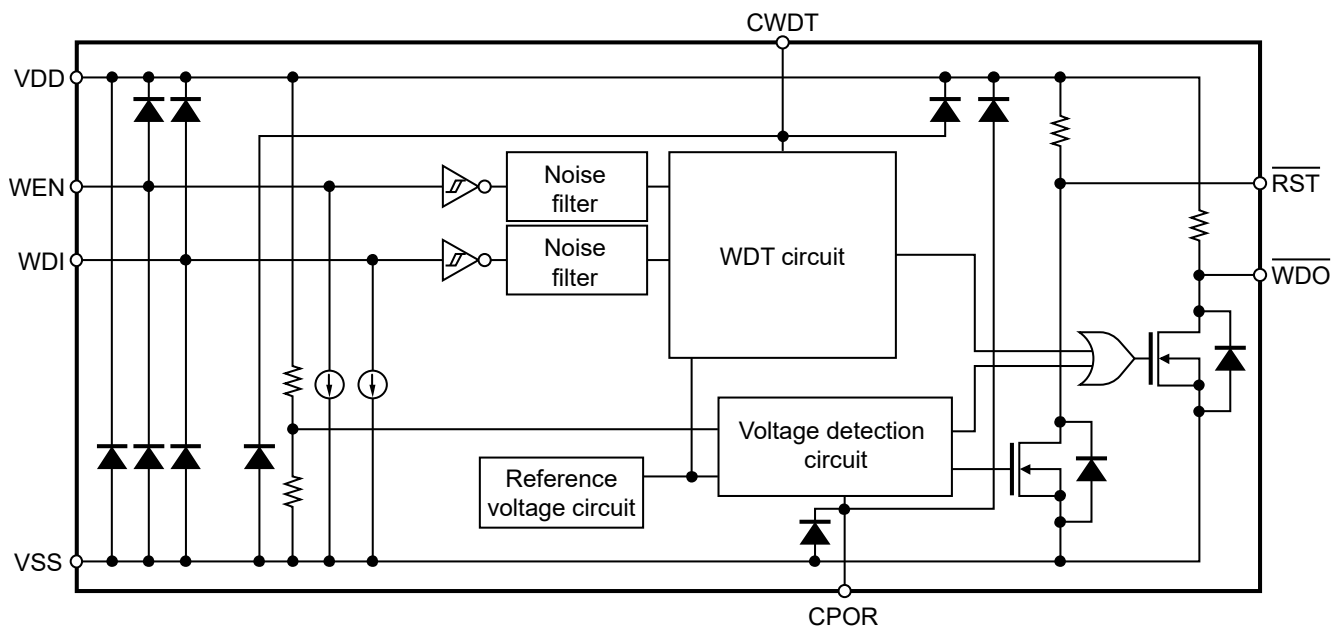


Figure 1

2. S-19405 Series D / E Type

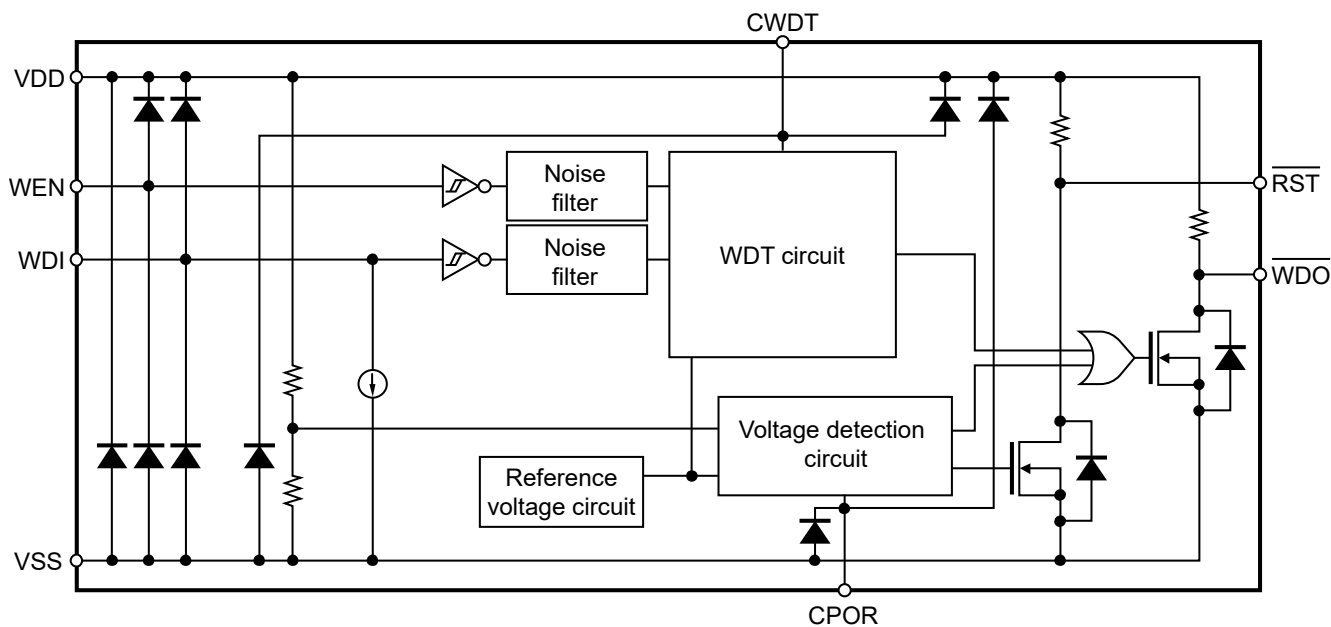


Figure 2

3. S-19405 Series G / H Type

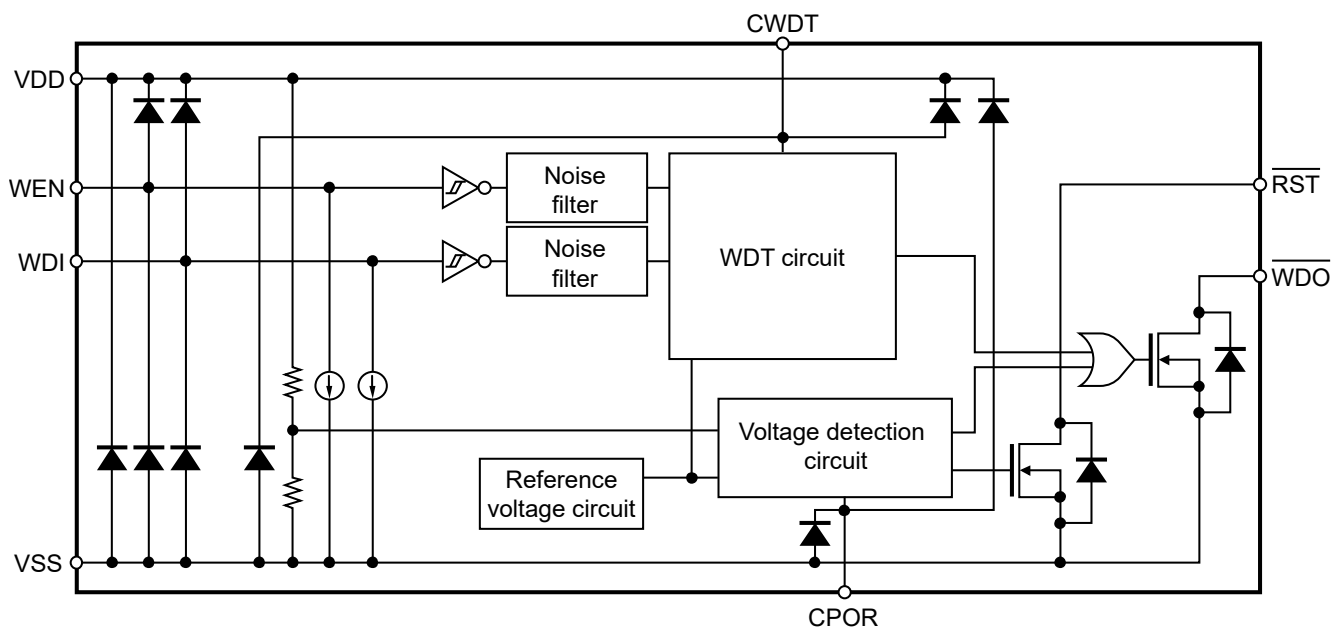


Figure 3

4. S-19405 Series J / K Type

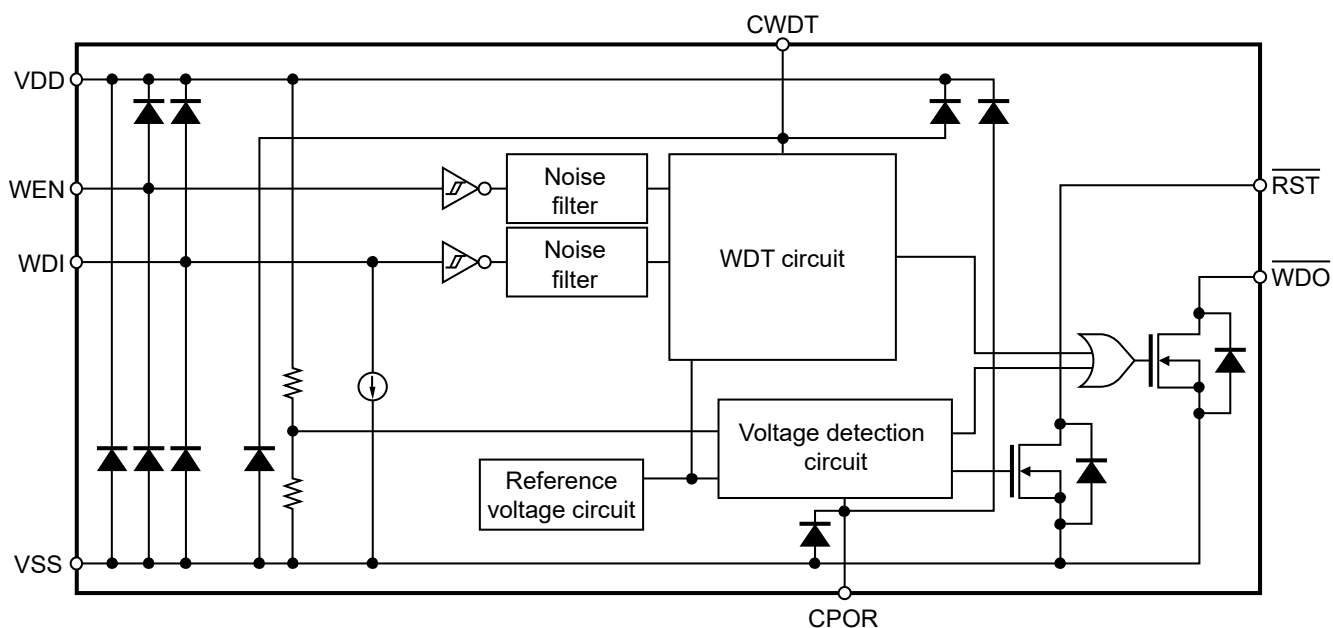


Figure 4

■ AEC-Q100 Qualified

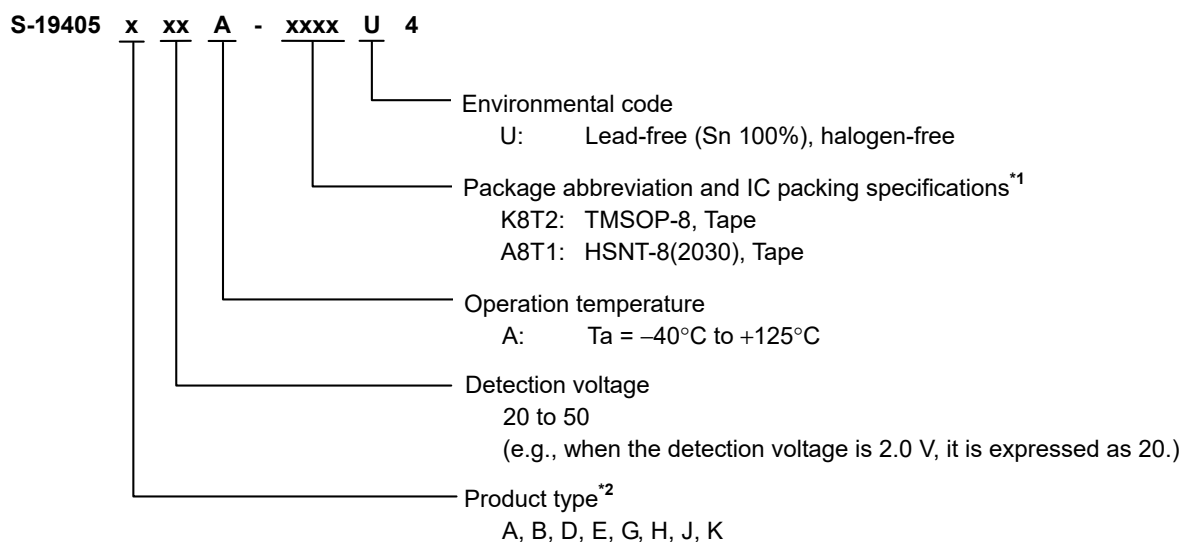
This IC supports AEC-Q100 for the operation temperature grade 1.

Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the product type, detection voltage, and package type for the S-19405 Series. Refer to "1. Product name" regarding the contents of product name, "2. Product type list" regarding the product types, "3. Packages" regarding the package drawings.

1. Product name



*1. Refer to the tape drawing.

*2. Refer to "2. Product type list".

2. Product type list

Table 1

Product Type	WEN Pin Logic	Constant Current Source Pull-down for WEN Pin	Input Edge	Output Pull-up Resistor
A	Active "H"	Available	Rising edge	Available
B	Active "H"	Available	Falling edge	Available
D	Active "L"	Unavailable	Rising edge	Available
E	Active "L"	Unavailable	Falling edge	Available
G	Active "H"	Available	Rising edge	Unavailable
H	Active "H"	Available	Falling edge	Unavailable
J	Active "L"	Unavailable	Rising edge	Unavailable
K	Active "L"	Unavailable	Falling edge	Unavailable

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	—
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

■ Pin Configurations

1. TMSOP-8

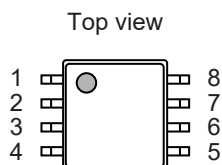


Figure 5

Table 3

Pin No.	Symbol	Description
1	RST	Reset output pin
2	CPOR	Reset time-out adjustment pin
3	CWDT	Watchdog time-out period adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	WDO	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

2. HSNT-8(2030)

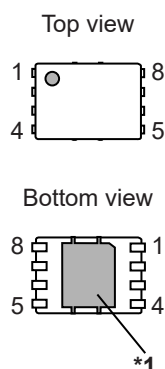


Figure 6

Table 4

Pin No.	Symbol	Description
1	RST	Reset output pin
2	CPOR	Reset time-out adjustment pin
3	CWDT	Watchdog time-out period adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	WDO	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.

■ Pin Functions

Refer to "■ Operations" for details.

1. $\overline{\text{RST}}$ pin

This is a reset output pin. It outputs "L" when detecting a low voltage.

Be sure to connect an external pull-up resistor (R_{extR}) to the $\overline{\text{RST}}$ pin in the product without an output pull-up resistor.

2. $\overline{\text{WDO}}$ pin

This is the watchdog output (time-out detection) pin.

Be sure to connect an external pull-up resistor (R_{extW}) to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor. **Table 5** shows the $\overline{\text{WDO}}$ pin and $\overline{\text{RST}}$ pin output statuses.

Table 5

Operation Status	$\overline{\text{WDO}}$ Pin	$\overline{\text{RST}}$ Pin
Normal operation	"H"	"H"
Low voltage detection	"L"	"L"
Time-out detection	"L"	"H"
When watchdog timer is in Disable	"H"	"H"

3. CPOR pin

This is a pin to connect an adjustment capacitor for reset time-out period (CPOR) in order to generate the reset time-out period (t_{RST}). CPOR is charged and discharged by an internal constant current circuit, and the charge-discharge duration is t_{RST} .

Refer to "■ Recommended Operation Conditions" and consider variation of CPOR to select an appropriate CPOR . t_{RST} is calculated by using the following equation.

$$t_{\text{RST}} [\text{ms}] = \text{CPOR delay coefficient} \times \text{CPOR} [\text{nF}] + t_{\text{RST0}} [\text{ms}]$$

Table 6

Item	Min.	Typ.	Max.
CPOR delay coefficient	3.9	6.5	9.1
$t_{\text{RST0}} [\text{ms}]$	0.0	0.2	0.6

4. CWDT pin

This is a pin to connect an adjustment capacitor for watchdog time-out period (CWDT) in order to generate the watchdog time-out period (t_{WDO}). CWDT is charged and discharged by an internal constant current circuit.

Refer to "■ Recommended Operation Conditions" and consider variation of CWDT to select an appropriate CWDT . t_{WDO} is calculated by using the following equation.

$$t_{\text{WDO}} [\text{ms}] = \text{CWDT delay coefficient 1} \times \text{CWDT} [\text{nF}] + t_{\text{WDO0}} [\text{ms}]$$

Table 7

Item	Min.	Typ.	Max.
CWDT delay coefficient 1	30	50	70
$t_{\text{WDO0}} [\text{ms}]$	0.0	1.1	3.0

5. WEN pin

This is a pin to switch Enable / Disable of the watchdog timer.

The voltage detection circuit independently operates at all times regardless of the watchdog timer operation.

In addition, the WEN pin has a noise filter. When the power supply voltage is 5.0 V, noise with a minimum pulse width of 200 ns can be eliminated.

5.1 S-19405 Series A / B / G / H type (WEN pin logic active "H" product)

The watchdog timer goes to Enable if the input is "H", and the charge-discharge operation is performed at the CWDt pin.

The WEN pin is connected to a constant current source (0.3 μ A typ.) and is pulled down internally.

5.2 S-19405 Series D / E / J / K type (WEN pin logic active "L" product)

The watchdog timer goes to Enable if the input is "L", and the charge-discharge operation is performed at the CWDt pin.

The WEN pin is not pulled down internally.

6. WDI pin

This is an input pin to receive a signal from the monitored object. By inputting an edge at an appropriate timing, the WDI pin confirms the normal operation of the monitored object.

The WDI pin is connected to a constant current source (0.3 μ A typ.) and is pulled down internally.

If the WEN pin is in Disable after the initialization and reset release are performed subsequent to the power supply voltage rise, the WDI pin will be able to receive input signals after the WEN pin goes to Enable and then the input setup time (t_{iset}) elapses.

In addition, the WDI pin has a noise filter. When the power supply voltage is 5.0 V, noise with a minimum pulse width of 200 ns can be eliminated.

■ Absolute Maximum Ratings

Table 8

(Ta = -40°C to +125°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VDD pin voltage	V _{DD}	V _{SS} - 0.3 to V _{SS} + 7.0	V
WDI pin voltage	V _{WDI}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0	V
WEN pin voltage	V _{WEN}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0	V
CPOR pin voltage	V _{CPOR}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0	V
CWDT pin voltage	V _{CWDT}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0	V
RST pin voltage	A / B / D / E type	V _{RST}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0
	G / H / J / K type		V _{SS} - 0.3 to V _{SS} + 7.0
WDO pin voltage	A / B / D / E type	V _{WDO}	V _{SS} - 0.3 to V _{DD} + 0.3 $\leq$ V _{SS} + 7.0
	G / H / J / K type		V _{SS} - 0.3 to V _{SS} + 7.0
Operation ambient temperature	T _{opr}	-40 to +125	°C
Storage temperature	T _{stg}	-40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 9

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	—	160	—	°C/W
			Board B	—	133	—	°C/W
			Board C	—	—	—	°C/W
			Board D	—	—	—	°C/W
			Board E	—	—	—	°C/W
		HSNT-8(2030)	Board A	—	181	—	°C/W
			Board B	—	135	—	°C/W
			Board C	—	40	—	°C/W
			Board D	—	42	—	°C/W
			Board E	—	32	—	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ Recommended Operation Conditions

Table 10

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD pin voltage	V _{DD}	Voltage detection circuit	0.9	—	6.0	V
		Watchdog timer circuit	2.5	—	6.0	V
Set detection voltage	-V _{DET(S)}	0.1 V step	2.0	—	5.0	V
External pull-up resistor for RST pin	R _{extR}	G / H / J / K type	10	100	—	k Ω
External pull-up resistor for WDO pin	R _{extW}	G / H / J / K type	10	100	—	k Ω
Adjustment capacitance for reset time-out period	C _{POR}	—	0.1	2.2	1000	nF
Adjustment capacitance for watchdog time-out period	C _{WDT}	—	0.1	0.47	1000	nF

■ Electrical Characteristics

Table 11 (1 / 2)

(WEN pin logic active "H" product, $V_{DD} = 5.0$ V, $T_a = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	−V _{DET}	−		−V _{DET(S)} × 0.98	−V _{DET(S)}	−V _{DET(S)} × 1.02	V	1
Hysteresis width	V _{HYS}	−		−V _{DET} × 0.03	−V _{DET} × 0.05	−V _{DET} × 0.07	V	1
Current consumption during watchdog timer operation	I _{SS1}	V _{WEN} = V _{DD}		−	3.8	9.0	μA	2
Current consumption during watchdog timer stop	I _{SS2}	V _{WEN} = 0 V		−	2.7	7.0	μA	2
Reset output voltage "H"	V _{ROH}	Only A / B / D / E type		V _{DD} − 1.0	−	−	V	4
Reset output voltage "L"	V _{ROL}	External pull-up resistor of 100 kΩ is connected for G / H / J / K type		−	−	0.4	V	5
Reset output pull-up resistance	R _{RUP}	Only A / B / D / E type		2.0	5.88	12.5	MΩ	−
Reset output current	I _{ROUT}	V _{DS} = 0.4 V	V _{DD} = 1.5 V	0.48	1.1	−	mA	6
			V _{DD} = 1.8 V	0.8	1.6	−	mA	6
			V _{DD} = 2.5 V	1.0	2.6	−	mA	6
			V _{DD} = 3.0 V	1.4	3.3	−	mA	6
Reset output leakage current	I _{RLEAK}	V _{DS} = 6.0 V, V _{DD} = 6.0 V		−	−	0.096	μA	7
Watchdog output voltage "H"	V _{WOH}	Only A / B / D / E type		V _{DD} − 1.0	−	−	V	8
Watchdog output voltage "L"	V _{WOL}	External pull-up resistor of 100 kΩ is connected for G / H / J / K type		−	−	0.4	V	9
Watchdog output pull-up resistance	R _{WUP}	Only A / B / D / E type		2.0	5.88	12.5	MΩ	−
Watchdog output current	I _{WOUT}	V _{DS} = 0.4 V	V _{DD} = 1.5 V	0.48	1.1	−	mA	10
			V _{DD} = 1.8 V	0.8	1.6	−	mA	10
			V _{DD} = 2.5 V	1.0	2.6	−	mA	10
			V _{DD} = 3.0 V	1.4	3.3	−	mA	10
Watchdog output leakage current	I _{WLEAK}	V _{DS} = 6.0 V, V _{DD} = 6.0 V		−	−	0.096	μA	11
Input pin voltage 1 "H"	V _{SH1}	WEN pin		0.7 × V _{DD}	−	−	V	12
Input pin voltage 1 "L"	V _{SL1}	WEN pin		−	−	0.3 × V _{DD}	V	12
Input pin voltage 2 "H"	V _{SH2}	WDI pin		0.7 × V _{DD}	−	−	V	12
Input pin voltage 2 "L"	V _{SL2}	WDI pin		−	−	0.3 × V _{DD}	V	12

Table 11 (2 / 2)

(WEN pin logic active "H" product, $V_{DD} = 5.0$ V, $T_a = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Input pin current 1 "H"	I_{SH1}	WEN pin, $V_{DD} = 6.0$ V, Input pin voltage = 6.0 V	–	0.3	1.0	μA	12
		A / B / G / H type	–	0.3	1.0	μA	12
Input pin current 1 "L"	I_{SL1}	WEN pin, $V_{DD} = 6.0$ V, Input pin voltage = 0 V	–0.1	–	0.1	μA	12
		D / E / J / K type	–0.1	–	0.1	μA	12
Input pin current 2 "H"	I_{SH2}	WDI pin, $V_{DD} = 6.0$ V, Input pin voltage = 6.0 V	–	0.3	1.0	μA	12
Input pin current 2 "L"	I_{SL2}	WDI pin, $V_{DD} = 6.0$ V, Input pin voltage = 0 V	–0.1	–	0.1	μA	12
Input pulse width "H"*2	t_{high1}	Timing Diagram 1	1.5	–	–	μs	13
Input pulse width "L"*2	t_{low1}	Timing Diagram 1	1.5	–	–	μs	13
Reset time-out period	t_{RST}	$C_{POR} = 2200$ pF, Timing Diagram 2, 5	8.7	14.5	20	ms	3
Watchdog time-out period	t_{WDU}	$C_{WDT} = 470$ pF, Timing Diagram 4, 5	15	24.6	34	ms	3
Watchdog output delay time	t_{WOUT}	Timing Diagram 2, 3-2	–	25	40	μs	3
Reset output delay time	t_{ROUT}	Timing Diagram 2, 3-1	–	25	40	μs	3
Input setup time	t_{iset}	Timing Diagram 4	1.0	–	–	μs	3

*1. $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

*2. Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ Electrical Characteristics".

■ Timing Diagrams on Electrical Characteristics

(1) Timing Diagram 1

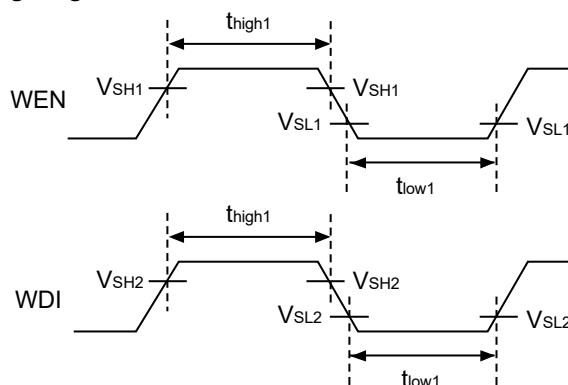


Figure 7 Input Pulse Width

(2) Timing Diagram 2

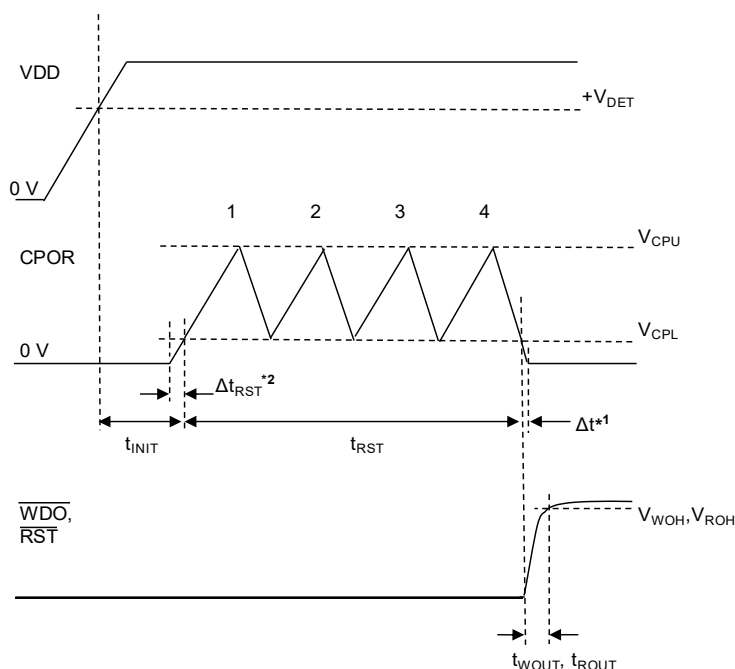


Figure 8 V_{DD} Rising

(3) Timing Diagram 3-1

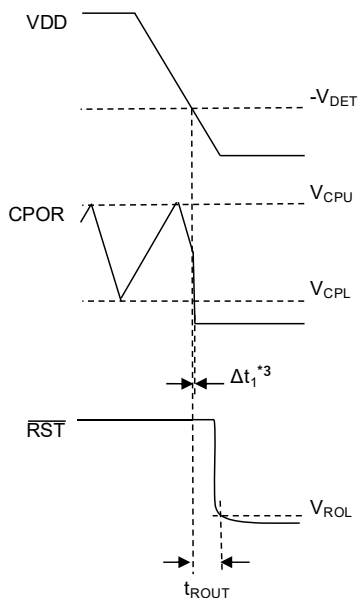


Figure 9 V_{DD} Falling during CPOR Pin Charge Operation

(4) Timing Diagram 3-2

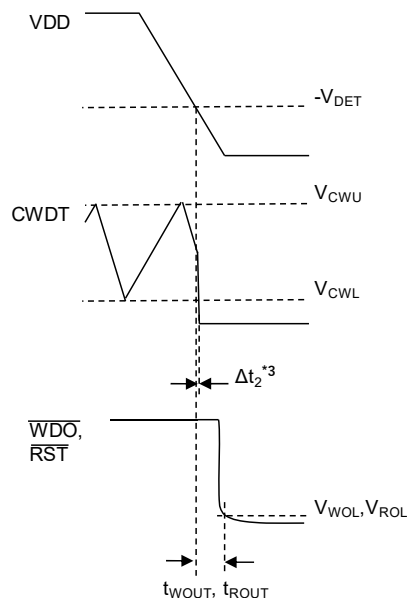


Figure 10 V_{DD} Falling during CWDT Pin Charge Operation

- *1. The CPOR pin voltage fall delay time (Δt) is sufficiently small compared to the reset time-out period (t_{RST}).
- *2. The time (Δt_{RST}) the CPOR pin voltage (V_{CPOR}) reaches the CPOR charge lower limit threshold (V_{CPL}) from 0 V is proportional to the adjustment capacitance for reset time-out period (C_{POR}). Thus, large C_{POR} results in large Δt_{RST} . Refer to "12. Initialization time (t_{INIT}) vs. Power supply voltage rise time (t_r)" in "■ Characteristics (Typical Data)".
- *3. CPOR pin voltage forced fall delay time (Δt_1) and the CWDT pin voltage forced fall delay time (Δt_2) is sufficiently small compared to t_{RST} in **Timing Diagram 2**.

Remark V_{CPU} : CPOR charge upper limit threshold (1.25 V typ.), V_{CPL} : CPOR charge lower limit threshold (0.20 V typ.)
 V_{CWU} : CWDT charge upper limit threshold (1.25 V typ.), V_{CWL} : CWDT charge lower limit threshold (0.20 V typ.)

(5) Timing Diagram 4

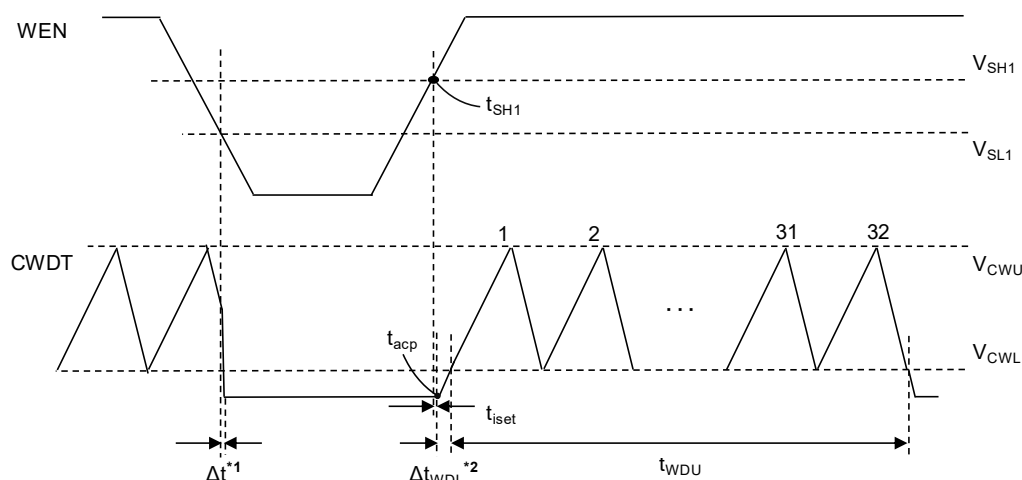


Figure 11 Counter Reset due to V_{WEN}

(6) Timing Diagram 5

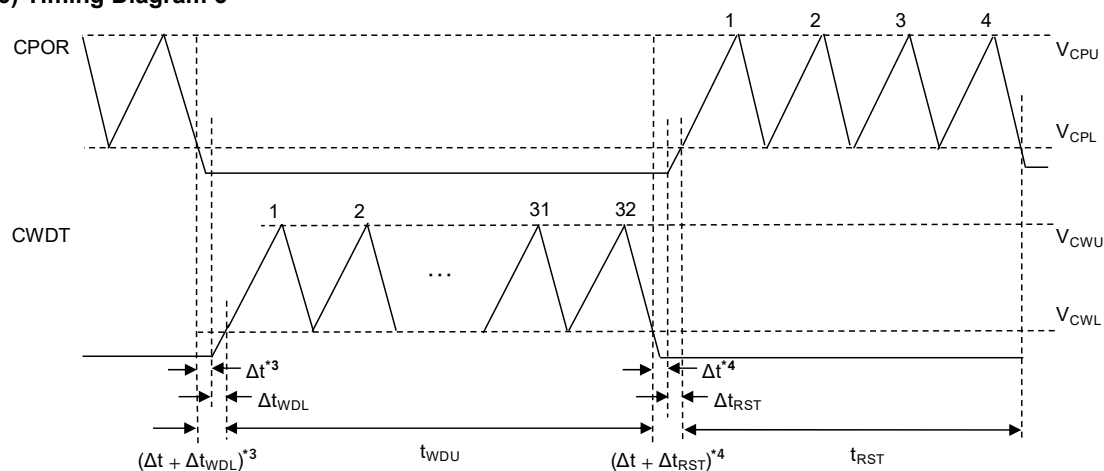


Figure 12 Watchdog Time-out Detection

- *1. CWDT pin voltage forced fall delay time (Δt) is sufficiently small compared to the watchdog time-out period (t_{WDU}).
- *2. The CWDT pin voltage rise delay time ($t_{iset} + \Delta t_{WDL}$) is sufficiently small (less than 1%) compared to t_{WDU} .
- *3. The delay time ($\Delta t + \Delta t_{WDL}$) from when the CPOR pin voltage (V_{CPOR}) falls to the CPOR charge lower limit threshold (V_{CPL}) to when the CWDT pin voltage (V_{CWDT}) reaches the CWDT charge lower limit threshold (V_{CWL}) is sufficiently small (less than 1%) compared to t_{WDU} .
- *4. The delay time ($\Delta t + \Delta t_{RST}$) from when V_{CWDT} falls to V_{CWL} to when V_{CPOR} reaches V_{CPL} is sufficiently small (less than 5%) compared to reset time-out period (t_{RST}).

Remark t_{iset} : Input setup time (less than 1 μ s)

The time from when V_{WEN} exceeds V_{SH1} (t_{SH1}) to when the WDI pin is able to receive input signals (t_{acp}).

(7) Timing Diagram 6-1

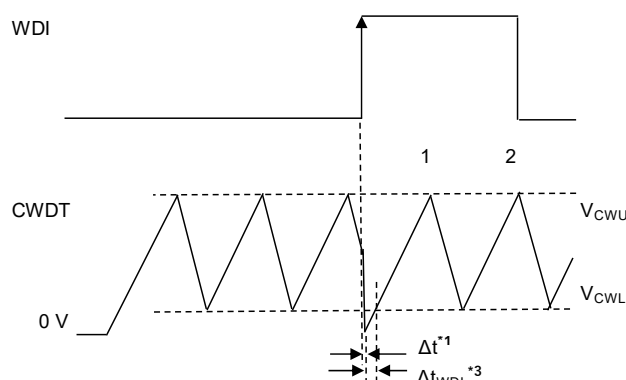


Figure 13 V_{WDI} Rising Edge

(8) Timing Diagram 6-2

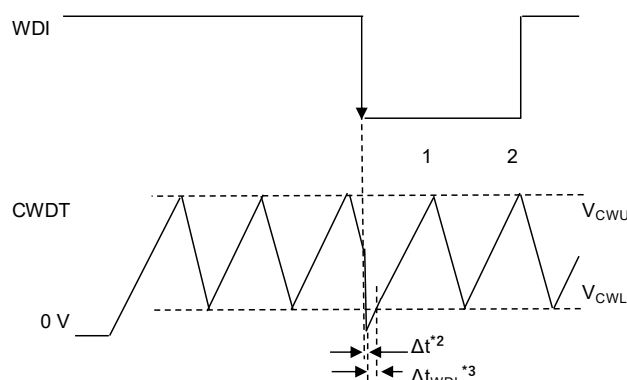


Figure 14 V_{WDI} Falling Edge

(9) Timing Diagram 6-3

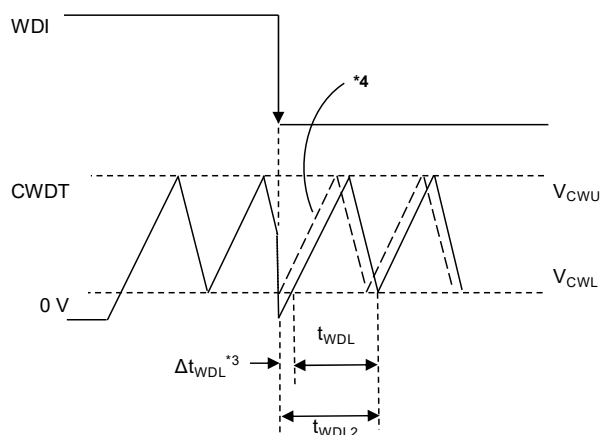


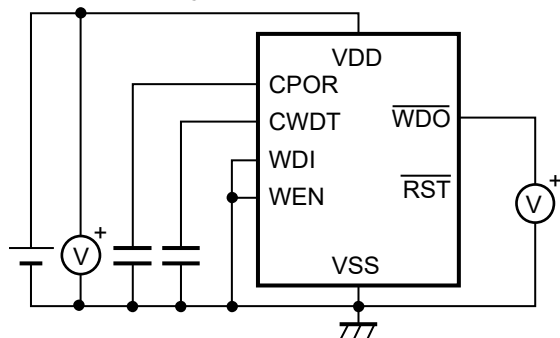
Figure 15 V_{WDI} Rising or Falling Edges

- *1. The delay time (Δt) from the WDI pin voltage (V_{WDI}) rising edge to the CWDT pin voltage (V_{CWDT}) rising start is sufficiently small (less than 1%) compared to t_{WDU} in **Timing Diagram 4** and **5**.
- *2. The delay time (Δt) from the V_{WDI} falling edge to the V_{CWDT} rising start is sufficiently small (less than 1%) compared to t_{WDU} in **Timing Diagram 4** and **5**.
- *3. The time (Δt_{WDL}) V_{CWDT} reaches V_{CWL} from 0 V is proportional to the adjustment capacitance for watchdog time-out period (C_{WDT}). Thus, large C_{WDT} results in large Δt_{WDL} .
- *4. As indicated by the waveform illustrated with dashed lines, if V_{CWDT} does not fall to 0 V when the V_{WDI} rising or falling edge is input, Δt_{WDL} may approach 0. Similar phenomena may occur in **Timing Diagrams 6-1** to **6-3** as well.

■ Test Circuits

Refer to "■ Recommended Operation Conditions" when setting constants of external pull-up resistors (R_{extR} , R_{extW}) and external capacitors (C_{POR} , C_{WDT}).

(1) A / B / D / E type



(2) G / H / J / K type

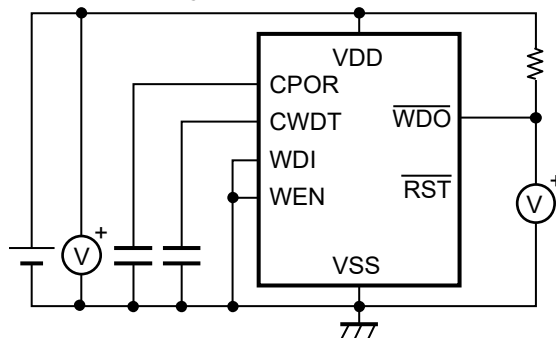


Figure 16 Test Circuit 1

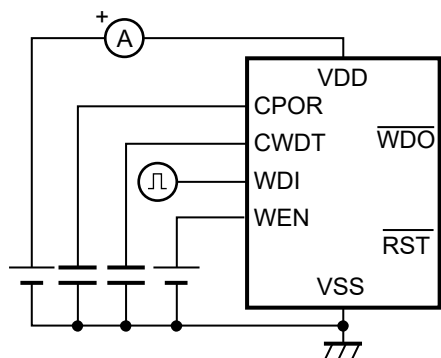
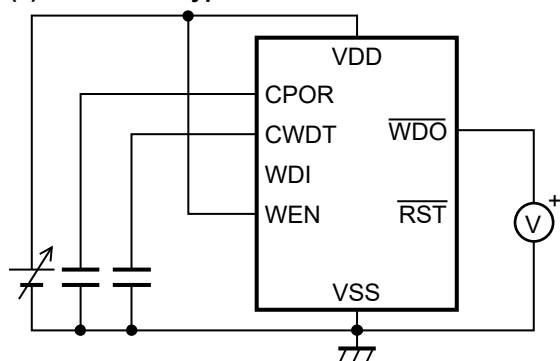


Figure 17 Test Circuit 2

(1) A / B / D / E type



(2) G / H / J / K type

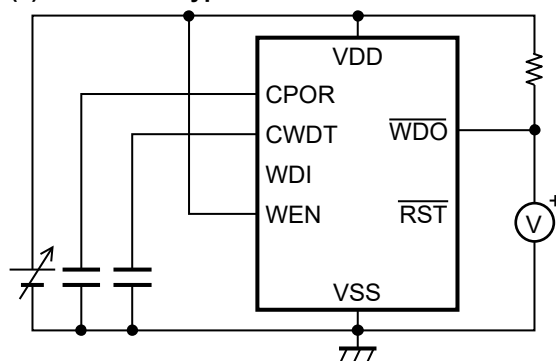


Figure 18 Test Circuit 3

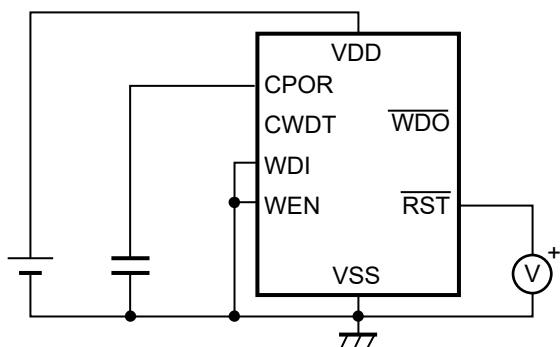
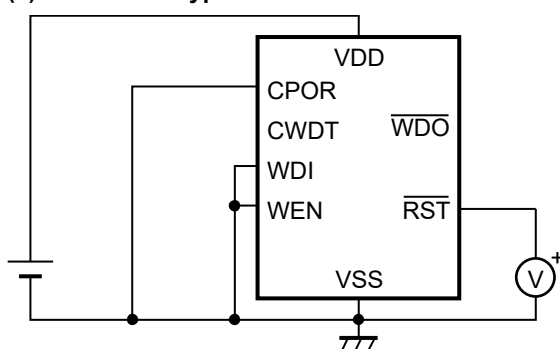


Figure 19 Test Circuit 4

(1) A / B / D / E type



(2) G / H / J / K type

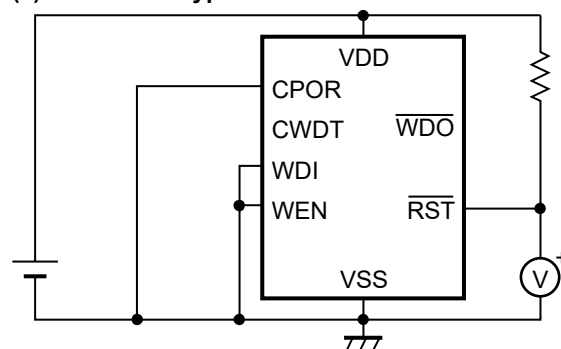


Figure 20 Test Circuit 5

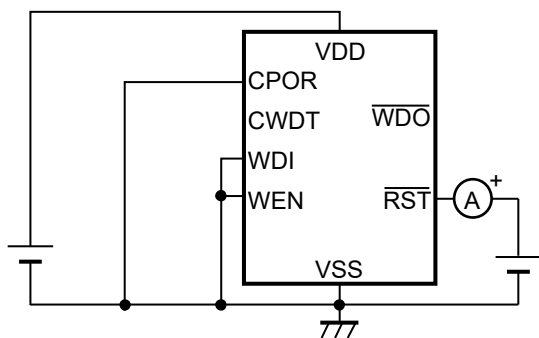


Figure 21 Test Circuit 6

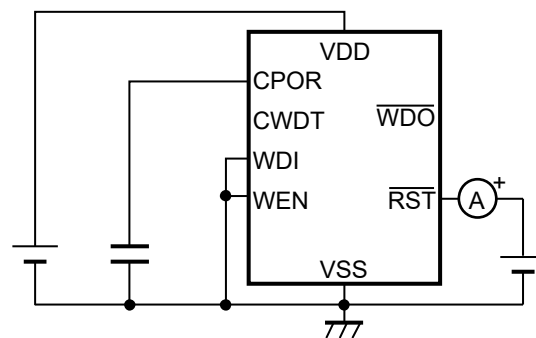


Figure 22 Test Circuit 7

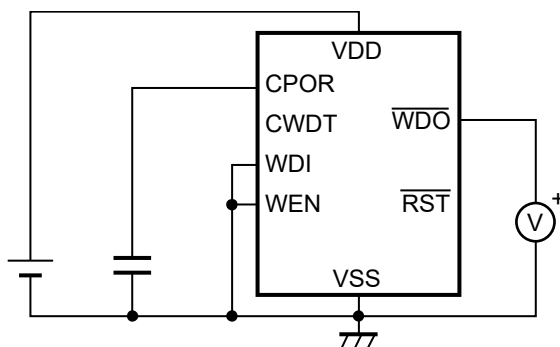
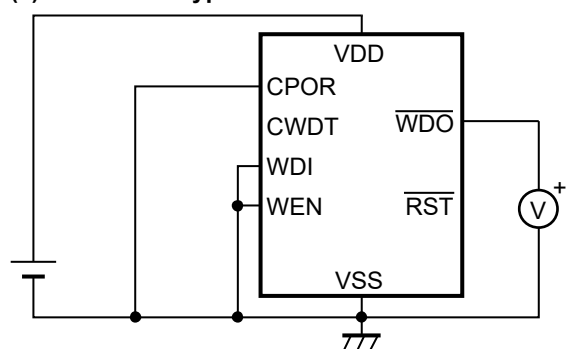


Figure 23 Test Circuit 8

(1) A / B / D / E type



(2) G / H / J / K type

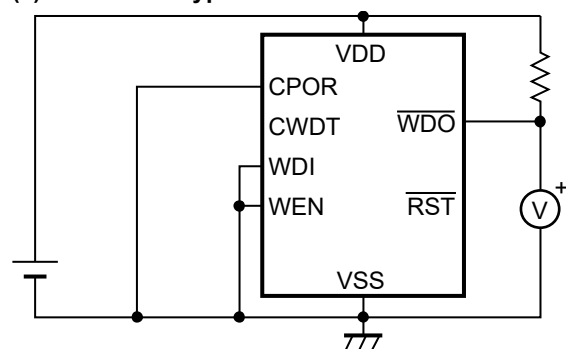


Figure 24 Test Circuit 9

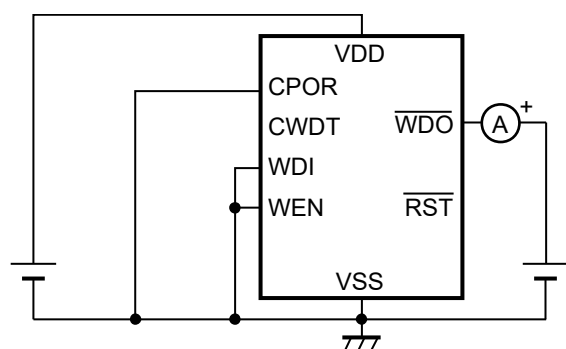


Figure 25 Test Circuit 10

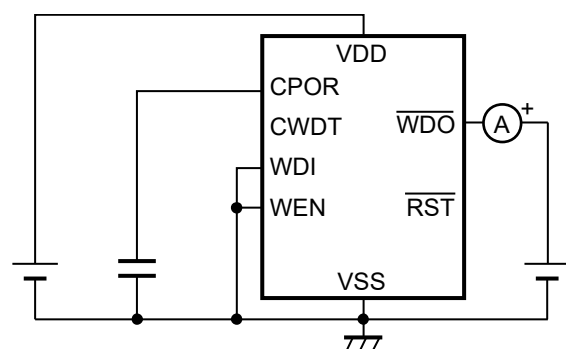
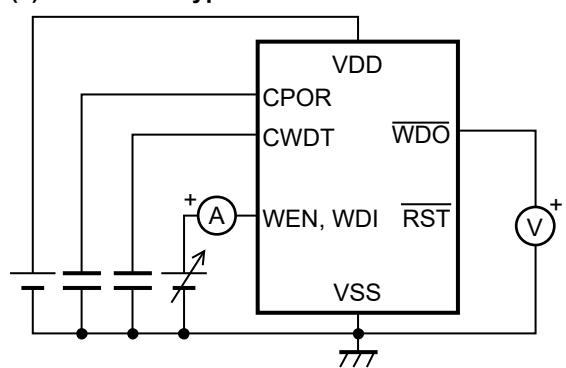


Figure 26 Test Circuit 11

(1) A / B / D / E type



(2) G / H / J / K type

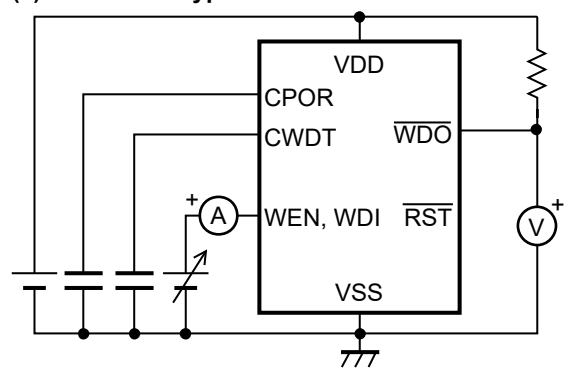
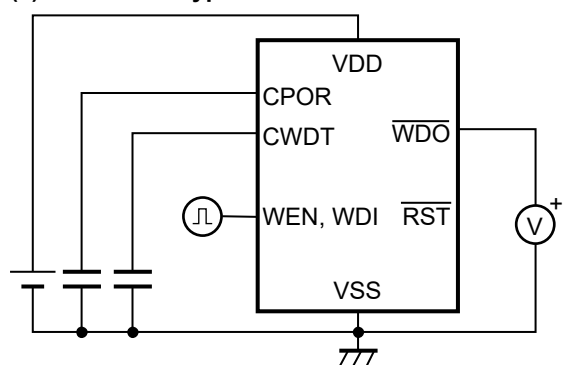


Figure 27 Test Circuit 12

(1) A / B / D / E type



(2) G / H / J / K type

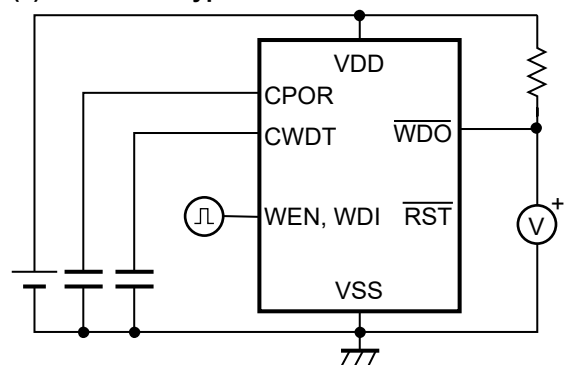
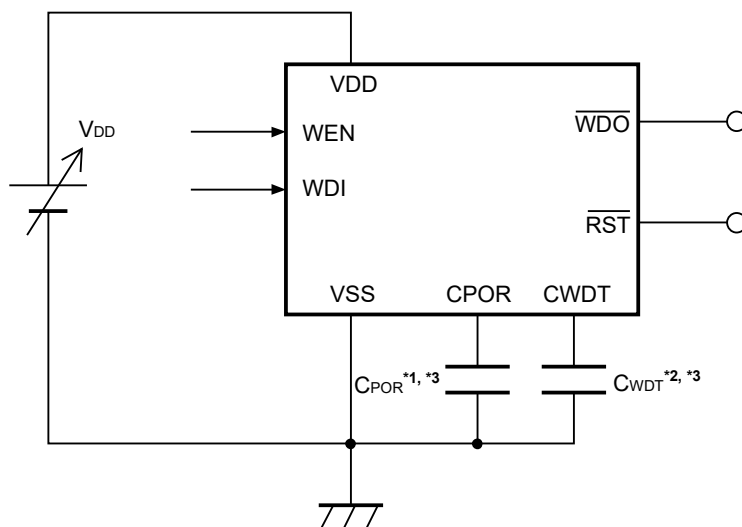


Figure 28 Test Circuit 13

■ Standard Circuits

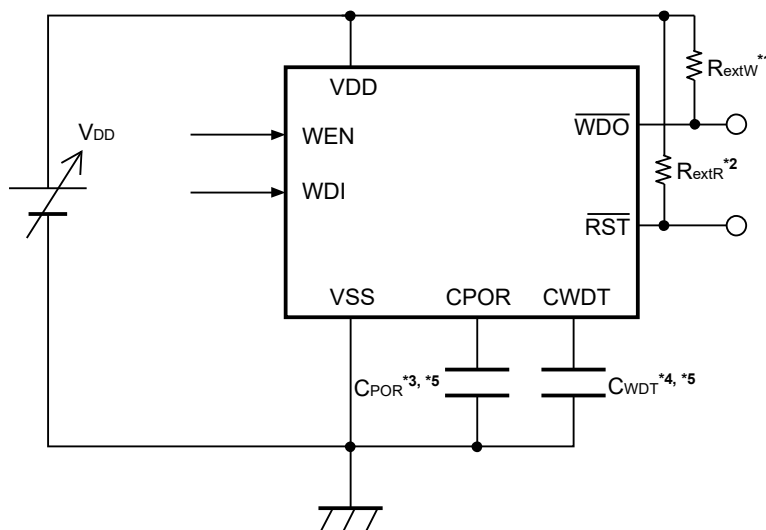
1. S-19405 Series A / B / D / E type



- *1. Connect the adjustment capacitor for reset time-out period (C_{POR}) directly between the CPOR pin and the VSS pin.
- *2. Connect the adjustment capacitor for watchdog time-out period (C_{WDT}) directly between the CWDT pin and the VSS pin.
- *3. A capacitor of 100 pF to 1 μ F can be used for C_{POR} and C_{WDT} . Even if the capacitance is within this range, cautions are still needed when the value is extremely large. Refer to "1. Low voltage operation when C_{POR} is extremely large" in "■ Precautions for Use".

Figure 29

2. S-19405 Series G / H / J / K type



- *1. R_{extW} is an external pull-up resistor for the $\overline{WDO}$ pin.
- *2. R_{extR} is an external pull-up resistor for the $\overline{RST}$ pin.
- *3. Connect the adjustment capacitor for reset time-out period (C_{POR}) directly between the CPOR pin and the VSS pin.
- *4. Connect the adjustment capacitor for watchdog time-out period (C_{WDT}) directly between the CWDT pin and the VSS pin.
- *5. A capacitor of 100 pF to 1 μ F can be used for C_{POR} and C_{WDT} . Even if the capacitance is within this range, cautions are still needed when the value is extremely large. Refer to "1. Low voltage operation when C_{POR} is extremely large" in "■ Precautions for Use".

Figure 30

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

■ Operations

1. Voltage detector circuit

1.1 Basic operation

- (1) When the power supply voltage (V_{DD}) is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N2) is turned off and "H" is output to the $\overline{RST}$ pin. Since the Pch transistor (P1) is turned on, the input voltage to the comparator (C1) is $\frac{R_B \cdot V_{DD}}{R_A + R_B}$.
- (2) Even if V_{DD} decreases to $+V_{DET}$ or lower, "H" is output to the $\overline{RST}$ pin when V_{DD} is the detection voltage ($-V_{DET}$) or higher. When V_{DD} decreases to $-V_{DET}$ (point A in **Figure 32**) or lower, N2 which is controlled by C1 is turned on, and then "L" is output to the $\overline{RST}$ pin. At this time, P1 is turned off, and the input voltage to C1 is $\frac{R_B \cdot V_{DD}}{R_A + R_B + R_C}$.
- (3) If V_{DD} further decreases to the IC's minimum operation voltage or lower, the $\overline{RST}$ pin output is "H".
- (4) When V_{DD} increases to the IC's minimum operation voltage or higher, "L" is output to the $\overline{RST}$ pin. In addition, even if V_{DD} exceeds $-V_{DET}$, the output is "L" when V_{DD} is lower than $+V_{DET}$.
- (5) When V_{DD} increases to $+V_{DET}$ (point B in **Figure 32**) or higher, N2 is turned off, and "H" is output to the $\overline{RST}$ pin after elapse of $t_{INIT} + t_{RST}$.

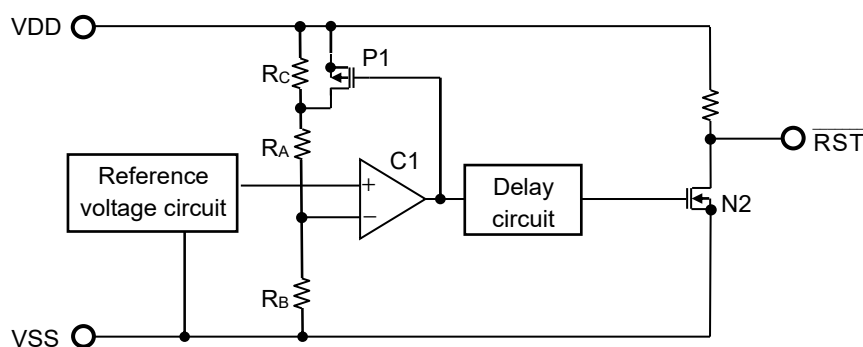


Figure 31 Operation of Voltage Detector Circuit

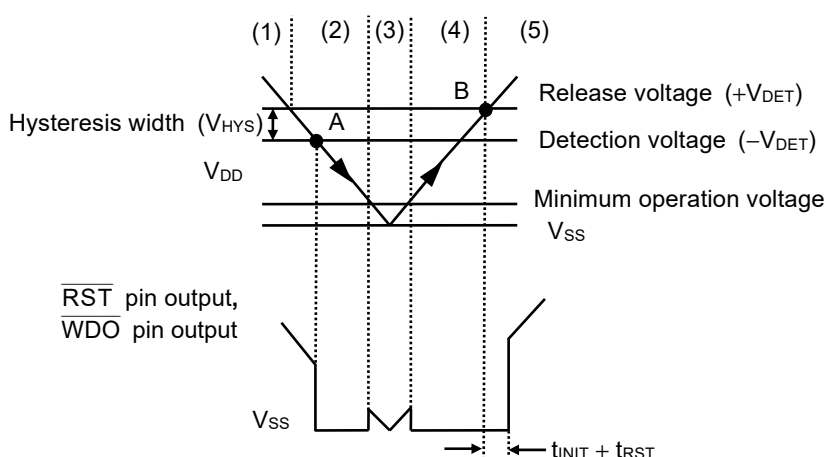


Figure 32 Timing Chart of Voltage Detector Circuit

1.2 From power-on to reset release

The S-19405 Series initiates the initialization if the VDD pin voltage exceeds the release voltage ($+V_{DET}$). The charge-discharge operation to the CPOR pin is initiated after the passage of the initialization time (t_{INIT}), and the $\overline{WDO}$ pin output and the $\overline{RST}$ pin output change from "L" to "H" after the operation is performed 4 times. Refer to **Figure 33**.

t_{INIT} changes according to the power supply voltage rise time (t_r). Refer to "12. Initialization time (t_{INIT}) vs. Power supply voltage rise time (t_r)" in "■ Characteristics (Typical Data)" for the relation between t_{INIT} and t_r .

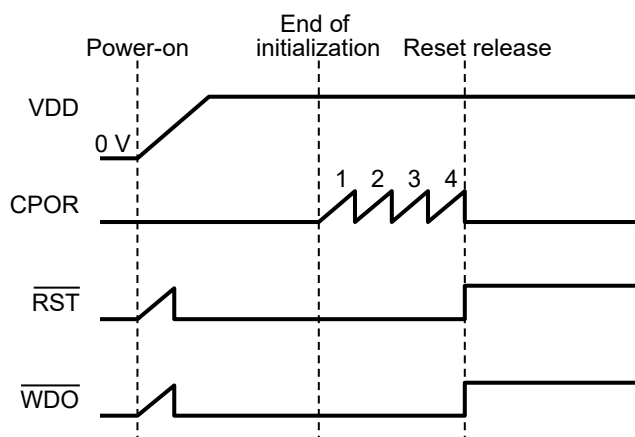


Figure 33

1.3 Operation of low voltage detection

The voltage detection circuit detects a low voltage if the power supply voltage falls below the detection voltage, and then "L" is output from the $\overline{WDO}$ pin and the $\overline{RST}$ pin. The output is maintained until the charge-discharge operation of the CPOR pin is performed 4 times.

The S-19405 Series can detect a low voltage even if either the CPOR pin or the CWDT pin performs the charge-discharge operation. In this case, no influence is exerted on the status of the WEN pin.

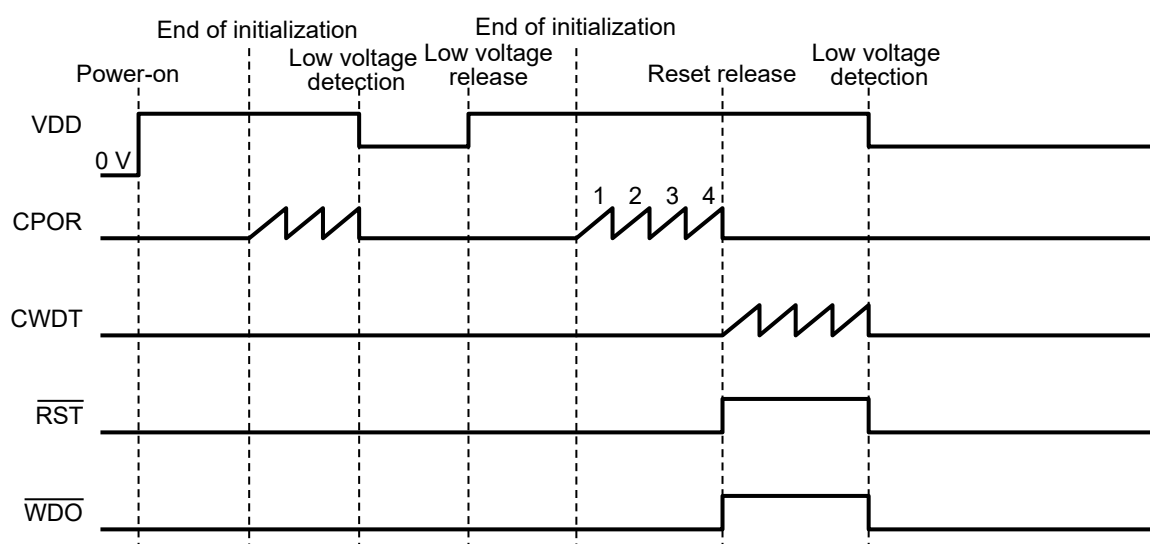


Figure 34

2. Watchdog timer

2.1 From reset release to initiation of charge-discharge operation to CWDT pin

The charge-discharge operation to the CWDT pin differs depending on the status of the WEN pin at the reset release.

2.1.1 When WEN pin is in Enable at reset release

Since the watchdog timer is in Enable, the S-19405 Series initiates the charge-discharge operation to the CWDT pin.

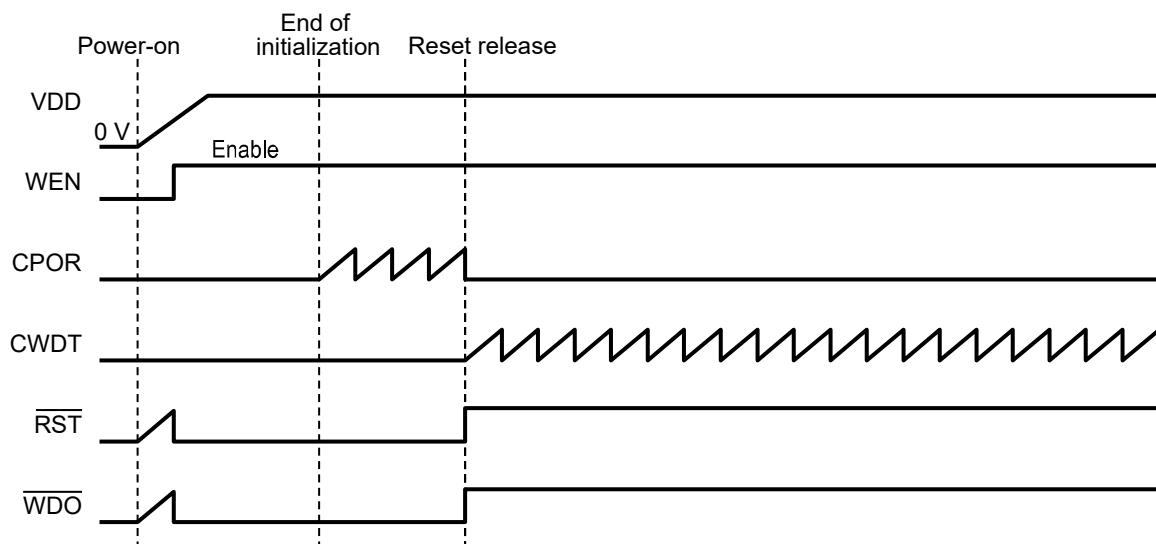


Figure 35 WEN Pin = "H"

2.1.2 When WEN pin is in Disable at reset release

Since the watchdog timer is in Disable after the CPOR pin performs the charge-discharge operation 4 times, the S-19405 Series does not initiate the charge-discharge operation to the CWDT pin. If the input to the WEN pin changes to "H" in this status, the S-19405 Series initiates the charge-discharge operation to the CWDT pin.

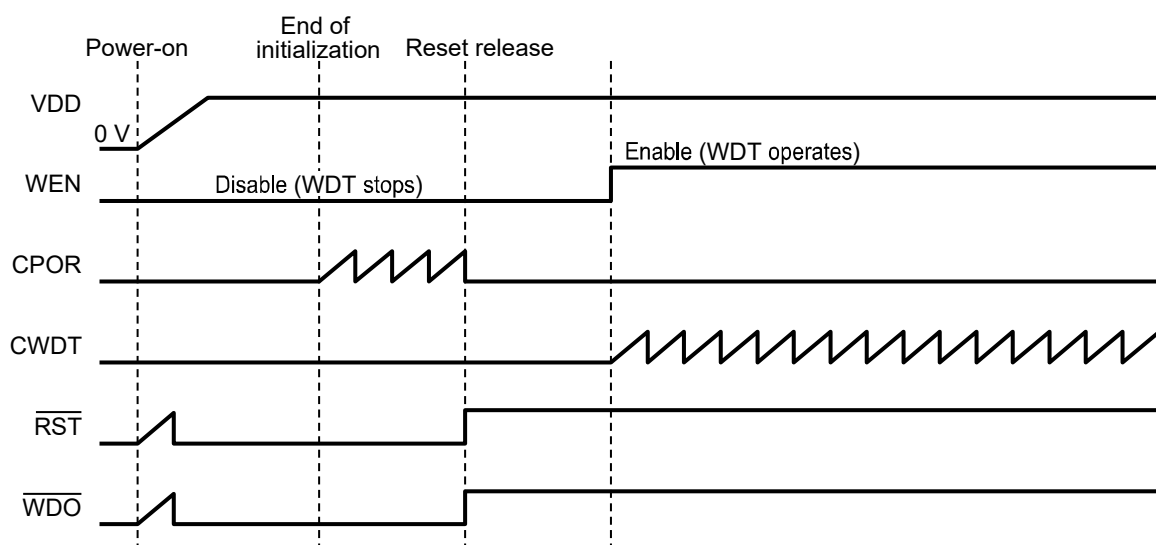


Figure 36 WEN Pin = "L" → "H"

2.2 Watchdog time-out detection

The watchdog timer detects a time-out after the charge-discharge operation to the CWDT pin is performed 32 times, then the $\overline{\text{WDO}}$ pin output changes from "H" to "L".

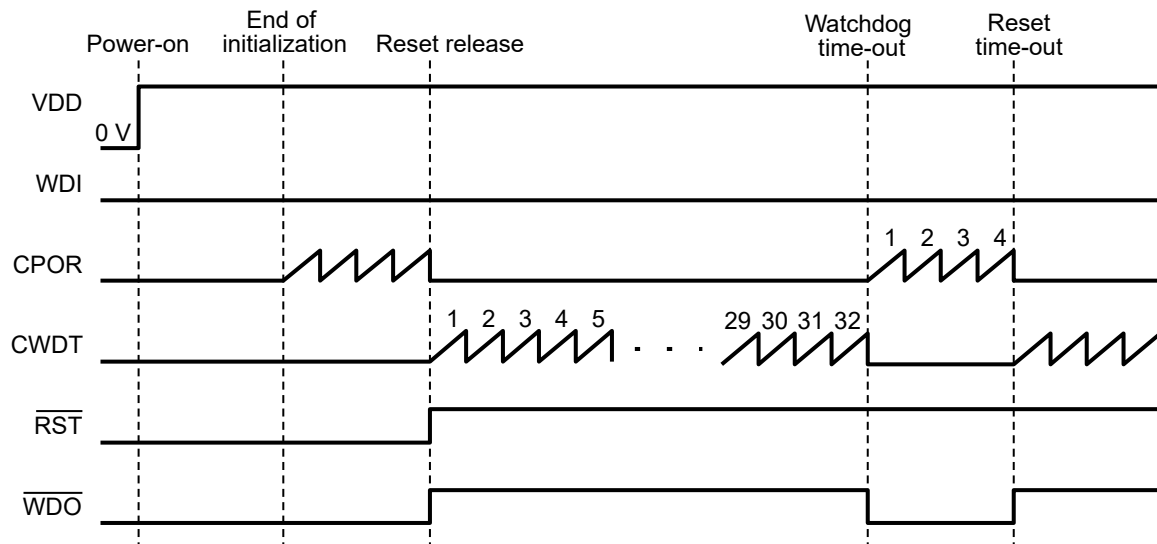


Figure 37

2.3 Internal counter reset due to edge

When the WDI pin detects an edge during the charge-discharge operation to the CWDT pin, the internal counter which counts the number of times of the charge-discharge operation is reset. The CWDT pin initiates the discharge operation when an edge is detected and initiates the charge-discharge operation again after the discharge operation is completed.

2.3.1 Counter reset due to rising edge

(S-19405AxxA, S-19405DxxA, S-19405GxxA, S-19405JxxA)

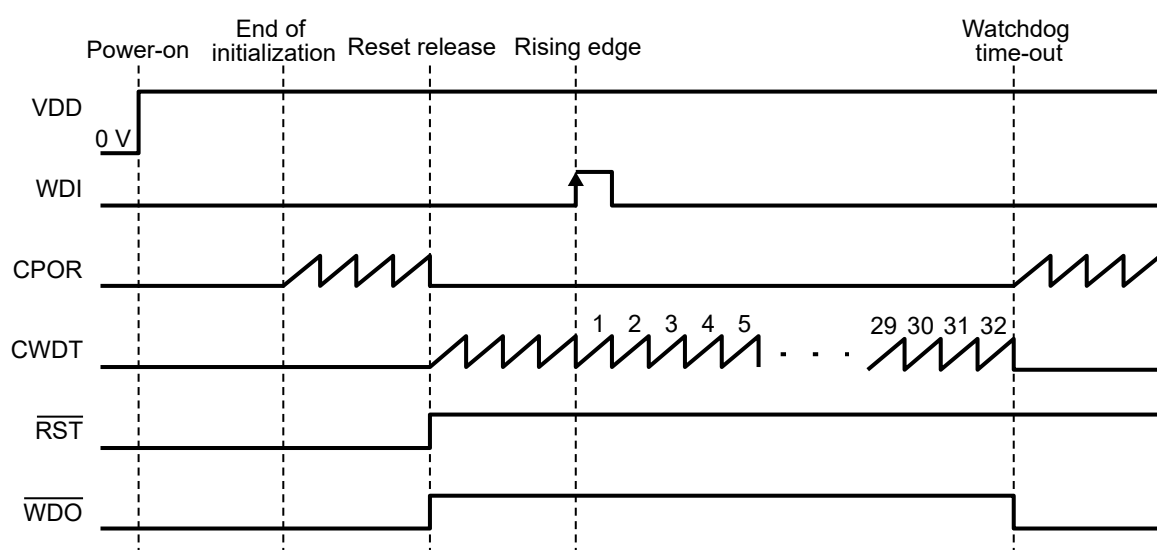


Figure 38

2.3.2 Counter reset due to falling edge (S-19405BxxA, S-19405ExxA, S-19405HxxA, S-19405KxxA)

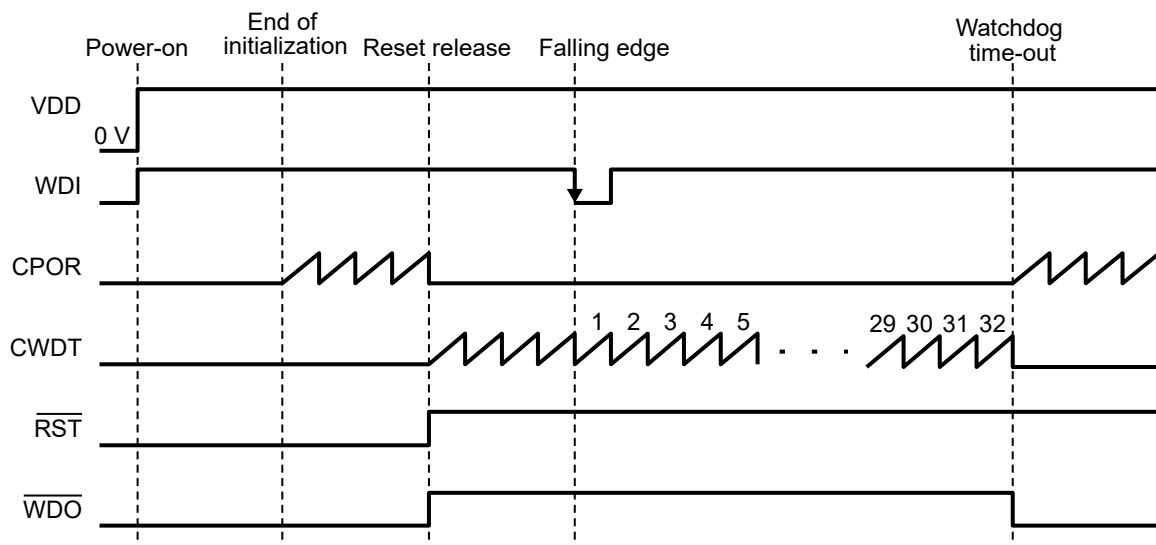


Figure 39

2.4 Counter reset due to WEN pin during the charge-discharge operation to CWDT pin

When the WEN pin changes from "H" to "L" during the charge-discharge operation to the CWDT pin, the CWDT pin performs the discharge operation. In addition, the internal counter which counts the number of times of the charge-discharge operation for the CWDT pin is also reset.

If the WEN pin changes to "H" again in this status, the CWDT pin initiates the charge-discharge operation.

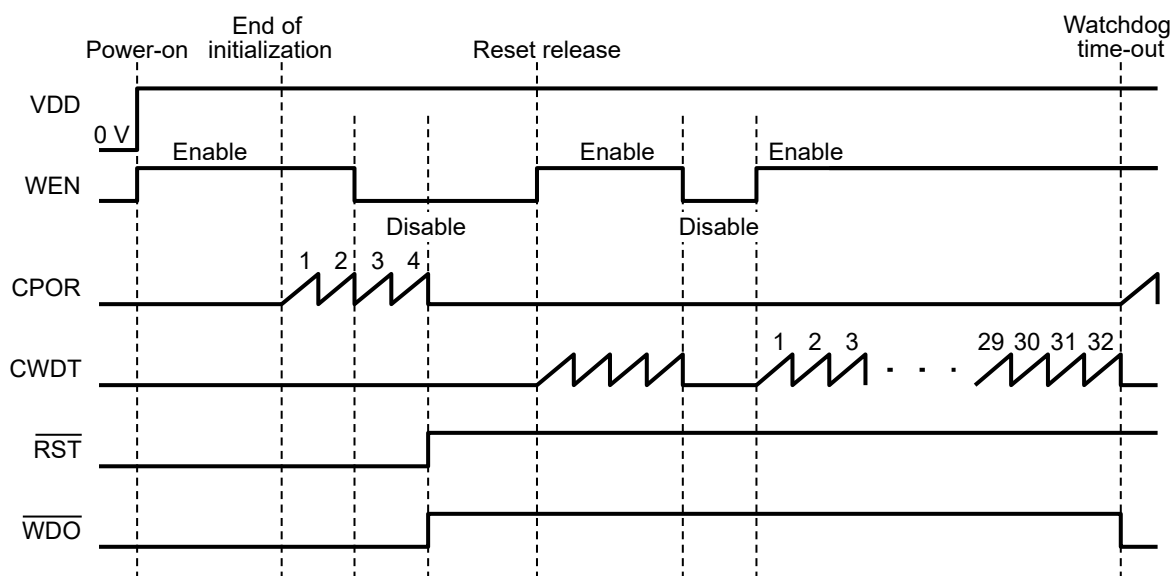


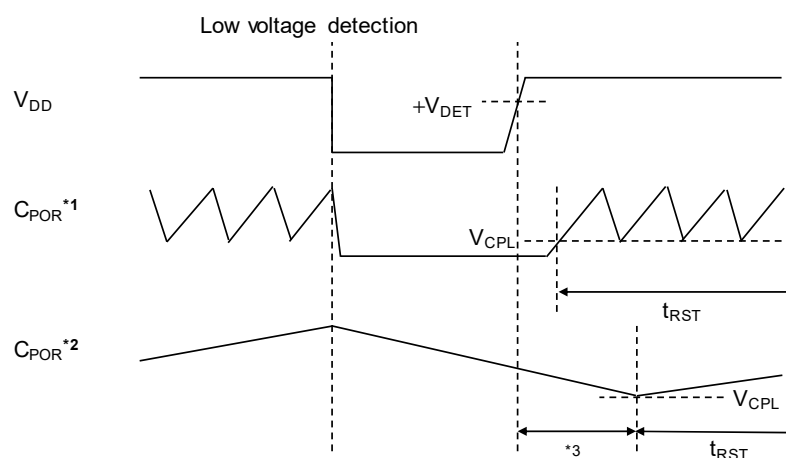
Figure 40

■ Precautions for Use

A capacitor of 100 pF to 1 μ F can be used for the adjustment capacitor for reset time-out period (C_{POR}) and the adjustment capacitor for watchdog time-out period (C_{WDT}). Even if the capacitance is within this range, cautions are still needed when the value is extremely large.

1. Low voltage operation when C_{POR} is extremely large

When the S-19405 Series detects a low voltage during the C_{POR} charge-discharge operation, it will take time for the C_{POR} discharge operation to be performed if C_{POR} is extremely large. Therefore, the discharge operation may not be completed by the time the power supply voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$). In this case, since the charge-discharge operation is performed after the discharge operation is completed, a delay time of the same length as the C_{POR} discharge operation time occurs by the time the reset time-out period (t_{RST}) count starts.



- *1. When the capacitance is sufficiently small.
- *2. When the capacitance is extremely large.
- *3. Delay time of the same length as the C_{POR} discharge operation time

Figure 41

2. Re-applying power supply

If the power supply voltage (V_{DD}) falls to 0.9 V or lower, a standby status for 20 μ s is required by the time low voltage detection is released in order for the discharge operation of internal circuit to be performed fully. If an appropriate amount of time is not secured for the standby status to be completed by the time the power supply is re-applied, the initialization start will be delayed. For this reason, a delay time of the same length as the time until the standby status has been completed occurs by the time the t_{RST} count starts after the power supply rises.

2. 1 If the time from when V_{DD} falls below 0.9 V to when it rises again is longer than 20 μ s

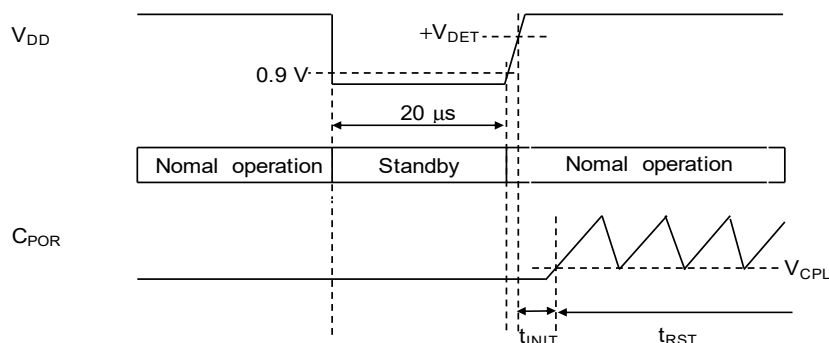
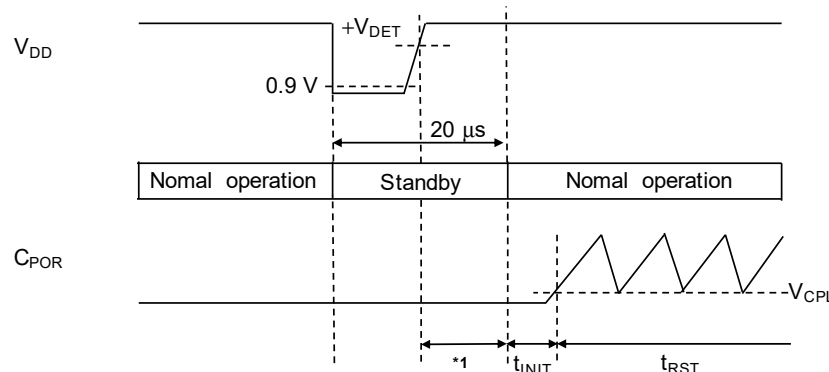


Figure 42

2. 2 If the time from when V_{DD} falls below 0.9 V to when it rises again is shorter than 20 μ s

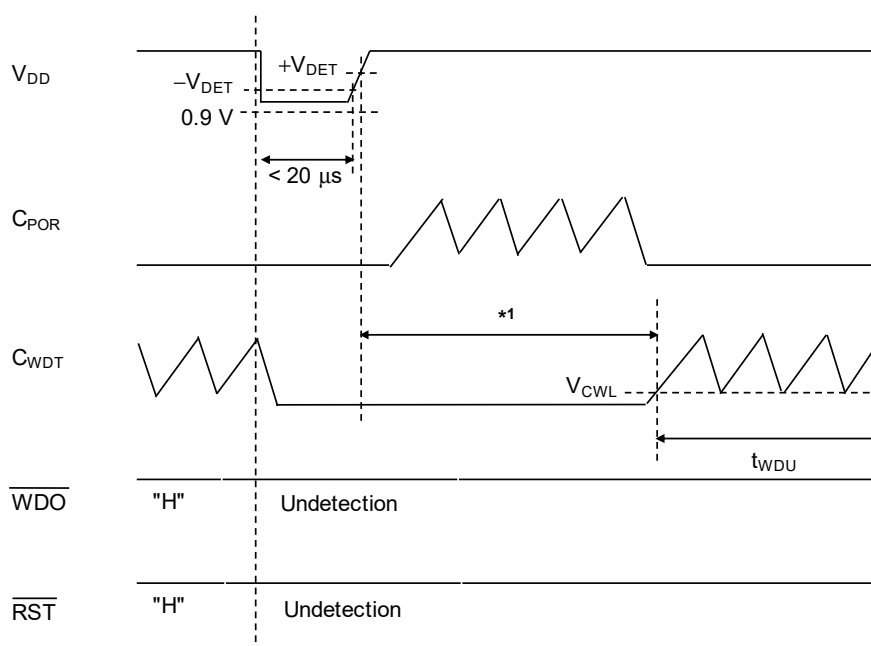


*1. Delay time of the same length as the time until standby status at power-on has been completed

Figure 43

3. Low voltage detection at instantaneous voltage drop

In the S-19405 Series, when the period of $0.9\text{ V} \leq V_{DD} \leq -V_{DET}$ is shorter than $20\text{ }\mu\text{s}$, the $\overline{\text{WDO}}$ pin and the $\overline{\text{RST}}$ pin may not output a low voltage detection signal. Even in this case, the S-19405 Series carries out the charge-discharge operation for C_{POR} in the same manner at power-on. For this reason, a delay time of the same length as the C_{POR} charge-discharge operation time occurs by the time the t_{WDU} count starts after the power supply rises.



*1. Delay time of the same length as the C_{POR} discharge operation time ($t_{INIT} + t_{RST}$)

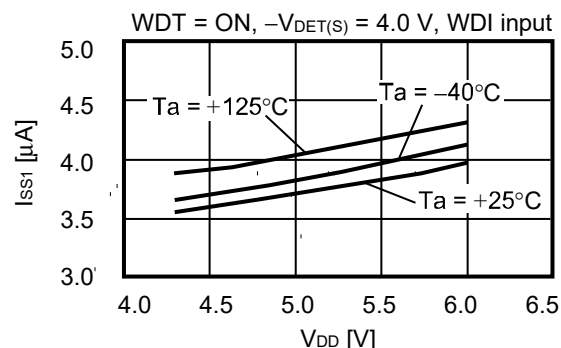
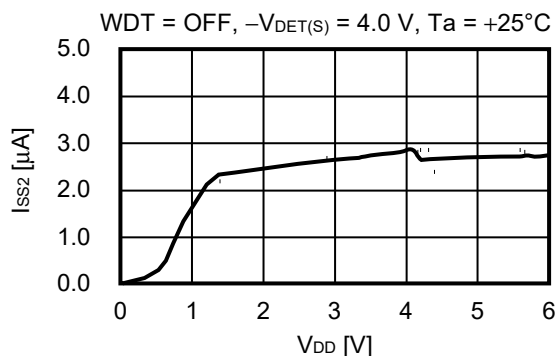
Figure 44

■ Precautions

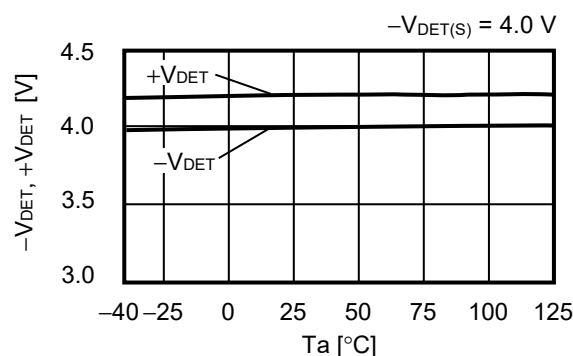
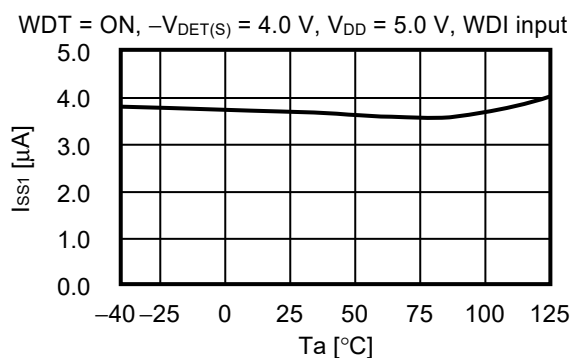
- Since input pins (the WEN pin and the WDI pin) in the S-19405 Series are CMOS configurations, make sure that an intermediate potential is not input when the S-19405 Series operates.
- Since the $\overline{\text{WDO}}$ pin and the $\overline{\text{RST}}$ pin are affected by external resistance and external capacitance, use the S-19405 Series after performing thorough evaluation with the actual application.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

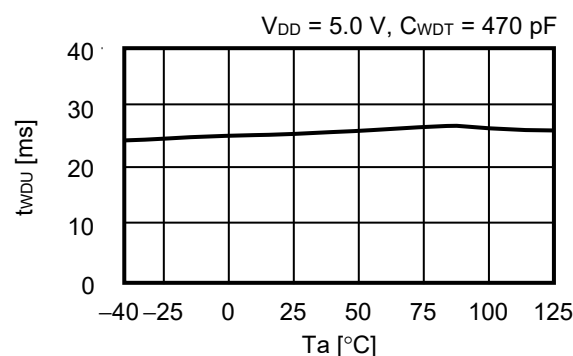
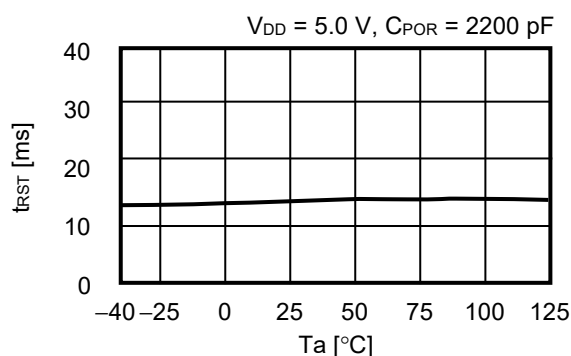
1. Current consumption during watchdog timer stop (I_{SS2}) vs. Input voltage (V_{DD})
2. Current consumption during watchdog timer operation (I_{SS1}) vs. Input voltage (V_{DD})



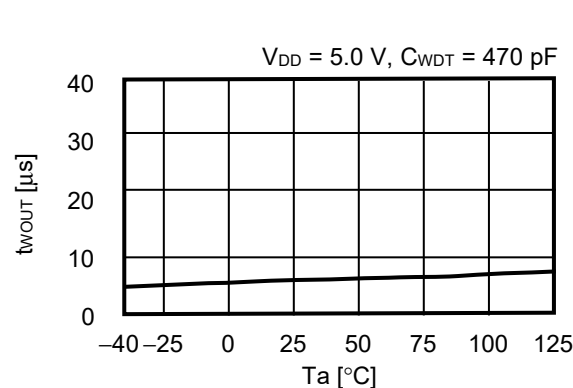
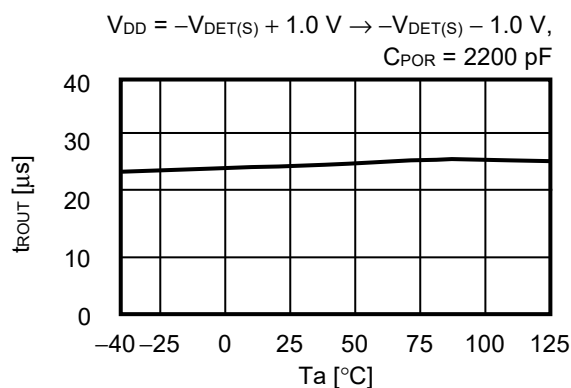
3. Current consumption during watchdog timer operation (I_{SS1}) vs. Temperature (T_a)
4. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (T_a)



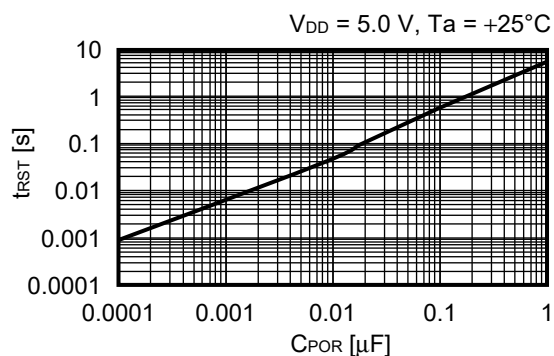
5. Reset time-out period (t_{RST}) vs. Temperature (T_a)
6. Watchdog time-out period (t_{WDU}) vs. Temperature (T_a)



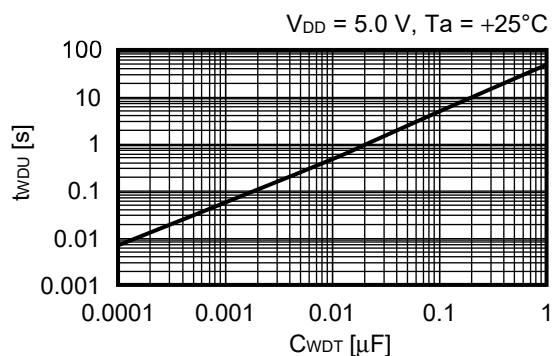
7. Reset output delay time (t_{ROUT}) vs. Temperature (T_a)
8. Watchdog output delay time (t_{WOUT}) vs. Temperature (T_a)



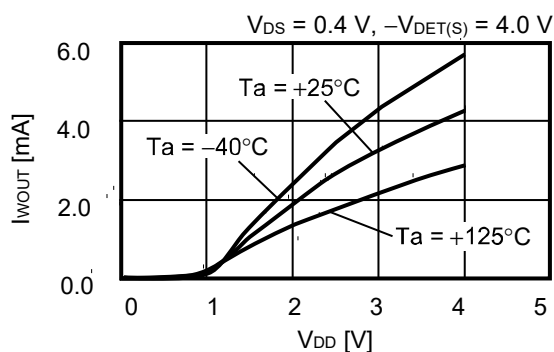
9. Reset time-out period (t_{RST}) vs. C_{POR}



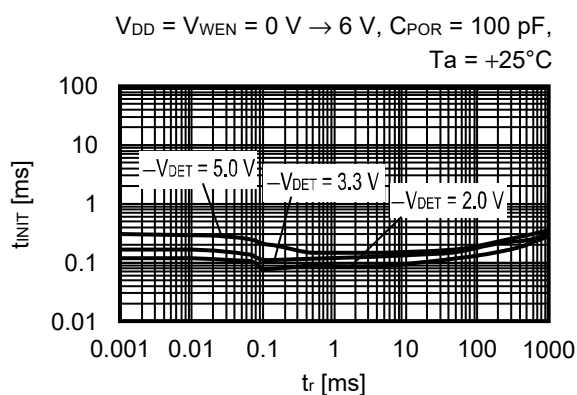
10. Watchdog time-out period (t_{WDU}) vs. C_{WDT}



11. Nch driver output current (I_{WOUT}) vs. Input voltage (V_{DD})

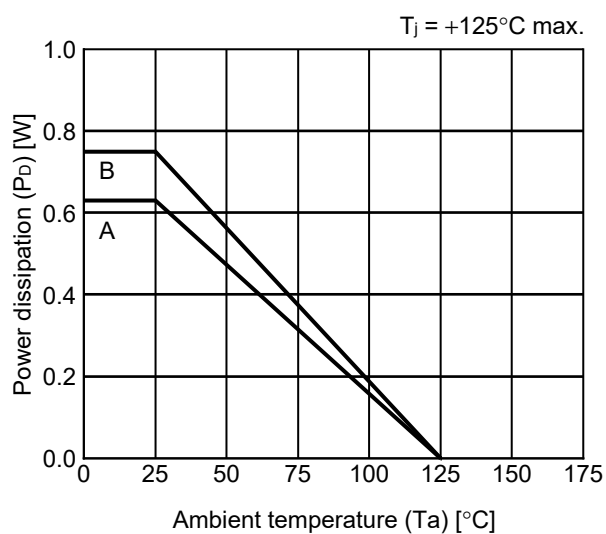


12. Initialization time (t_{INIT}) vs. Power supply voltage rise time (t_r)



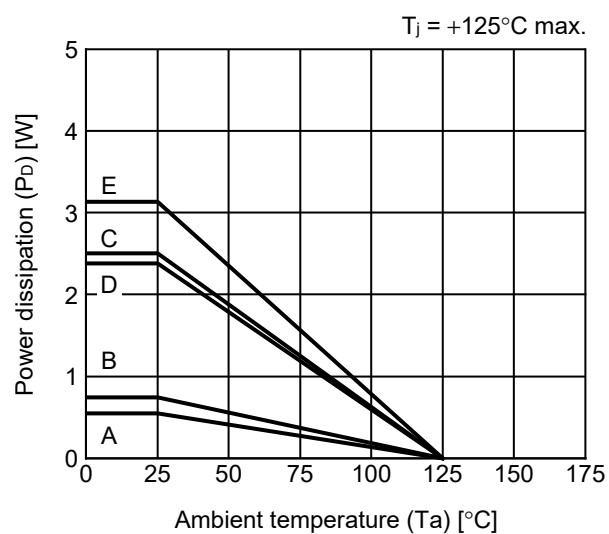
■ Power Dissipation

TMSOP-8



Board	Power Dissipation (P_D)
A	0.63 W
B	0.75 W
C	—
D	—
E	—

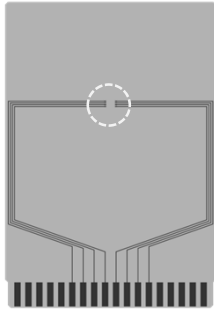
HSNT-8(2030)



Board	Power Dissipation (P_D)
A	0.55 W
B	0.74 W
C	2.50 W
D	2.38 W
E	3.13 W

TMSOP-8 Test Board

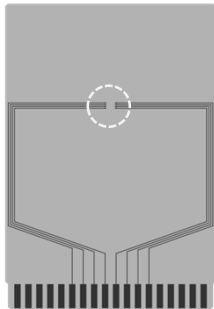
(1) Board A



 IC Mount Area

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



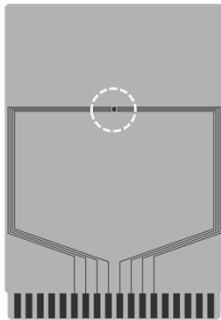
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

HSNT-8(2030) Test Board

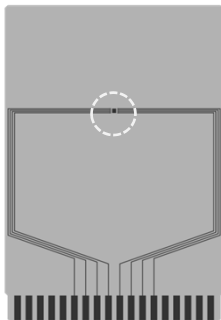
 IC Mount Area

(1) Board A



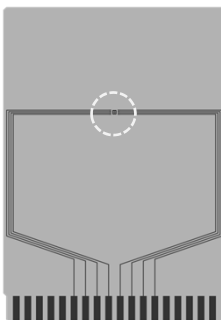
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



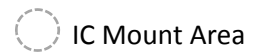
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



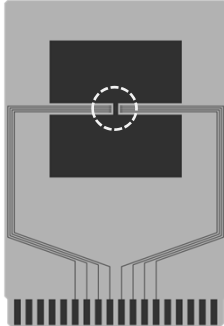
enlarged view

No. HSNT8-A-Board-SD-2.0

HSNT-8(2030) Test Board



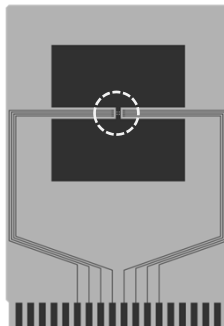
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

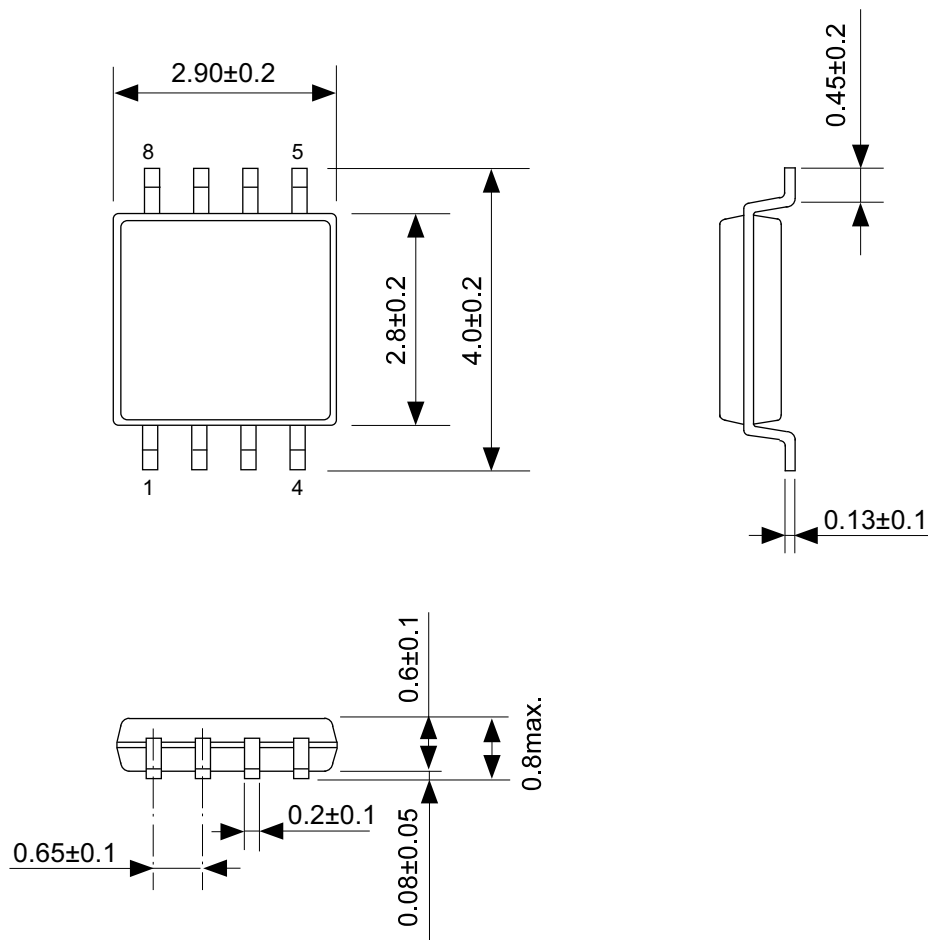
(5) Board E



enlarged view

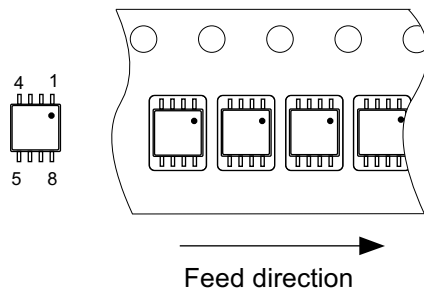
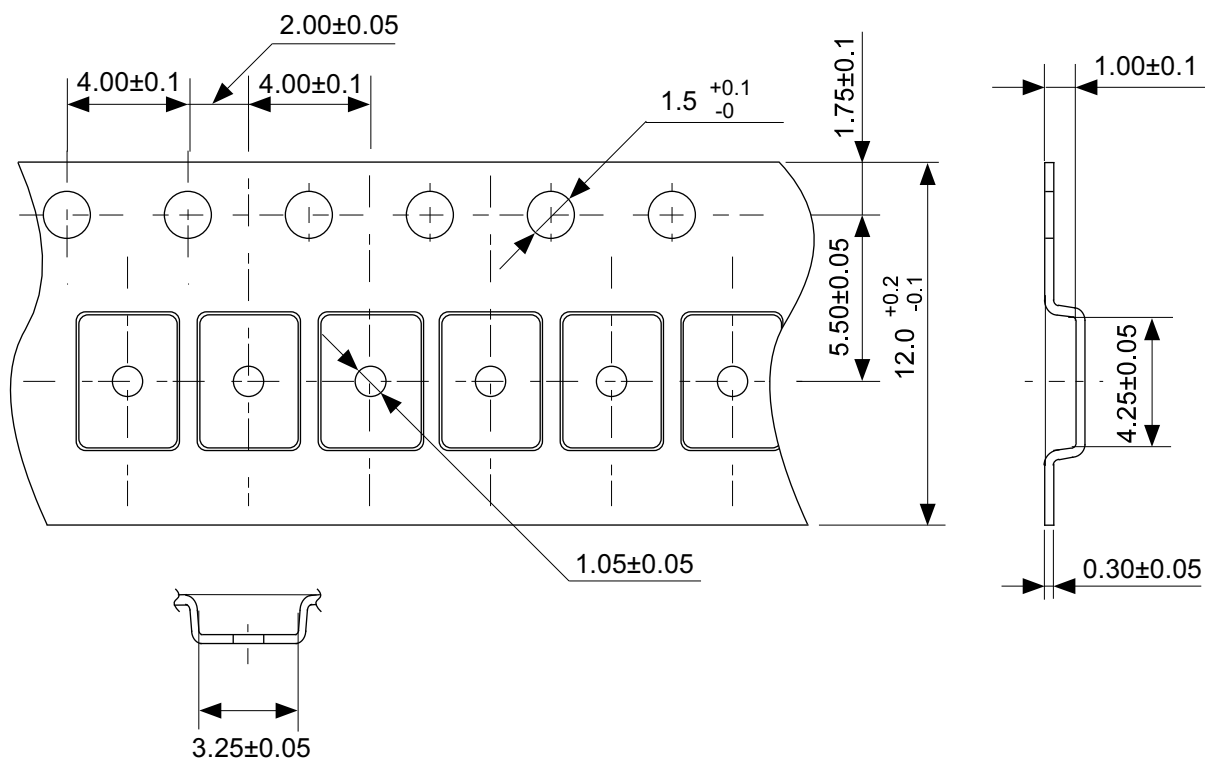
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm ² t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0



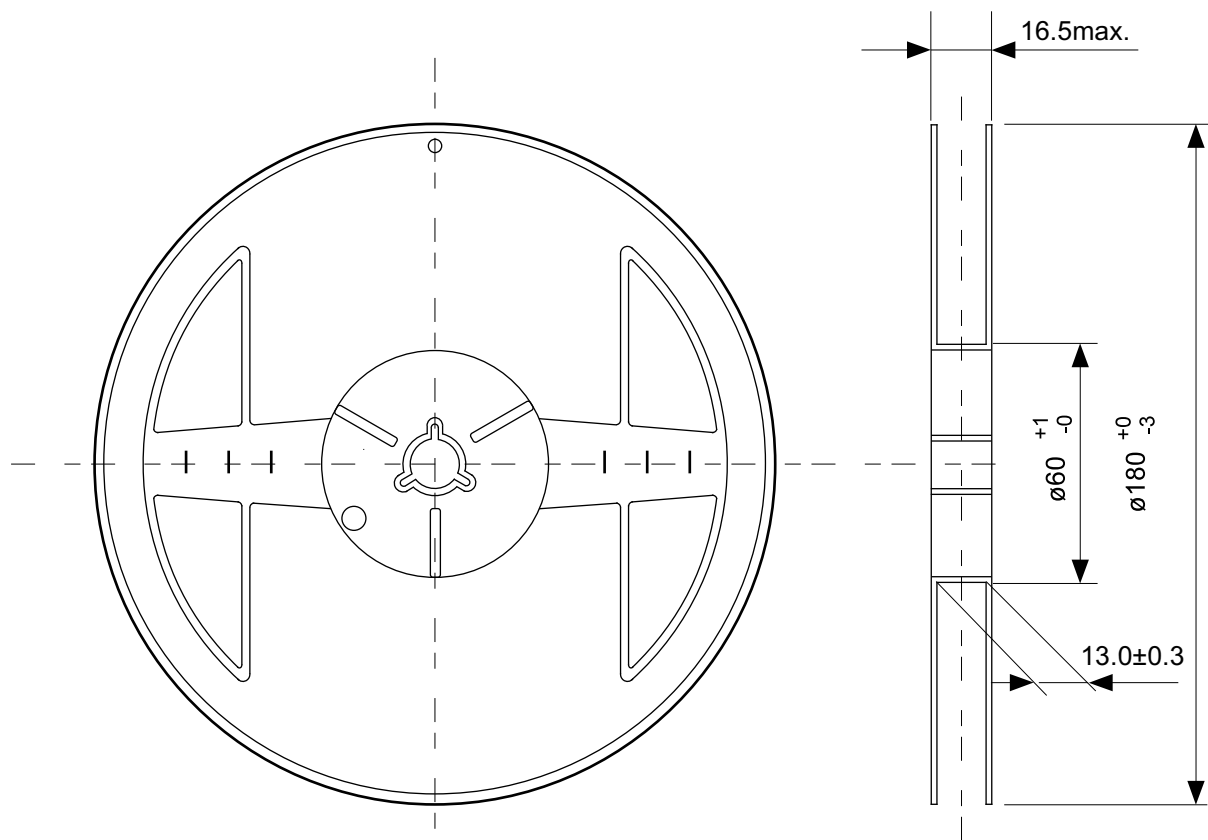
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	

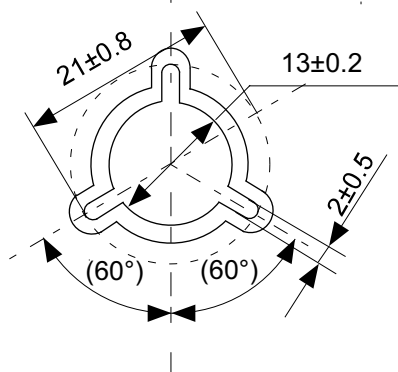


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

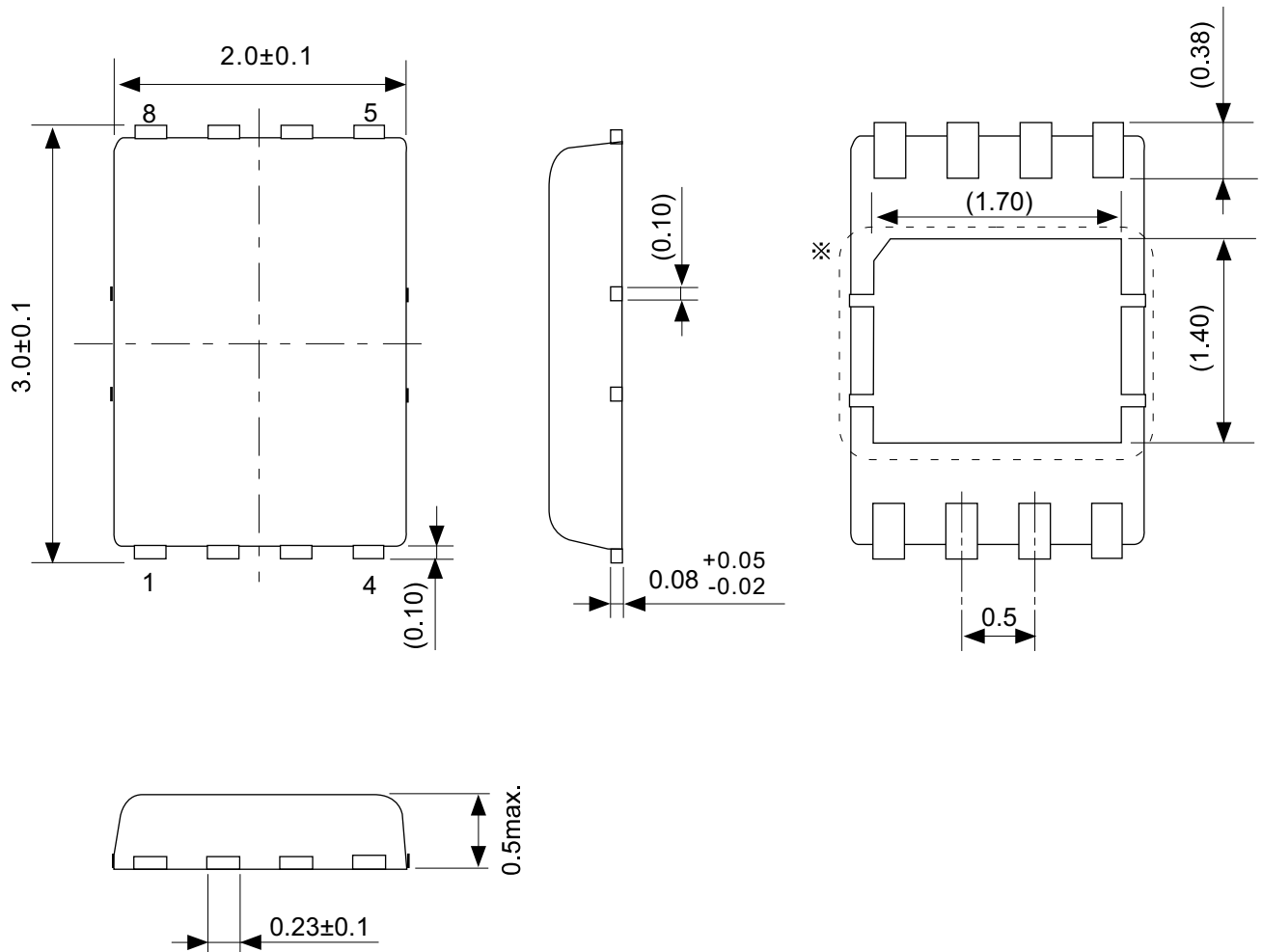


Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

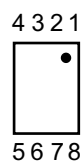
TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



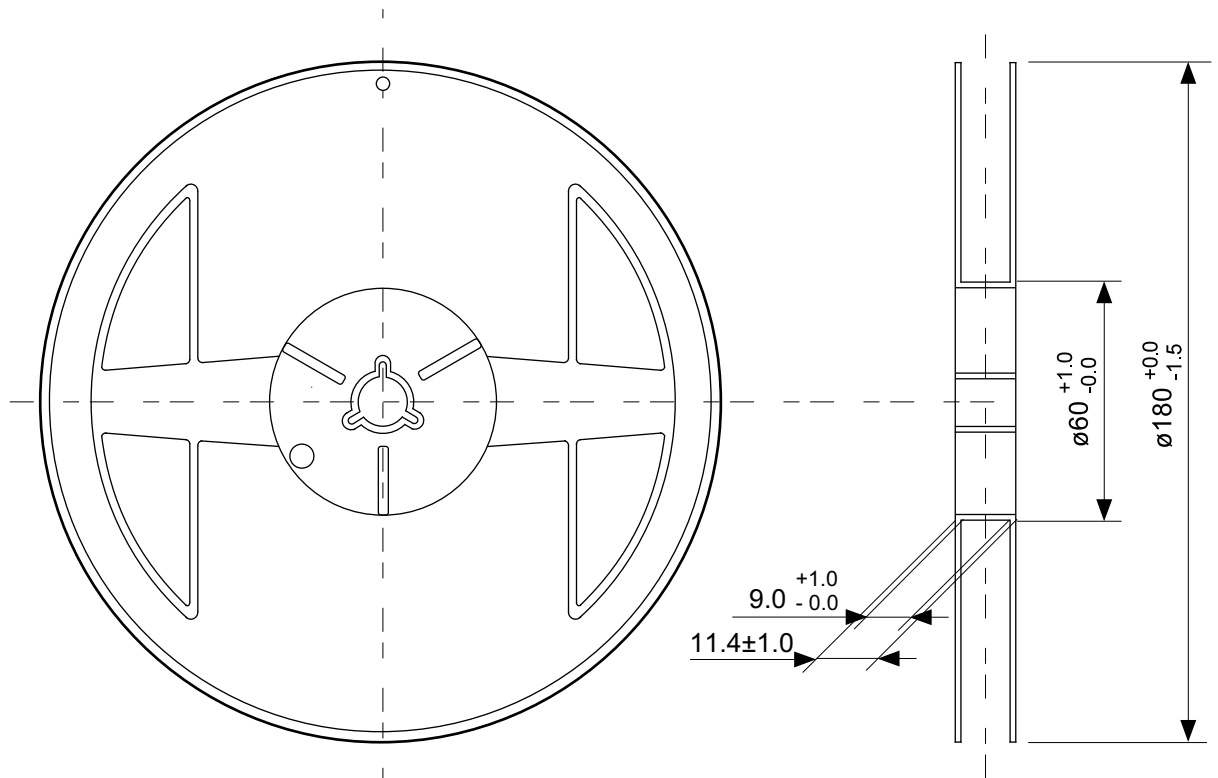
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PP008-A-P-SD-2.0

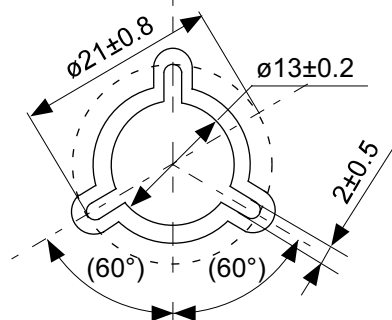
TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

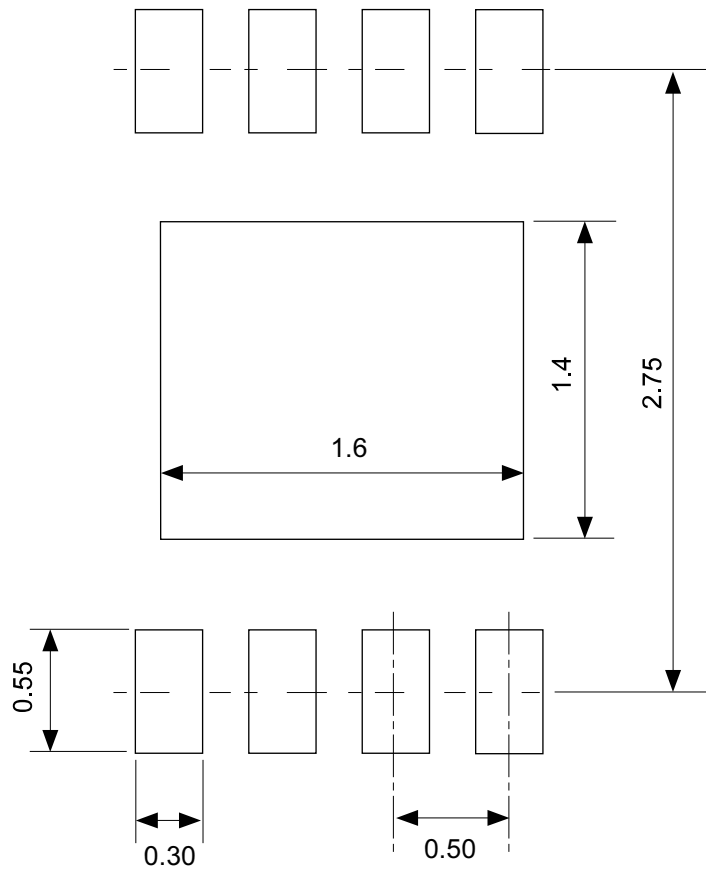


Enlarged drawing in the central part



No. PP008-A-R-SD-1.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



No. PP008-A-L-SD-1.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07