STM32C5 Nucleo-144 board (MB2310)

Introduction

The STM32C5 Nucleo-144 board based on the MB2310 reference board (order code NUCLEO-C5A3ZG) provides an affordable and flexible way for users to try out new concepts and build prototypes by choosing from the various combinations of performance and power-consumption features provided by the STM32C5 microcontroller.

The NUCLEO-C5A3ZG Nucleo-144 board offers an easy means to expand the functionality of the Nucleo open development platform with a wide choice of specialized shields through several connectors:

- ARDUINO® Uno V3 connector
- ST morpho headers providing access to the MCU I/O pins

The board contains an M.2 Key A serial memory connector connector, which allows a memory extension with Quad-SPI, Octo-SPI, or Hexadeca-SPI devices.

The NUCLEO-C5A3ZG board does not require any separate probes as it integrates the STLINK-V3EC debugger/programmer. It comes with the comprehensive free STM32 software libraries and examples available with the STM32CubeC5 MCU Package.

Figure 1. NUCLEO-C5A3ZG top view

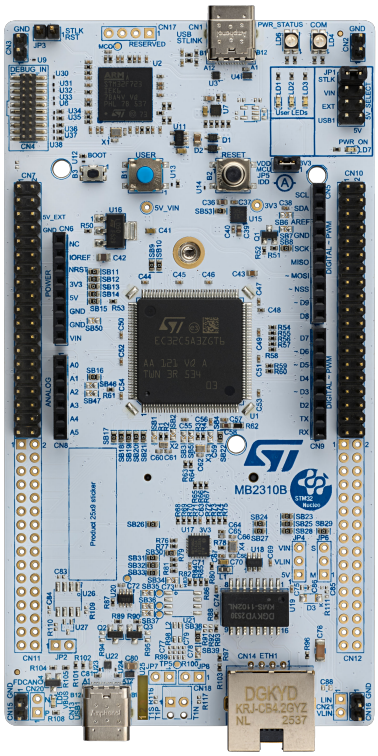
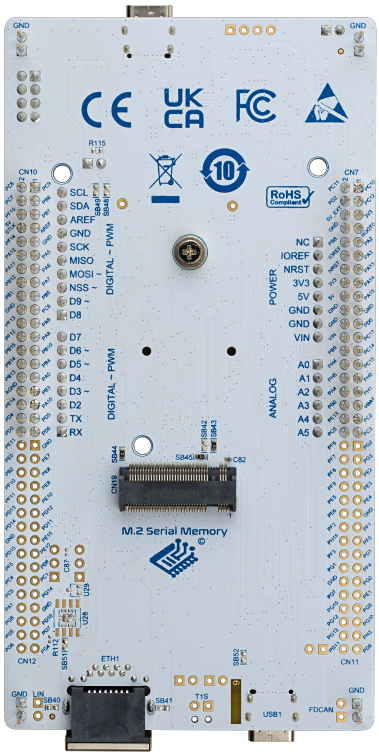


Figure 2. NUCLEO-C5A3ZG bottom view



Pictures are not contractual.

1 Features

- STM32C5A3ZGT6 microcontroller based on the Arm® Cortex®-M33 core in an LQFP144 package
- 32.768 kHz LSE crystal oscillator
- 48 MHz HSE crystal oscillator
- Three user LEDs
- Three push-buttons: user, reset, and boot
- USB Type-C® FS Sink device
- Ethernet compliant with IEEE-802.3-2002
- Board connectors:
  - USB Type-C® connector
  - M.2 Key A serial memory connector
  - MIPI20 connector for debugging (SWD, JTAG, 4-bit Trace)
  - 10/100 Mbit/s Ethernet connector
  - ARDUINO® Uno V3 connector
  - ST morpho expansion connectors for full access to most the STM32 I/Os
- Flexible power-supply options: ST-LINK USB V_{BUS}, USB connector, or external sources
- On-board STLINK-V3EC debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeC5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

arm

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2 Ordering information

To order the NUCLEO-C5A3ZG Nucleo-144 board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board references	Target STM32
NUCLEO-C5A3ZG	MB2310[1]	STM32C5A3ZGT6

1. *Subsequently called main board in the rest of the documentation.*

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

NUCLEO-XXYYZT	Description	Example: NUCLEO-C5A3ZG
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32C5 series
YY	MCU product line in the series	STM32C59x/5A3 product line
Z	STM32 package pin count: • Z for 144 pins	144 pins
T	STM32 flash memory size: • G for 1 Mbyte	1 Mbyte

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10 or 11, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to USB Type-C® cable

Note: *macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.*

Linux® is a registered trademark of Linus Torvalds.

Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

3.4 EDA resources

All board design resources, including schematics, EDA databases, manufacturing files, and the bill of materials, are available from the NUCLEO-C5A3ZG product page at *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between pin 1 and pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Safety recommendations

5.1 Targeted audience

This product targets users with at least basic electronics or embedded software development knowledge like engineers, technicians, or students.

This board is not a toy and is not suited for use by children.

5.2 Handling the board

This product contains a bare printed circuit board and like all products of this type, the user must be careful about the following points:

- The connection pins on the board might be sharp. Be careful when handling the board to avoid injury.
- This board contains static sensitive devices. To avoid damaging it, handle the board in an ESD-proof environment.
- While powered, do not touch the electric connections on the board with your fingers or anything conductive. The board operates at a voltage level that is not dangerous, but components might be damaged when shorted.
- Do not put any liquid on the board and avoid operating it close to water or at a high humidity level.
- Do not operate the board if it is dirty or dusty.
- The pins of the board are exposed and must not come into contact with a metal surface, as this can produce a short circuit and damage the board.

5.3 Delivery recommendations

Before the first use, inspect the board for any damage that may have occurred during shipment. Ensure that all socketed components are securely fixed in their sockets and that nothing is loose in the plastic bag.

5.4 Power supply

A power supply unit or auxiliary equipment complying with the EN 62368-1:2014+A11:2017 standard (or the one replacing it) and safety extralow voltage (SELV/ES1) with limited power capability (LPS/PS2) must power this equipment.

6 Quick start

The NUCLEO-C5A3ZG board is a low-cost and easy-to-use development kit, to evaluate quickly and start development with an STM32C5A3ZGT6 microcontroller in a LQFP144 package.

Before installing and using the product, accept the evaluation product license agreement from the *www.st.com/epla* webpage. For more information on the NUCLEO-C5A3ZG board and demonstration software, visit the *www.st.com/stm32nucleo* webpage.

6.1 Getting started

Follow the sequence below to configure the NUCLEO-C5A3ZG Nucleo-144 board and launch the demonstration application (refer to Figure 5. NUCLEO-C5A3ZG top layout for component locations):

1. Check the jumper position on the board (refer to Section 6.2 for the default board configuration).
2. Connect the NUCLEO-C5A3ZG board to a PC using a USB cable (USB Type-A or USB Type-C® to USB Type-C®) and the ST-LINK USB connector (CN1) to power the board.
3. The PWR_ON (LD7), COM (LD4), and PWR STATUS (LD6) LEDs light up and the three user LEDs (LD1, LD2,and LD3) are blinking.
4. Press the blue user button (B1) and observe how the blinking of the user LEDs (LD1, LD2,and LD3) changes.
5. Download the demonstration software and several software examples to use the STM32 Nucleo features, available from the *st.com* website.
6. Develop a custom application using the available examples.

6.2 Default board configuration

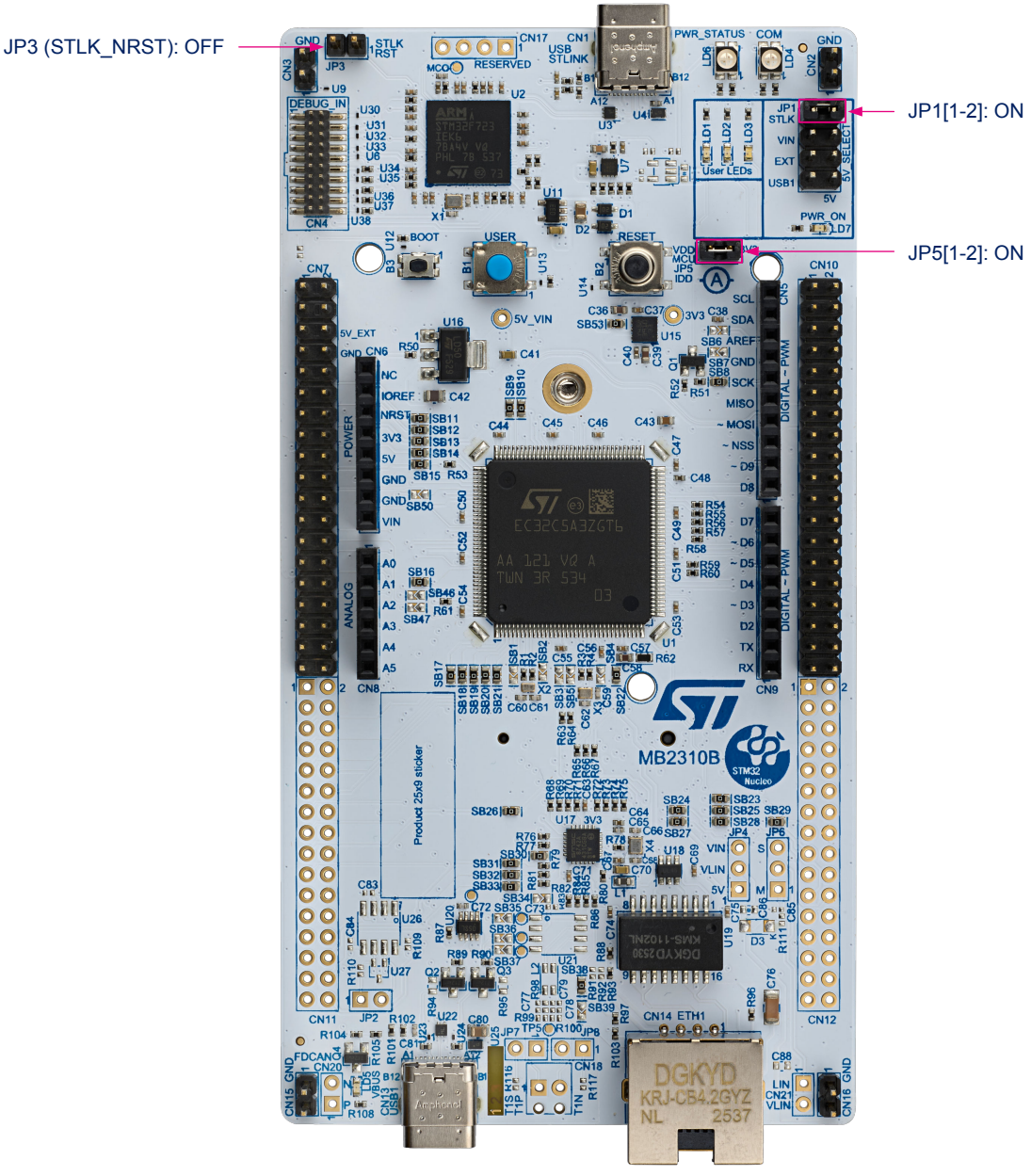
By default, the NUCLEO-C5A3ZG board is configured with STLINK-V3EC power. The different jumper configurations and voltage settings are shown in Table 4.

Table 4. Jumper configuration

Jumper	Definition	Position	Comment
JP1	5 V power selection (user USB power source selection)	**[1-2]**	**5 V from STLINK-V3EC**
		[3-4]	5 V source from ARDUINO® VIN 7-12 V
		[5-6]	5 V source from ST morpho connector 5V_EXT
		[7-8]	5 V source from USB Type-C®
		OFF	No 5 V power source; configuration when external 3V3 power source is used
JP3	STLK_RST	ON [1-2]	Used to keep the STLINK-V3EC MCU in reset state when an external debug probe is used
		OFF	**Normal mode: uses STLINK-V3EC debug probe**
JP5	IDD measurement	**ON [1-2]**	**VDD_MCU = 3V3**
		OFF	Use ammeter to measure VDD_MCU power consumption, or external 3V3 source can be connected to pin 2 (STLINK-V3PWR tools with STM32CubeMonitor-Power or ULPBench probe, for example)

1. *The default configuration is shown in bold.*
2. *It is recommended to select only one 5 V power source.*

Figure 3. Default board configuration



7 Hardware layout and configuration

The NUCLEO-C5A3ZG board is designed around the STM32C5A3ZGT6 microcontroller in an LQFP144 package. Figure 4 shows the connections between the STM32 and its peripherals. Figure 5 and Figure 6 show the location of these features on the NUCLEO-C5A3ZG board. The mechanical dimensions of the board are shown in Figure 7.

7.1 Hardware layout

Figure 4. NUCLEO-C5A3ZG block diagram

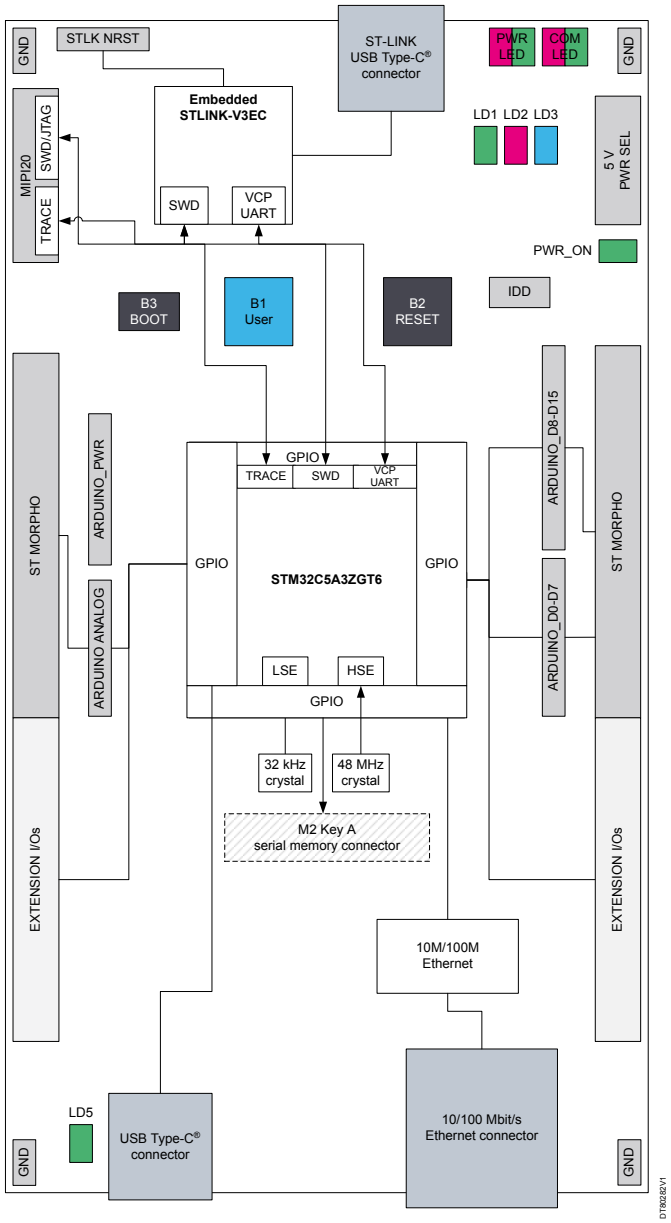


Figure 5. **NUCLEO-C5A3ZG top layout**

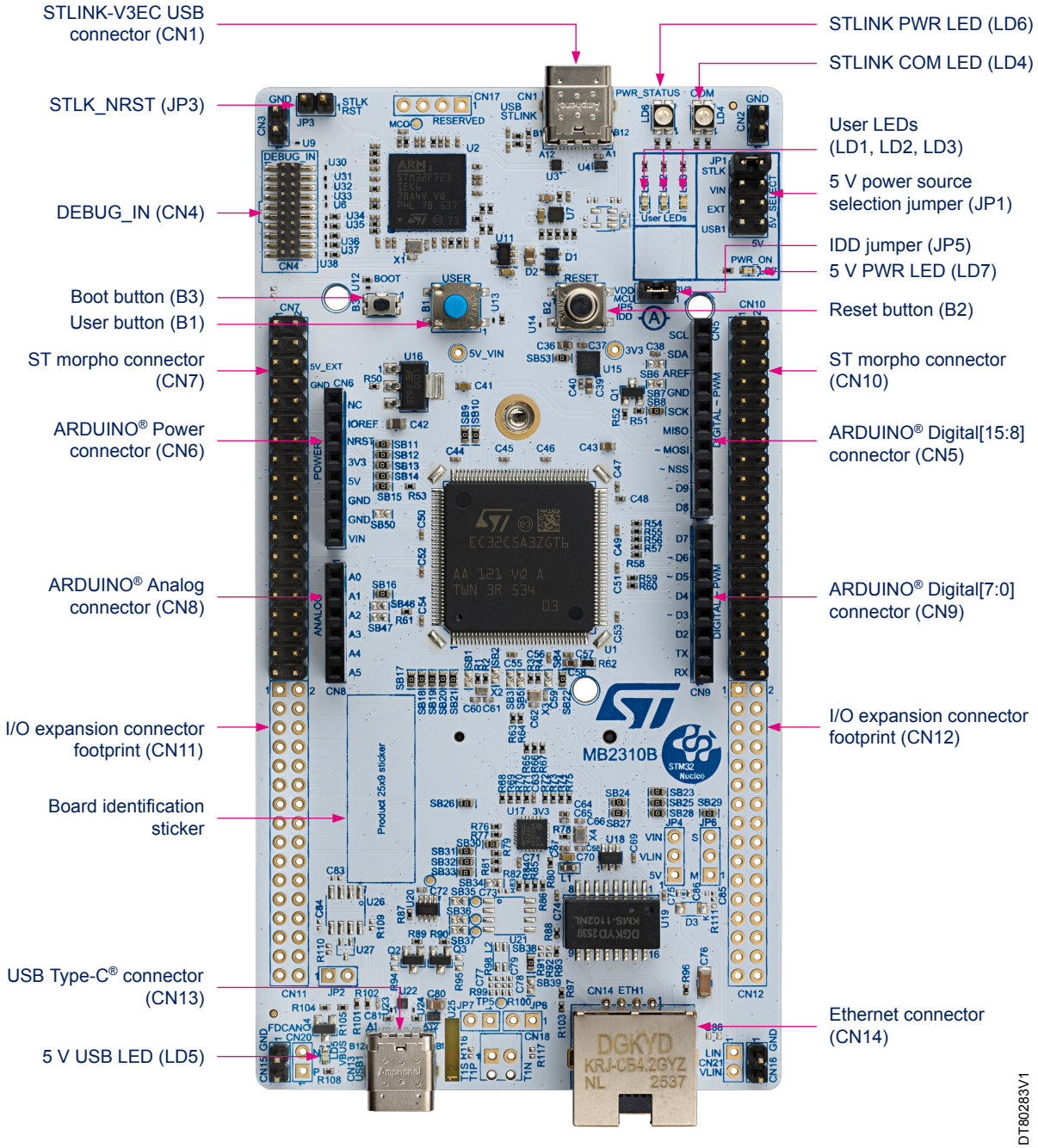
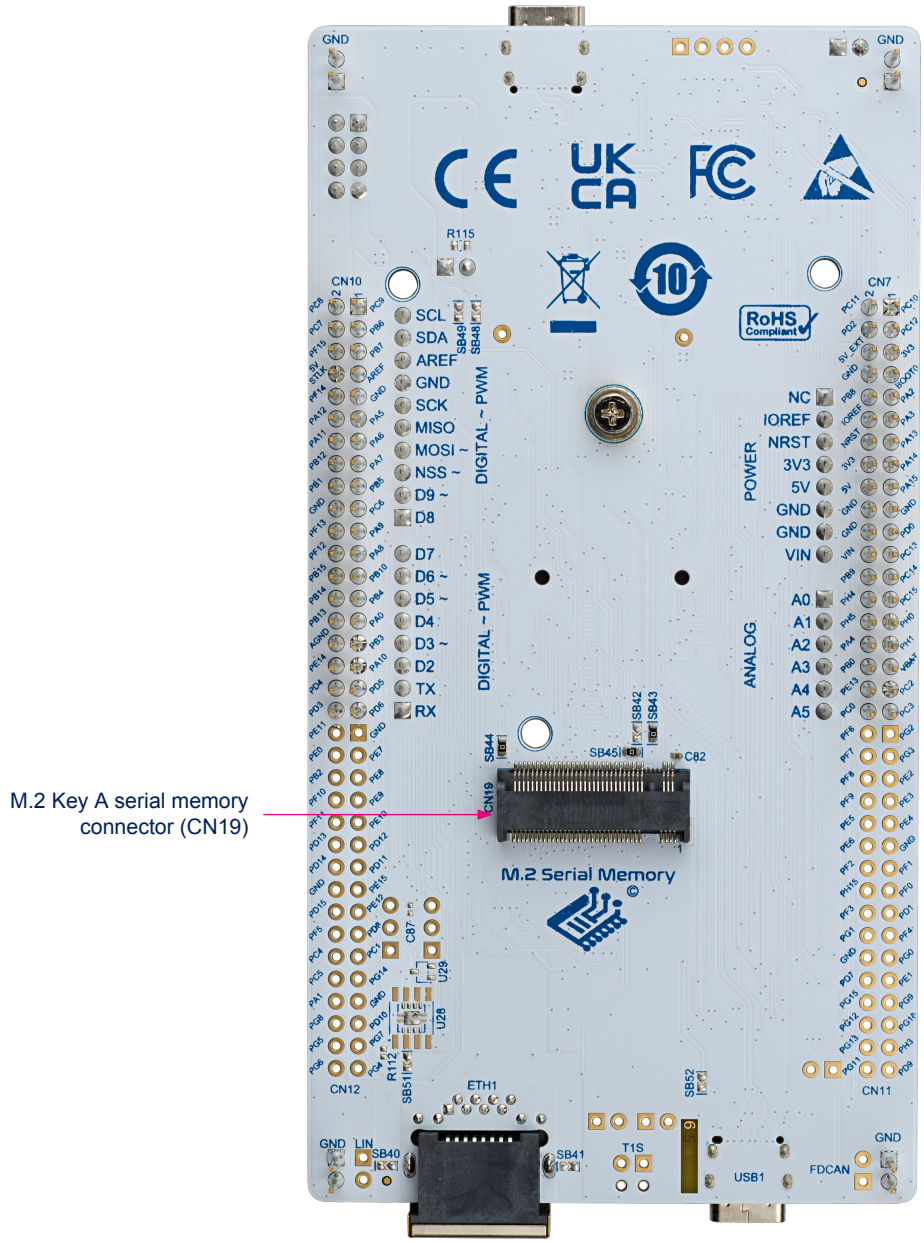


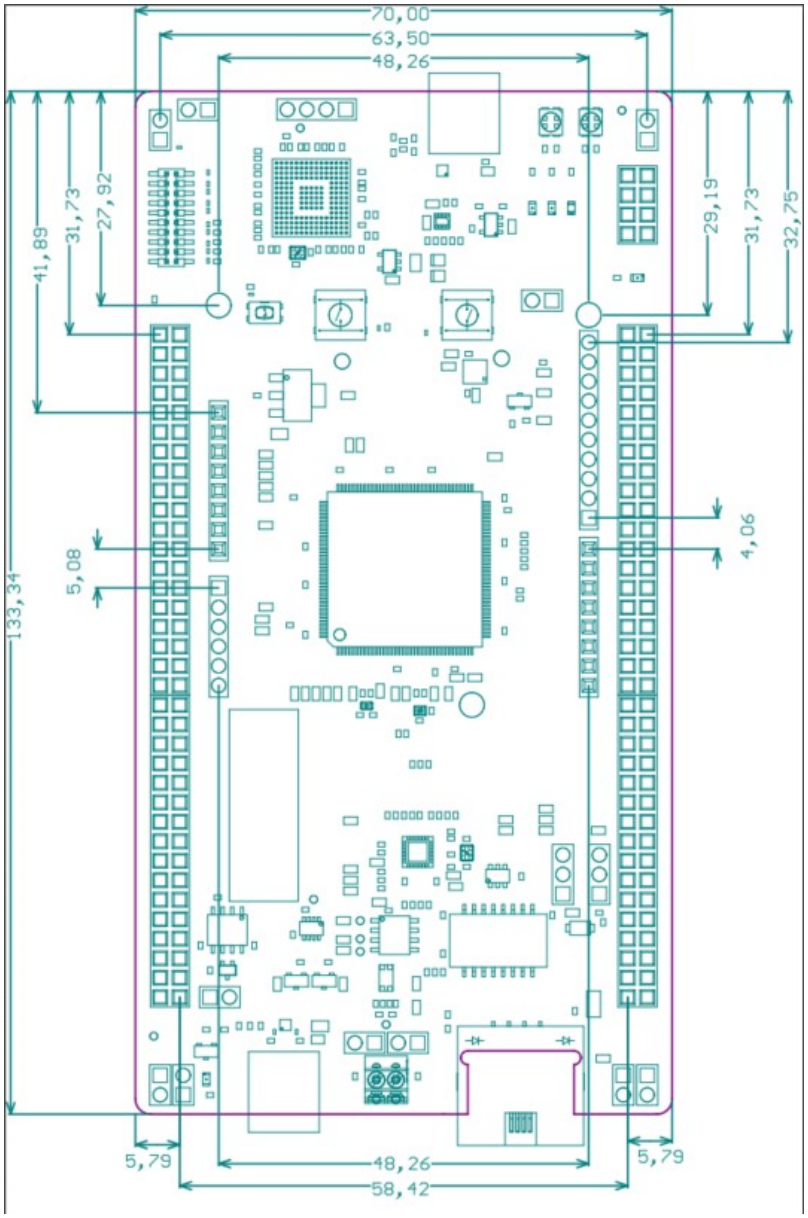
Figure 6. NUCLEO-C5A3ZG bottom layout



DT80284V1

7.2 Mechanical dimensions

Figure 7. **Board mechanical drawing (in millimeters)**



7.3 Embedded STLINK-V3EC

This chapter provides information about the implementation of the embedded STLINK-V3EC on this NUCLEO-C5A3ZG Nucleo-144 board.

For further details on ST-LINK capabilities, LED management, and driver and firmware for STLINK-V3EC, refer to the technical note *Overview of ST-LINK derivatives* (TN1235).

For more information about the debugging and programming features of STLINK-V3EC, refer to the user manual *STLINK-V3SET debugger/programmer for STM8 and STM32* (UM2448).

7.3.1 Description

There are two different ways to program and debug the onboard STM32 MCU:

- Using the embedded STLINK-V3EC.
- Using an external debug tool connected to the DEBUG_IN connector base on the MIPI20 pinout (SWD/JTAG/TRACE).

Refer to Table 4. Jumper configuration for details on how to switch between STLINK-V3EC and an external debug probe using JP3.

The STLINK-V3EC tool for debugging and programming is integrated into this NUCLEO-C5A3ZG Nucleo-144 board. It provides the following features:

- 5 V/500 mA power supplied by the USB Type-C® connector (CN1)
- USB 2.0 high-speed compatible interface
- JTAG and Serial Wire Debug (SWD) with Serial Wire Viewer (SWV)
- Virtual COM port (VCP)
- 3.3 V application voltage
- Tricolor (green, orange, and red) COM status LED (LD4) that blinks during communication with the PC
- Tricolor (green, orange, and red) power status LED (LD6) that provides information about the STLINK-V3EC target power
- USB Type-C® overvoltage protection (U7) with current limitation

7.3.2 Drivers

Driver installation is not required for Windows® 10 or later. However, installing the driver assigns an ST-specific name to the ST-LINK COM port in the system device manager.

7.3.3 Firmware upgrade

STLINK-V3EC includes a firmware upgrade mechanism (stsw_link007) through the USB port. The firmware can change during the STLINK-V3EC lifetime, to add new features, correct errors, and support new microcontroller families. Visit the www.st.com website regularly and before using this board to stay up to date with the latest firmware version.

7.3.4 Using an external debug tool to program and debug the on-board STM32

When using the external debug connector (CN4), it is possible to supply power to the STM32 Nucleo-144 board through the STLINK-V3EC USB connector (CN1) or another power supply source, as described in Section 7.4: Power supply.

It is not mandatory to set the STLINK-V3EC to reset mode (JP3: ON) when using an external debug probe on CN4. However, it is possible to set the STLINK-V3EC to reset mode by putting a jumper on JP3. This configuration makes it impossible to power the board through the STLINK-V3EC USB connector (CN1) or to debug using the STLINK-V3EC. Select another 5 V power source on JP1 and connect an external debugger to CN4.

Figure 8 shows the location of the different STLINK-V3EC components on the NUCLEO-C5A3ZG Nucleo-144 board required for connecting an external debug tool. Table 5 provides the pinout for the MIPI20 debug connector.

Note: The DEBUG_IN interface, which is based on the MIPI20 TRACE connector, supports a 3.3 V target reference voltage. When using the external DEBUG_IN connector (CN4), the STLINK-V3EC can supply power to the board through the CN1 USB Type-C® connector.

Figure 8. Connecting an external debug tool

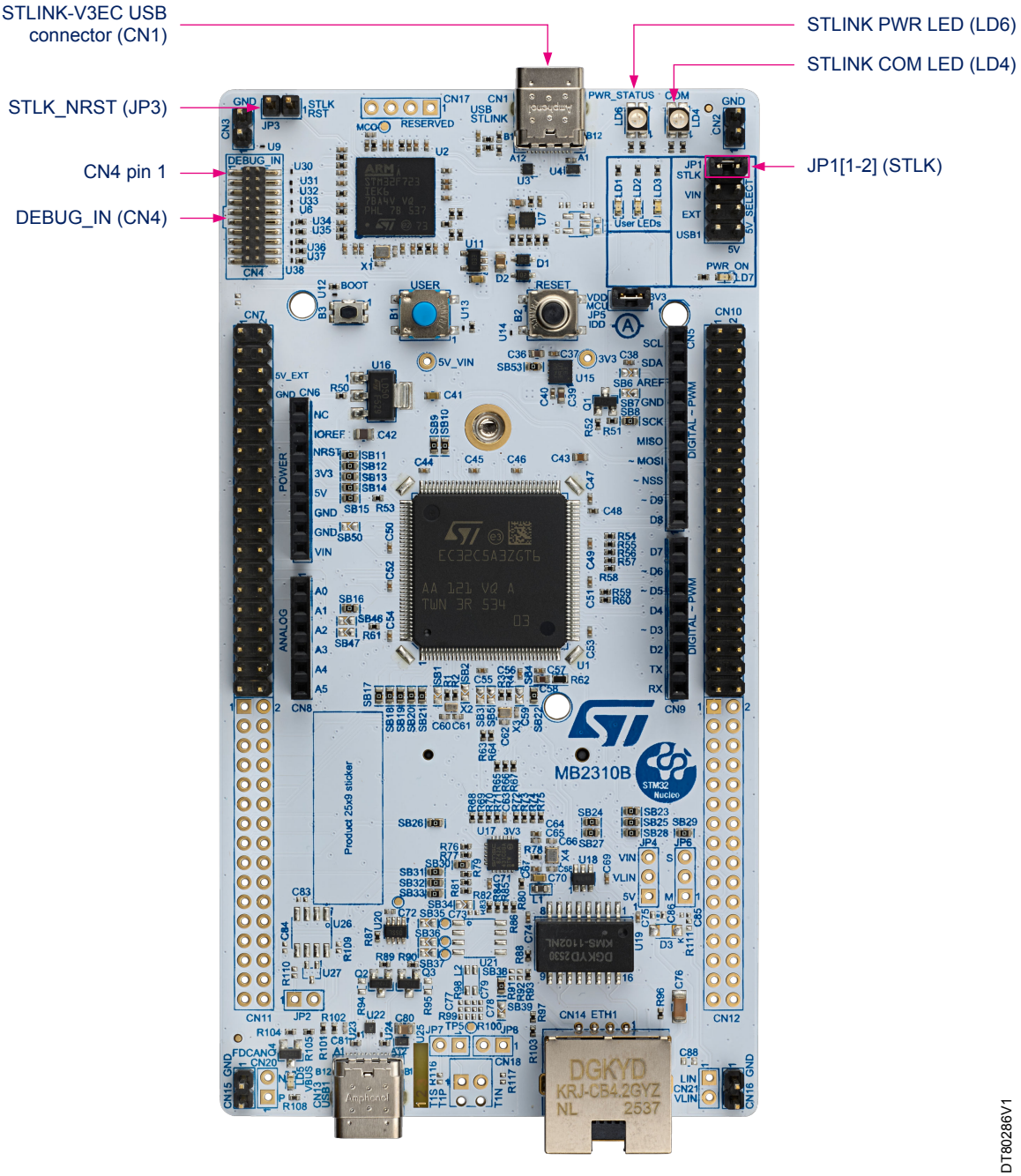


Table 5. MIPI20 debug connector (CN4) pinout

MIPI20 pin	CN4	Designation
1	VTref	Target reference voltage (fed from 3V3)
2	SWDIO/JTMS	Target SWDIO using SWD protocol or target JTMS using JTAG protocol
3	GND	Ground
4	SWCLK/JTCK	Target SWCLK using SWD protocol or target JTCK using JTAG protocol
5	GND	Ground
6	SWO/JTDO	Target SWO using SWD protocol or target JTDO using JTAG protocol
7	KEY	Not connected
8	JTDI	Not used by SWD protocol, target JTDI using JTAG protocol
9	GND	Ground
10	NRST	Target NRST
11	TgtPwr	5 V target power to the target MCU; not used, to be disconnected (R46 OFF)
12	TRACECLK	Trace CLK
13	TgtPwr	5 V target power to the target MCU; not used, to be disconnected (R46 OFF)
14	TRACED0	Trace Data0
15	GND	Ground
16	TRACED1	Trace Data1
17	GND	Ground
18	TRACED2	Trace Data2
19	GND	Ground
20	TRACED3	Trace Data3

7.4 Power supply

7.4.1 Power source selection

The NUCLEO-C5A3ZG Nucleo-144 board can take any of the following sources as its power supply:

- A host PC or a wall charger connected to CN1 through a USB cable (STLK default configuration).
- An external 7 to 12 V power supply from the ARDUINO Uno V3 (CN6) or ST morpho (CN7) connector (VIN), with a 5 V adaptation from LDO (U16).
- An external 5 V power supply from the ST morpho connector (CN7 pin 6; 5V_EXT).
- An external 5 V USB charger connected to the STLINK-V3EC USB Type-C® connector (CN1).
- A host PC connected to the USB Type-C® connector (CN13).
- 3V3 from the ST morpho connector (CN7 pin 5, or the 3.3 V test point).

The power supply for the STM32 Nucleo-144 board can be provided by the host PC through the USB cable, or by an external source: VIN (7 to 12 V), E5V (5 V), or 3.3 V power supply pins on CN6 or CN7. If the power supply is 3.3 V, STLINK-V3EC is not powered and cannot be used.

Note: To power the STM32 Nucleo-144 board and the associated shield, use a power source that supports up to 5 V at 500 mA, or 3.3 V at 500 mA for the 3.3 V use case.

The power supply capabilities are summarized in Table 6.

Table 6. Power source capability

Power supply	Connector pins	Voltage range	Recommended current	Limitation
5V_STLK	CN1 USB connector JP1[1-2]	4.75 to 5.25 V	500 mA	Maximum current depending on the presence or absence of USB enumeration: • 100 mA without enumeration. • 500 mA with enumeration.
VIN/5V_VIN	CN6 pin 8 CN7 pin 24 JP1[3-4]	7 to 12 V	500 mA	From 7 to 12 V only; input current capability is linked to input voltage: • 800 mA input current when V_{IN}=7V. • 450 mA input current when 7 V < V_{IN} < 9 V. • 250 mA input current when 9 V < V_{IN} < 12 V.
5V_EXT	CN7 pin 6 JP1[5-6]	4.75 to 5.25 V	1 A	The maximum current depends on the power source. 1 A maximum is recommended for this board.
USB1	CN13 USB connector JP1[7-8]	4.75 to 5.25 V	1 A	The maximum current depends on the presence or absence of USB enumeration and the USB power source capacity used to power the board.
External 3V3	CN7 pin 5 3V3 test point	3 to 3.6 V	500 mA	The maximum current depends on the 3V3 source. With external 3.3 V, STLINK-V3EC is not powered and cannot be used.
VDD_MCU	JP5 pin 2	2.7 to 3.6 V	500 mA	It is possible to power only the MCU power supply pins by applying a voltage source on JP5 pin 2 (VDD_MCU). External functions, like debug, LEDs, or expansion connectors are not powered. This option can be used for MCU power consumption measurement.

5V_STLK

The NUCLEO-C5A3ZG Nucleo-144 board and shield can be powered from the STLINK-V3EC connector CN1 (5 V, 500 mA).To select the 5V_STLK power source, fit the 5 V power selection jumper (JP1) on pins 1 and 2 (STLK), as shown in Figure 9. This is the default configuration.

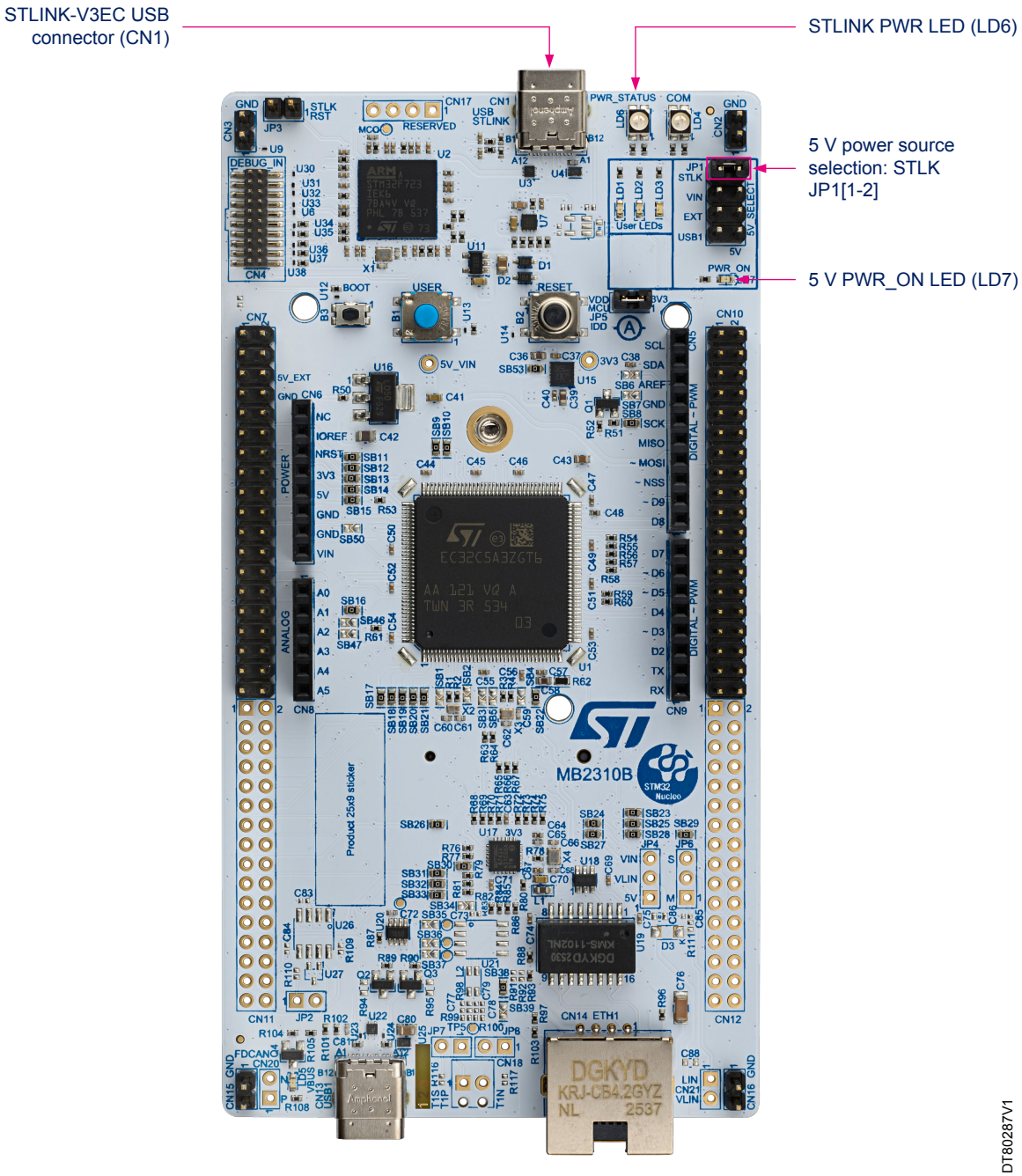
If the USB enumeration succeeds, the 5V_STLK power is enabled by asserting the T_PWR_EN signal from STLINK-V3EC. This pin is connected to a power switch (U7), which powers the board. This power switch also features a current limitation, to protect the PC in case of an onboard short circuit. If an overcurrent condition (current greater than 500 mA) occurs, the POWER status LED (LD6) lights up in red.

The NUCLEO-C5A3ZG Nucleo-144 board and its shield can be powered by the STLINK-V3EC USB connector (CN1). If the host can provide the required power, the power switch (U7) is enabled and the green LED (LD7) is turned on. The board and its shield can consume up to 500 mA.

If the host cannot provide the requested current, enumeration fails. The power switch (U7) remains OFF, and the MCU, including the extension board, is not powered. Consequently, the green LED (LD7) remains off. In this case, use an external power supply.

Warning: *If the maximum current consumption of the NUCLEO-C5A3ZG Nucleo-144 board and its shield boards exceeds 500 mA, power the board using an external power supply connected to VIN, EXT, or USB1.*

Figure 9. **JP1 [1-2]: 5V_STLK power source**

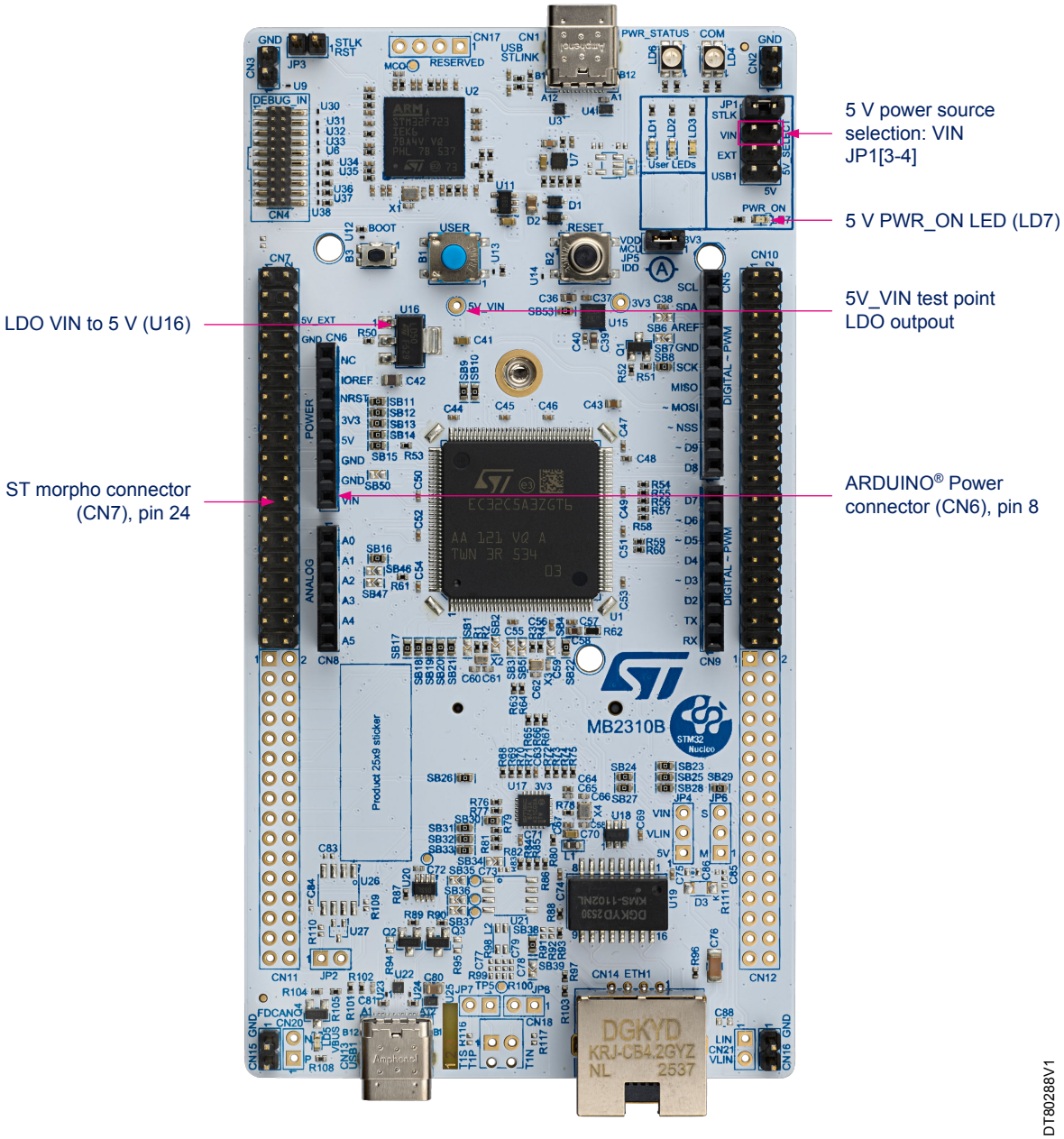


VIN (5V_VIN)

VIN (5V_VIN) is the 7 to 12 V DC power from the ARDUINO® connector (CN6) pin 8 (VIN) or from the ST morpho connector (CN7) pin 24. An onboard LDO (U16) provides a fixed 5 V supply from VIN (7 to 12 V).

For a 5V_VIN power supply, the JP1 jumper is fitted on [3-4] (VIN), as shown in Figure 10.

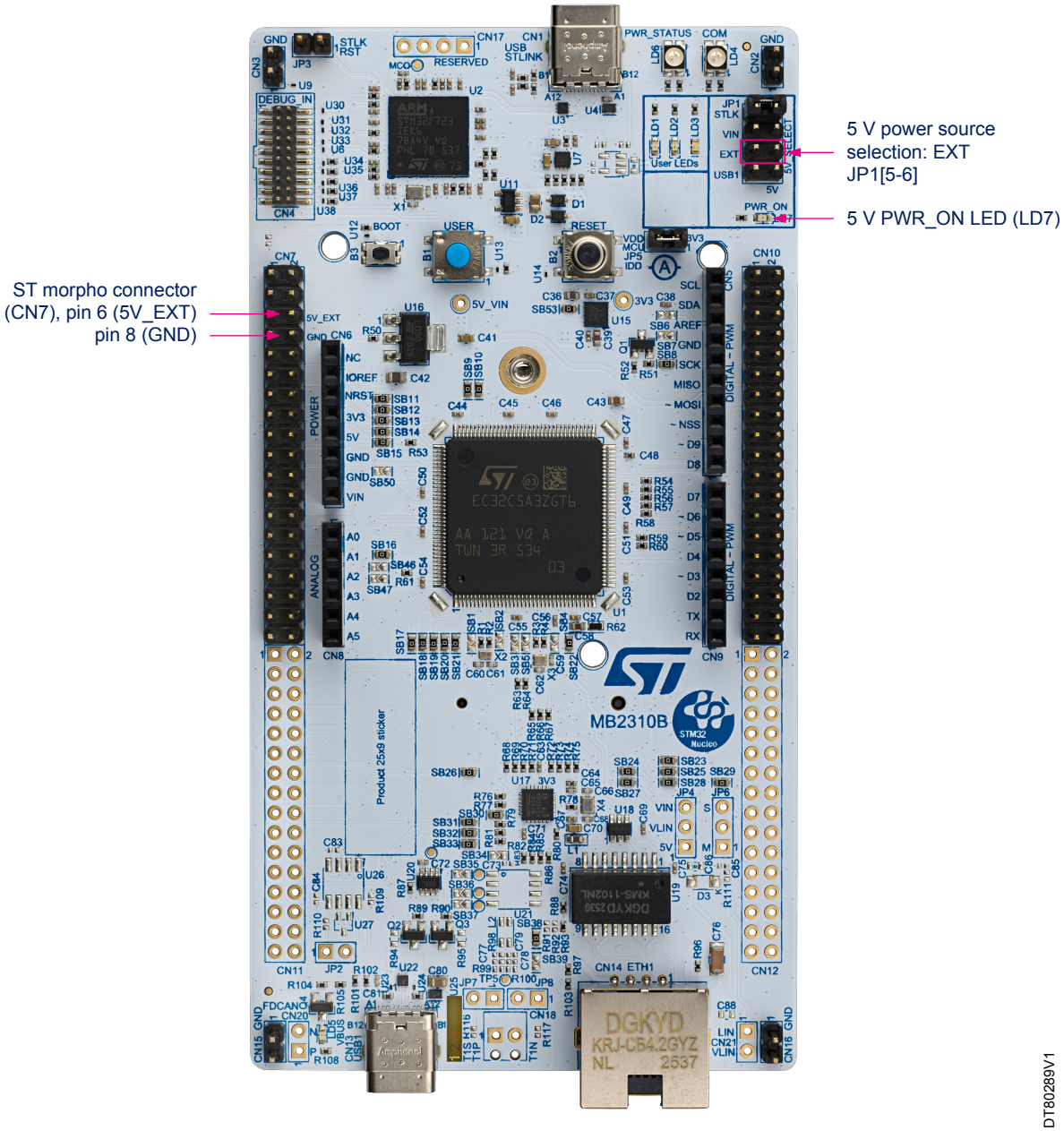
Figure 10. JP1 [3-4]: 5V_VIN power source



5V_EXT

5V_EXT is the DC power coming from an external 5 V DC power source from the ST morpho connector (CN7) pin 6. The 5 V jumper selection (JP1) must be fitted on [5-6] (EXT) to select the E5V power source on the JP1 connector, and it must be configured as shown in Figure 11.

Figure 11. JP1[5-6]: 5V_EXT power source

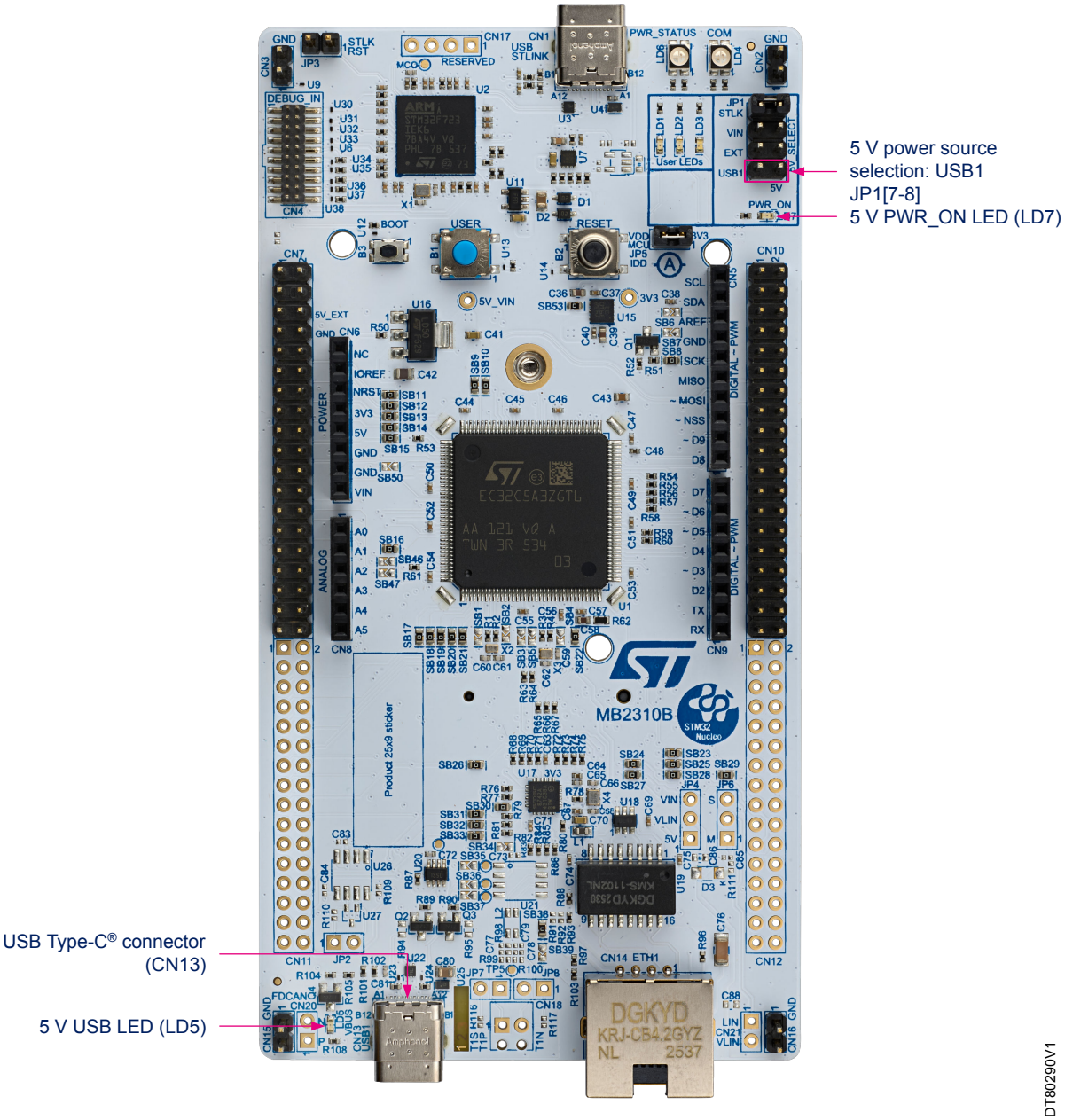


USB1

USB1 is the DC power supply from the USB Type-C® user connector (CN13, 5 V/500 mA).

To select this power supply source, the JP1 jumper must be on [7-8], as shown in Figure 12. The green LED (LD5) is turned on.

Figure 12. JP1 [7-8]: 5V_USB_SNK power source



External 3V3

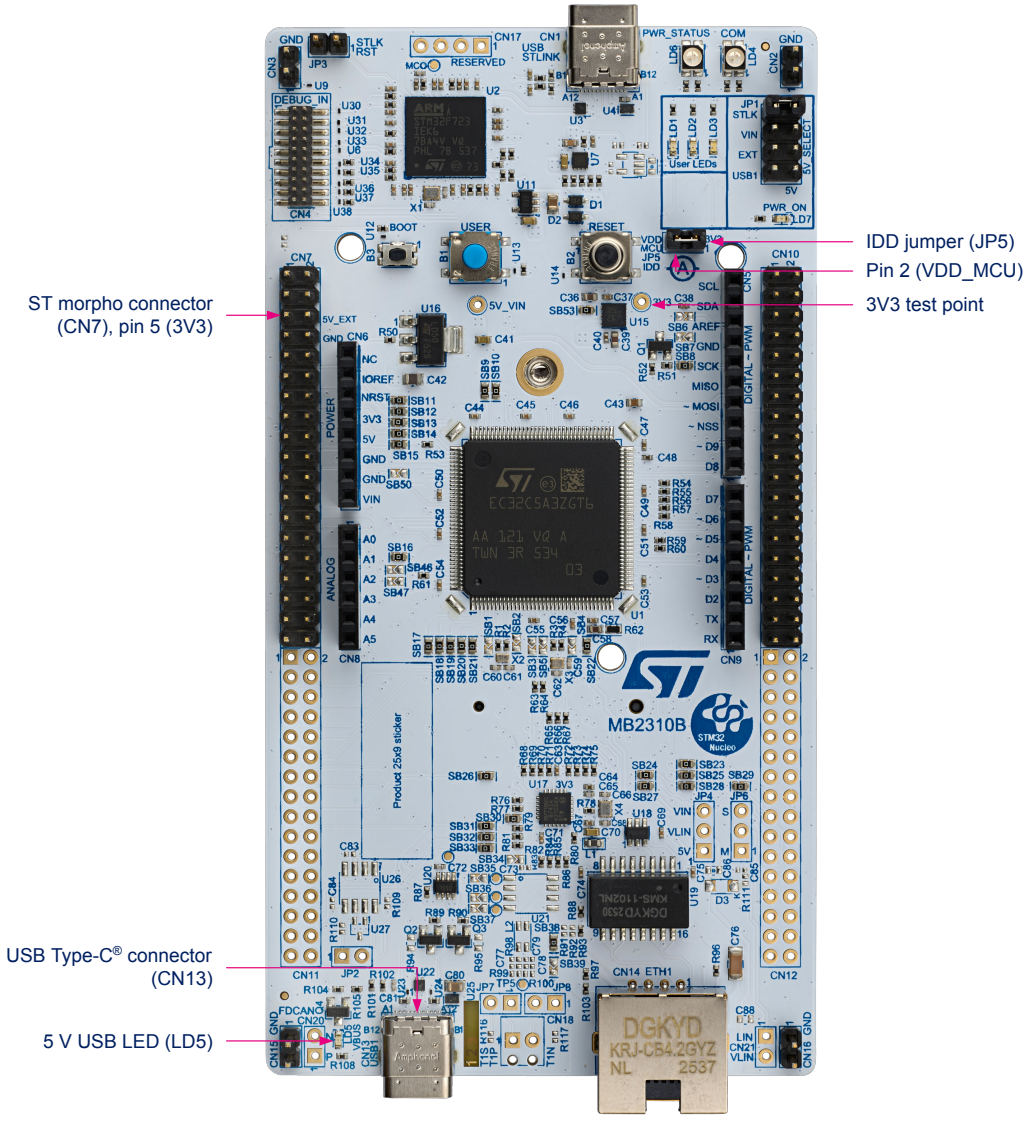
In certain scenarios, like when the 3.3 V supply is provided by an extension board, it can be interesting to use an external 3.3 V source on the 3V3 input (CN7 pin 5 or 3.3 V test point). When the NUCLEO-C5A3ZG Nucleo-144 board is powered by a 3.3 V source only, STLINK-V3EC is not powered and programming and debugging are unavailable.

Warning: *When using the 3V3 input, the STLINK-V3EC part is not supplied. For this configuration, it is recommended to remove SB53 to avoid backward voltage through U15.*

VDD_MCU

In certain scenarios, it can be interesting to use an external power source from 2.7 to 3.6 V, to power only the MCU power supply pins (JP5 pin 2). In this configuration, external functions like debug, LEDs, or the expansion connector are not powered. This option can be used to optimize MCU power consumption measurement.

Figure 13. 3V3 power source



7.4.2 Programing/debugging when the power supply is not from STLINK-V3EC (5V_STLK)

When powered by VIN, EXT, or USB1, it is still possible to use STLINK-V3EC for Virtual COM port (VCP), programming, or debugging. The following power sequence procedure must be followed:

1. Set the JP1 jumper according to the selected 5 V external power source.
2. Connect the external power source as per the JP1 configuration.
3. Turn on the external power supply.
4. Verify that the 5 V green LED (LD7) is illuminated.
5. Connect the PC to the USB connector (CN1) for programming and debugging.

If this sequence is not respected, VBUS from STLINK-V3EC might power the board first, and the following risks can occur:

- If the board requires more current than the STLINK-V3EC can provide, the PC may be damaged, or the current can be limited by the PC. Therefore, the board is not powered correctly.
- 500 mA is requested at enumeration. There is a risk that the request is rejected, and enumeration fails because the PC cannot provide this current.

7.4.3 Power supply output

5V

Regardless of the power source (5V_STLK, 5V_VIN, 5V_EXT, or USB1), the 5 V generated is available on CN6 pin 5 or CN7 pin 18. It can be used as an output power supply for an ARDUINO® shield or an extension board. In this case, the maximum current of the power source specified in Table 6 must be adhered to.

3V3

The internal 3V3 on CN6 pin 4 or CN7 pin 16 can also be used as a power supply output. The current is limited by the maximum current capability of the U15 regulator.

7.4.4 Measurement of the microcontroller current consumption

The IDD jumper (JP5) is used to measure the current consumption of the STM32 microcontroller. To perform the measurement, remove the jumper and connect an ammeter or another current measurement tool.

- Jumper ON: the STM32 microcontroller is powered by the internal 3.3 V source (default).
- Jumper OFF: connect an ammeter or an external 3.3 V power source to power and measure the STM32 microcontroller current consumption.

7.5 Clock sources

Three clock sources are available:

- LSE: 32.768 kHz crystal for the STM32 embedded RTC.
- MCO: 8 MHz clock from STLINK-V3EC for the STM32 microcontroller.
- HSE: 48 MHz oscillator for the STM32 microcontroller.

7.5.1 LSE clock references

There are three methods to set up the pins associated with the low-speed clock (LSE), which are detailed below. Refer to the application note *Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs* (AN2867) for further details, such as typical frequencies, capacitors, and resistors.

LSE on-board oscillator X2 crystal (default configuration)

The X2 crystal has the following characteristics: 32.768 kHz, 9 pF, and 20 ppm. The following configuration is needed:

- R1 and R2 ON
- SB1 and SB2 OFF

External oscillator on PC14

The input clock comes from an external oscillator via the PC14 signal on the ST morpho connector (CN7 pin 25). This clock requires the following configuration:

- SB1 ON for connection from the ST morpho connector (CN7) pin 25
- R1 and R2 OFF
- SB2 is optional

LSE not used

PC14 and PC15 are used as GPIOs instead of low-speed clocks. This requires the following configuration:

- R1 and R2 OFF
- SB1 and SB2 ON

7.5.2 HSE clock references

There are four ways to configure the pins corresponding to the external high-speed clock (HSE), which are detailed below. Refer to the application note *Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs* (AN2867) for further details, such as typical frequencies, capacitors, and resistors.

HSE onboard oscillator X3 crystal (default configuration)

The X3 crystal has the following characteristics: 48 MHz, 6 pF, and 20 ppm. The following configuration applies:

- R3 and R4 ON
- SB3, SB4, and SB5 OFF

This crystal is connected by default.

MCO from STLINK-V3EC

The MCO output of the STLINK-V3EC MCU is used as an input clock. By default, its frequency is fixed at 8 MHz and it is connected to the PH0 OSC_IN pin of the STM32 microcontroller. The frequency may be changed during an ST-LINK firmware upgrade (refer to RN0093 for further details). The use of this clock source requires the following configuration:

- R3 and R4 OFF
- SB5 (MCO) ON
- SB3 and SB4 OFF

The resistor (R7) and capacitor (C3) can be adapted for the CLK shape.

By default, this clock is not connected.

External oscillator on PH0

The input clock comes from an external oscillator through PH0, on the extension connector (CN7) pin 29. The following configuration is required:

- R3 and R4 OFF
- SB5 (MCO) OFF
- SB3 ON for connection from the ST morpho connector (CN7), pin 29
- SB4 optional

By default, this clock is not connected.

HSE not used

PH0 and PH1 are used as GPIOs instead of clocks. This requires the following configuration:

- R3 and R4 OFF
- SB5 (MCO) OFF
- SB3 and SB4 ON

By default, this clock is not connected.

7.6 Boot modes

One BOOT (PH2-BOOT0) pin is connected to this board to select the boot mode:

- **BOOT0 = 0: boot from user flash memory (default configuration)**
- BOOT0 = 1: boot from system memory (bootloader).

The BOOT0 pin is pulled down with an external resistor. To achieve a high voltage, there are two options:

- Press the boot button (B3) to pull BOOT0 to a high voltage level. Once the button is released, BOOT0 returns to a low level.
- Use a jumper to short CN7 pin 5 and CN7 pin 7 (BOOT0 is shorted to VDD).

7.7 Reset sources

The reset signal of the NUCLEO-C5A3ZG Nucleo-144 board is active LOW. The reset sources include:

- Reset button (B2)
- Embedded STLINK-V3EC (CN1)
- ARDUINO® connector (CN6 pin 3)
- ST morpho connector (CN7 pin 14)

7.8 LEDs

The NUCLEO-C5A3ZG Nucleo-144 board contains seven LEDs:

- Three user LEDs (LD1, LD2, LD3).
  - This green LED is a user LED connected to GPIO PA5 (SB8 ON), which corresponds to the ARDUINO® D13 signal. To light LD1, write a high logic state ("1") to GPIO PA5. A transistor drives LD1.
    The function of the user LED (LD1) can be modified and programmed to indicate another status signal relevant to the board.
    LD1 consumption does not affect the VDD_MCU power measurement, because LD1 is isolated from this power supply.
    A second GPIO, PG0, can be connected by positioning SB7 instead of SB8 to drive LD1. This configuration allows the ARDUINO® D13 function to be used in parallel with the green LED function. In this configuration, the user LEDs are off when the STM32 I/O is in a high state, and on when the STM32 I/O is in a low state.
  - The red LED (LD2) is connected to PG1.
  - The blue LED (LD3) is connected to PG2.

  These user LEDs are OFF when the STM32 I/O is in a high state, and ON when the STM32 I/O is in a low state.
- Two STLINK-V3EC tricolor (green, orange, and red) LEDs (LD4 and LD6). These LEDs provide information about the STLINK-V3EC communication (LD4) and power (LD6) status. For detailed information about these LEDs, refer to the technical note *Overview of STLINK derivatives* (TN1235).
- USB Type-C® 5 V LED (LD5). This green LED indicates the presence of V_{BUS} on CN13.
- 5V_PWR LED (LD7). This green LED indicates that the STM32 part is powered by a 5 V source.

Table 7 provides an overview of the different LEDs on the NUCLEO-C5A3ZG Nucleo-144 board. Refer to Figure 5 to locate the LEDs on the board.

Table 7. **NUCLEO-C5A3ZG LEDs**

Color	Reference	System element monitored
Green	LD1	Free for user function
Red	LD2	Free for user function
Blue	LD3	Free for user function
Green, orange, red	LD4	Onboard STLINK-V3EC communication status
Green	LD5	V_{BUS} presence indicator on USB1 user connector (CN13)
Green, orange, red	LD6	Onboard STLINK-V3EC power status
Green	LD7	+5 V power indicator, board powered

7.9 Push-buttons

Three push-buttons are available on the NUCLEO-C5A3ZG Nucleo-144 board:

- Blue user button (B1)
- Black reset button (B2)
- Black boot mode button (B3)

Refer to Figure 5 to locate the push-buttons on the board.

Blue user button (B1)

The user button connects to the PC13 STM32 I/O pin by default. Depending on the supported microcontroller, this pin can support a wake-up function and a tamper function.

A pull-down resistor supports the tamper function. Remove this resistor if the I/O pin is used only in wake-up mode. In this case, the software must set an internal I/O pull-up in the microcontroller.

When the button is pressed, the logic state is HIGH. Otherwise, the logic state is LOW.

There is no hardware filter. The user must program a filter by software if needed. This reduces the bill of materials (BOM) cost by eliminating the external hardware debounce filter (capacitor).

Warning: *Set the PC13 I/O for the user button to input mode with debounce. Do not set PC13 to output mode or drive it to a low level. This configuration prevents a short circuit when the user button is pressed.*

Black reset button (B2)

This push-button connects to NRST and resets the microcontroller. When the button is pressed, the logic state is low; otherwise, the logic state is high.

Black boot mode button (B3)

This push-button connects to the BOOT pin and selects the boot mode during the reset phase. When the button is pressed, the logic state is high; otherwise, an external pull-down resistor drives the logic state low.

- No button press during the reset phase: BOOT pin is at level 0. Boot from user flash memory.
- Button press during the reset phase: BOOT pin is at level 1. Boot from system memory.

7.10 USB Type-C® FS

The NUCLEO-C5A3ZG Nucleo-144 board supports USB full-speed (USB FS) communication through a USB Type-C® connector (CN13). The board also supports USB Device mode and can be powered by the USB Type-C® connector (CN13), with a 500 mA current limitation.

The green USB power LED (LD5) lights up when VBUS is powered by a USB Host and the board works as a USB Device.

USB FS Device

When the USB stack is integrated in the STM32 microcontroller, and a USB Host connection to the USB Type-C® connector (CN13) on the board is detected, the NUCLEO-C5A3ZG Nucleo-144 board operates as a USB Device. Depending on the power capability of the USB Host, the board can be powered by the connector VBUS terminal. This configuration corresponds to position [7-8] (USB1) on the 5 V power source selection jumper (JP1). The board supports any USB-compliant 5 V voltage. Table 8 shows the hardware configuration for the USB FS interface.

Table 8. Hardware configuration for the USB interface

IO	SB	Setting(1)	Configuration(1)
PA11	SB10	OFF	PA11 used as USB_FS_N diff pair interface. No other muxing.
		ON	**PA11 can be used as USB data interface and PA11 is also available on the ST morpho connector.** **USB function can be used, but performances may be impacted due to the track length on the expansion module and track impedance mismatch.**
PA12	SB9	OFF	PA12 used as USB_FS_P diff pair interface. No other muxing.
		ON	**PA12 can be used as USB data interface and PA12 is also available on the ST morpho connector.** **USB function can be used, but performances can be impacted due to the track length on the expansion module and track impedance mismatch.**
PE15	SB29	OFF	PE15 not used for USB. PE15 is available on the extension connector CN12, pin 15.
		ON	**PE15 is used for VBUS detection.** **PE15 is also available on the extension connector CN12, pin 15.**

1. *The default configuration is shown in bold.*

USB power mode

The NUCLEO-C5A3ZG Nucleo-144 board can be used in two USB power modes:

- In Self-powered mode, transistors Q2 and Q3 are fitted. They are driven by the onboard 3.3 V supply. In OFF mode, the 5.1 kΩ Rd resistors are not present on the connector CCx lines. (This is the default configuration.)
- In Bus-powered mode, resistors R94 and R95 are fitted. They are used in dead-battery mode and at the USB Host plug to start enumeration. (This configuration is optional; R94 and R95 must be soldered manually).

Note: SB51 can demonstrate MCU USB Host mode capabilities through the USB Type-C® connector. This mode is intended for testing purposes and is not USB Type-C® certifiable or compliant in its current state. The objective is to provide 5 V on the USB Type-C® user connector (CN13) to enable connection of a device as mass storage. In this mode, never connect a source or dual-role power (DRP) peripheral, such as a PC. Negotiation through the CC lines is not possible. Device detection is not available, so the MCU USB controller must be forced into USB Host mode. The power budget of the board does not support delivering current on the 5 V line of the USB Type-C® connector. Depending on the connected device, the product might not operate correctly. Use of this USB host mode must be performed with full knowledge and under the responsibility of the user.

7.11 Ethernet

The NUCLEO-C5A3ZG Nucleo-144 board supports 10/100-Mbit Ethernet communication with a PHY and integrates an RJ45 connector (CN14). The Ethernet PHY connects to the STM32 microcontroller through the RMII interface. The PHY RMII_REF_CLK signal generates the 50 MHz clock for the STM32 microcontroller.

Table 9 describes the pinout of the Ethernet function.

Note: To achieve the expected low-power mode current, set the Ethernet PHY to power-down mode. In this mode, the Ethernet PHY reference clock turns off. Configure the Ethernet PHY basic control register (address 0x00), bit 11 (power-down), to '1'.

Set the Ethernet PHY to power-down mode before using the STM32 microcontroller I/Os on the extension connector. Alternatively, remove the associated solder bridgeas described in Table 9.

Table 9. Ethernet pin configuration

Pin name	Function	Solder bridge	Setting(1)	Description(1)
PA1	RMII reference clock	SB27	**ON**	**PA1 is used as RMII REF CLK.**
			OFF	PA1 can be used as GPIO on the extension connector CN12, pin 26.
PE12	RMII MDIO	SB28	**ON**	**PE12 is used as RMII MDIO.**
			OFF	PE12 can be used as GPIO on the extension connector CN12, pin 17.
PC1	RMII MDC	SB24	**ON**	**PC1 is used as RMII MCD.**
			OFF	PC1 can be used as GPIO on the extension connector CN12, pin 21.
PD1	RMII CRS_DV	SB26	**ON**	**PD1 is used as RMII CRS_DV.**
			OFF	PD1 can be used as GPIO on the extension connector CN11, pin 17.
PC4	RMII RXD0	SB25	**ON**	**PC4 is used as RMII RXD0.**
			OFF	PC4 can be used as GPIO on the extension connector CN12, pin 22.
PC5	RMII RXD1	SB23	**ON**	**PC5 is used as RMII RXD1.**
			OFF	PC5 can be used as GPIO on the extension connector CN12, pin 24.
PG11	RMII TX enable	SB31	**ON**	**PG11 is used as RMII TX EN.**
			OFF	PG11 can be used as GPIO on the extension connector CN11, pin 32.
PG13	RMII TXD0	SB32	**ON**	**PG13 is used as RMII TXD0.**
			OFF	PG13 can be used as GPIO on the extension connector CN11, pin 30.
PG12	RMII TXD1	SB33	**ON**	**PG12 is used as RMII TXD1.**
			OFF	PG12 can be used as GPIO on the extension connector CN11, pin 28.
PG14	ETH_INTN	SB38	**ON**	**PG14 is used as an interruption from the Ethernet transceiver to the STM32 MCU for the Ethernet function.**
			OFF	PG14 can be used as GPIO on the extension connector CN12, pin 23.
PG15	ETH_LED	SB39	ON	Configuration forbidden.
			OFF	**Green Ethernet LED present on the CN14 connector is driven by PG15. PG15 is also connected to the extension connector CN11, pin 26.**

1. *The default configuration is shown in bold.*

7.12 Virtual COM port (VCP)

An STM32 serial interface connects to the STLINK-V3EC debug interface as a Virtual COM port (VCP).

Communication between the target microcontroller and the STLINK-V3EC microcontroller is enabled on USART2, using I/Os PA2 (USART2_TX) and PA3 (USART2_RX).

This interface supports bootloader mode.

Due to muxing constraints, the VCP interface, ARDUINO® Uno V3 UART, and ST morpho UART share the same UART2 instance. The VCP interface is exclusive with ARDUINO® Uno V3 UART and ST morpho UART. To use both interfaces simultaneously, set PA2/PA3 in LPUART1 as the VCP UART and set the LPUART_CR2.SWAP bit to swap the Rx and Tx pins.

8 Board connectors

8.1 M.2 Key A serial memory connector (CN19)

The bottom side of the NUCLEO-C5A3ZG Nucleo-144 boardcontains an M.2 Key A serial memory connector (CN19) for memory extension using daughter boards. Refer to Figure 6 to locate the connector on the board.

The external serial memory module connector is connected to the STM32 XSPI interface and supports Quad-SPI, Octo-SPI, and Hexadeca-SPI memories. A serial memory pack containing five different nonvolatile serial memory add-on boards is available from STMicroelectronics. For further information, including detailed documentation, visit the B-M2MEM-PACK1 webpage.

Table 10 provides the configuration of the M.2 Key A serial memory connector for this NUCLEO-C5A3ZG board.

Table 10. M.2 Key A serial memory connector (CN19) pinout

MCU pin	Signal name	Pin name	CN19 pin number	CN19 pin number	Pin name	Signal name	MCU pin
GND			1	2	3V3	3V3	-
-	-	NC	3	4	3V3	3V3	-
-	-	NC	5	6	VDDIO1	-	-
GND			7	Key A			
Key A			16	GPIO_SPI_SCK	SPI_SCK	PA5	
PA7	SPI_MOSI	GPIO_SPI_MOSI	17	18	GPIO_LDO_EN	M2_GPIO_LDO_EN	PG9
PA6	SPI_MISO	GPIO_SPI_MISO	19	20	XSPI_CS2N(1)	XSPI1_NCS1 / XSPI1_NCS2	PE11 / PE0
PG10	M2_SPI_NSS	GPIO_SPI_NSS	21	22	XSPI_CS1N	XSPI1_NCS1	PE11
GND			23	24	GND		
PB2	XSPI1_DQS0	XSPI_DQS0	25	26	XSPI_D6	XSPI1_IO6	PE9
PE10	XSPI1_IO7	XSPI_D7	27	28	XSPI_D5	XSPI1_IO5	PE8
GND			29	30	GND		
PE7	XSPI1_IO4	XSPI_D4	31	32	XSPI_D3	XSPI1_IO3	PF6
GND			33	34	XSPI_D2	XSPI1_IO2	PF7
PF8	XSPI1_IO1	XSPI_D1	35	36	GND		
PF9	XSPI1_IO0	XSPI_D0	37	38	GPIO_LED2	M2_GPIO_LED2	PG8
GND			39	40	GPIO_ERR_INT1	M2_GPIO_ERR_INT1	PG6
PF10	XSPI1_CLK	XSPI_CLK1	41	42	GPIO_LED1	M2_GPIO_LED1	PG7
PF11	XSPI1_NCLK	XSPI_NCLK1	43	44	GND		
GND			45	46	Reserved		
PE10	XSPI1_IO7	XSPI_D15	47	48	Reserved		
PE9	XSPI1_IO6	XSPI_D14	49	50	GND		
GND			51	52	XSPI_NCS4	-	-
PE8	XSPI1_IO5	XSPI_D13	53	54	XSPI_NCS3	XSPI1_NCS2	PE0
PE7	XSPI1_IO4	XSPI_D12	55	56	HSPI_DQS1	XSPI1_DQS0	PB2
GND			57	58	I2C_SDA	I2C2_SDA	PF0
PF6	XSPI1_IO3	XSPI1_D11	59	60	I2C_SCL	I2C2_SCL	PF1

MCU pin	Signal name	Pin name	CN19 pin number	CN19 pin number	Pin name	Signal name	MCU pin
PF7	XSPI1_IO2	XSPI_D10	61	62	GPIO_ERR_INT2	M2_GPIO_ERR_INT2	PG5
GND			63	64	VDDIO_SPI_I2C	3V3	-
PF8	XSPI1_IO1	XSPI_D9	65	66	NRST	NRST	-
PF9	XSPI1_IO0	XSPI_D8	67	68	VDDIO2	-	-
GND			69	70	GND		
PF10	XSPI1_CLK	XSPI_CLK2	71	72	3V3	3V3	-
PF11	XSPI1_NCLK	XSPI_NCLK2	73	74	3V3	3V3	-
GND			75	-			

1. *The NCSx selection uses a solder bridge: SB20 for NCS1 (default configuration) or SB18 for NCS2 (optional configuration).*

8.2 ARDUINO® Uno V3 connectors (CN5, CN6, CN8, CN9)

The ARDUINO® connectors (CN5, CN6, CN8, and CN9) are female connectors supporting the ARDUINO® Uno V3 standard.

Note: Most STM32 MCU I/O pins are 5 V tolerant. However, some pins are only compatible with 3.6 V. The ARDUINO® Uno V3 connector is 5 V compatible. For details on I/O structures, refer to the STM32 MCU data brief and datasheet.

Figure 14 indicates where the connectors are situated on the board and tables 11, 12, 13, and 14 provide their pinout configurations.

Figure 14. **ARDUINO® Uno V3 connectors**

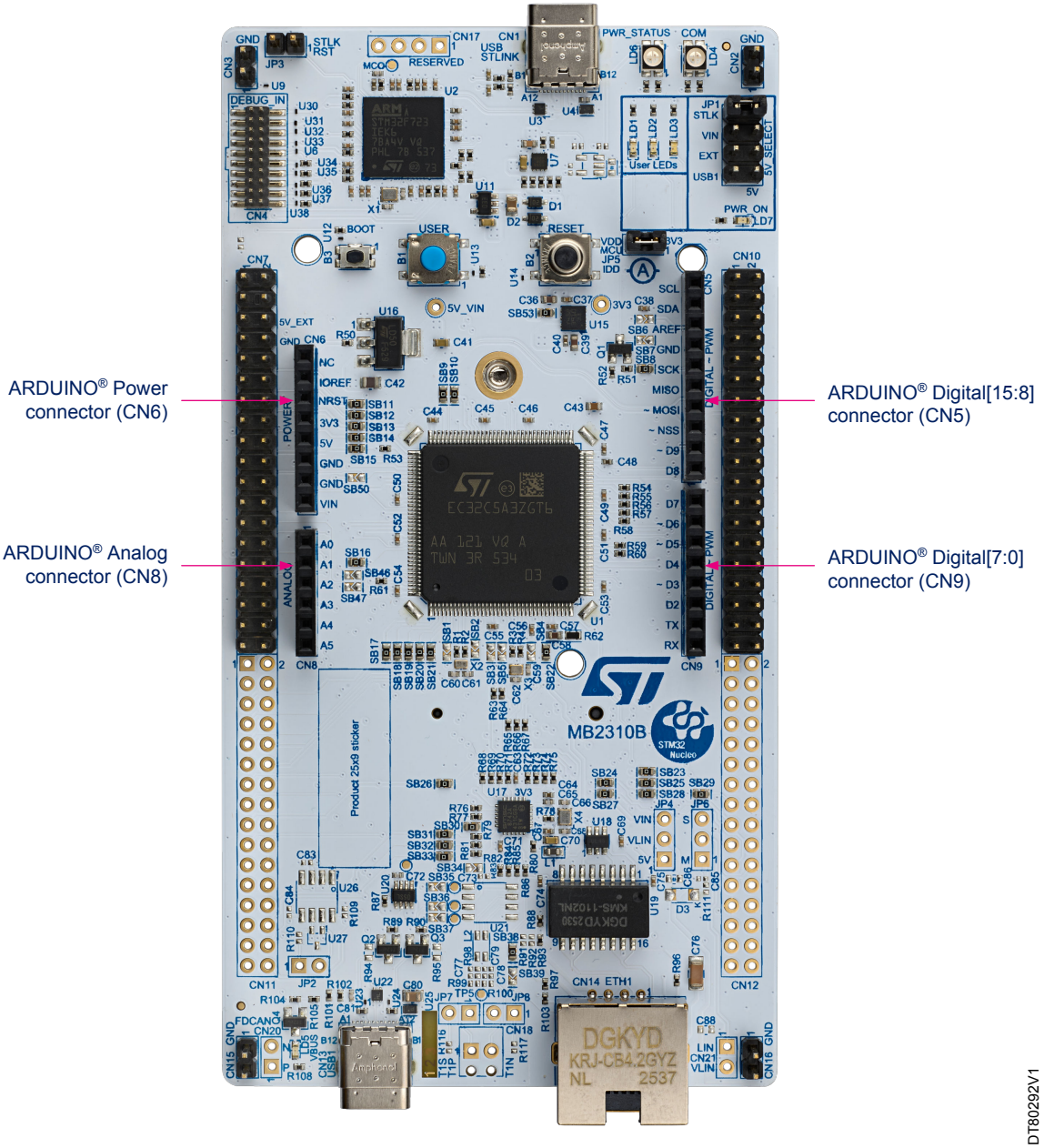


Table 11. ARDUINO® Power connector (CN6) pinout

Pin	Pin name	Signal name	MCU pin	Power function
1	NC	-	-	RESERVED
2	IOREF	IOREF	-	3.3 V IO REF
3	NRST	NRST	NRST	RESET
4	3V3	3V3	-	3V3 OUT
5	5V	5V	-	5 V OUT
6	GND	GND	-	GND
7	GND	GND	-	GND
8	VIN	VIN	-	VIN (7-12 V)

Table 12. ARDUINO® Analog connector (CN8) pinout

Pin	Pin name	Signal name	MCU pin	MCU function(1)
1	A0	ADC	PH4	ADCx_INPy
2	A1	ADC	PH5	ADCx_INPy
3	A2	ADC	PA4	ADCx_INPy
4	A3	ADC	PB0	ADCx_INPy
5	A4	ADC	PE13	ADCx_INPy
6	A5	ADC	PC0	ADCx_INPy

1. *The alternate function depends on the target MCU. Refer to the product datasheet to determine the alternate functions available on the ARDUINO® Uno V3 connector.*

Table 13. ARDUINO® Digital[7:0] connector (CN9) pinout

Pin	Pin name	Signal name	MCU pin	MCU function(1)
1	D0	UART_RX	PD6	USART_RX(2)
2	D1	UART_TX	PD5	USART_TX(2)
3	D2	IO	PA10	GPIO
4	D3	PWM	PB3	TIM2_CH2
5	D4	IO	PA0	GPIO / WKUP
6	D5	PWM	PB4	TIMx_CHy
7	D6	PWM	PB10	TIM2_CH3
8	D7	IO	PA8	GPIO

1. *The alternate function depends on the target MCU. Refer to the product datasheet to determine the alternate functions available on the ARDUINO® Uno V3 connector.*
2. *Due to muxing constraints, ARDUINO® UART (D0/D1) is exclusive with the VCP. Refer to Section 7.12: Virtual COM port (VCP) for further details.*

Table 14. **ARDUINO® Digital[15:8] connector (CN5) pinout**

Pin	Pin name	Signal name	MCU pin	MCU function(1)
1	D8	IO	PA9	GPIO
2	D9	PWM	PC6	TIMx_CHy
3	D10	SPI_NSS / PWM	PB5	SPI_NSS / TIMx_CHy
4	D11	SPI_MOSI / PWM	PA7	SPI_MOSI / TIMx_CHy
5	D12	SPI_MISO	PA6	SPI_MISO
6	D13	SPI_SCK	PA5	SPI_SCK
7	GND	-	-	-
8	AREF	AREF	VREFP	VREFP(2)
8	D14	I2C_SDA / I3C_SDA	PB7	I2C_SDA / I3C_SDA
10	D15	I2C_SCL / I3C_SCL	PB6	I2C_SCL / I3C_SCL

1. *The alternate function depends on the target MCU. Refer to the product datasheet to determine the alternate functions available on the ARDUINO® Uno V3 connector.*
2. *A solder bridge (SB6) is used to disconnect the STM32 VREFP from the ARDUINO® Uno V3 connector CN5 pin 8.*
   - *SB6 OFF: the STM32 input power pin VREFP is not connected to the ARDUINO® Uno V3 connector CN5 pin 8 (AREF, default configuration). The STM32 input power pin VREFP is directly connected to the internal 3.3 V through R62, which must be ON.*
   - *SB6 ON: The STM32 input power pin VREFP is connected to the ARDUINO® Uno V3 connector CN5 pin 8 (AREF) for an external analog reference. R62 must be OFF.*

8.3 ST morpho connectors (CN7, CN10)

The ST morpho connectors consist of the CN7 and CN10 2.54-pitch male pin headers. They can be used to connect the NUCLEO-C5A3ZG Nucleo-144 board to any of the following:

- Extension board
- Prototype/wrapping board
- Oscilloscope
- Logic analyzer
- Voltmeter

The default shields compatible with the Nucleo-144 ST morpho connector pinout are:

- X-NUCLEO-IHM16M1 for motor control
- X-NUCLEO-GFX01M2 for graphics user interface and SPI memory

Figure 15 shows the location of the ST morpho connectors on the board. Table 15 and Table 16 show the pin assignments for the connectors.

Note: Alternate function availability depends on the target microcontroller. Refer to the product datasheet to determine the alternate functions available to the ST morpho connector.

Figure 15. **ST morpho connectors**

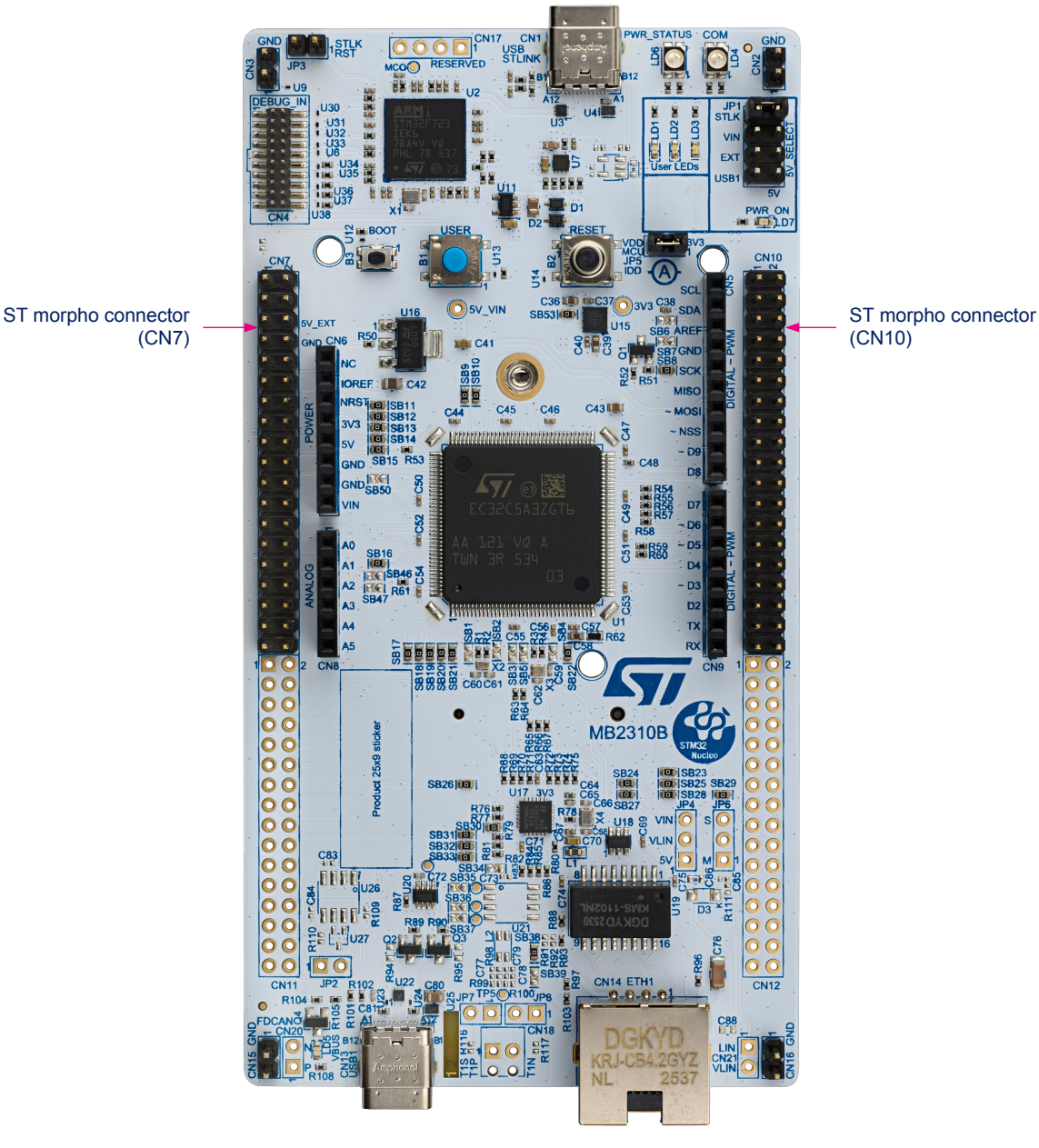


Table 15. ST morpho connector (CN7, left) pinout

MCU		ST morpho connector		MCU	
GPIO	Function(1)	Pin number	Pin number	Function(1)	GPIO
PC10	SDMMC_D2 / I2S_SCK	1	2	SDMMC_D3 / I2S_SDI	PC11
PC12	SDMMC_CK / I2S_SDO	3	4	SDMMC_CMD	PD2
-	3V3	5	6	5V_EXT	-
BOOT0	BOOT0	7	8	GND	-
PA2	GPIO	9	10	GPIO	PB8
PA3	GPIO	11	12	IOREF	-
PA13	SWDIO(3)	13	14	NRST	NRST
PA14	SWCLK(3)	15	16	3V3	-
PA15	JTDI(3) / TIM2_CH1 / I2S_WS	17	18	5V	-
-	GND	19	20	GND	-
PD0	GPIO	21	22	GND	-
PC13	WKUP(2)	23	24	VIN	-
PC14	OSC32_IN	25	26	GPIO	PB9
PC15	OSC32_OUT	27	28	ADCx_INPy	PH4
PH0	OSC_IN	29	30	ADCx_INPy	PH5
PH1	OSC_OUT	31	32	ADCx_INPy / DACx_OUTy	PA4
-	~~VBAT~~	33	34	ADCx_INPy	PB0
PC2	ADCx_INPy / SPI_MISO	35	36	ADCx_INPy	PE13
PC3	ADCx_INPy / SPI_MOSI	37	38	ADCx_INPy	PC0

1. *Alternate function availability depends on the STM32 Nucleo configuration.*
2. *Common pin with the user button (B1) WKP.*
3. *These I/Os are shared with SWD signals connected to STLINK-V3EC.*

Table 16. ST morpho connector (CN10, right) pinout

MCU		ST morpho connector		MCU	
GPIO	Function(1)	Pin number	Pin number	Function(1)	GPIO
PC9	SDMMC_D1 / LIN_RX	1	2	SDMMC_D0 / LIN_TX	PC8
PB6	I2C_SCL / I3C_SCL	3	4	GPIO	PC7
PB7	I2C_SDA / I3C_SDA	5	6	GPIO	PF15
VREFP	VREFP(2)	7	8	5V_STLK(3)	-
-	GND	9	10	GPIO	PF14
PA5	SPI_SCK	11	12	USB_P / FDCAN_TX	PA12
PA6	SPI_MISO	13	14	USB_N / FDCAN_RX	PA11
PA7	SPI_MOSI / TIMx_CHy	15	16	TIM1_BKIN / FDCAN_RX	PB12
PB5	SPI_NSS / TIMx_CHy	17	18	ADCx_INPy	PB1
PC6	GPIO	19	20	GND	-
PA9	TIM1_CH2	21	22	GPIO	PF13
PA8	TIM1_CH1	23	24	GPIO	PF12
PB10	TIM2_CH3	25	26	TIM1_CH3N	PB15

MCU		ST morpho connector		MCU	
GPIO	Function(1)	Pin number	Pin number	Function(1)	GPIO
PB4	TIMx_CHy / LINB_RX	27	28	TIM1_CH2N	PB14
PA0	GPIO / WKUP	29	30	TIM1_CH1N / SPI_SCK / FDCAN_TX	PB13
PB3	TIM2_CH2 / SWO / LINB_TX	31	32	VREFM	AGND
PA10	TIM1_CH3	33	34	ADCx_INPy	PE14
PD5	USARTx_TX(4)	35	36	USARTx_RTS	PD4
PD6	USARTx_RX(4)	37	38	USARTx_CTS	PD3

1. *Alternate function availability depends on the STM32 Nucleo configuration.*
2. *A solder bridge (SB6) is used to disconnect the STM32 VREFP from the ARDUINO® Uno V3 connector CN5 pin 8.*
   - *SB6 OFF: the STM32 input power pin VREFP is not connected to the ARDUINO® Uno V3 connector CN5 pin 8 (AREF, default configuration). The STM32 input power pin VREFP is directly connected to the internal 3.3 V through R62, which must be ON.*
   - *SB6 ON: The STM32 input power pin VREFP is connected to the ARDUINO® Uno V3 connector CN5 pin 8 (AREF) for an external analog reference. R62 must be OFF.*
3. *5V_STLK is the 5 V power signal, coming from the STLINK-V3EC USB connector. It rises before the 5 V signal of the board.*
4. *Due to muxing constraints, ST morpho UART is exclusive with the VCP. Refer to Section 7.12: Virtual COM port (VCP) for further details.*

8.4 Expansion connectors (CN11, CN12)

The expansion connectors consist of two footprints, CN11 and CN12. The connector is not mounted by default. Use these footprints to connect the STM32 Nucleo-144 board to an extension or prototype board with a 2.54 mm pitch. It is also possible to probe this connector with an oscilloscope, a logic analyzer, or a voltmeter.

The I/Os on these connectors are used for STM32 Nucleo-144 functions, like Ethernet, TRACE, or the M.2 Key A serial memory connector. To use them for external purposes, remove the relevant solder bridges, when available, to avoid conflicts.

Figure 16 shows the location of the ST morpho connectors on the board. Table 17 and Table 18 show the pin assignments for the connectors.

Note: Alternate function availability depends on the target microcontroller. Refer to the product datasheet to determine the alternate functions available to the ST morpho connector.

Figure 16. **Expansion connectors**

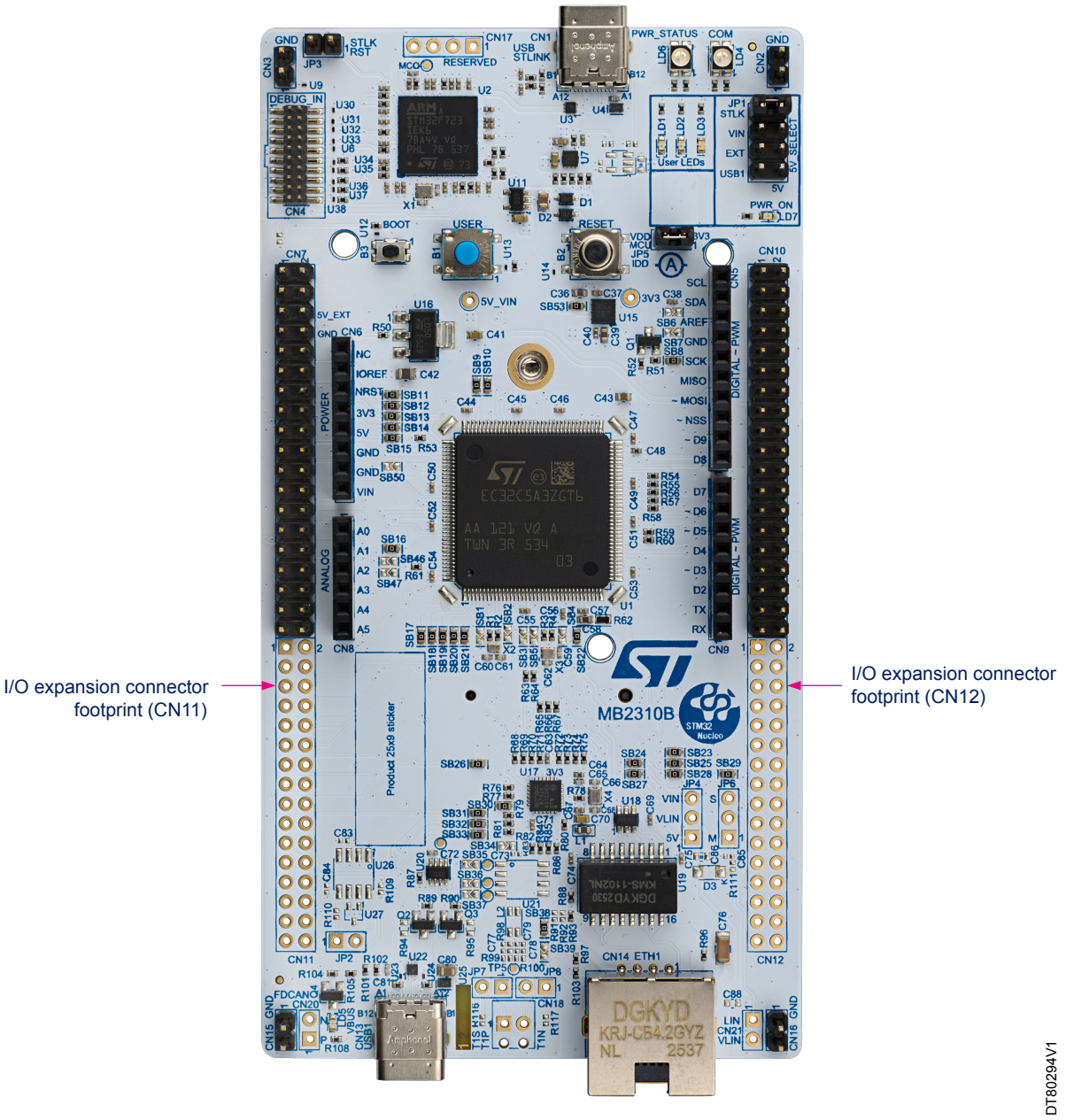


Table 17. **Expansion connector (CN11, left) pinout**

MCU		Expansion connector				MCU	
Pin number	Function	Solder bridge	Pin number	Pin number	Solder bridge	Function	Pin number
PG2	BLUE LED(3)	-	1	2	R63	XSPI1.IO3(1)	PF6
PG3	-	-	3	4	R64	XSPI1.IO2(1)	PF7
PE2	TRACE.CLK(4)	SB17	5	6	R65	XSPI1.IO1(1)	PF8
PE3	TRACE.D0(4)	SB18	7	8	R66	XSPI1.IO0(1)	PF9
PE4	TRACE.D1(4)	SB19	9	10	SB20	TRACE.D2(4)	PE5

MCU		Expansion connector				MCU	
Pin number	Function	Solder bridge	Pin number	Pin number	Solder bridge	Function	Pin number
GND	-	-	11	12	SB21	TRACE.D3(4)	PE6
PF1	M2_I2C_SCL(1)	-	13	14	-	-	PF2
PF0	M2_I2C_SDA(1)	-	15	16	-	-	PH15
PD1	RMII.CRS_DV(2)	SB26	17	18	-	-	PF3
PF4	-	-	19	20	-	RED_LED(3)	PG1
PG0	GREEN_LED	SB7	21	22	-	-	GND
PE1	-	-	23	24	-	-	PD7
PG9	M2_GPIO_LDO_EN(1)	-	25	26	-	ETH_LED	PG15
PG10	M2_SPI_NSS(1)	-	27	28	SB33	RMII.TXD1(2)	PG12
PH3	-	-	29	30	SB32	RMII.TXD0(2)	PG13
PD9	T1S.TX	SB35	31	32	SB31	RMII.TX_EN(2)	PG11

1. *No solder bridge on this I/O. Remove the external M.2 module to use this I/O on the expansion connectors.*
2. *The onboard Ethernet PHY must be set to power-down mode before using this I/O. Refer to Section 7.11: Ethernet for further details.*
3. *No solder bridge on this I/O. Remove the current LED resistors to use the I/O externally.*
4. *No solder bridge on this I/O. Remove the external debugger on CN4 DEBUG_IN to to use the I/O on the expansion connectors.*

Table 18. Expansion connector (CN12, right) pinout

MCU		Expansion connector				MCU	
Pin number	Function	Solder bridge	Pin number	Pin number	Solder bridge	Function	Pin number
GND	-	-	1	2	R54	XSPI.NCS1(1)	PE11
PE7	XSPI.IO4(1)	R58	3	4	R61	XSPI.NCS0(1)	PE0
PE8	XSPI.IO5(1)	R57	5	6	R60	XSPI.DQS0(1)	PB2
PE9	XSPI.IO6(1)	R56	7	8	R67	XSPI.CLK(1)	PF10
PE10	XSPI.IO7(1)	R55	9	10	R59	XSPI.NCLK(1)	PF11
PD12	-	-	11	12	-	-	PD13
PD11	-	-	13	14	-	-	PD14
PE15	VBUS_DETECT	SB29	15	16	-	-	GND
PE12	RMII.MDIO(2)	SB28	17	18	-	-	PD15
PD8	T1S.RX	SB37	19	20	SB51	LIN.SLPN	PF5
PC1	RMII.MDC(2)	SB24	21	22	SB25	RMII.RXD0(2)	PC4
PG14	ETH_INTN(2)	SB38	23	24	SB23	RMII.RXD1(2)	PC5
GND	-	-	25	26	SB27	RMII.REF_CLK(2)	PA1
PD10	T1S.ED	SB36	27	28	-	M2_GPIO_LED2(1)	PG8
PG7	M2_GPIO_LED1(1)	-	29	30	-	M2_GPIO_ERR_INT2(1)	PG5
PG4	-	-	31	32	-	M2_GPIO_ERR_INT1(1)	PG6

1. *No solder bridge on this I/O. Remove the external M.2 module to use this I/O on the expansion connectors.*
2. *The onboard Ethernet PHY must be set to power-down mode before using this I/O. Refer to Section 7.11: Ethernet for further details.*

8.5 Solder bridge configuration for connectors

Table 19 provides an overview of the solder bridge configuration for the NUCLEO-C5A3ZG Nucleo-144 board. Use these solder bridges to switch between internal configuration and external usage of the I/O pins on the expansion connector.

Table 19. Solder bridge configuration

Function	Solder bridge	Setting[1]	Comments
LSE (PC13, PC14)	SB1/SB2	**OFF**	**PC14/PC15 connected to the embedded crystal for LSE function (R1/R2 ON).**
		ON	PC14/PC15 connected to the ST morpho connector. 32 kHz crystal not used (R1/R2 must be OFF).
HSE (PH0, PH1)	SB3/SB4	**OFF**	**PH0/PH1 connected to the embedded crystal for HSE function (R3/R4 ON).**
		ON	PH0/PH1 connected to the ST morpho connector. 48 MHz crystal not used (R3/R4 must be OFF).
	SB5	**OFF**	**MCO (8MHz) from STLINK-V3EC not used for HSE**
		ON	MCO (8 MHz) from STLINK-V3EC can be used for HSE. 48 MHz crystal not used (SB3 and R3 must be OFF).
DEBUG SWD/JTAG (PA13, PA14, PA15, PB3)	SB13, SB14, SB15, SB16	OFF	GPIOs are used for debugging and are not connected to the expansion connectors. Only the SWD/JTAG interface with STLINK-V3EC is connected. This configuration avoids conflict between STLINK-V3EC and the external interface.
		ON	**GPIOs used for debugging are shared between the expansion connectors and SWD/JTAG interface. This configuration helps to probe the SWD/JTAG interface on the expansion connector.**
VCP (PA2, PA3)	SB11, SB12	OFF	GPIOs are used for VCP and are not connected to expansion connectors. Only the VCP interface with STLINK-V3EC is connected. This configuration avoids conflicts between STLINK-V3EC and the external interface.
		ON	**GPIOs used for VCP are shared between the expansion connectors and VCP interface on STLINK-V3EC. This configuration helps to probe the VCP interface on the expansion connector.**
TRACE (PE2, PE3, PE4, PE5, PE6)	SB17, SB18, SB19, SB20, SB21	OFF	GPIOs are used for the trace and are not connected to the expansion connectors. Only the trace interface on the MIPI20 connector is connected. This configuration avoids conflicts between the trace and the external interface.
		ON	**GPIOs used for the trace are shared between the expansion connectors and the trace on the MIPI20 connector. This configuration helps to probe the trace interface on the expansion connector.**

Function	Solder bridge	Setting[1]	Comments
ETHERNET (PA1, PC1, PC4, PC5, PD1, PE12, PG11, PG12, PG13,	SB23, SB24, SB25, SB26, SB27, SB28, SB31, SB32, SB33,	OFF	GPIOs are not used for the Ethernet and not connected to the internal Ethernet PHY. The GPIOs are available on the expansion connector for the external interface. This configuration avoids conflicts between the Ethernet and external interface.
		ON	**GPIOs are used for the Ethernet and are shared with the expansion connectors. This configuration helps to probe the Ethernet interface on the expansion connector.**
USB (PA11, PA12)	SB9, SB10,	OFF	GPIOs are used for USB and are not connected to the expansion connectors. USB P/N track layout is optimized. This configuration avoids conflicts between the trace and external interface.
		ON	**GPIOs are used for USB and are shared with the expansion connectors. This configuration helps to probe the USB interface on the expansion connector.**
USB (PE15)	SB29	OFF	GPIOs are not used for USB detection. The GPIOs are available on the expansion connector for the external interface. This configuration avoids conflicts between the Ethernet and external interface.
		ON	**GPIO is used for USB and is shared with the expansion connectors. This configuration helps to probe the USB detection on the expansion connector.**
T1S (PD8, PD9, PD10)	SB35, SB36, SB37	**OFF**	**GPIOs are not used for the T1S function. The GPIOs are available on the expansion connector for the external interface. This configuration avoids conflicts between the T1S function and external interface.**
		ON	GPIO is used for the T1S function and is shared with the expansion connectors. This configuration helps to probe the T1S interface on the expansion connector.
XSPI (PB2, PE0, PE7, PE8, PE9, PE10, PE11, PF6, PF7, PF8, PF9, PF10, PF11)	R54, R55, R56, R57, R58, R59, R60, R61, R63, R64, R65, R66, R67 (3):	OFF	GPIOs are not used for the XSPI, nor connected to the M.2 Key A serial memory connector. The GPIOs are available on the expansion connector for external interface. This configuration avoids conflicts between the M.2 memory module and the external interface.
		ON	**GPIOs are used for the M.2 memory module and are shared with the expansion connectors. This configuration helps to probe the XSPI interface on the expansion connector.**

1. *The default configuration is shown in bold.*
2. *The serial resistor on the XSPI interface can be adjusted to improve signal integrity.*

9 NUCLEO-C5A3ZG product information

9.1 Product marking

The product and each board composing the product are identified with one or several stickers. The stickers, located on the top or bottom side of each PCB, provide product information:

- Main board featuring the target device: product order code, product identification, serial number, and board reference with revision.

  Single-sticker example:

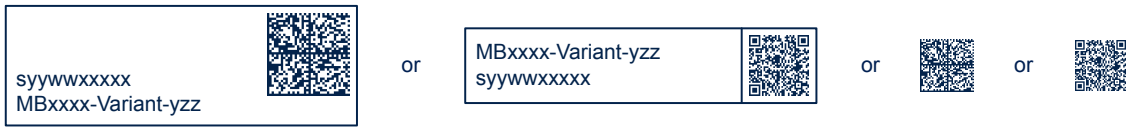
  

  Dual-sticker example:

- Other boards if any: board reference with revision and serial number.

  Examples:

On the main board sticker, the first line provides the product order code, and the second line the product identification.

On all board stickers, the line formatted as *"MBxxxx-Variant-yzz"* shows the board reference *"MBxxxx"*, the mounting variant *"Variant"* when several exist (optional), the PCB revision *"y"*, and the assembly revision *"zz"*, for example B01. The other line shows the board serial number used for traceability.

Products and parts labeled as *"ES"* or *"E"* are not yet qualified or feature devices that are not yet qualified. STMicroelectronics disclaims any responsibility for consequences arising from their use. Under no circumstances will STMicroelectronics be liable for the customer's use of these engineering samples. Before deciding to use these engineering samples for qualification activities, contact STMicroelectronics' quality department.

"ES" or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the ordering part number of the evaluation tool that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

9.2 NUCLEO-C5A3ZG product history

Table 20. Product history

Order code	Product identification	Product details	Product change description	Product limitations
NUCLEO-C5A3ZG	NUC5A3ZG$KR1	MPU: STM32C5A3ZGT6 silicon revision "Z"	Initial revision	TS_CAL1 calibration is wrongly calibrated with a value measured at VREF+ = 3.0 V instead of 3.3 V. Therefore, the formula to retrieve the temperature from ADC conversion data yields incorrect results. Workaround: The temperature sensor is linear. To retrieve the TS_CAL1 calibration value at 3.3 V, use the following formula: TS_CAL1 (3.3V) = TS_CAL1 (3.0V) × (3.0/3.3)
		MCU errata sheet: *STM32C5A3xG, STM32593xG, and STM32591xG device errata* (ES0677)		
		Boards: • MB2310-C5A3ZG-B02 (main board)		
	NUC5A3ZG$KR2	MPU: STM32C5A3ZGT6 silicon revision "Z"	Temperature sensor TS_CAL1 calibrated at 3.3 V	No limitation
		MCU errata sheet: *STM32C5A3xG, STM32593xG, and STM32591xG device errata* (ES0677)		
		Boards: • MB2310-C5A3ZG-B02 (main board)		

9.3 Board revision history

Table 21. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB2310 (main board)	C5A3ZG-B02	Initial revision	Due to muxing constraints, the VCP interface, ARDUINO® Uno V3 UART, and ST morpho UART share the same UART2 instance. Refer to Section 7.12: Virtual COM port (VCP) for further details.

10 Compliance statements and conformity declarations

10.1 Federal Communications Commission (FCC) compliance statement

Part 15.19

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

Responsible Party - U.S. Contact Information:

Francesco Doddo
STMicroelectronics, Inc.
200 Summit Drive | Suite 405 | Burlington, MA 01803
USA
Telephone: +1 781-472-9634

10.2 Innovation, Science and Economic Development Canada (ISED) compliance statement

This product complies with the ICES-003 standard class B of the ISED regulation.

ISED Canada ICES-003 Compliance Label: CAN ICES (B)/NMB (B).

Note: Use only shielded cables.

Ce produit est conforme à la norme NMB-003 classe B de la ISDE.

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES (B) / NMB (B).

Note: Utiliser uniquement des câbles blindés.

10.3 UKCA conformity

Simplified UK declaration of conformity

Hereby, the manufacturer STMicroelectronics, declares that the equipment type NUCLEO-C5A3ZG is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK SI 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK SI 2012 No. 3032).

Note: Use only shielded cables.

10.4 CE conformity

10.4.1 Simplified EU declaration of conformity

Hereby, STMicroelectronics declares that the equipment type NUCLEO-C5A3ZG is in compliance with directives 2011/53/EU and 2015/863/EU (RoHS), and 2014/30/EU (EMC).

Note:
- *RoHS: Restriction of hazardous substances*
- *EMC: Electromagnetic compatibility*

Note: Use only shielded cables.

10.4.2 Déclaration de conformité UE simplifiée

STMicroelectronics déclare que l'équipement électrique du type NUCLEO-C5A3ZG est conforme aux directives 2011/53/UE et 2015/863/UE (LdSD), et à la directive 2014/30/UE (CEM).

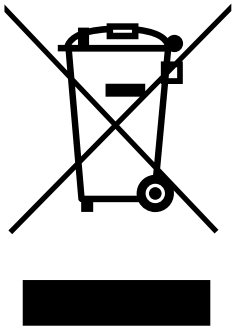
Note:
- *LdSD : directive sur la limitation de l'utilisation des substances dangereuses*
- *CEM : compatibilité électromagnétique*

Note: Utiliser uniquement des câbles blindés.

11 Product disposal

Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories must not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, separate these items from other types of waste and recycle them responsibly at a designated collection point to promote the sustainable reuse of material resources.

Household users:

Contact the retailer that you purchased the product from or your local authority for details of your nearest designated collection point.

Business users:

Contact your dealer or supplier for further information.

Revision history

Table 22. **Document revision history**

Date	Revision	Changes
27-Feb-2026	1	Initial release.
06-Mar-2026	2	Updated Table 20. Product history.

Contents

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