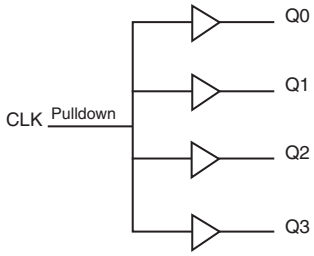
General Description

The 8304I is a low skew, 1-to-4 Fanout Buffer. The 8304I is characterized at full 3.3V for input V_{DD}, and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the 8304I ideal for those clock distribution applications demanding well defined performance and repeatability.

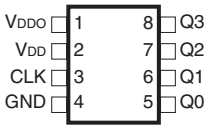
Features

- Four LVCMOS / LVTTL outputs
- LVCMOS clock input
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 166MHz
- Output skew: 60ps (maximum)
- Part-to-part skew: 650ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) compliant package

Block Diagram



Pin Assignment



8304I
8-Lead SOIC
3.8mm x 4.8mm, x 1.47mm package body
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDO}	Power		Output supply pin. Connect to 3.3V or 2.5V.
2	V_{DD}	Power		Positive supply pin. Connect to 3.3V.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground. Connect to ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

NOTE: *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			15	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

Table 3C. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.6			V
		I_{OH} = -16mA	2.9			V
		I_{OH} = -100uA	3			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V
		I_{OL} = 16mA			0.25	V
		I_{OL} = 100uA			0.15	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Section, “3.3V Output Load Test Circuit”.

TABLE 3D. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		2.1			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Section, “3.3V/2.5V Output Load Test Circuit”.

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2		3.3	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, Integration Range 12kHz – 20MHz		0.17		ps
tsk(o)	Output Skew; NOTE 2, 4	f = 133MHz			50	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 166MHz unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

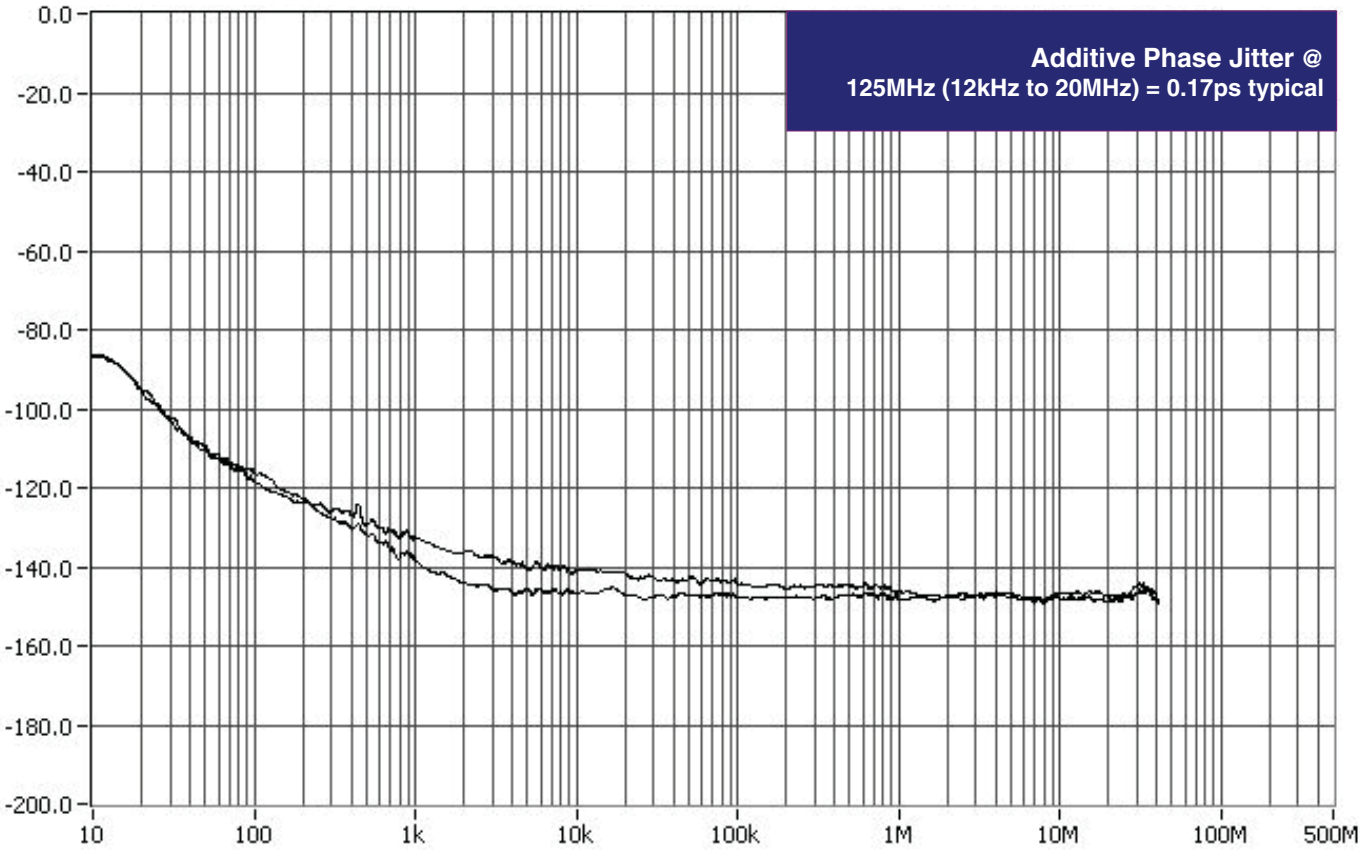
TABLE 4B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2.3		3.7	ns
tsk(o)	Output Skew; NOTE 2, 4	f = 133MHz			60	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				650	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at 166MHz unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

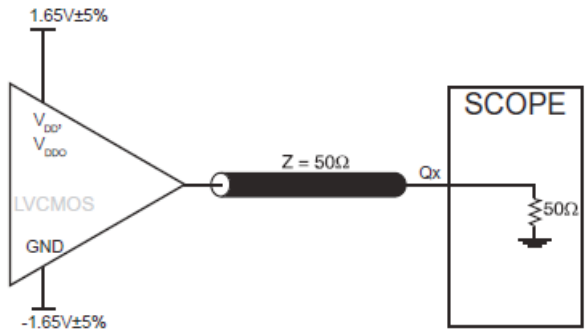
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

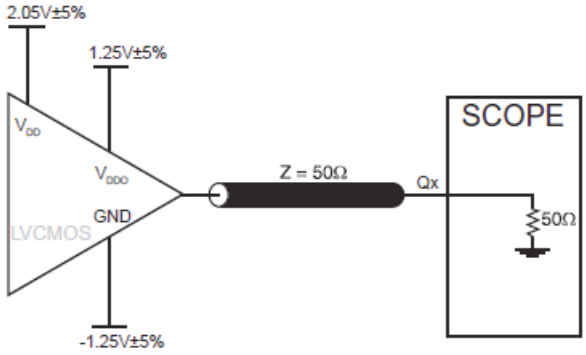


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

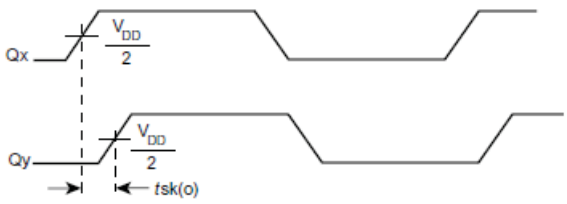
Parameter Measurement Information



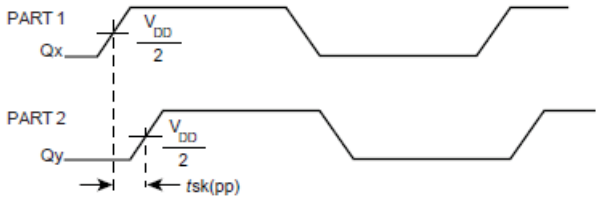
3.3V Output Load AC Test Circuit



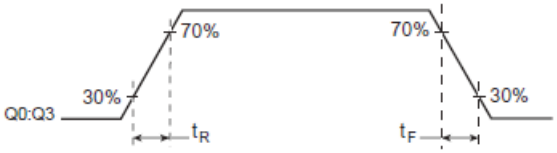
2.5V Output Load AC Test Circuit



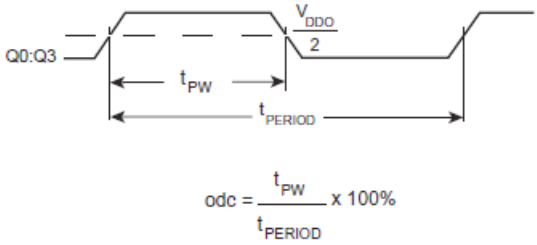
Output Skew



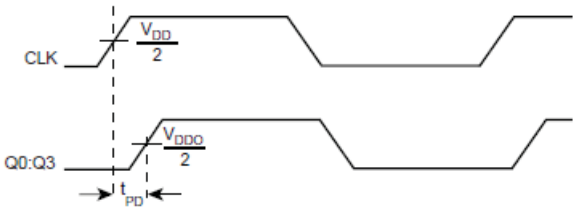
Part-to-Part Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8304I is: 416

Package Outline and Dimensions

Package Outline - Suffix M for 8 Lead SOIC

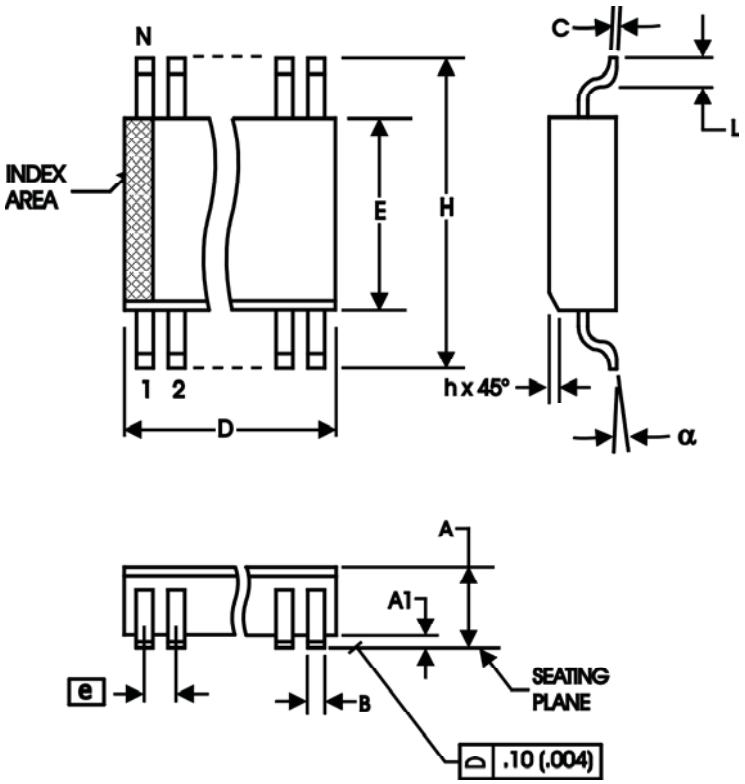


Table 6. Package Dimensions - Suffix M

SYMBOL	Millimeters	
	MINIMUN	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8304AMILF	8304AMIL	8 lead “Lead Free” SOIC	Tube	-40°C to +85°C
8304AMILFT	8304AMIL	8 lead “Lead Free” SOIC	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	3B	3	LVCMOS/LVTTL DC Characteristics Table, added I_{OH} and I_{OL} Test Conditions to V_{OH} and V_{OL} rows.	4/4/02
B	T7	1 8	Features Section - added lead-free bullet. Ordering Information Table - added lead-free part number, marking and note. Updated datasheet format.	11/09/06
C	T4A T7	4 6 9	3.3V AC Characteristics Table - added Buffer Additive Phase Jitter spec. Added Buffer Additive Phase Jitter Plot. Ordering Information - Deleted “ICS” from the Part/Order number column.	2/11/09
D	T1 T2	1 2 2	Pin Assignment - corrected “pullup” label to “pulldown” label. Pin Description Table - deleted pullup from note. Pin Characteristics Table - deleted Rpullup row.	10/29/10
D	T7	9	Removed ICS in the part numbers. Removed LF note at the bottom of the Ordering Information table. Removed the quantity of 2500 from the Tape & Reel in the Ordering information table. Updated datasheet header and footer.	12/10/15

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